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ABSTRACT

This course is intended to train Air Force personnel to become electronic computer and switching systems specialists. One part of the course consists of a three-volume career development course. Topics are maintenance orientation (15 hours), electronic principles and digital techniques (87 hours), and systems maintenance (51 hours). Each volume provides both theoretical and factual information, exercises, and answers for exercises. Volume review exercises accompany each volume. The course also contains nine modules on these topics: introduction to digital techniques and numbering systems (12 hours); clock/pulse generators (12 hours); combination logic and converters (12 hours); computers, peripherals, and storage media (21 hours); semiconductors and semiconductor devices (3 hours); digital logic and Boolean algebra (12 hours); sequential logic (9 hours); corrosion control (6 hours); and basic techniques of waveform measurement using an oscilloscope (9 hours). Module components are student-centered objectives, informative material on those objectives, exercises, and answers for exercises. (YLB)

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ED272706

ELECTRONIC COMPUTER AND SWITCHING SYSTEMS SPECIALIST

(AFSC 30554)

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Extension Course Institute

Air University

ECI COURSE MATERIALS SHIPPING LIST

COURSE NUMBER	COURSE TITLE	EFFECTIVE DATE
30554	ELECTRONIC COMPUTER AND SWITCHING SYSTEMS SPECIALIST (AFSC 30554)	6 Jun 86

INSTRUCTIONS The following materials are needed to complete this course. Check this list immediately upon receiving your course package, and if any materials are missing or incorrect (numbers don't match), notify ECI immediately. Use the ECI Form 17 for this purpose, and be sure to include your identification number, address, course and volume number, and VRE form designation (if a VRE is involved). Send all correspondence separately from your answer sheet.[1]

ITEM	TYPE	DESIGNATION OR TITLE	INVENTORY CONTROL NUMBER	VRE ANSWER SHEET IDENTIFICATION
3	VOL	VOL 1, Maintenance Orientation	30554 01 8501	
4	VRE	VOLUME REVIEW EXERCISE (VOL 1)	30554 01 25	30554 01 25
5	VOL	VOL 2, Electronic Principles and Digital Techniques	30554 02 8112	
6	MOD	MODULE, Introduction to Digital Techniques and Numbering Systems	30554 02 S34 8112	
7	MOD	MODULE, Clock/Pulse Generators	30554 02 S36 8112	
8	MOD	MODULE, Combinational Logic and Converters	30554 02 S38 8112	
9	MOD	MODULE, Computers, Peripherals and Storage Media	30554 02 S39 8112	
10	MOD	MODULE, Semiconductors and Semiconductor Devices (5 Skill Level)	30554 02 S42 7811	
11	MOD	MODULE, Digital Logic and Boolean Algebra	30554 02 S50 8309	
12	MOD	MODULE, Sequential Logic	30554 02 S51 8312	
13	VRE	VOLUME REVIEW EXERCISE (VOL 2)	30554 02 23	30554 02 23
14	VOL	VOL 3, Systems Maintenance	30554 03 8201	
15	MOD	MODULE, Corrosion Control	30554 03 S21 7807	
16	MOD	MODULE, Basic Techniques of Waveform Measurement Using An Oscilloscope	30554 03 S48 8112	
17	VRE	VOLUME REVIEW EXERCISE (VOL 3)	30554 03 21	30554 03 21

NOTE: DIRECT ANY QUESTION OR COMMENTS RELATING TO ACCURACY OR CURRENCY OF TEXTUAL MATERIALS TO AUTOVON 868-3057.

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[1] SEE REVERSE SIDE FOR ADDITIONAL INSTRUCTIONS.

LIST OF CHANGES

COURSE NUMBER
30554

EFFECTIVE DATE OF SHIPPING LIST
6 Jun 86

CAREER FIELDS, POLICIES, PROCEDURES, AND EQUIPMENT CHANGE. ALSO, ERRORS OCCASIONALLY GET INTO PRINT. THE FOLLOWING ITEMS UPDATE AND CORRECT YOUR COURSE MATERIALS. PLEASE MAKE THE INDICATED CHANGES.

NOTE: PLEASE MAKE THE CORRECTIONS INDICATION BELOW. THESE CORRECTIONS MAY OMIT SOME ERRORS, SUCH ASTYPOS, THAT DO NOT AFFECT THE MEANING OF THE MATERIAL.

1. CHANGES FOR THE MODULE: 30554 02 S34 8112

a Page 2, col 1, line 3 fr bot: After "under" add "HYBRID." Col 2, line 1: Change "detects the presence or nonpresence of information" to "uses numbers to represent data."

b. Page 3, col 2, line 18 fr bot: After "Semiconductor" add "independently."

c. Page 4, Table 1-1, line 4: Delete duplicate Legend.

d. Page 9, col 1, line 4: Change "systems" to "system."

e. Page 12, col 2, line 10 fr bot: Change "2^{P4}" to "2^{-4}."

f. Page 24, Exercises (014)-2: Change "$405.1_{(8)}$" to "$400.1_{(8)}$."

g. Page 32, col 2, line 8: Change "5 2 4 7 0 C" to "5 2 3 7 0 C."

h. Page 33, col 1, line 14: Change "+ F 0 2 B 6" to "+ F D 2 B 6." Line 16: Change "1 E 8 A C 6" to "1 E 8 A C O."

i. Page 35, col 1, line 7 fr bot: Change "0 10" to "0010."

j. Page 36, Exercises (021)-3.a: Change "11000110" to "10011010."

k. Page 39, answer 007-2.a: Change "10001111" to "11001111."

l. Page 40, answer 019-1.a: Change "80AE" to "81AE." Answer 019-1.b: Change "28391" to "26501." Answer 019-2.b: Change "10E" to "00E." Answer 020-1.a: Change "10111" to "1 0111." Answer 020-1.b: Change "10101" to "1 0101."

2. CHANGES FOR THE MODULE: 30554 02 S36 8112

a. Page 4, col 2, line 1: Change "+25-volts" to "-25-volts."

b. Page 12, col 2, line 14 fr bot: Change "R2" to "R1."

c. Page 17, col 2, line 26: Change "9.1" to "91.1."

d. Page 18, col 1, line 19: Change "L2 to L2" to "L1 to L2."

e. Page 19, col 1, line 2 fr bot: Change "sctions" to "sections."

f. Page 20, col 2, line 1 fr bot: Change "$= \frac{.159}{\sqrt{.064} \times 10^{-15}} = \frac{.159}{\sqrt{64} \times 10^{-18}}$"

to "$= \frac{.159}{\sqrt{.064 \times 10^{-15}}} = \frac{.159}{\sqrt{64 \times 10^{-18}}}$"

LIST OF CHANGES

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CAREER FIELDS, POLICIES, PROCEDURES AND EQUIPMENT CHANGE. ALSO, ERRORS OCCASIONALLY GET INTO PRINT. THE FOLLOWING ITEMS UPDATE AND CORRECT YOUR COURSE MATERIALS. PLEASE MAKE THE INDICATED CHANGES.

2. CHANGES FOR THE MODULE: 30554 02 S36 8112 (Continued)

g. Page 20, col 2, line 2 fr bot: Change "$= \frac{.159}{\sqrt{.016} \times 10^{-3} \times 4 \times 10^{-12}}$" to "$= \frac{.159}{\sqrt{.016 \times 10^{-3} \times 4 \times 10^{-12}}}$."

h. Page 21, Exercises (011)-6: Delete "and there is . . . of the circuit."

i. Page 22, col 1, line 5: Change "Flat" to "Fast."

j. Page 24, col 2, line 4: Change "$Q=X_L$" to "$Q=\frac{R}{X_L}$."

k. Page 25, col 1, line 10: Change "maximum" to "minimum."

l. Page 36, col 2, line 5 fr bot: Change "3f" to "$\frac{3f}{4}$." Line 6 fr bot: Change "f(X-1)" to "$\frac{f(X-1)}{X}$."

m. Page 40, col 1, line 6: Change "off-numbered" to "odd-numbered." Col 2, lines 2-3 fr bot: Change "If you multiply" to "When multiplying."

n. Page 41, col 1, line 2: Change "Since" to "If" and "in the AN/TTC-30" to "of a." Line 3: After "nearest" add "sampling rate." Line 4: Change "could" to "can." Lines 5-6: Change "was" to "is" and delete "The 12.5 . . . AN/TTC-30." Line 6: Change "If" to "When."

o. Page 44, col 2, line 11: Change "the AN/TTC-30 ESC" to "an electronic switching center." Line 12: Change "AN/TCC-30 ESC" to "switching center."

p. Page 46, Exercises (021)-2: Change "part" to "parts."

q. Page 50, answer 008-1: Change "current" to "circuit." Answer 011-6: Delete "; unilateralization; neutralization." Answer 014-1(1): After "j." add "g."

r. Page 51, answer 015-4: Change "Bl" to "Rl." Answer 019-2: Change "ration" to "ratio."

3. CHANGES FOR THE MODULE: 30554 02 S38 8112

a. Page 2, col 2, line 10: Change "one low input" to "two low inputs."

b. Page 5, Exercises (001)-1(16): After the blank space add "binary digits." Exercises (001)-1.dd: After "dd." add "ee. Inhibited and."

c. Page 12, col 2, line 3 fr bot: After "8" add "will be satisfied. Follow the outputs of AND-gates 3 and 8."

d. Page 13, Figure 1-15, bottom left: Under "KEYBOARD" change "A B C D" to "D C B A."

LIST OF CHANGES

COURSE NUMBER 30554	CAREER FIELDS, POLICIES, PROCEDURES AND EQUIPMENT CHANGE. ALSO, ERRORS OCCASIONALLY GET INTO PRINT. THE FOLLOWING ITEMS UPDATE AND CORRECT YOUR COURSE MATERIALS. PLEASE MAKE THE INDICATED CHANGES.
EFFECTIVE DATE OF SHIPPING LIST 6 Jun 86	

3. CHANGES FORTHE MODULE: 30554 02 S38 8112 (Continued)

e. Page 27, col 1, line 1: Change "B(MS + MS)" to "$B(MS + \overline{MS})$."

f. Page 32, col 2, line 11: Change "in" to "pin."

g. Page 35, col 2, line 29: Change "$(T7_s + T7_a)5\ (T7_s + T7_b) \bullet (T7_a$." to "$(T7_s + T7_a) \bullet (T7_s + T7_b) \bullet (T7_a +$."

h. Page 36, Exercises (013)-3: Change "OR-gate" to "OR-gate 1." Col 2, line 11: Change "$\overline{A}BCD\overline{E}$" to "$A\overline{B}C\overline{D}E$."

i. Page 37, col 2, line 9 fr bot: Change "na" to "an."

j. Page 41, col 1, line 2: Change "1-35" to "1-37." Line 7 fr bot: After "this" add "time."

k. Page 51, col 1, line 27 fr bot: Change "$Y = \overline{A}B + D\ A\overline{B}$" to "$Y = \overline{A}B + A\overline{B}$."

l. Page 61, answer 001-1(13): Change "NAND" to "Inhibited and." Answer 005-3: Change "21" to "31." Answer 006-1: Change "13" to "12." Answer 013-3: Change to read "B error = $[(\overline{T7}_t \bullet T7_b) + (T7_t \bullet \overline{T7}_b)]$.

4. CHANGES FOR THE MODULE: 30554 02 S39 8112

a. Page 2, Figure 1-2: Under "INPUT MEDIA" add "KEYBOARD."

b. Page 10, col 1, line 5: Change "he" to "the."

c. Page 32, col 2, line 19: Change "drowned" to "downward."

d. Page 48, col 2, line 10 fr bot: Change "$\frac{Hm}{2}$" to "$\frac{-Hm}{2}$."

e. Page 49, Exercises (022)-4: Change "$\frac{Hm}{2}$" to "$\frac{-Hm}{2}$."

f. Page 82, answer (022)-4: Change "-B subscript s" to "+B subscript r."

5. CHANGES FOR THE MODULE: 30554 02 S42 8112

a. Page 5, col 1, last line: Change "minimum" to "maximum." Col 2, line 11: Change "or" to "and."

b. Page 18, Figure 1-15A, B and C: Change "Clamping DC Reference" to "Clamping Reference."

c. Page 20, Figure 1-16A, B and C: Change "Clamping DC Reference" to "Clamping Reference."

d. Page 29, answer 009-3: Change "PNP" to "NPN."

LIST OF CHANGES

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EFFECTIVE DATE OF SHIPPING LIST 6 Jun 86	

6. CHANGES FOR THE MODULE: 30554 02 S50 8309

a. Page 13, col 2, Figure 1-43C: Under OUTPUT, change "AB" to "$\overline{AB}$."

b. Page 18, col 1, line 15: Change "base" to "cathode." Col 2, line 10: Change "ANd" to "AND."

c. Page 21, Figure 1-52.A: The true table for a NOR-gate negative logic should read as follows:

A	B =	$\overline{C}$
H	H	L
H	L	H
L	H	H
L	L	H."

d. Page 29, col 1, Figure 1-59, Legend: Change "OR" to "AND."

e. Page 31, col 1, Figure 1-66: In "output" expression, change "D+E" to "[D+E]." Figure 1-67: Insert another state indicator at OR-gate output.

f. Page 33, col 1, Figure 1-76: Change "$\overline{JK}$" to "$\overline{\overline{J}K}$" in both places. Exercises (023)-11A: Change "E/qX" to "E=X."

g. Page 36, Exercises (023)-14B: Change "($\overline{E}+\overline{F}$)" to "$\overline{E+F}$."

h. Page 46, Exercises (023)-12B: Change "=$\overline{X}$" to "=X."

7. CHANGES FOR THE MODULE: 30554 02 S51 8112

a. Page 5, col 2, line 6: After "flip-flops" add "in Figure 1-1."

b. Page 24, col 1, line 20: Change "FF-4" to "FF-A."

c. Page 43, col 2, line 4: Change "shift" to "transfer." Line 7: Change "FF-1" to "FF-S1."

d. Page 45, col 2, line 8 fr bot: Change "FF-3" to "FF-2."

e. Page 58, answer 008-8: Change "if" to "is."

8. CHANGES FOR THE MODULE: 30554 03 S48 8112

a. Page 5, col 2, line 8: In the equation change "$\frac{1}{10-3}$" to "$\frac{1}{10^{-3}}$."

b. Page 10, col 1, line 6 fr bot: Change "EXT/10" to "EXT ÷ 10." Line 24 fr bot: Change "Axiom ÷ 2" to "Axiom #2."

c. Page 14, col 1, line 5: Change "990" to "009."

d. Page 19, col 1, line 4 fr bot: Change "6" to "2."

e. Page 22, Appendix A, line 12: Change "40,00,000" to "40,000,000."

LIST OF CHANGES

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CAREER FIELDS, POLICIES, PROCEDURES AND EQUIPMENT CHANGE. ALSO, ERRORS OCCASIONALLY GET INTO PRINT. THE FOLLOWING ITEMS UPDATE AND CORRECT YOUR COURSE MATERIALS. PLEASE MAKE THE INDICATED CHANGES.

8. CHANGES FOR THE MODULE: 30554 03 S48 8112 (Continued)

f. Page 25, col 1: Immediately after answer 002-2, change "022-3" to "002-3", "022-4" to "002-4" and "022-5" to "002-5. Answer 002-5: Change "250 Hz" to "250 kHz."

9. CHANGE FOR THE TEXT: VOLUME 1

Page 52, col 1, line 2 fr bot: Delete "(fig. 6-6)." Line 3 fr bot: After "Request" add "(fig. 6-6)."

10. CHANGE FOR THE VOLUME REVIEW EXERCISE: VOLUME 1

The following questions are no longer scored and need not be answered: 12, 76, 89 and 95.

11. CHANGE FOR THE VOLUME REVIEW EXERCISE: VOLUME 2

The following questions are no longer scored and need not be answered: 43, 81 and 90.

12. CHANGE FOR THE VOLUME REVIEW EXERCISE: VOLUME 3

The following questions are no longer scored and need not be answered: 14, 90, 93 and 96.

30554 00 S01 8507

CHANGE SUPPLEMENT

CDC 30554

ELECTRONIC COMPUTER AND SWITCHING SYSTEMS SPECIALIST

(AFSC 30554)

IMPORTANT: Make the corrections indicated in this supplement before beginning study of Volumes 1, 2, and 3. This supplement contains both "pen-and-ink" changes and replacement pages. It is perforated and three-hole-punched so that you can tear out the replacement pages and insert them in your volume. You are not required to post any changes listed in this supplement which correct typographical errors, unless such errors change or otherwise affect the meaning of the material.

Extension Course Institute
Air University

CHANGES FOR THE TEXT: VOLUME 1

Pen-and-Ink Changes

Page-Col	Subject	Line(s)	Correction
1R		3	Change "computer" to "Computer."
1R		15	After "Specific" add "Specialty."
1R		18	Change "perform" to "maintain."
2L		16 fr bot	Change "Electron" to "Electronic."
2R		15 Fr bot	After "more" add "difficult."
3L		25 fr bot	Change "buffer" to "buffers."
3L		4 fr bot	Change "of" to "a."
3L		3 fr bot	Change "oscilloscopes" to "oscilloscope."
3R		10	Delete "A Minimum ... Electronics 80."
5L		4	Delete "for."
5R		21-24	Delete "The guidance is ... a particular activity."
5R		3 fr bot	Delete "and is involved ... the guide pertains to."
6L		2	Delete "in connection with the effort involved."
6L		5	Delete "and material involved."
6L		16	Change "USAF" to "DOD."
7L		21	Change "suth" to "such."
7R		32	Change "thee" to "these."
12L		3	Change "which" to "while."
15R		6	Change "injury" to "injure."
17L		7 fr bot	Change "on" to "or."
22R		14	Change "Sine" to "Since."
23L		22	Change "FM" to "TM."
24R		18	Change "EAch" to "Each."

Page-Col	Subject	Line(s)	Correction
29R		17	Delete "action to ground aircraft,."
29R		18-20	Change "ground communications," to "the equipment." and delete "electronics, or use ... will be taken."
34L		5	Change "5-20" to "5-2."
35L		23	Change "preduct" to "predict."
35L		10-11 fr bot	Delete "and expected completion time" and change have to "has."
36L		10-16	Delete "job proficiency training ... special purpose vehicles."
37L		24	Delete "Volume 5, ... that volume."
44	(047)-3		Change "a" to "is."
48R		8	Change "ship" to "shop."
49L		5	Change "1755-2" to "1577-2."
55	007-4		Change "A listing of" to "To list."
56	036-3		Change "00-561" to "00-5-1."

CHANGES FOR THE TEXT: VOLUME 2

Pen-and-Ink Changes

Page-Col	*Subject*	*Line(s)*	*Correction*
iii	Preface	6–7	Delete ". and supplement to it" and after "which" change "are" to "is."
2R		7	Change "V_Q" to "V_G."
4R		7 fr bot	After "on." add "The positive voltage on the gate will establish the operating point."
9R		4 fr bot	Change "$\frac{R^4}{R^3 \pm R^4}$" to "$\frac{R^4}{R^3 + R^4}$".
		1 fr bot	Change "$\frac{F^1 + R^2}{R^2}$" to "$\frac{R^1 + R^2}{R^1}$."
10L	213-4		Change "no" to "one."
12R		7 fr bot	Change "electrons" to "electronics."
20		10	Change "289" to "299."

CHANGES FOR THE TEXT: VOLUME 3

Pen-and-Ink Changes

Page-Col	*Subject*	*Line(s)*	*Correction*
ii		4 fr bot	Change "Basic Techniques of Waveform Measurement Using an Oscilloscope" to "Oscilloscope Measurements." Change page number 182 to number 181a.
4R		19 fr bot	Change "10^{-6}" to "10^{-9}."
24L		16	Change "2-10" to "2-11."
28L		19	Change "cycle" to "interval."
58L		4	Change "AZA4XA7-6" to "A2A4XA7-6."
76R		11 fr bot	Change "bolt" to "volt."
108R		15 fr bot	Change "part" to "point."
129L		9 fr bot	After "one" add "and 1/4."
		15 fr bot	Change "1" to 1′" to "1¼" to 1½" to provide sufficient shiner length."
155L		15	Change "hold" to "hole."
166L		17 fr bot	Change "6-20, A" to "6-21,A."
179R		25	Change "rectifir nnuiinit thpn" to "rectifier unit type."

Page Changes:

Remove Pages	*Insert Pages*
147–150	147–150
181–182	181–182
191–192	191–192

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CDC 30554

ELECTRONIC COMPUTER AND SWITCHING SYSTEMS SPECIALIST

(AFSC 30554)

Volume 1

Maintenance Orientation

This material includes "FOR OFFICIAL USE ONLY" information which cannot be released to unauthorized persons. The provisions of AFR 12-30 apply.

Extension Course Institute
Air University

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MCMXLVII
UNITED STATES OF AMERICA

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Preface

THIS CDC was prepared for airmen assigned to on-the-job training (OJT) to the 30554 skill level. Training was organized under the dual-channel OJT program to provide an orderly means of learning fundamental knowledge through self-study and the development of job proficiency through supervised instruction. This three-volume CDC presents the fundamentals needed for your career knowledge development, which is the first part of the OJT program. The second part, job proficiency development, is based on your performance as you develop the skills needed to accomplish assigned tasks.

In this three-volume career development course (CDC), the first volume presents several subjects common to the majority of maintenance career fields. The subjects included are: career progression, security, the Air Force Occupational Safety and Health (AFOSH) Program, technical publications, communication-electronics maintenance (CEM) management, and maintenance documentation. Volume 2 covers electronic principles and digital techniques, and knowledges required in support of this specialty knowledge test (SKT). Volume 3 discusses systems maintenance principles and techniques. The many types of hardware and test equipment used within the 305X4 Career Field prohibits the discussion of specific equipment.

Code numbers appearing on figures are for preparing agency identification only.

The inclusion of names of any specific commercial product, commodity, or service in this publication is for information purposes only and does not imply, indorsement by the Air Force.

NOTE: If you know this course contains erroneous or outdated information or does not provide the knowledge that the current specialty training standard (STS) requires you to have for upgrade training, contact your unit OJT advisor and fill out AF form 1284, Training Quality Report. If you need an immediate clarification of information in these study materials, call the author between 0800 and 1600 (CT), Monday through Friday.

Consult your education officer, training officer, or NCO if you have questions on course enrollment or administration, Your key to a Successful Course, and irregularities (possible scoring errors, printing errors, etc.) on the volume review exercises and course examination. Send questions these people can't answer to ECI, Gunter AFS AL 36618-5643, on ECI Form 17, Student Request for Assistance.

This volume is valued at 15 hours (5 points).

Material in this volume is technically accurate, adequate, and current as of September 1984.

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Answers for Exercises ... 55

NOTE: This course teaches through numbered lesson segments, each containing a behavioral objective, text, and exercises. The objective sets your learning goal. The text gives you the information you need to reach that goal, and the exercises let you check your achievement. When you complete each segment, see whether your answers match those in the back of the volume. If your response to an exercise is incorrect, review the objective and its text.

CHAPTER 1

305X4 Career Progression

CONGRATULATIONS! You have successfully completed a formal technical school course and have been awarded the Air Force Specialty Code 30534, Electronic Computer and Switching Systems Specialist. You are now entering a phase of self-study designed to provide you with the necessary knowledge to be awarded the 5 skill level in your Air Force specialty. As you begin your study of this CDC, keep in mind the following quote from AFR 35-1, Military Personnel Classification Policy.

> Individual Responsibility. An Air Force member's career progression is directly related to the amount of personal effort made to gain and keep specialty qualification. Accordingly, specialty knowledge and proficiency are primarily the responsibility of each individual. Several programs are available through the Base Education Service Centers (for example, Community College of the Air Force). Each officer and airman is encouraged to use every opportunity available that would enhance individual technical, military, and professional qualities.

Successful completion of this CDC is one of your responsibilities in your career progression. More specific responsibilities and duties are outlined in AFR 39-1, *Airman Classification Regulation*, and AFR 39-6, *The Enlisted Force Organization*.

1.1. Your Air Force Speciality Code (AFSC)

You have been assigned an Air force speciality code which identifies your specific job and your level of qualification. This code will change as your job or qualification changes.

001. State the meaning of each digit of the 305X4 AFSC, and specify the significance of primary, duty, and control AFSCs.

Air Force Specialty Code. Throughout your Air Force career, your duty assignments are governed by an Air Force specialty code (AFSC) assigned in accordance with the "airman coding system." When initially reporting for basic training, you were given a reporting identifier code number "99000" for basic airman. When selected for a particular career field, you were assigned the "helper level" AFSC for that field. For Example, in the Electronic Computer and Switching Systems Specialist/Technician Career Field, the helper level is 30514, Electronic Computer and Switching Systems Helper.

Coding Method. Each AFSC consists of five numerical digits. The first two digits identify the career field - in your case, the Electronics Equipment Maintenance Systems Career Field (30). The third digit, in combination with the first two, identifies the subdivision of the field, i.e., Electronic computer and Switching Systems (5). The fourth digit identifies the skill level of the AFS. This may be a 1,3,5,7 or 9 level. In your case, it is the 5 level, which means skilled or specialist. The fifth digit identifies a specific specialty. The AFSC of 30554 is then labeled specifically as Electronic Computer and Switching Systems Specialist. Broken down and labeled, the AFSC looks like this:

30 = Career Field	Communications Electronics
5 = Subdivision	Electronic Computer and Switching Systems
5 = Skill Level	Skilled (Specialist)
4 = Specific	Technician

In some career fields it is necessary to further identify the particular equipment an airman is qualified to operate or perform. In such cases a letter suffix is used and this becomes a part of the AFSC. In addition, a letter prefix may also be used to designate a special type of duty that is common to more than one AFS. For example, the prefix "T" means instructor and the suffix "A" means assigned to aircrew duty.

Types of AFSCs. Throughout your Air Force career, you will perform duties and be assigned in accordance with three types of AFSCs, as follows:

(1) Your primary AFSC (PAFSC) is the AFSC in which you are most highly trained and qualified to perform duty.

(2) Your duty AFSC (DAFSC) is the AFSC in which you actually perform duty. In most cases this is the same as the PAFSC; however, it may vary. For example, as a 3-level helper, you may be assigned duty in a 5-level position due to a lack of 5-level personnel.

(3) Your control AFSC (CAFSC) is used as a management tool to control airman assignment actions against authorized worldwide manning requirements.

Exercises (001):

1. What do the first two, fourth, and fifth digits of an AFSC indicate?

2. Your primary AFSC is the AFSC in which you are:

____
____
____
____
____
____
____________________ .

1-2. Duties of AFS 30554

You must understand your AFSC specialty description in AFR 39-1. This specialty description has been developed from occupational surveys and job evaluations. These surveys are conducted as needed to collect information about work performed by airmen in a specialty. They are followed by job evaluations to insure that skill levels match the level of difficulty and responsibility of work performed. Thus, the specialty descriptions appearing in AFR 39-1 describe your duties as accurately and completely as possible.

002. State the regulation which contains the specialty summary for AFS 305X4, and state the tasks required by the 30574 specialty.

Speciality Summary. AFR 39-1. *Airman Classification Regulation,* describes the Electron Computer and Switching System Specialty as follows:

> *Installs, maintains and repairs electronic computer and switching systems, including transmission, processing, and display equipment.*

The specialty summary for AFSC 30574 differs from AFSC 30554 in that technicians have added responsibilities due to their enlisted grade and experience as follows:

> Inspects, installs, troubleshoots, repairs, overhauls, and modifies high-speed general-purpose and special electronic computer and switching systems, and supervises electronic computer and switching systems activities.

Exercises (002):

1. What regulation describes the specialty summary for AFSC 30554?

2. One of the tasks required by the specialty summary for a 30574 is to modify what type of systems?

003. Specify the duties and responsibilities of AFSC 305X4.

Duties and Responsibilities. The Electronic Computer and Switching Systems Specialist duties and responsibilities, as stated in AFR 39-1, are described thus:

a. Installs electronic computer and switching systems equipment. Checks equipment visually and by use of tools and test equipment for serviceability prior to installation. Assembles, connects, and interwires components of data transmission, processing, and display equipment. Conducts detailed test of installed equipment for proper assembly of components and compliance with technical orders. Places in operation and adjusts and aligns components to obtain maximum efficiency.

b. Performs preventive maintenance on electronic computer and switching systems equipment. Inspects and tests electronic data equipment at specified intervals to locate defects, such as discolored or cracked resistors, loose mountings, poor connections, faulty tubes, sluggish relays, or overheated components. Adjusts or replaces defective parts. Turns on equipment, sets controls in various operating positions, and evaluates equipment performance, using prescribed operational testing procedures.

c. Repairs and modifies electronic computer and switching system equipment. Isolates malfunctions by using operational troubleshooting and testing techniques, logic diagrams and equations, test programs, visual inspections, static voltage checks, resistance measurements, observation of waveforms, and other tests requiring specialized electronic test equipment. Repairs associated data transmitting, processing, and display equipment using hand tools, soldering irons, and specialized test equipment. Calibrates and aligns system components according to technical orders, manufacturers' handbooks, and local procedures. Accomplishes the prescribed and authorized modifications. Performs progressively more repair duties as specifically directed by the chief of maintenance.

d. Maintains inspection and maintenance records. Posts entries on applicable maintenance and inspection records. Records meter reading, test data, and other pertinent data in equipment performance logs. Completes maintenance data collection forms. Recommends methods to improve equipment performance and maintenance procedures.

e. Supervises electronic computer and switching systems repair personnel. Assigns work and reviews completed repairs for compliance with local procedures of installation, maintenance, and repair of electronic computer and switching systems equipment. Conducts or participants in on-the-job training programs.

Exercises (003):

1. One of the duties of the Electronic Computer and Switching Systems Specialist is the accomplishment of prescribed and authorized __________ .

2. During performance or supervision of preventive maintenance on electronic computer and switching systems, one of the performance evaluations calls for evaluation of equipment performance, using prescribed ______ ______________ ____________________________ .

3. During the supervision of electronic computer and switching systems repair personnel, the text states: "Assigns ______________ and ________ completed repairs to insure compliance with local procedures of installation, maintenance, and repair of electronic computer and switching equipment."

004. Specify the AFSC 305X4 Specialty qualifications and mandatory requirements.

Specialty Qualifications. The qualifications for AFSC 30554, as listed in AFR 39-1, are comprised of knowledge, education, experience, and training elements. This CDC helps support the knowledge portion of your specialty qualifications.

You must have a knowledge of electronic principles including integrated and transistor circuits; pulsing techniques, shift registers, counters, buffer, logic gates, and flip-flops; capabilities, limitations, operation and functional use of electronic test equipment; understanding of binary, octal, and hexidecimal numbering systems; basic computer programming techniques; ability to write diagnostic test routines for locating failures; and ability to interpret technical orders, wiring diagrams, and schematic drawings. All the above are mandatory. A knowledge of radar and communications principles is desirable also. As you can see, the knowledge requirements are vast and it is incumbent upon you to stay abreast of the latest developments in the field. Regaining knowledge and gaining new information create a never-ending cycle within the electronics maintenance field.

In the area of education, the completion of high school with courses in physics and mathematics is desirable.

Experience qualifications include installing, repairing, testing, or modifying electronic computer and switching systems equipment; using electronic test equipment; applying of broadband, highly-sensitive oscilloscopes for circuit analysis; and using proper methods of triggering and synchronizing of oscilloscopes in order to examine elusive single or transient pulses. All the above are mandatory.

The completion of a basic electronic computer or switching system maintenance course is mandatory before award of the semiskilled AFSC. You have probably just finished that course and are now ready for the job and OJT to begin.

Other mandatory requirements for your AFSC are:

- Normal color vision, as defined in AFR 160-43, *Medical Examination and Medical Standards.*
- A minimum aptitude level of Electronic 80.
- A Secret security clearance is mandatory for award and retention of the semiskilled/skilled AFSC unless the clearance is administratively downgraded, without prejudice, according to AFR 205-32, *USAF Personnel Security Program.*

Your specialty qualifications are extensive and varied. It is your responsibility to maintain these qualifications and seek maximum proficiency in all areas.

Exercises (004):

1. What document lists the mandatory knowledge requirements for your AFSC?

2. The completion of high school courses in ________ and __________ is desirable.

3. Experience, qualifications related to electronic computer and switching systems equipment include four mandatory functions. List them.

4. A Secret security clearance and eligibility for access to classified information is in accordance with which control document?

1-3. Graduate Evaluation Program

You will be involved in the improvement of formal technical training courses by your participation in the Graduate Evaluation Program. You and your supervisor can insure that future graduates receive correct and useful training by providing accurate data.

005. Name the types of graduate evaluation, and specify the supervisor's responsibilities in the graduate evaluation program.

Graduate Evaluation. The Air Force has established a program to evaluate graduates of the various technical schools. The program is described in AFR 50-38, *Field Evaluation of Education and Training Programs.* The purpose of the program is to improve personnel management courses and formal training programs.

The evaluation system is divided into two parts: (1) field evaluation visits and (2) direct correspondence questionnaire. Field evaluation visits are performed by representatives of the training activity. They visit the using agencies about 4 to 6 months after the graduate has been assigned. In the second method of evaluation, you, as a supervisor, enter into the picture. You are requested to fill out a direct correspondence questionnaire for the school graduates assigned to your unit. You observe the performance of the school graduates in the normal work situation as they perform the tasks listed in the specialty training standard (STS). You record your daily observations in terms of their performance and the supervision they require.

Since these evaluations are needed to pinpoint the ability of graduates to perform the tasks they were trained to do, you should be as accurate in your evaluations as possible. The forms you receive are designed so that you can compare the graduate's performance of tasks with the performance level shown in the STS. In most cases, the performance level for the course and the 3-level AFSC are the same. However, there are some items that the formal course is not capable of teaching to the desired level. In these cases, compare the graduate with the course level code. Be sure that you properly indicate the STS items that are not performed or required. If you have not had a chance to have the graduate perform an STS task, indicate it as "Not performed" on the questionnaire. If a particular task is not required in your unit, the questionnaire should indicate "Not required."

If a graduate does not satisfactorily meet all of the training codes listed in the STS, you should prepare an AF Form 1284, Training Quality Report. Submit this form to ATC and to the Technical Training Center that sent out the questionnaire. Remember, your accuracy in answering the questionnaire and submitting AF Form 1284 aids in improving the formal technical training course.

Exercises (005):

1. What are the two parts of the evaluation system?

2. What do you use as a standard when you are filling out a graduate evaluation questionnaire?

3. What form should you use to report graduates whose training is not up to standard?

4. Why are STS evaluations required from the supervisor?

Security

LIKE SAFETY, security is a topic that applies to each of us all the time. The word "security," of course, refers to the protection of Air Force information and materials. This protection is designed to provide for the Air Force the freedom and secrecy of actions needed to do our part in the national defense.

The fact that you don't handle items marked "classified" doesn't mean you are exempt from taking part in the security program. In fact, those who seldom work in, or with, a security atmosphere, may well be the most vulnerable to another nation's collection of facts related to Air Force operations.

2-1. Security Directives

All Air Force personnel who have knowledge of, or access to, classified information must be familiar with the security directives that apply to them in the performance of their duties.

006. Identify the primary regulation which directs the security program.

Regulations. The Department of Defense has established procedures for control of classified information. DOD 5200.1-R, *Information Security Program* establishes the system for classifying, downgrading, and declassifying information within the United States military organization. DOD 5200.1-R also directs the procedures to safeguard classified information and provides procedures for violations of security.

AFR 205-1, *Information Security Program,* reprints the entire text of DOD 5200.1-R and includes Air Force policy and procedures to supplement Department of Defense policy.

Protection of Air Force resources from ground-based hostile acts is provided by AFR 207-1, *The Air Force Physical Security Program.*

AFR 125-37, *The Resources Protection Program,* gives guidance for protection of nonpriority resources, USAF property, Government resources, USAF property, Government funds, nonnuclear munitions storage areas, and firearms.

Other security directives are found in the 205 series regulations.

Exercises (006):

1. Which regulation directs the classification of information?
2. Which Air Force publication provides Air Force policy on safeguarding information?
3. USAF computers are provided protection from hostile acts by which regulation?

007. Specify the purpose and use of Security Classification Guides and Essential Elements of Friendly Information.

Security Classification Codes. In any action or activity where security is a factor, or access to classified information is called for, certain responsibilities are levied upon the commander or other official charged with the success of the project. These responsibilities include furnishing you with the security classification guidance for the information involved. This guidance is prepared by highly qualified persons who have the needed knowledge and technical intelligence to make reasonable security classification decisions. Once these determinations are made, they are published in the form of a *security classification guide.*

Purpose. As its title suggests, a security classification guide gives you guidance. The guidance is clear, direct instructions, relevant to the most appropriate security classification category of information used in a particular activity. In order to be certain that the correct information is given adequate protection, classification guidance must be detailed enough to allow you to identify the specific information involved. Conversely, the instructions must be flexible enough to permit you to apply a security classification to other information or materials developed during the lifespan of the original activity. The foregoing are the two most important reasons that you must have ready access to an appropriate security classification guide. Its use by anyone who originates classified material or information, and who is not authorized to assign an original security classification, is critical to assuring adequate protection of such information.

Use. When you make any decisions involving classified information or material, you should consult the classification guide issued for the particular activity involved. Using it in this way, a security classification guide helps you:

a. Isolate and identify each piece of information that needs to be classified and is involved in the effort the guide pertains to.

b. Identify the specified level of classification to be applied to each piece of information and material that is developed in connection with the effort involved.

c. Determine the appropriate schedule for phased downgrading and declassification action for each piece of classified information and material involved.

d. Ascertain the provisions that have been established for periodic reviews to determine the currency and accuracy of the classification, downgrading, and declassification guidance provided.

Essential Elements of Friendly Information. To help counter security deviations and help plug intelligence leaks, a program known as Essential Elements of Friendly Information (EEFIs) is used throughout the Department of Defense. This long phrase describes the types or categories of information that, if known by an enemy, could jeopardize the success of a USAF operation. In the Air Force, EEFIs are included in transmission security (TRANSEC). EEFIs are nothing more than listings of sensitive information that should be protected. Air Force regulations require each major command (or separate operating agency) to publish a general listing of EEFIs that apply to the command's overall mission. EEFIs are most effective, however, when prepared by supervisors, and tailored for use in individual workcenters/duty sections.

The following list illustrates the type of information considered Essential Elements of Friendly Information:

(1) Introduction of new equipment.

(2) Security clearances of individuals.

(3) Itineraries of important visitors and purpose of visit.

(4) Requirements or actions that indicate possible operational intent.

(5) Mapping requirements that indicate operational intent.

(6) Nicknames, short titles, or security classification of activities.

(7) Equipment or personnel deficiencies that indicate impairment.

(8) Status of tactical training, combat readiness, or combat efficiency.

(9) Identify, location, movement, or changes in the strength of forces.

(10) Changes in command, mission, organization, or equipment.

You can use EEFIs as a guide to help prevent disclosure of information about your job, your unit, your base, etc. Similar EFFIs are also used by communications security (COMSEC) support units as criteria to evaluate the communications security posture of friendly forces.

Exercises (007):

1. What document identifies the specified levels of classification required for your equipment?

2. How can you verify the accuracy of the date for downgrading the classification of a document?

3. When are EEFIs most effective?

4. What is the purpose of EFFIs?

008. State the purpose, controls, and importance of the industrial security program.

Industrial Security Program. To accomplish its mission as effectively and as economically as possible, the Air Force often enters into contracts with civilian agencies. Some of these agencies, or contractors, at times need classified information to do their job. Of course, when this happens the Air Force releases the needed information. This release does not lessen the sensitivity of the classified information involved or the need for its protection — far from it. The security that must be given classified information in the hands of a contractor is just as important as the protection we give it at our Air Force installations, for any compromise of classified information could seriously affect national defense. This is why the Department of Defense developed the industrial security program.

The industrial security program regulates the protection of classified Government information in the hands of industry. When the Air Force enters into a contract with a civilian contractor who needs classified information, a Security Agreement is drawn up as part of the contract. This is a formal agreement by the contractor to abide by the policies and procedures established by the Department of Defense for the protection of classified information. These policies and procedures are published in the DOD 5220.22-M, *Industrial Security Manual for Safeguarding Classified Information*, and AFR 205-4, *Air Force Participation in the DOD Industrial Security Program*.

This program prescribes the uniform security practices that must be used in industrial plants, educational institutions, and all other facilities used by contractors who have access to, or possession of, classified Government information. Also, it applies to all aspects of contract activity, including preparation of bids and proposals, precontract negotiations, actual performance of the contract, and all postcontract activity.

Exercises (008):

1. What is the purpose of the industrial security program?

2. What controls are levied on a contractor possessing classified USAF information and materials?

3. Why is the industrial security program important?

2-2. Physical Security

In this instance, the term "physical security" applies to the physical security of COMSEC equipment, material, and information. Actually, this COMSEC element is an adaptation of two separate security programs — Information Security and Physical Security. The physical security element of COMSEC simply means using physical measures to prevent unauthorized people from gaining access to COMSEC equipment, material, and documents. Normally, you will not be concerned with this aspect of communications security unless you work in an area where cryptographic material is used. If this is the case, additional guidance would be provided by your local COMSEC custodian.

The physical security program is designed to produce direct and indirect influences. These influences are such that they dissuade or deter an enemy from starting hostile operations against the Air Force. To deter suth actions throughout the Air Force, realistic, gradually increasing levels of protection must be applied to our operational resources, including aircraft, missiles, weapons systems, and associated equipment. Our protective capabilities must also be relative in size and strength to the degree the resource is engaged in retaliatory action. And further, the physical security must be equal to, or better than, the level of ground threat confronting each base and each resource. Several factors are involved in applying these concepts to our resources. The two basic factors you must be aware of are discussed in the following paragraphs.

009. List the priorities assigned operational resources, and define security areas.

Resource Priorities. Each operational resource is evaluated to determine the amount of security it needs. Once this determination is made, the resource is placed in one of three security priorities.

Priority A. Priority A is strictly limited to those Air Force resources most vital to the United States' warmaking ability. These resources include nuclear weapons in storage, on alert, or in transit; selected command, control, and communication facilities; Worldwide Airborne Command Post alert aircraft; and aircraft designated to transport the President of the United States. Priority A security provides for positive and complete control over authorized entry to a restricted area; prevents overt, covert, or clandestine entry to a restricted area; and is designed to make sure that hostile forces seeking to damage or destroy an Air Force resource are intercepted and overcome.

Priority B. Priority B is applicable to nonnuclear alert forces; high value, limited number, or one-of-a-kind aircraft systems; and selected command control and communication facilities. Priority B security requires positive entry control of authorized personnel to a restricted area, and a reasonable means of detecting unauthorized entry into a restricted area at the boundary, while accepting the risk of minimum damage to resources during overt attack.

Priority C. Priority C is assigned to nonalert Air Force resources, which are operational and can be generated to alert status in a minimum of time, and selected command control and communication facilities. Priority C security provides the ability to maintain a reasonable means of intercepting and neutralizing covert intrusions into the restricted area.

Once a security priority is assigned to a resource, it does not mean it will always have the same priority. For example, if a bomber aircraft is removed from alert status, and it does not have nuclear weapons on board, the security priority is changed. In the case of our example, the aircraft may become a priority B resource, if there are no problems with the aircraft. Conversely, if the aircraft needs major repairs, enters maintenance status, and is thus not operational, it would most likely not be assigned any priority.

Security Areas. Whenever a resource has a priority assigned, it must be placed in a secure area. The degree of control over and within thee areas depends upon the priority of the resource. Obviously, the most stringent controls are associated with the highest priority resource. In any case, the security area boundaries are marked clearly with signs, ropes, fences, painted lines, and the like. The two types of security areas are *restricted* and *national defense.*

Restricted area. Used when priority resources are on land under the control or administration of the Department of Defense (DOD), as, for example, on an Air Force base.

National defense area. Used when priority A resources are on land *not* under the control or jurisdiction of the DOD. An example of this would be a priority A alert aircraft that made an emergency landing at a civilian airport.

Exercises (009):

1. What is the concept of the physical security program?

2. List the three priorities of resources in order of their importance.

3. Define the two types of security areas.

010. Identify given threatening situations according to the types of threats they pose.

Nonpriority Resource Vulnerabilities. The protection of Air Force nonpriority resources is outlined in AFR 125-37, *The Resources Protection Program*. This regulation also contains the protective measures needed for such specific resources (USAF property) as nonpriority aircraft, Government funds, nonnuclear munitions storage areas, and firearms.

The following vulnerabilities are presented to give you an overview of the threat that faces our nonpriority resources.

Damage and destruction. This category encompasses any willful act of rendering Air Force equipment or property to a state of uselessness.

What makes people damage or destroy property? This question is so complex that it would take learned professionals to give us any conclusive data. Usually, the short and simple answer is mental disorder or acts of revenge. But don't be alarmed, we are not going to bore you with a long, involved dissertation on mental disorders. All we want to do here is to make you realize that these acts of damage and destruction are common in our society, and that our Air Force is not immune to them. For instance, the person who throws a handful of rocks into the air intake of a jet engine, those who throw rocks at runway lights, shoot small rifles at passing aircraft, or those who kick holes in cabinets housing sensitive radar or computer mechanisms. Granted, these people may not be in the same class as the "Boston Strangler" or San Francisco's "Mr Z," but they are every bit as dangerous to you and to USAF resources.

Loss. Surely, you have heard someone say that "We are our own worst enemy" when describing, as they see it, our involvement in some particular condition or situation. While in most cases this is to harsh an indictment of our people, the old cliché has merit when used in the context of losses of USAF resources.

Losses generally occur when some person fails to properly safeguard resources. It's that simple. Then, why do we continue to lose resources? Why don't people do their jobs and safeguard them? This of course, is an age-old problem that we don't claim to have any simple or sure-cure solutions for. Many factors contribute to losses of resources. These range from inadequate or insufficient management, supervision, training, guidance, and/or discipline, to individual irresponsibility, negligence, complacency, forgetfulness, and even laziness. While these factors are mostly intangible, they indeed hamper the capability of the Air Force to accomplish its mission.

Theft. The term "theft," as used here, is synonymous with pilferage, stealing, and larceny. Each involves the illegal and deliberate taking of USAF property, of any value. This is done either for personal gain or for the benefit of someone other than Air Force. The term "robbery" is nearly the same as theft, since it also involves the illegal and deliberate taking of someone else's property. Robbery, however, differs from theft in that it has the added ingredients of force, violence, or fear.

Theft is committed in many different ways, but it generally results from action planned in advance by one or more persons. This usually involves the circumvention of human controls and physical security measures. On the other hand, is impromptu theft brought about by opportunity? This form, commonly known as *theft of opportunity*, usually stems from another person's failure to safeguard property. The result is that thieves stumble upon an insecure piece of property and take it for their own use.

Regardless of the form it takes, theft is real. It is a problem experienced throughout the Air Force. Theft is clearly very costly, both in terms of money and mission completion capability.

Vandalism. This is the willful or malicious destruction of property. Usually an act of vandalism is less severe than a revengeful act of damage or destruction of resources. Vandalism is normally associated with the destruction of parts of equipment, for instance, smashing the windshield out of a truck, as opposed to rendering the truck completely useless by placing a bomb on the starter.

Hijacking. Aircraft hijacking, a mass kidnap-hostage tactic, has the same basic purpose as the abduction of a single victim. *Skyjacking*, as it is often called, has been a primary weapon of many terrorist groups. But, you must also be concerned with the hijacking or theft of an aircraft from a parked position at an air base. As you will soon see, it can take place.

Resources Affected. When attempting to relate the preceding threats to resources, we could address many areas. However, you should be most concerned with the following.

Nonnuclear munitions. Your prime concern in relation to nonnuclear munitions is the threat of theft because of their value to terrorist, criminal, or dissident factions. Many of these munitions are well suited for illegal purposes. But even worse than that, a terrorist group could use stolen munitions to support their efforts to steal a nuclear weapon. Other threats that must not be overlooked are those of explosion by saboteurs and damage by mentally deranged persons. Any of these acts would certainly have an adverse effect on public confidence in the ability of the military to protect its resources. More directly, such acts would probably impact unfavorably upon you.

Nonpriority aircraft. Nonpriority aircraft are all Air Force aircraft that do not qualify for a specific security priority under the Air Force 207 series security standards. There are several types of threats that you must guard against. Although it may sound unlikely, one of these threats is theft. But who would want to steal an airplane? Believe it or not, it has happened. One incident that stands out, and also one that received worldwide publicity, happened in England. An airman stole a C-130 Hercules and headed out over the Atlantic

Ocean. No one can be absolutely sure why he did it, because no trace of him or the plane was ever found. Some of the other, more obvious and potentially serious threats are those of hijacking, vandalism, and sabotage. Certainly you have read about acts such as these in your local newspaper and can see the impact such an act would have.

Firearms. Firearms are, of course, highly susceptible to theft. Additionally, there is a real danger that stolen military firearms might be used in the commission of criminal or terrorist acts. It is also suspected that many of the weapons stolen from arms rooms throughout the U.S. are traded in foreign countries for narcotics. Additionally, what better source could a terrorist group use to obtain weapons?

Funds. What? Theft — a threat to funds? Who would want to steal money from the Air Force? Certainly the major threat in the case of funds is theft. Pick up any newspaper. Most certainly you can find a news item pertaining to some type of theft of funds. Still, it would amaze you to see how lax some people become about the protection of funds — until they get ripped off.

Exercise (010):

1. Match the hypothetical situations in column A with the statement that best describes the threat to resources in column B, by writing the column B letter in the space provided. Column B items may be used once or not at all.

Column A

___(1) Your base has been alerted to an increase of terrorist activity in the local area. As a precautionary measure your base commander has ordered the posting of guards near the base small arms storage facility.

___(2) In an overseas area a large group of foreign national Air Force employees have been released from their jobs because they are no longer needed. Since their release, the employees have been demonstrating their displeasure by picketing at the main gate. Your base commander has ordered the posting of additional Security Policy in the area near the employees former place of work.

___(3) Your local OSI detachment has uncovered information that leads them to believe a small group of communist sympathizers are strongly interested in relocating to a communist nation. Your commander has ordered an increase in the number of motor patrols assigned to the base transient aircraft area, and Security Policy have been posted at the base aircraft passenger terminal.

___(4) A fire recently destroyed the youth activity center at your base. Since then most youth programs have declined and the base housing occupants have been reporting an increased number of slashed car tires, painted windows, etc. The base commander has thus ordered a curfew and increased motor patrolling on the entire base.

Column B

a. Damage & destruction.
b. Loss.
c. Theft.
d. Vandalism.
e. Hijacking.

011. Identify the individual responsibilities described in the physical security program, and define the terms "Helping Hand" and "Covered Wagon."

Individual Responsibilities. Every person in the Air Force, military or civilian, has responsibilities under the physical security program. Your responsibilities can be broken down into the three progressive "steps" discussed in the following text.

Detection. You are responsible for being alert on your job to detect any security violation or hostile act that may occur.

Alarm. Here, you are responsible for sounding the alarm by shouting "Helping Hand" or "Covered Wagon," as appropriate, and notifying your base Central Security Control (CSC). You tell CSC *what* you detected, *where* it happened, *when* it happened, and, if possible, *who* you detected doing it.

Response. Your final step is to respond to the act you detected. In response, you are responsible for doing whatever you can to either prevent damage, limit damage, stop the person(s) involved, and/or otherwise keep the situation from getting worse. You do these things until the Security Police arrive at the scene at take over from you.

Helping Hand. This is a nickname used Air Force-wide for reporting that a possible hostile event has happened in connection with priority A or B resources. Remember, the keyword here is *possible*. Anytime you suspect that something is wrong, report it to your Security Police unit. In such cases, you should be prepared to give the Security Police a brief description of what you have seen.

Covered Wagon. As with the Helping Hand, this nickname is used to quickly sound the alarm that an actual or probable hostile action has occurred against priority A or B resources. If you discover such actions, you notify the Security Police using the word "Covered Wagon." Again, a brief description helps assure that Security Police can provide correct compensatory actions.

Exercises (011):

1. What are your individual responsibilities under the physical security program?

2. How do you accomplish these responsibilities?

3. Define Helping Hand.

4. Define Covered Wagon.

5. Match the situation in column A with its reporting code terminology in column B by writing the column B letter in the space provided.

Column A	*Column B*
___ (1) You are driving on the flight line and see two individuals crawling on the ground outside the priority A resource area.	a. Helping Hand.
___ (2) As you are reporting your observance of the two individuals, you hear small arms fire coming from the priority A resource area.	b. Covered Wagon.
___ (3) You are working inside a priority B resource area and observe a sergeant not displaying his restricted area credentials authorizing him to be in the area. When you question him about his credentials, he states, "I forgot and left them at home."	

2-3. Electronic Security

The equipment you work on will probably process information which we do not wish to fall into enemy hands. The equipment design includes electronic security protection to prevent transmission of unintentional signals. The following areas include general practices to prevent degrading the security protection built into your equipment.

012. State the purpose of tempest and cryptosecurity.

Tempest. "Tempest" is an unclassified short name referring to investigations and studies of compromising emanations usually electromagnetic in nature. Tempest is concerned with the escape of emanations from equipment processing classified information. Emanation is the unintentional transmission of electromagnetic signals. Escape of signals from equipment that is not processing classified information is not a concern of tempest.

Cryptosecurity. This is the component of COMSEC that results from applying technically sound cryptosystems and their proper use to our communications. In other words, modern electrical means are used to encode, scramble, and otherwise mix up (encrypt) information. This is done so that an enemy intelligence force cannot decipher the meaning of the information, when the information is transmitted from one point to another.

Exercises (012):

1. What is tempest?

2. What is the purpose of cryptosecurity?

3. When are emanations from equipment a security concern?

013. State the maintenance actions that will increase emission security.

Emission security. this part of COMSEC results from all the measures we take to deny unauthorized persons information of value. In particular, this element deals with reducing enemy attempts at intercepting and analyzing information coming from (emanating) cryptographic and telecommunications.

You can help increase emission security when processing classified information by:

- Using and maintaining equipment properly.
- Maintaining the built-in tempest protection.
- Securing all panels and installing all screws.
- Keeping all grounds connected.
- Following TO guidance for maintenance.
- Leaving test equipment disconnected.
- Using radio receivers in areas away from the equipment.

If you find a tempest problem, tell your supervisor and tempest representative, but do not spread the word any further. Tempest weaknesses are classified as high as the highest classified information being processed. Knowledge of a tempest weakness is like having the combination to the safe. Contact your tempest representative with any questions or problems concerning security.

Exercises (013)

1. What is the objective of emission security?

2. What should you check before allowing operators to process classified information on equipment that has been repaired?

3. Whom should you tell if you find a tempest weakness?

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CHAPTER 3

Air Force Occupational Safety and Health (AFOSH) Program

A FEW YEARS AGO, at one of the large bases on the eastern seaboard, a young electronics maintenance man was killed which changing fuses in a ground radio transmitter. The victim was highly skilled, with more than 4 years of experience in electronics work, yet he was killed while performing the simple and uncomplicated task of changing a fuse. After an extensive investigation, it was concluded that the victim's high level of skill and experience probably was the main cause of the accident; he had become overconfident and careless from constant exposure to a high-voltage environment. The investigation report showed that he was electrocuted while removing a 3000-volt fuse *with his bare hands!* This happened even though less than 4 feet away there was a safety board containing protective gloves and insulated fuse pullers needed to remove the fuse safely.

What happened to the young electronics man is not uncommon. When initially assigned to work in a dangerous environment, such as near high voltage or currents, the average person tends to be highly cautious. After an extended period without accidents, however, the mind begins to relax and take for granted that, when no accidents happen, the whole thing cannot possibly be as dangerous as it originally seemed. The electronics man we mentioned was not killed due to lack of skill; instead, he was killed because he had become so familiar with equipment that he relaxed and ignored one of the basic rules of electronics safety: *Never relax your safety standards, because surrounded by high voltage, you seldom get more than one chance to make an error.* Unfortunately, accidents are not restricted to electrocutions.

In this chapter we will discuss the Air Force Occupational Safety and Health (AFOSH) program and hazards encountered in the 305X4 Career Field.

014. State the purpose of the AFOSH program and the individual responsibilities under the program.

The AFOSH Program. The requirement for an Air Force safety and health program was established as a result of the Occupational Safety and Health Act and Executive Order 11807. AFR 127-12, *Air Force Occupational Safety and Health Program*, establishes the Air Force policy and designates organizations responsible for the program.

The program's purpose is to develop and enforce standards to insure safe and healthful working conditions for all personnel in the Air Force. Periodic inspections and evaluations will be conducted by qualified safety, fire prevention, and medical personnel. Any unhealthy or unsafe conditions discovered will be eliminated. An important requirement of the program is that all supervisors and employees will be given safety and health training. Make sure the training is given anytime a change in assignment, equipment, procedure, process, and/or standards occurs.

Under this regulation you have a responsibility to yourself and others to maintain a safe and healthy work environment. Specific individual responsibilities are as follows:

a. Comply with AFOSH standards.

b. Report unsafe or unhealthy standards, using AF Form 457, USAF Hazard Report.

c. Report any injury or illness acquired due to job-related circumstances.

d. Wear or use required protective clothing and equipment.

e. Work safely.

Exercises (014):

1. What would your responsibility be if you discovered an unsafe condition on the job?

2. State an important requirement of the AFOSH program concerning all supervisors and employees.

3. What is the purpose of the AFOSH program?

3-1. Accident Sources

Equipment components are possible accident sources even though they are quite safe under normal conditions. Carelessness combined with an accident source can result in personal injury or equipment damage. A knowledge of common accident sources is necessary if you are to avoid the hazards.

015. Identify hazards associated with voltage/current sources, and state the corresponding precautions to take.

Voltage/Current. There is a common misconception that it takes a high voltage to kill you — somewhere from 300 volts on up. It is not the voltage that kills; it is the current. Even a low voltage kills if there is enough current. A high voltage may be harmless if the amount of current is small. It takes only 1/10 of an ampere to kill the average person.

Resistance to electrical current depends on skin thickness and on such body conditions as:

• *External resistance:*	
Dry skin	100,000 to 600,000 ohms
Wet skin	1,000 ohms
• *Internal resistance:*	
Hand to foot	400 to 600 ohms
Ear to ear	100 ohms

You can see from these figures that the internal resistance of the body is fairly low. Further, you can see that the skin offers a fairly high resistance unless it it wet. Even then it is considerably higher than the internal resistance of the body. Suppose, for example, that you were standing on a good electrical ground. Assuming a total resistance of 1500 ohms (skin, body, and ground contacts), it would take only 150 volts to produce the 1/10 ampere required to kill. This circuit also follows the rules of ohms law. The body resistance could be lower and the voltage required to produce a fatal current would also be lower. Less than fatal current will cause muscular contractions and breathing difficulty. Muscular contractions have led to other injuries and caused fatal contact with higher voltage.

Another factor to consider is the path of current flow. A path from the right hand to the right elbow would be less likely to kill than current flow from the left hand, through the heart area, to the right hand. Current flow through the heart could cause it to stop. Keeping one hand in your pocket could prevent this situation.

Power supplies. Power supplies are a source of both voltage and current. They have the current capability to kill if your body resistance is low enough. A high-current capability in the low-voltage power supplies can make a ring red hot in an instant, producing nasty burns. The problem doesn't end at the power supply because the power distribution system carries the high-current capability to all parts of the computer.

Capacitors. Capacitors are designed to store a voltage charge. Some capacitors can discharge a considerable current through rings, screwdrivers, or probe tips. This usually arc-welds the metal to the capacitor terminal and spatters molten metal into eyes or on nearby skin. The capacitor will store the voltage for a long time after the equipment is turned off. Some capacitors tend to recharge themselves after you discharge them through an external resistance. If you have to work close to these, you could clip on a resistor across the terminals to keep them discharged until you are finished.

Storage batteries. Batteries have high-current capability that can arc-weld metal to its terminals. In addition to splattered molten metal, the spark produced could ignite the hydrogen gas which is present because of the charging action of the battery. The explosion that results could also rupture the battery case spreading the battery acid over the area and anyone nearby, producing burns and possibly blindness. The explosion could also be triggered by smoking near a battery.

Exercises (015):

1. What hazards are present with power supplies?

2. What precautions should you take when working near capacitors?

3. How can you avoid the hazards related to batteries?

016. Specify the hazards associated with cathode ray tubes and the corresponding precautions.

Cathode Ray Tubes. You should exercise extreme cautious when handling a cathode ray tube (CRT). The glass envelope encloses a high vacuum, and because of the large surface area, the envelope is subject to considerable force from atmospheric pressure. The total force due to atmospheric pressure exerted on a 10-inch CRT, for example, is 3750 pounds, or nearly 2 tons. Over 1000 pounds are exerted on the face alone. Flying glass form an imploding CRT can cause serious injury. Extra precautions are necessary when handling high-vacuum tubes.

For protection of both tubes and personnel, tubes are packaged and centrally positioned in cardboard containers. Retain CRTs in their original shipping container until removed for actual installation or for inspection and test. Never store a CRT without its original packaging.

In addition to the danger of implosion due to breakage, rough handling may also cause displacement of the electrodes within the tube. Eye protection is required for all personnel working in the immediate vicinity of an exposed CRT. Handling of larger diameter tubes should be accomplished by two workers.

Required handling practices for all tubes are:

(1) Prior to handling a tube, ground all pin connections including high voltage connection to preclude electrical shock.

(2) During installation or removal of cathode ray tubes larger than 6 inches in diameter, personal protective equipment consisting of a heavy-canvas apron, gauntlet-type gloves, and full face shield will be worn to prevent injuries if it implodes.

(3) Avoid scratching the glass of a tube, since such

scratches weaken the tube and can cause failure.

(4) Do not place a tube on its side on a flat surface. Instead, place the tube face down on a nonabrasive pad of suitable material.

(5) Remove tube from its shipping/storage container face up by grasping the larger, or bell end. Avoid handling large tubes by the neck since the narrow portion of the tube is particularly susceptible to breakage from bumping or striking other objects.

(6) Special-handling instructions are normally provided by manufacturers for tubes having an external insulation coating applied to areas of the bell end. Avoid touching the coated areas. If not otherwise instructed, the installation can usually be done by grasping the rim of the bell, holding the neck end only for guiding the base into position.

(7) For those tubes not having integral implosion protection, a safety glass faceplate is used over the screen. Newer tubes use a bonded faceplate or a similar method of integral implosion protection, eliminating this requirement. Many of the older type tubes are still in use, however, and the safety precautions will be observed.

(8) Old or unusable tubes will be handled with the same precautions that apply to new tubes. Unless otherwise directed, destroy old or unusable tubes prior to disposal. Place the tube in a steel container or sealed carton that has a hole in the top just large enough for a crowbar or similar instrument and smash the tube. An alternate method is to break the evacuation tube located at the end of the neck. After destroying the tube, and before placing into bulk waste containers, seal the residue in the original shipping/storage container or equivalent container, using tape.

(9) If broken glass from the tube cuts the skin, such cuts are to be washed immediately to remove dirt, phosphorus, or other particles. Immediate medical attention will be obtained for all cuts.

(10) In the event of equipment fires, personnel will use only Halon 1211 or 1301 extinguishers on sets containing cathode ray tubes. Using a carbon dioxide fire extinguisher on a CRT may cause it to fracture and implode.

(11) Contact bioenvironmental engineering services for an evaluation of the potential X-ray hazard and appropriate shielding required for tubes operating at higher than 16 kV rating.

Exercise (016):

1. What personal protective equipment should you use during CRT installation?

2. Why do you ground the pin connections of a CRT before handling it?

3. What causes the implosion hazard with a CRT?

4. Why can't you use a carbon dioxide fire extinguisher on a CRT?

017. Specify soldering hazards and corresponding precautions.

Soldering. Soldering is a safe process if you recognize the hazards and observe normal safety precautions.

When using soldering irons and guns, be careful to select the proper wattage for the job. You don't need a blowtorch to unsolder a resistor; a 20- to 40-watt pencil-type iron will do the job without damaging surrounding components or injuring you.

Care must be taken to prevent burns from a soldering iron. If soldering is done on a regular basis it is essential to develop a work area for this task. Within this area you will need a holder for the soldering iron that will reliably hold the iron and protect people from accidentally touching the tip. Keep flammables such as paper and solvents away from this area to prevent fire. A fire extinguisher should be close at hand just in case. Don't leave the soldering iron on and unattended. The next person could get burned because they thought it was off.

Hot melted solder is a problem if in the wrong places. Don't flick the solder off the tip; instead, a damp sponge does an excellent job of removing excess solder and old flux. It is necessary to wear clothing that will prevent molten solder from splashing on your skin. Your reaction to a solder-splash burn might cause you to cut yourself on sharp edges or contact high voltage. If you are doing light soldering, use safety glasses or prescription glasses to prevent solder from splashing into your eyes. If you are doing heavier work, a face shield would give you more protection. Keep in mind that the finished solder connection is still hot enough to burn even after the solder has solidified. Allow the finished item to cool before handling.

A small vise or clamp attached to your workbench will make your work easier and safer. You will be less likely to drop the item or get burned.

Ventilation is important in the soldering work area. Inhaling the vaporized fluxes is annoying and unhealthy. The amount of ventilation depends on the amount of flux vapors generated. If you are doing heavy soldering in a confined area, you should use a respirator.

Some of the fluxes used are acids which adds to the problem. These acid-core solders should not be used on electronic equipment because they will cause corrosion problems. In addition the acid may spatter on your skin and on the electronic components during the soldering operation.

Exercises (017):

1. What are some of the things you can do to prevent burning yourself on a soldering iron?

2. Why should you use a clamp or vice to hold the unit to be soldered?

3. What can you do to reduce the possibility of splattering molten solder in your eyes?

018. Specify the hazards encountered with sharp edges within equipment cabinets.

Sharp Edges. Equipment cabinets are designed to look good and have no sharp edges. That is true of the outside of the cabinets but inside is a different story. As a maintenance person, you will spend a lot of time with your hands and arms inside the cabinets. Most of the steel cabinets are stamped out of sheet metal. The manufacturing process leaves a sharp, ragged edge similar to a serrated steak knife. If care is not taken, these edges can cause severe cuts, especially when you become engrossed in your task or when you react to an electrical shock. Wearing long-sleeved fatigues will give some protection to your arms. Make it a habit to keep hands and arms clear of these edges when using meters or oscilloscopes inside the cabinets. Leave yourself plenty of room and don't overreach or lose your balance. You can use shields to protect you from the sharp edges and the high voltage.

Some solder joints and wirewrap connections leave the pointed ends of wires sticking out like needles. This might not cause too much injury, but your reaction may bring you in contact with high voltage or the sharp cabinet edges.

Exercises (018):

1. What factor makes the sharp edges inside an equipment cabinet more likely to cause injury?

2. What risk does a maintenance person encounter inside a computer cabinet?

3. What precautions should you take when working inside equipment cabinets?

019. Specify the hazard associated with the misuse of tools.

Misuse of Tools. In performing our job of computer equipment maintenance, we use a wide variety of tools, from the common screwdriver to oscilloscopes. All of these tools can injury you if used improperly or carelessly.

Small wrenches and screwdrivers are the most commonly misused handtools. Most people fail to select the proper wrench or screwdriver for the job. When a tool is too small for the job, the blade does not fill the width of the slotted screw, bolt, etc. Pressure is exerted upon too small a surface, and there is inadequate leverage. This damages the tool, the screw, the bolt, or other unit.

In selecting screwdrivers and wrenches, you should exercise the same care. Be sure you select the right size, shape, and length to do the job. Never use a screwdriver or a wrench as a pinch bar, lever, or chisel. Never use a screwdriver or wrench to check an electrical circuit. DANGER OF SEVERE BURNS, BLINDNESS, AND EVEN DEATH occurs if the tool is shorted across a high-potential source. This can occur even if power was removed from the electrical circuit prior to starting maintenance.

It is also dangerous when you hold work in your hand. If the tool slips, you can be cut; or if the tool is a screwdriver, you can sink the blade directly into your hand. Be careful when working on separate end-item equipment. Put it on the bench or, if possible, in a vise to steady it while attempting adjustment or disassembly.

Pliers, hammers, punches, and wire strippers fall into similar categories when handtool safety is considered. For instance, by using the wrong size or type of pliers you may damage equipment. Generally, a wrench will do the job much better. Disastrous results can only be expected when you misuse tools. Misuse of tools costs the Air Force many dollars in lost time, damaged equipment, and mission degradation.

When using an abrasive device on electronic equipment, such as a small file or emery cloth, be sure to clean up the residue created before installing the device and power-on operation. The residue from the metal deposits could be a perfect path for current flow, and just might end up too close for comfort.

When using a paint scraper or a wire brush, be sure to wear goggles. This will protect your eyes from flying paint chips. If using a portable electric drill with a wire brush in it, be sure to properly use a grounded drill case, as well as a safe 3-wire extension cord, when necessary. When stripping paint with a brush-on or spray-on paint remover, use gloves. When necessary to work on vertical surfaces, be sure to wear an apron. This will protect your clothing as well as your skin.

We have mentioned most of the tools of the cleaning trade except the vacuum cleaner. Remember: *Do not stick the metal nozzle of a vacuum cleaner into equipment with the power still applied to the equipment.* If it is necessary to vacuum the inside of the cabinets or drawers, remove the power first, and then use the crevice attachment on the end of the vacuum hose to get into all of the corners.

Occasionally, there might be a sandblasting operation in progress on your equipment, installation, or antenna. For your own safety, stay as clear of the area as you can. Notice the protective clothing and equipment the operators must use. Safety and caution are the bywords.

When using test equipment, be sure to select the correct test instrument for the test to be performed. Some electrical computer or switching equipment may use power supplies that are isolated from the ground; therefore, it is very important to use an isolation transformer with the equipment and employ test equipment. Be sure to consult the TO or technical manual for specific information concerning operation and any warnings or cautions about the use of the equipment. Beforehand preparation should always include inspection of scope or meter leads to assure that they are serviceable and not dangerous to use. In all cases, when possible, connect the test instrument to be used into the circuit before turning the power on. If you find it necessary to make a power-on check, take extreme care in inserting test leads into live circuits. Another precaution is to be sure that you use the proper scale for the voltage, current, or waveform to be observed. Otherwise, damage to the test instrument or personal injury could result.

Use circuit extenders when possible. This reduces the possibility of short-circuiting other components when a power-on test must be performed. Another factor that is related to the use of circuit extenders or drawer extender cables is the proper selection of test-lead connectors. In today's modern miniaturized circuitry, many specialized connectors are used in conjunction with existing standard test leads. Consequently, selecting the proper test-lead connector can be an important factor to both your safety and the safety of the equipment.

The care of handtools and power equipment is more the application of common sense than anything. Who really likes to reach into a toolbox and grab a greasy screwdriver or wrench? Not only is it going to get your hands dirty, but if you use the tool when it is not clean, your hand could slip; then you are right back into the accident-prone pattern of haphazard maintenance, which damages equipment and injures personnel. Clean all tools before storage and be sure that they are repaired properly. If not, tell your supervisor about the problem so that the faulty equipment can be replaced before an accident happens. The same principle applies to test equipment. If for some reason you receive a shock from the test gear while using it, don't put it back on the shelf. Repair it immediately to prevent an accident. PREVENTION OF ACCIDENTS IS 90 PERCENT OF THE BATTLE.

Exercises (019):

1. Give the safety precautions you should take when using these items.
   a. Screwdriver.

   b. Pliers.

   c. Punch.

   d. Soldering iron or gun.

   e. Paint scraper.

   f. Paint remover.

   g. Vacuum cleaner.

2. What safety precautions should you observe when selecting a piece of test equipment for circuit measurement?

3. Why is it important for you to select the proper test-lead connectors?

020. Specify the precautions to consider when using cleaning chemicals.

Cleaning Chemicals. The first and most common of the cleaning agents used in the operations and maintenance sections is a general, *all-purpose cleaner* that is good for cleaning any equipment surface. There are no particular precautions in handling this agent except during cleaning of equipment when the power is on. Excessive use of this liquid could cause it to seep into energized circuits and cause something to blow. Therefore, use it sparingly — just enough to get the job done without bathing the equipment.

Another general area is the paint-up, fix-up projects that are part of our necessary equipment maintenance. In these projects, you will be using paints of both the brush-on and spray-on type. Painting should always be done in a well-ventilated area. Before using a specific type of paint, READ THE LABEL! It will tell you what precautions to observe and how to clean up when you have completed the job. It will provide specific directions to insure perfect results.

When using an *aerosol-type spray paint*, be careful not to pierce the can with any sharp object. This could result in the entire contents either exploding or, at the very least, spewing out and getting in your eyes. If this occurs, flush your eyes immediately with running water, and report to a doctor. While using the brush-on type paints, there is usually no danger present until the job is completed. Brush cleanup is done with either water or some type of *paint thinner*. Paint thinner is normally extremely volatile. Don't smoke or strike a match while accomplishing this task or the results *will be disastrous*.

In many instances, before painting, a brush-on or spray-on *paint remover* is used to get rid of old scaled or bubbled paint. This paint remover is very caustic and, if accidentally splashed into the eyes or on your hand, flush immediately with running water and report to a doctor. You should wear gloves or other protective gear when using a paint remover. In the maintenance environment, use the above mentioned items on an as needed basis. In addition, you will be using some of the chemicals or cleaning agents discussed in the following paragraphs.

The normal cleaning agents found in the maintenance shop are: (1) Freon, (2) isopropyl alcohol, (3) trichloroethylene, (4) contact cleaner, and (5) water dispersal lubricant, which is an aromatic hydrocarbon solvent. Though this is not a complete list, these are the most common chemicals in the shop.

Freon is normally used for cleaning printed circuit boards, integrated circuit components, and board assemblies. It leaves no oily residue and, consequently, no possible path for accidental current flow or component shorting. The only precaution to be observed while using Freon is not to spray it toward yourself. Although there might not be any physical damage if you get it into your eyes, the sudden cooling effect of Freon might cause you to react violently, and with temporary loss of sight, you could injure yourself on some object within your immediate area.

Isopropyl alcohol is normally used to clean glass areas without leaving any film or residue. It cleans quickly and thoroughly, but be careful not to smoke or light a match while using it or an instant explosion or a fire will result. Another cleaner similar to isopropyl alcohol and its cleaning ability is *trichloroethylene*. The biggest difference between the two is that trichloroethylene is practically nonflammable. It is normally used for cleaning all electronic equipment and is accepted as the all-purpose cleaner in ground electronics. Trichloroethylene is a narcotic and anesthetic material. Organic injury rarely results from acute exposure, but chronic overexposure can cause anemia and liver damage. Use it only in a well-ventilated space, and make sure that users keep their hands out of it.

Occasionally, when you have a problematic potentiometer that works part of the time only, *contact cleaner* can be the answer. Normally, you use it for cleaning switches and potentiometers. Be careful not to spray it into your eyes on your coworker's eyes. If contact cleaner is sprayed into a potentiometer it tends to spray out the other holes in unexpected directions. A cloth can be used to catch the cleaner and prevent it from dripping on other parts. Be sure to read all cautions on the label for any particular hazards.

Water dispersal lubricant, described as an aromatic hydrocarbon solvent, is normally used in corrosion control actions. It has the characteristic of doing what its name implies — dispersing water from within an area where it might be trapped. The only precaution needed here is to READ THE LABEL.

Normally, external storage is required for volatile substances. Also, there will be NO SMOKING signs posted, indicating no smoking within 50 feet. This 50-foot rule also applies to areas where diesel fuel is stored. Note the specific instructions contained in the Site Operating Procedures. Always comply with all ground safety regulations pertinent to storage of volatile substances.

Don't store oily cloths — get rid of them! If they are reusable, send them to the base laundry. Paper wipes are often used while cleaning equipment and should be thrown away when the job at hand has been finished. Cotton-tipped swabs are also often used and should likewise be disposed of.

Exercises (020):

State the precautions that you should use for the following cleaning agent or equipment.

1. Storing volatile solutions.

2. Smoking in or around an area containing volatile solutions or diesel fuel.

3. Contact cleaner.

4. Using a spray-on or brush-on paint removal agent.

021. Specify the housekeeping practices that contribute to making the work area safer.

Housekeeping. Right now you are probably thinking, "I do all those things to eliminate accident sources and causes," Do you? Take a look around your work area.

Are all the tools either in use or in their proper places; how about the test equipment? Are the dust covers on the equipment properly; if not, is it because someone is working on the equipment? If a dust cover is off, is it in the aisle where it can be damaged, or is it stored properly? Let's look further. Are rags, cleaning solvents, lubricants, or miscellaneous hardware lying about, on or under the workbench? What does the floor look like? In your tour of the area, did you have to step over or around trash, tools, test equipment, or TOs that should not have been there? Were there any slick spots on the floor caused by some spilled liquid, such as oil, coffee, or coke? We have only scratched the surface, but by now you probably have a good idea of what we are talking about.

Tools, tech orders, and test equipment should never be left on ladders or in the aisles once the work has stopped. Also, they should not be left lying on a bench once the job is done. If we put our equipment away when we are through working, we not only eliminate a possible accident, we also know where to find the equipment the next time we need it.

Equipment dust covers are helpful because they cut down equipment problems due to dust and dirt in the air. A misplaced cover could become a tripping or slipping hazard if allowed to remain on the floor. Putting things in their proper places is essential to a safe shop.

The disposal of oily or dirty rags and the storage of flammable liquids are of considerable concern to all of us. Fire not only destroys millions of dollars worth of buildings and equipment each year, but it also claims thousands of lives. Simple measures, such as storing flammable liquids in an outside storage area and putting rags in a can with a self-closing lid, reduce the chance of fire.

Objects on the floor and slick spots due to spilled coffee, water, wax, etc., in combination with a person in a hurry, could cause a broken leg, arm, or worse. Small scraps of wire in and around the main distribution frame (MDF), unused patchcords around a patch panel, and punchcard/paper tape residue around peripheral equipment are often sources of potential accidents.

Good housekeeping in the work area is an essential ingredient of the safety and health program. It not only makes a safe work area, it also gives your work place that clean, professional appearance. Poor housekeeping practices such as putting matches or cigarettes in trash cans, and messy work areas can cause accidents.

Exercises (021):

1. Why is it a good practice to install dust covers on equipment that is not in use?

2. What may result from storing oily rags in an open container?

3. Why can't you wait until the end of the shift to clean up the paper tape residue around the paper tape punch?

3-2. Precautions

Because of the hazards which are around your work area, you need to observe precautions to prevent injury and damage. The best safety precaution will be worthless unless you use it.

022. Correlate the precautions used around computer equipment to the hazards that should be avoided.

Safety Observer. Let's talk about a safety procedure that can be one of the most important to you. We call it the buddy system. Some commands have been using this system for a long time; maybe yours is one. You may call it something difference, but the policy is "Do not work alone around electronic equipment in the shop if you can possibly avoid it." If the equipment you are working on is capable of 50 volts and 100 milliamperes AC or 500 milliamperes DC, you must use the two-man concept or buddy system. In fact, AFOSH Standard 127-50, *Ground Communications-Electronics (C-E) Systems,* states that you must use the two-man concept, or buddy system. In fact, AFOSH 127-50 directs that there be a safety observer present anytime someone works on high-voltage equipment. Be sure to read AFOSH 127-50 in regard to safety practices around voltage and equipment.

The reason the buddy system is so effective should not need much explaining; surely you see the advantage. It is one of those extra-extra safety precautions that truly pay off if someone should get into trouble. This trouble might be touching a live circuit and suffering shock, or it might be falling from a stand or ladder. In either case, the buddy system can help keep an accident from becoming a fatality by providing immediate aid.

The buddy system has a practical side in addition to the safety it provides. Anytime you are working on electronic gear that requires the operation of remote switches or controls, it is handy and saves time if you have someone to operate them. This benefit is just as valuable in shop maintenance as outside the shop. In this type of cooperative maintenance, make sure that you have your signals straight as to when switches or controls are to be activated. Confusion over signals could cause you to touch a live circuit that you thought was dead.

Equipment Grounding. Make certain that the equipment is properly grounded. Ground all test equipment to the equipment under test. If you experience a tingle when touching two pieces of equipment, something is wrong with the grounding system and needs to be corrected before the tingle becomes deadly.

Insulating Equipment. Rubber floor matting is extra insurance against electrical shock. Use rubber gloves when called for in the maintenance procedure. Make sure the gloves are in good condition. Check them for holes and insulation breakdown.

Technical Guidance. Technical guidance provides the safest method to perform a task. Some shortcuts can lead to problems. If you have an idea that will improve procedures, get it approved before you put it into practice.

Safety Boards. Safety boards provide an easily identifiable location for safety equipment. AFOSH Standard 127-50 lists the items of equipment to place on the safety board.

Terminal Strip Shields. Shields over terminal strips reduce the exposure to voltage/current. Some are provided with small holes for test probes.

Extender Boards. Use extender boards when possible to prevent working in a tight situation and shorting the circuit.

Fuses/Circuit Breakers. Fuses and circuit breakers were designed to protect the equipment, but they should not be expected to protect people. When working in the equipment, pull the fuses or circuit breakers to insure the equipment is not energized.

Signs. Put a sign on the fuse/breaker box to prevent others from turning them on while you are working. Signs inform people and prevent accidents.

Fire Extinguishers. Have the correct type available. A bad situation could become a disaster by using a water-type extinguisher on energized circuits or a carbon dioxide extinguisher on a CRT.

AFOSH Standard 127-50, *Ground Communications-Electronic (C-E) Systems*, provides the guidance to prevent accidents in the maintenance area, but only you can prevent the accident.

Exercises (022):

1. Match the hazard in column B to the precautions in column A.

Column A

___ (1) Safety observer.
___ (2) Rubber gloves.
___ (3) Terminal strip shields.
___ (4) Signs.
___ (5) Equipment grounding.
___ (6) Extender boards.
___ (7) Fire extinguisher.

Column B

a. Shorting circuits.
b. Fire.
c. Electrical shock.
d. Exposed voltage.
e. Voltage potential between equipment cabinets.
f. Loss of life due to electrical shock.
g. Other people energizing equipment while you are working on it.

CHAPTER 4

Air Force Publication

HAVE YOU EVER started to do a job without any idea of how to do it, where to start, or what you need to complete it? For us in the Air Force, this is where the publications system comes into play. The Air Force's publication management system will save you time and energy. Why should you waste time making up procedures when others have already done it for you?

4-1. Organization of Publications

As computer maintenance people, we are concerned with two categories of Air Force publications, standard publications, and technical orders. Standard publications provide us with guidance in administrative task while technical orders direct our maintenance activities.

023. Identify Air Force publications as either departmental or field.

Classes of Publications. Air Force publications are divided into two general classes — departmental and field.

Departmental. These publications which are issued by Headquarters USAF, may apply to that specific headquarters and one or more major commands. All Department of Defense (DOD) directives and instructions are implemented through USAF. Examples of Air Force departmental publications are Air Force regulations (AFRs), Air Force manuals (AFMs), and Air Force pamphlets (AFPs). As you can see, all begin with AF, which makes them readily identifiable as departmental publications.

Field. Field publications are issued at the major command level (or below) for use within the jurisdiction of the issuing organization. Examples of field publications are: Strategic Air Command manuals (SACMs), Tactical Air Command regulations (TACRs), and Air Training Command pamphlets (ATCPs). Each command issues manuals, regulations, and pamphlets as necessary. The fact that AF is not used to designate a field publication, and the abbreviations of the major command are used, makes it easy to identify this type of publication. Therefore the class of a publication can be determined by noting the alpha characters preceding the publication number.

Exercises (023):

1. How do departmental publications and field publications differ in origin?

2. Identify the following publications as either departmental or field.
   a. AFR 10-1.
   b. AFR 30-1.
   c. ATCM 52-2.
   d. ADCM 65-1.
   e. SACR 66-1.

024. Identify each Air Force publication with the proper publication category.

Categories of Published Material. Published material issued by the Air Force are categorized as: standard publications, specialized publications, periodicals, non-Air Force publications or miscellaneous issuances.

Standard publications. Standard publications are established for issuance by the Secretary of the Air Force; Chief of Staff, USAF; commanders; and staff officials at all levels to announce policies, assign responsibilities, prescribe procedures, direct actions, and inform or motivate people. Authorized types include regulations, manuals, operating instructions, supplements, pamphlets, visual aids, bulletins, and staff digests.

Specialized publications. Headquarters USAF or major commands may authorize a command to use a specialized system of publications to issue information of a highly specialized nature that cannot be published in a standard publication (for example, the technical order system and career development courses). A specialized publication system is a "standalone" system. It does not interface with, change, or supersede any standard publication.

Periodicals. These are informally written publications, such as magazines and newsletters, used to publish nondirective material needed by an organization to accomplish its assigned mission. Their main purpose is to foster greater understanding and knowledge of the Air Force and its varied missions and functions. The *Airman Magazine* and *Driver* are examples of periodicals.

Non-Air Force publications. The Air Force uses publications that originate in other Federal departments or agencies, such as the Department of Defense, Office of Personnel Management, and Federal Aviation Administration (FAA), when they apply or are of interest to Air Force organizations.

Miscellaneous issuances. The Air Force issues other printed material such as: administrative orders, Air Force newspapers, base guides, directories, and recruiting material.

Exercise (024):

1. Match the publication category in column A to the description in column B.

Column A	*Column B*
___ (1) Standard.	a. An FAA regulation.
___ (2) Specialized.	b. "Flying Safety" magazine.
___ (3) Periodical.	c. PCS orders.
___ (4) Non-Air Force.	d. AFP 39–7.
___ (5) Miscellaneous.	e. CDC 30554.

4-2. Standard Publications

In an organization as large as the Air Force it is necessary to organize and standardize our efforts. Standard publications provide the guidance for this organization and standardization. To use this guidance you must be able to find the information for each task you perform. The structure of the standard publication system provides a place in the file for each type of information.

025. Identify types of publications by functions and descriptions.

Types of Publications. Standard publications are frequently used throughout the Air Force. There are eight types of standard publications: regulations, manuals, operating instructions, supplements, pamphlets, visual aids and staff digests.

Regulations. Air Force regulations (AFR) contain directive and policy material and assign responsibilities. They may include brief procedural details when necessary. Regulations are usually permanent in nature. Air Force regulations are the most numerous of all Air Force standard publications.

Manuals. Air Force manuals (AFM) give detailed instructions that tell personnel how to perform their duties. It may include policies and assign responsibilities. Because of their similarity to regulations they are being converted to regulations as they are revised.

Operating instructions. Operating instructions (OIs) are similar to regulations but apply only within the issuing headquarters. These instructions are designated "Headquarters Operating Instructions" (HOI), "Branch Operating Instructions" (BOI), etc. OIs must comply with existing higher level directives and be updated accordingly.

Supplements. Supplements are used by lower headquarters to implement, amplify, interpret, or clarify a higher level publication. A supplement does not change the intent of the basic publication.

Pamphlets. Air Force pamphlets (AFP) usually contain information of a nondirective nature. They are written in an informal style and are usually published in brochure or booklet form.

Visual aids. Visual aids are charts, posters, or graphic illustrations for indefinite use or display. They are used in connection with planned operations or programs.

Bulletins. Bulletins contain announcements, notices, and temporary instructions. For example, daily or weekly bulletins fall into this category.

Staff digests. These contain summaries of significant staff actions, important announcements, and special notices. They are issued periodically, or when needed, and at various command levels.

Exercises (025):

Identify the type of each standard publication described below.

1. Similar to regulations, but apply only within the issuing headquarters.

2. Illustrations for indefinite use in conjunction with planned operations or programs.

3. Contain directive and policy material and assign responsibilities.

4. Are written in an informal style and usually contain information of a nondirective nature.

5. May direct the step-by-step performance of a specific task.

026. State the significance of each part of the standard publication numbering system.

Numbering Systems. The Air Force has adopted a subject and numbering system to identify publications as to their subject and organize filing procedures. Complete details are contained in AFR 5–4, *Numbering Publications.* The first digit identifies a broad area. For example the 5 in AFR 5–4 tells us that it deals with the area of publications management. This number is referred to as the publication base number. Some of the base numbers you will use are:

Base No.	*Subject Area*
0	Indexes
35	Military Personnel
39	Enlisted Personnel
50	Training
67	Supply
205	Security

To designate subjects more specifically, a dash and another number (dash number) is added. For example, AFM 67-1, AFP 67-2, and AFR 67-4, all deal with the "Supply" area. The dash numbers indicate a specific area within Supply.

Remember that every Air Force publication is given a number and a subject title. These two items are of great importance because they make it possible to index and categorize all publications in an orderly fashion. This in turn makes it simple for you to locate any publication quickly and easily for reference purposes.

Exercises (026):

1. What is the purpose of the first number in a publication number?
2. What does the dash number of a publication number indicate?
3. Why do Air Force publications have a double-number system?

027. Identify publication indexes with their contents.

Indexes. There were two indexes to Air Force publications which you will work with most often. AFR 0-2, *Numerical Index of Standard and Recurring Air Force Publications,* lists all current regulations, manuals, pamphlets and visual aids and the latest publication date of each. AFR 0-9, *Numerical Index of Departmental Forms*, lists all forms and current edition date.

AFR 0-2 is arranged in numerical order and by subject numbers and lists all publications on a subject. A listing in the front of AFR 0-2 provides all the subjects and the corresponding base number. Information on the office which is responsible for the publication is included in the OPR column (office of primary responsibility). Information on distribution of each publication is also listed in AFR 0-2.

The information contained in these indexes can be used to verify that you are using the correct up-to-date information. These indexes are published every 3 months to keep them current.

Exercises (027):

1. What index would you use to verify that an Air Force publication is current?
2. What index do you use to find the title if you know the form number?
3. What publication lists the office of primary responsibility for each regulation?

028. State filing procedures used to update and maintain standard publications.

Filing Procedures. You may not be required to file publications, but you should be able to verify that the publications you use are available and current. AFR 0-2 is used for this purpose. The procedure is similar for standard and other publications. First, go to the official file and check the publication date in the index. The AFR 0-2 lists regulations, manuals, and pamphlets mixed in one section. Sine all three publications may have the same number, the letters R, M, and P will have to be used to distinguish between the types. Your publication account representative will use a system of writing a status symbol in the left margin in front of each publication ordered for the file. A plus (+) is written for each publication on hand. A minus (−) indicates that a publication is needed and ordered but is not on hand. Publications not required have no marks in front of them.

Plus and minus signs also indicate which changes are included in the publication. Supplements by commands and below are listed in their index.

Exercises (028):

1. Where can you find an updated reference indicating all publications in your file?
2. What annotation in AFR 0-2 indicates a publication is on order?
3. How can you verify that the copy of a regulation that you are using is the latest version?

4-3. Technical Orders

As a maintenance specialist, you must know how to use Air Force technical orders (TOs). You are also required to operate and maintain your equipment according to procedures described in the TO for your system. These policies and requirements are established by AFR 8-2, *Air Force Technical Order System.* AFR 8-2 describes the TO system as the official method for disseminating technical data, instructions, and safety procedures relating to the operation, installation, maintenance and modification of Air Force equipment and materials.

029. List the types of Air Force technical orders, and state the kind of information found in them.

Types of Technical Orders. There are many types of technical orders. However, we are going to limit ourselves to the type you will be working with most often. More extensive, procedural information on TOs is given in Technical Orders 00-5-1 and 00-5-2, the *AF Technical Order System* and the *Technical Order Distribution System,* respectively.

Technical manuals (TMs). A TM contains instructions designed to meet the needs of personnel engaged or being trained in the operation, maintenance, service, overhaul, installation, and inspection of equipment and material. The FM can be general in nature, dealing with a subject area such as transistor fundamentals, or it may be directed at specific equipment, such as your computer or switching system.

A second type of technical manual is the Methods and Procedures Technical Order (MPTO). This TO is used to establish policies and provide information and instructions on maintenance management or administration, configuration management, etc. Examples are all 00-5 series, 00-25 series, 00-35 series, and D-series publications.

Time compliance technical order (TCTO). A TCTO gives instructions for modifying equipment, performing or initially establishing special inspections, or imposing temporary flight restrictions. TO 00-5-15, *Air Force Time Compliance Technical Order System,* establishes policies and procedures for the TCTO system. We will go into much greater detail about TCTOs later in this chapter.

Abbreviated TOs. These TOs are primarily work simplification devices such as checklists, inspection workcards, lubrication charts, or sequence charts. Preventive maintenance workcards that you will use for your equipment fall in this category. These workcards follow the guidance setup by MPTOs and are written for specific pieces of equipment.

Index type technical orders. These technical orders are lists that show the availability of technical orders. They also provide a cross-reference to other publications when necessary. Any technical order can be located when you know how to use index-type technical orders. A further discussion of these TOs and their importance is contained in the next section.

Preliminary TO. This type of TO is made up in a small quantity to test and verify the information that it contains. Preliminary TOs are used for the first test or early production of new equipment or systems. You can use these TOs for training but they are not to be used for operation or maintenance of the equipment. After the data in a preliminary TO is debugged, it may become the formal TO for the equipment or system.

Use of commercial manuals. Some of you may have equipment or systems that are new to the Air Force inventory. In this case, you may have to use the commercial manuals which come with the system. If the commercial literature is usable from a technical standpoint and it would be cheaper to use, the Air Force will assign a TO number and manage it like any other TO in the system. The essential requirement for using the manufacturer's technical data is that it must not degrade the system operation, support, or reliability.

Exercises (029):

1. What TOs give you the procedural information on how to use the technical order system?

2. What kind of TO is used for testing or training but not for operation of a system?

3. If you wanted to locate a TO on your system, what type of TO should you use?

4. List the types of TOs you work with most often.

030. Identify parts of a technical order number by their functions.

Numbering System. The TO numbering system is designed to give us as much information as possible in an alphanumeric combination. If you understand the various parts of the TO number, it will be easier to locate the proper TO and to maintain a TO file.

Technical order numbers are divided into three or more parts, each part separate from the others by a dash (-). Each numerical index and requirement table (NI&RT) has a preface which explains the numbering system for that index. For the purposes of explanation, we are going to dissect the TO number 33A1-12-216-1. This TO is the operating and service instructions for a Model 260 volt-ohm-milliameter. The first two digits of this TO number are 33 which represents the TO category, namely, General Purpose Test and Associated Equipment. The NI&RT is TO 0-1-33-1 and the preface to that index explains the breakdown of the TO number as outlined below.

TO 33A1 - 12 - 216 - 1

Category = 33
Major Group = A
Specific Type of Major Group = 1
Specific Item = 12
General Series, Type, Model, or Part Number = 216
Kind of TO and Individual Publication = 1

The last and final part of the TO number reflects the type of publication as follows:

Operating Instructions: −1, −11, −21, etc., through −491.
Service or maintenance instructions: −2, −12, −22, etc., through −492.
Overhaul instructions and/or circuit and schematic diagrams: −3, −13, −33, etc., through −493.
Illustrated Parts Breakdown/Parts catalog: −4, −14, −44, etc., through −494.
Planning data and/or installation instructions: −5, −15, −55, etc., through −495.
Preventive maintenance instructions: −6, −16, −66, etc., through −496.
Standard installation instructions: −7, −17, −77, etc., through −497.
Inspection and testing procedures: −8, −18, −88, etc., through −498.
Alignment procedures: −9, −19, −99, etc., through −499.
E&I standards: −10, −20, −30, etc.
Time compliance technical orders: −501 through −1000, then −1500 through −2000.

Letters within a TO number may also identify a kind of TO. These represent the abbreviated TOs discussed earlier in the text and are identified as follows:

CL	Check List
CT	Checkout Tape or Cards
SC	Sequence Chart
S	Operational Supplement
SS	Safety Supplements
VS	Visual Slide
WC	Work Card
WS	Work Sheet

TO 33A1-12-216-1 has not been fully identified. With the TO and equipment in hand you should be able to correctly operate the Model 260 for maximum benefit in your maintenance effort.

Exercises (030):

1. What kind of TO is TO 31S5-4-52-16WC-1?

2. The last part of a four-part TO number is −44; what do those digits indicate?

3. Where in the NI&RT is the explanation for the TO numbers assigned in that index?

031. Specify the correct TO index required to locate the information needed on a system.

Indexes. The index-type TO, which was identified earlier, gives you a means of locating the information needed to perform operational and maintenance tasks on your equipment or system. There are two options you may use to locate a technical order. First are the many numerical indexes available that are grouped according to equipment type, such as airborne, ground, special purpose, etc. Second is the alphabetical index which allows you to locate a TO number from an equipment-group name.

Numerical index and requirement tables (NI&RTs). TO 0-1-01, the index of all indexes, is the first place to go for general information about the NI&RTs and a list of all indexes in numerical order. EAch NI&RT covers TOs that have been grouped together, based on the similarity of equipment functions or family grouping. The numbering pattern of each category of TO is outlined in the preface of the NI&RT category can be determined from the first part of the TO number as shown in figure 4-1. Examples of the numbers used for specific categories of equipment you should be familiar with are:

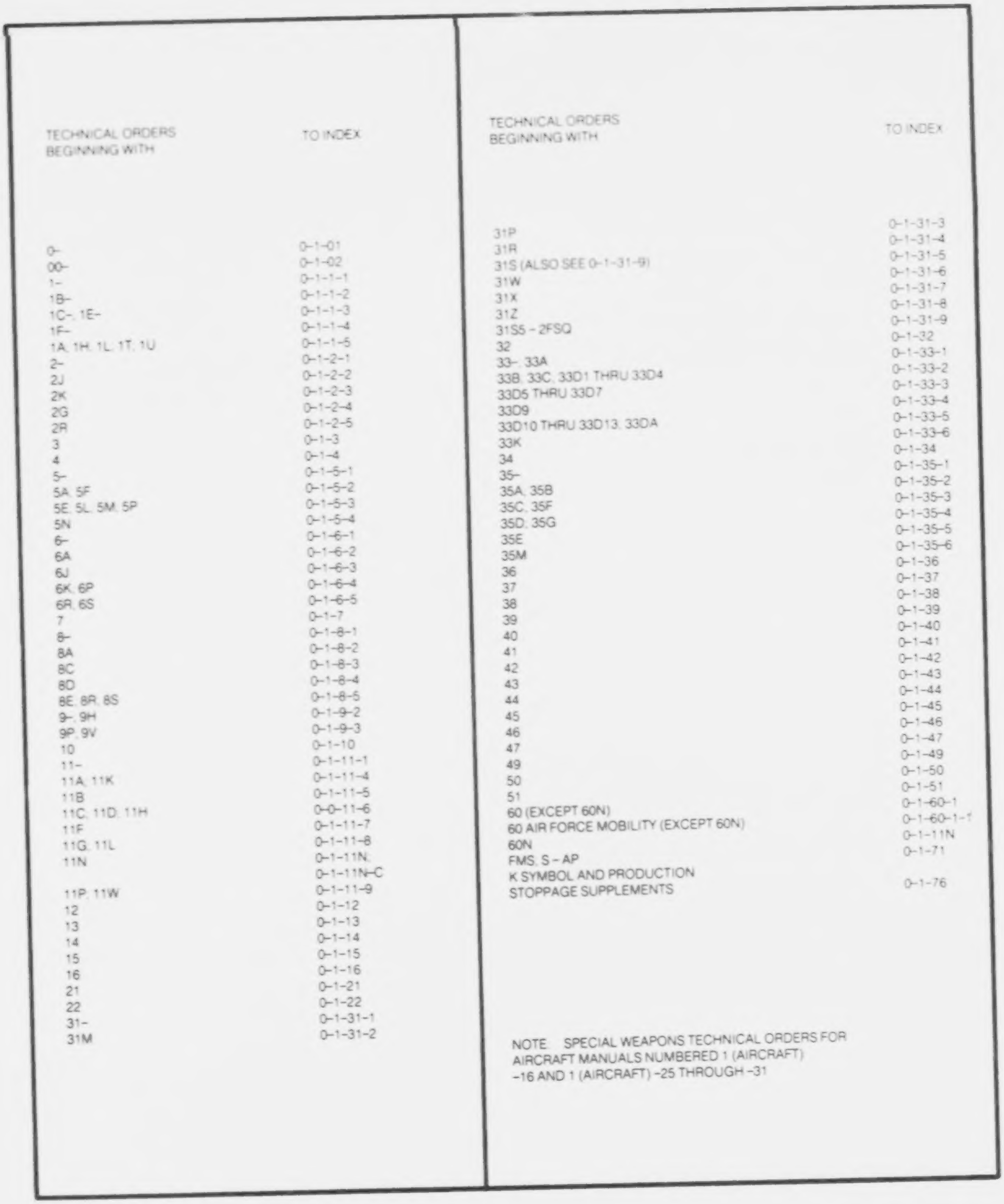
- 0, Indexes.
- 00, General Technical Orders.
- 12, Airborne Electronic Equipment.
- 31, General Electronic.
- 33, General Purpose Test and Associated Equipment.

Along with numerical listings, the NI&RT will indicate the availability of a TO, the issue date, date of any change(s), and its security classification, if it has one.

Alphabetical index. The alphabetical index, TO 0-2-1, provides an easy method of locating the correct TO category when the type of equipment is known. This TO does not give the status but refers you to the proper NI&RT category. The list of applicable technical orders provides listings of all TOs applicable to a specific weapon or system. It helps determine the contents of limits TO files, which may need to be established. Proper use of these indexes will enable you to locate other TOs needed to perform your duties.

Exercises (031):

1. What is the TO number of the index of indexes?



TECHNICAL ORDERS BEGINNING WITH	TO INDEX
0–	0–1–01
00–	0–1–02
1–	0–1–1–1
1B–	0–1–1–2
1C–, 1E–	0–1–1–3
1F–	0–1–1–4
1A, 1H, 1L, 1T, 1U	0–1–1–5
2–	0–1–2–1
2J	0–1–2–2
2K	0–1–2–3
2G	0–1–2–4
2R	0–1–2–5
3	0–1–3
4	0–1–4
5–	0–1–5–1
5A, 5F	0–1–5–2
5E, 5L, 5M, 5P	0–1–5–3
5N	0–1–5–4
6–	0–1–6–1
6A	0–1–6–2
6J	0–1–6–3
6K, 6P	0–1–6–4
6R, 6S	0–1–6–5
7	0–1–7
8–	0–1–8–1
8A	0–1–8–2
8C	0–1–8–3
8D	0–1–8–4
8E, 8R, 8S	0–1–8–5
9–, 9H	0–1–9–2
9P, 9V	0–1–9–3
10	0–1–10
11–	0–1–11–1
11A, 11K	0–1–11–4
11B	0–1–11–5
11C, 11D, 11H	0–0–11–6
11F	0–1–11–7
11G, 11L	0–1–11–8
11N	0–1–11N, 0–1–11N–C
11P, 11W	0–1–11–9
12	0–1–12
13	0–1–13
14	0–1–14
15	0–1–15
16	0–1–16
21	0–1–21
22	0–1–22
31–	0–1–31–1
31M	0–1–31–2
31P	0–1–31–3
31R	0–1–31–4
31S (ALSO SEE 0–1–31–9)	0–1–31–5
31W	0–1–31–6
31X	0–1–31–7
31Z	0–1–31–8
31S5 – 2FSQ	0–1–31–9
32	0–1–32
33–, 33A	0–1–33–1
33B, 33C, 33D1 THRU 33D4	0–1–33–2
33D5 THRU 33D7	0–1–33–3
33D9	0–1–33–4
33D10 THRU 33D13, 33DA	0–1–33–5
33K	0–1–33–6
34	0–1–34
35–	0–1–35–1
35A, 35B	0–1–35–2
35C, 35F	0–1–35–3
35D, 35G	0–1–35–4
35E	0–1–35–5
35M	0–1–35–6
36	0–1–36
37	0–1–37
38	0–1–38
39	0–1–39
40	0–1–40
41	0–1–41
42	0–1–42
43	0–1–43
44	0–1–44
45	0–1–45
46	0–1–46
47	0–1–47
49	0–1–49
50	0–1–50
51	0–1–51
60 (EXCEPT 60N)	0–1–60–1
60 AIR FORCE MOBILITY (EXCEPT 60N)	0–1–60–1–1
60N	0–1–11N
FMS, S – AP	0–1–71
K SYMBOL AND PRODUCTION STOPPAGE SUPPLEMENTS	0–1–76

NOTE: SPECIAL WEAPONS TECHNICAL ORDERS FOR AIRCRAFT MANUALS NUMBERED 1 (AIRCRAFT) –16 AND 1 (AIRCRAFT) –25 THROUGH –31

Figure 4-1. Preface page from NI&RT 0–1–01.

2. Using the TO 0-1-01 listing in figure 4-1, what would you use to determine the latest basic date of a TO in the 33C series?

032. Specify TO filing procedures.

Filing Procedures. You may, at one time or another, be assigned to maintain your organization's TO file. If not, you surely will need a TO when performing maintenance and accomplishing preventive maintenance inspections (PMIs). Therefore, you must know how to find out if the TO file has the TO you need and, secondly, is the TO current and filed correctly? For these reasons and because it is required that a TO be used for performing maintenance tasks on equipment, a knowledge of TO files and how to use them is important.

TO 00-5-2, *Technical Order Distribution System*, states: "technical order files are authorized to provide quick access to TOs required by all personnel at all echelons for the most efficient, economical, and safe accomplishment of assigned duties." TO 00-5-2 provides the policy and procedures necessary to establish and maintain TO files. If you are tasked to maintain a TO file, this TO will be your guidance. Several types of files are authorized but you will be primarily concerned with the operational type.

The operational file is located within the maintenance organization and contains only those TOs that are required for maintenance of assigned equipment and/or systems. Maintenance of the file record is the responsibility of the activity that keeps the file in a current status. Normally, only one copy of a TO will be in the file unless you are required to do the same maintenance action at the same time at different places. These additional copies are authorized only if they are mission essential. Of course, your file record must indicate the number of copies you have on hand. Speaking of a file record, what is it?

The file record is made up of the AFTO Form 110, Technical Order Distribution Record, as shown in figure 4-2A and figure 4-2B. One form is completed for every TO in your file and the form is arranged in NI&RT sequence. The AFTO 110s are used to maintain a record of TOs required, received, redistributed, and TOs maintained, if your activity maintains one or more separate TO files.

All entries to the AFTO 110 should be in pencil to permit changing the information required. The AFTO 110 contains information such as the TO number, the NI&RT reference, number of copies authorized, number of copies on hand, date of the basic TO and changes, and date of distribution. By comparing dates on this form with dates listed in the NI&RT, you can verify if your TO is current before you begin to use it.

Exercises (032):

1. Who must maintain a file of AFTO Forms 110?

2. What is the AFTO Form 110 compared against to insure TO files are current?

3. Where would you find the information on how to establish a TO file?

4. What is the essential requirement for having more than one copy of a TO in an operational file?

033. State the types of technical manuals and their purposes.

Technical Manuals. Technical manuals provide guidance on installation, operation, servicing, and overhaul of Air Force equipment and material. Some complex systems or equipment require a specific type of manual such as a maintenance manual or parts breakdown. These manuals may be published in sections. Each section is a separate publication and has a separate TO number. For less complex items, specific types of instructions may be published in a single manual.

The operating instructions technical manual provides a general description of the equipment, a detailed description of the component parts (or assemblies), the preparation for operation instructions, and the operating instructions.

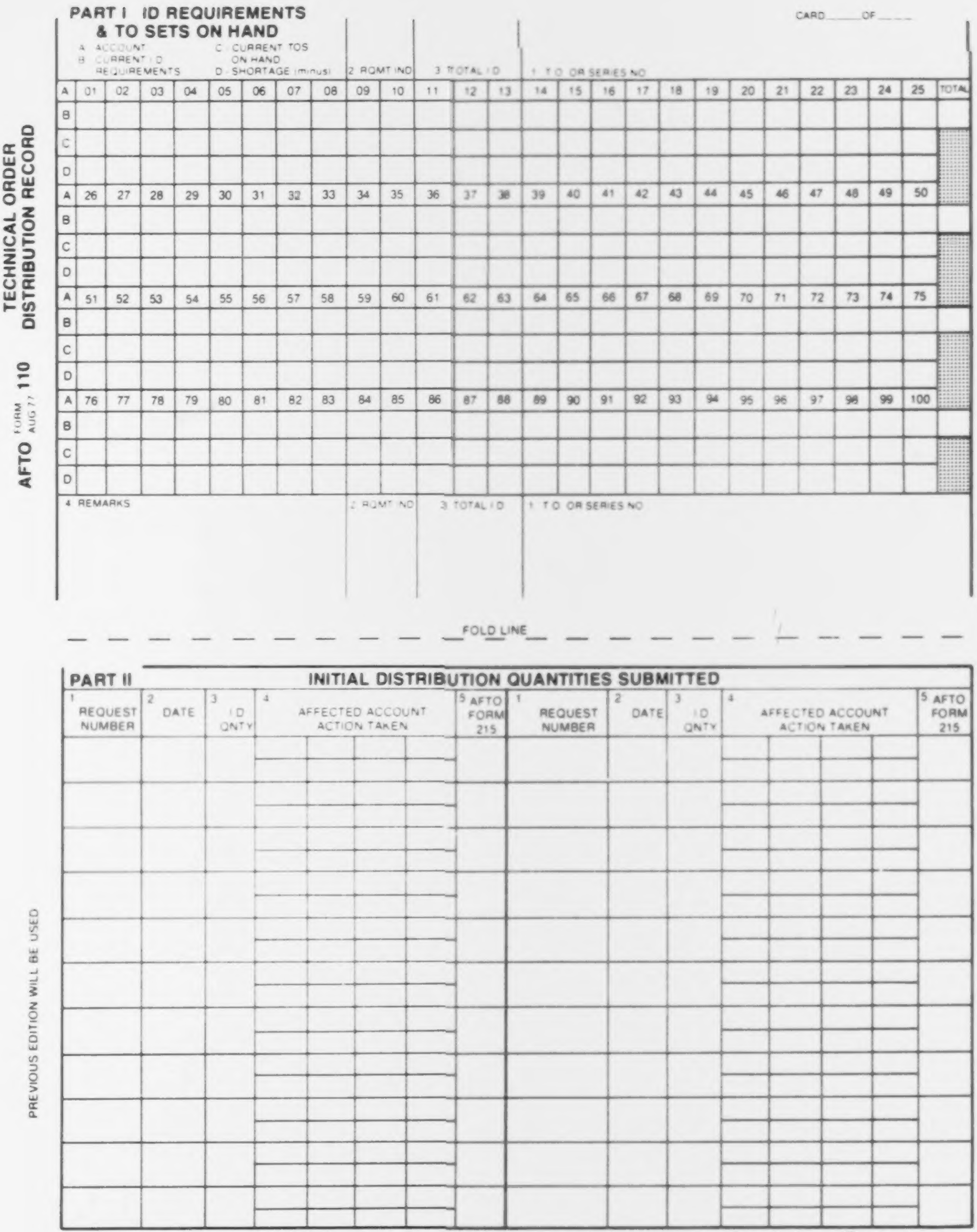
The servicing instructions contain information pertinent to the periodic inspection, maintenance, and lubrication of the components in the item of equipment. Some of these technical manuals also include troubleshooting and calibration instructions.

The illustrated parts breakdown (IPB) technical manuals contain component part breakdowns that are used for identifying, requisitioning, storing, and determining disassembly and reassembly sequence. Each component parts breakdown lists part numbers, nomenclature, and other information necessary to support the item of equipment. Also, it includes illustrations of assemblies and subassemblies which identify in detail each component part.

A technical manual for less complex equipment, published as one manual, may contain the following:

a. Operation, service, and repair instructions. In addition to a description of component parts, operation procedures, and other characteristics, these manuals contain instructions for equipment repair, inspection, lubrication, and adjustments.

b. Overhaul instructions. These manuals describe equipment characteristics and provide detailed instruc-



AFTO FORM AUG 77 110 TECHNICAL ORDER DISTRIBUTION RECORD

PART I ID REQUIREMENTS & TO SETS ON HAND

CARD ____ OF ____

A - ACCOUNT
B - CURRENT I D REQUIREMENTS
C - CURRENT TOS ON HAND
D - SHORTAGE (minus)

2 RQMT IND

3 TOTAL I D

1 T O OR SERIES NO

A	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	TOTAL
B																										
C																										
D																										
A	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	
B																										
C																										
D																										
A	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	
B																										
C																										
D																										
A	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	
B																										
C																										
D																										

4 REMARKS

2 RQMT IND

3 TOTAL I D

1 T O OR SERIES NO

FOLD LINE

PART II INITIAL DISTRIBUTION QUANTITIES SUBMITTED

1 REQUEST NUMBER	2 DATE	3 I D QNTY	4 AFFECTED ACCOUNT ACTION TAKEN	5 AFTO FORM 215	1 REQUEST NUMBER	2 DATE	3 I D QNTY	4 AFFECTED ACCOUNT ACTION TAKEN	5 AFTO FORM 215

PREVIOUS EDITION WILL BE USED

[illegible] 3-[illegible]

Figure 4-2A. AFTO Form 110 (front).

44

PART III INITIAL DISTRIBUTION RECORD

1. TECHNICAL ORDER NO. SUP/CHG/ CHG NO. OR REV	2. T.O. DATE	3. CLAS	4. QNTY RCVD	5. DISTR DATE	6. ACCOUNT AND QUANTITY SHORT											7. TOTAL SHORT	8. SHORTAGE RCVD DATE

FOLD LINE

PART IV REQUISITION DISTRIBUTION RECORD

1. TECHNICAL ORDER NUMBER	2. DATE OF RQN	3. REQUEST NUMBER	4. QUANTITY RQND	5. ACCOUNT AND QUANTITY REQUISITIONED											6. DATE RCVD	7. AMT RCVD	8. AFTO 215/ 221 RCVD

Figure 4-2B. AFTO Form 110 (back).

tions on the disassembly and reassembly of major components.

c. Overhaul instructions with parts breakdown. In addition to the instructions on disassembly and reassembly, these manuals contain breakdowns used for identifying, requisitioning, storing, and determining the sequence for disassembly and reassembly.

d. Inspection instructions. These manuals contain requirements for maintenance inspection and replacement of accessories and components.

Exercises (033):

1. Which technical manual is used for identifying and requisitioning parts?

2. Where are periodic inspections of items of equipment found?

3. Which technical manual contains a detailed description of component parts or subassemblies?

034. List the types of TCTOs, and state how they are used.

Time Compliance Technical Orders (TCTOs). We briefly defined TCTOs earlier in this chapter. Now we are going to look at them in greater detail. As we said earlier, TCTOs are the instructions for modifying equipment, doing special inspections, and imposing flight restrictions when they become necessary. These instructions, depending on the severity of the TCTO, will have an established time limit in which the work must be done. Because of the urgent nature of these publications, you must be familiar with the policies and procedures established by TO 00-5-15.

Each TCTO is assigned a degree of urgency at the time it is approved. Only three urgency designations are authorized for TCTOs. These designations are the Immediate, Urgent, and Routine action TCTOs. If the problem if very urgent, the TCTO is first issued as an Interim technical order, which is transmitted by electrical message or another means of rapid communication. The degree of urgency is indicated in the instructions by specifying when compliance is required. The highest degree of urgency is assigned to the Immediate Action TCTO.

Immediate action TCTOs are issued when unsafe conditions exist that could result in fatal or serious injury to personnel or damage to property. The urgency of these TCTOs will require immediate action to ground aircraft, prevent launch of missiles, discontinue operation of ground communication – electronics maintenance (CEM) systems, or use of related support equipment. How to correct the condition will also be included in the TCTO, if known. The words IMMEDIATE ACTION are printed in red at the top of the first page with a border of red X's included around the first page. Because of their urgency, commanders shall insure that Immediate Action TCTOs are disseminated to all affected personnel within 4 hours after receipt.

Urgent action TCTOs are issued when combat necessity or potentially hazardous conditions, which could result in injury to personnel, damage to property, or unacceptable reductions in combat efficiency occur. The urgency of these TCTOs require compliance within 1 to 10 days. If compliance is not accomplished by the end of the 10-day limit, action to ground aircraft, discontinue operation of ground communications, electronics, or use of support equipment, personnel equipment, materials, or munitions, will be taken. The words URGENT ACTION are printed in red at the top center of the first page and a series of red diagonals alternately spaced with circled red X's are printed around the border of the first page.

Routine Action TCTOs contain instructions to remedy defects of equipment or faulty procedures. Failure to solve these problems might reduce operational life, affect efficiency, or create a hazard through prolonged use of the equipment. This type of TCTO is printed on plain white paper without any red border symbols. There are several classes of this TCTO with a number of categories in each class. Routine TCTOs deal primarily in the areas affecting safety or logistics support and whether or not a problem reduces or degrades the ability to accomplish an assigned mission. Time compliance for a TCTO in this category varies depending upon the class and who is assigned responsibility for accomplishing the TCTO. Complete guidance on the routine action TCTO is contained in TO 00-5-15.

Exercises (034):

1. List the three authorized urgency designations used with TCTOs.

2. What is the time for compliance when an immediate action TCTO is received?

3. What purpose does the Interim technical order serve?

4. What action is taken on the expiration of the compliance time period of an Urgent Action TCTO?

035. Identify the abbreviated technical orders with their use and contents.

Abbreviated Technical Orders. Primarily, these technical orders are used as work simplification devices which aid personnel in carrying out instructions that are contained in other types of technical orders.

Inspection workcards. These are sets of cards that prescribe minimum inspection requirements given the –6 technical manual in a checklist form. Because they are card size, they can be taken to the job while performing a scheduled inspection. Work assignment information is given on each card; this feature makes it convenient when assigning work to maintenance personnel. Also, the work can be arranged by areas, leading to efficient maintenance scheduling and planning. The inspection requirements on each card are arranged to provide a logical sequence of performance. Charts on the reverse side of selected cards pictorially located each work area and indicate the code and title of the areas referred to in each set of cards. In the planned inspection maintenance concept, the inspection workcards are used with the inspection sequence charts.

Inspection sequence charts. These are also provided in sets similar to the workcards. However, sequence charts are used only for scheduled inspections, and they show a basic planned-work schedule or sequence which permits efficient accomplishment of the inspection. The charts serve as a guide in preparing the actual work schedule for each particular inspection, and they are intended to control the assignment of work during an inspection.

Checklist. Checklist contain tasks listed chronologically for a maintenance team to perform. Each task is performed in the proper sequence and is checked off when it has been completed. Certain checklist are arranged in a two-column, demand-response format. Demands, which are the tasks listed in sequence, are in the left column; and responses to the demands are marked in the right-hand column. Like the workcards, checklists are printed in sets and in a size that is convenient to use on the job. The letters "CL" are part of a checklist's technical order numerical designator.

You may use checklists that are authorized and prepared by the headquarters of your particular command. You may use other checklists prepared locally by your maintenance activity. In any case, the importance of following the steps as given in these checklists cannot be overemphasized.

Exercises (035):

1. What is the purpose of an abbreviated TO?

2. State the format used in a two-column, demand-response checklist?

3. What provides the minimum inspection requirements of the –6 technical order in a convenient form?

036. Specify selected procedures, authority, and sources of data related to technical order deficiency reporting.

Technical Order Deficiency Reporting. The term "deficiency" denotes an error or defect that changes the meaning of instructions or terms or affects equipment operation or maintenance. A deficiency with a technical order would be an error or omission of a technical nature that prevents the adequate performance of maintenance required for mission accomplishment. Typographical errors and misspelled words are not reportable under the TO reporting system.

If you discover a condition requiring a change to a technical order, submit an AFTO Form 22 (fig. 4-3). There are three types of reports described in TO 00–5–1. These are the emergency, urgent, and routine improvement reports. Emergency reports will be submitted immediately after discovery of the condition, urgent reports on an expedited basis, and routine reports are soon as practicable.

Complete the report form with the specific information that identifies the suspected error. Only one deficiency is authorized per form. Provide the TO number in columns 6 through 30; include the page and paragraph number in blocks 7 and 8 and the figure number in block 9 if you are referring to a schematic. Enter other information as required by TO 00–5–1 and be sure to include a well-written description of the deficiency and recommend changes.

What happens to the AFTO Form 22 once it is initiated? First, your supervisor checks to see if the deficiency is valid and warrants reporting. Second, the report goes to the quality control section for approval. Then, it goes to the Air Force Logistics Command (AFLC) depot responsible for the TO. Action is then taken on the report.

Your organization will follow up on an emergency report after 60 hours, an urgent report after 45 days, and a routine report after 90 days. Submit the followup request through the same channels as the original report.

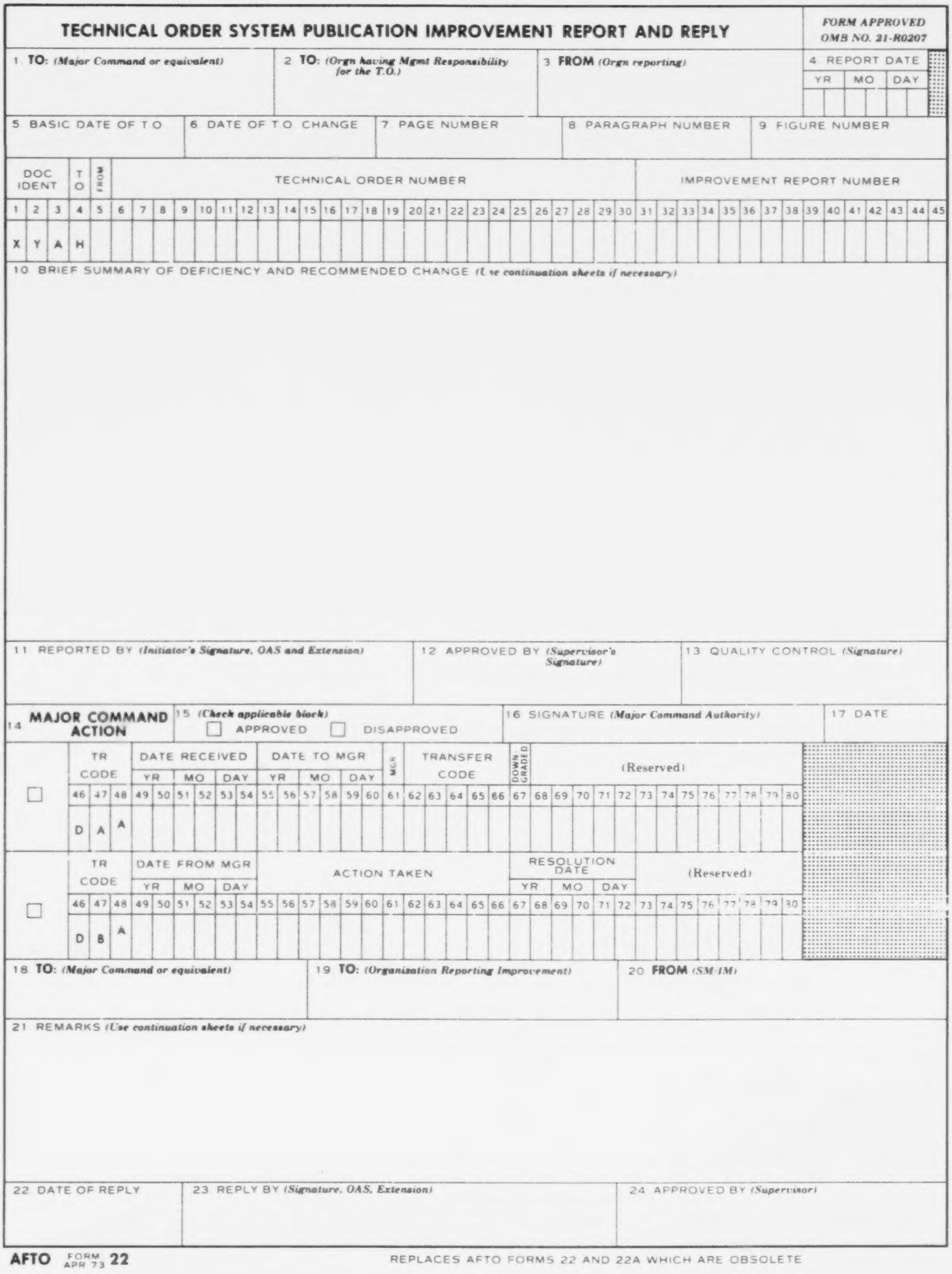
Exercises (036):

1. Who should submit an AFTO Form 22?

2. What type of errors should not be reported?

3. If you found a suspected error, where should you look to find out how to report this error?

4. When should you follow up on a routine report?



TECHNICAL ORDER SYSTEM PUBLICATION IMPROVEMENT REPORT AND REPLY

FORM APPROVED
OMB NO. 21-R0207

1. **TO:** *(Major Command or equivalent)*

2. **TO:** *(Orgn having Mgmt Responsibility for the T.O.)*

3. **FROM** *(Orgn reporting)*

4. REPORT DATE — YR | MO | DAY

5. BASIC DATE OF T.O.

6. DATE OF T.O. CHANGE

7. PAGE NUMBER

8. PARAGRAPH NUMBER

9. FIGURE NUMBER

DOC IDENT			TO	FROM	TECHNICAL ORDER NUMBER																									IMPROVEMENT REPORT NUMBER														
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45
X	Y	A	H																																									

10. BRIEF SUMMARY OF DEFICIENCY AND RECOMMENDED CHANGE *(Use continuation sheets if necessary)*

11. REPORTED BY *(Initiator's Signature, OAS and Extension)*

12. APPROVED BY *(Supervisor's Signature)*

13. QUALITY CONTROL *(Signature)*

14. **MAJOR COMMAND ACTION**

15. *(Check applicable block)* ☐ APPROVED ☐ DISAPPROVED

16. SIGNATURE *(Major Command Authority)*

17. DATE

☐	TR CODE			DATE RECEIVED						DATE TO MGR						MGR	TRANSFER CODE					DOWN GRADED	(Reserved)												
				YR		MO		DAY		YR		MO		DAY																					
	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
	D	A	A																																

☐	TR CODE			DATE FROM MGR						ACTION TAKEN												RESOLUTION DATE						(Reserved)							
				YR		MO		DAY														YR		MO		DAY									
	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
	D	B	A																																

18. **TO:** *(Major Command or equivalent)*

19. **TO:** *(Organization Reporting Improvement)*

20. **FROM** *(SM/IM)*

21. REMARKS *(Use continuation sheets if necessary)*

22. DATE OF REPLY

23. REPLY BY *(Signature, OAS, Extension)*

24. APPROVED BY *(Supervisor)*

AFTO FORM APR 73 **22**

REPLACES AFTO FORMS 22 AND 22A WHICH ARE OBSOLETE

Figure 4-3.

CHAPTER 5

Communications-Electronics Maintenance Management

WHEN YOU CONSIDER the number of people involved and the thousands of maintenance jobs that must be performed, it is quite obvious that the worldwide operation of the Air Force demands a streamlined maintenance management concept. This maintenance concept is presented in Air Force Regulation 66-1, *Maintenance Management Policy.*

Perhaps the best way to understand your position in the maintenance area is to get an overview of the entire program. This chapter should give you a broad perspective of the range of the maintenance management system, including a review of what has been proven and determined through day-to-day use to be practical.

5-1. C-E Maintenance Management Concept

The USAF maintenance community is made up of mission-oriented units organized as detachments or squadrons within the operating commands and supported by industrial centers normally operated by Air Force Logistics Command (AFLC).

037. Define maintenance as used in the maintenance management program, and list the task it includes.

Objective of Maintenance. The objective of maintenance is to keep equipment in service. This means that the equipment does the job for which it was designed and purchased by the Air Force. However, the Air Force has gone further than the above simple statement in explaining the objective of maintenance. Air Force Regulation 66-1 describes maintenance as "as a functional element of the organization, responsible for insuring that Air Force materiel is serviceable, safely operable, and properly configured to meet the mission requirements." Maintenance includes, but is not limited to, inspection, repair, overhaul, modification, preservation, testing, and analysis of condition or performance with maximum effort expended toward completing those tasks on a preplanned, scheduled basis. Proper planning provides supervisory personnel with the workload plans required for timely accomplishment through the efficient use of personnel, facilities, and equipment. Proper planning reduces unscheduled maintenance events and allows for an orderly progression of maintenance actions toward returning malfunctioning equipment to a safe and operable condition.

Exercises (037):

1. Define maintenance as used in the maintenance management program.

2. List the tasks included under the maintenance program.

038. State the responsibilities and capabilities of the levels of the maintenance organization.

Mission-Oriented Unit. The mission-oriented unit performs its assigned tasks to produce mission-ready systems. These maintenance tasks are divided into two categories: on-equipment and off-equipment. Both maintenance categories may be preventive or corrective in nature. Preventative maintenance includes lubrication, cleaning, and other actions which will keep the equipment in operating condition. Corrective maintenance includes all actions to return equipment to a serviceable condition.

On-Equipment maintenance. On-equipment maintenance includes those tasks of servicing, loading, inspecting, modifying, and repairing by removal and replacement actions. These actions are accomplished with skills and equipment possessed by the unit.

Off-equipment maintenance. This includes the tasks which cannot be performed on C-E equipment items, but which can be accomplished with the skills and equipment possessed by the unit. This includes repair of units or subassemblies that were removed from the equipment by replacing components of the units or subassembly.

Industrial center/AFLC. Maintenance actions which are beyond the capability of a mission oriented unit are sent to the responsible industrial center or AFLC depot for repair. These facilities have the specialized equipment or skills that are not available to the mission-oriented unit.

Exercises (038):

1. What is the difference between on-equipment and off-equipment maintenance?

2. What maintenance tasks are performed by industrial centers and AFLC?

3. What maintenance tasks are performed by the mission-oriented unit?

5-20. C-E Maintenance Organization

Each wing is organized in the most effective and efficient manner to perform its mission. This will permit maximum application of resources to production.

039. State the responsibilities of persons within the C-E maintenance organization.

Wing or Unit Commander. The commander has overall responsibility for the accomplishment of the unit or wing mission. Normally a maintenance complex is organized under the trideputy structure which assigns deputy commanders for: operations, maintenance and resources management. Commanders provide leadership and management for their wing or unit, and they consolidate the functions of the maintenance complex to the maximum extent possible depending upon mission, size, location and resources.

Chief of Maintenance. The chief of maintenance (COM) is synonymous with deputy commander for maintenance (DCM) and is also used to denote the senior manager for C-E maintenance. The chief of maintenance manages the maintenance complex for the most efficient use of personnel, money, and material while still accomplishing the mission. Most of the responsibilities of the COM are accomplished by the COM staff under supervision of the COM.

Exercises (039):

1. What is another name for the chief of maintenance?

2. Under the trideupty structure, deputy commanders are assigned to which functions?

3. What is the function of the wing or unit commander?

5-3. Chief of Maintenance Duties

Maintenance organizations vary greatly because of the mission, assigned equipment, location, and size of each organization. Though shops performing similar jobs among the major commands differ in organizational structure, any maintenance organization needs certain elements. One of these elements is the chief of maintenance (COM) staff.

040. State the primary functions of the chief of maintenance and how the responsibilities of the COM are satisfied.

Responsibilities. The position of the COM is at the highest level of control in the maintenance activity. The COM is the executive manager of the maintenance organization with centralized control and direction of all functions of the activity. The maintenance staff agencies act in the name of the COM on those matters for which they have been given responsibility. In the maintenance manager concept (upon which the Air Force maintenance system is based), the COM, through staff functions, plans, controls, and schedules maintenance. For example, skilled specialists with special equipment are sent out to do a highly technical job. Putting them where needed requires a system of scheduling, priority assignments, dispatch, and control from a central agency — the chief of maintenance. We will discuss each staff agency individually so that you can grasp the general management concept and the special function of each agency. Understanding the basic responsibilities of the organization structure is a necessary part of the training for each officer, enlisted person, and civilian in the Air Force.

The COM is a manager. The maintenance organization must be run in accordance with policies and procedures outlined in AFR 66-1. The COM must apply the principles of leadership and management, and supervisors are expected to do the same. The COM and staff must provide direction and guidance for all subordinates in the maintenance organization. This direction must comply with local and higher authority policies and instructions. The COM must be capable of estimating and programming facilities, equipment, manpower, and training requirements through study and analysis of the organization.

Exercises (040):

1. What is the overall function of the chief of maintenance?

2. How are the responsibilities of the COM satisfied?

041. State the functions of the staff under the chief of maintenance.

Functions. Depending on the size and mission of the maintenance activity, the following functions may appear separately or in consolidated forms.

Administration. The office of the COM is the administrative center for the maintenance organization. Its duties include the preparation and maintenance of reports, correspondence, and local maintenance directives, and the control of keypunch services.

Production analysis. Production analysis is the primary management information source for the COM. It operates as a data surveillance and statistical unit. Its overall objective is to improve the maintenance operation by examining various maintenance management output products and reports to identify trends that are developing. Raw data alone can be misleading and must be carefully analyzed by production analysis personnel before it is used by management.

Supervisors who need specific information about maintenance trends in their shop should request the data from production analysis. If the analyst can obtain the data from existing reports and data, the analyst will perform a special analysis. The results of this analysis can be used to define or product maintenance deficiencies that can be corrected before they impair the mission.

Logistics support. This function provides management support to the COM to make sure that a continuing maintenance capability exists whenever mission requirements change. The logistics support section makes plans to insure that maintenance tasks are accomplished in support of mobility requirements; gathers and submits budget estimates for items such as TDY, equipment, and supplies; and serves as the focal point for any maintenance contracts on assigned equipment. Essentially, what this staff agency does is to make sure, through direction of other elements within the maintenance complex, that the resources are available for you to do your job.

Maintenance control. The personnel assigned to maintenance control determine and authorize the expenditures of manpower and material within the maintenance activity. They dispatch the parts, materials, specialists, and support equipment required to do the work. Supervisors must plan and adjust work center actions to meet the requirements and instructions of maintenance control. This agency is made up of the job control, materiel control, and plans and scheduling elements.

Job control. Job control has control of all maintenance; no work can be done until it has been assigned a job control number (JCN) and its priority and expected completion time have been determined. Any action, scheduled or unscheduled, must be coordinated through job control. Job control monitors the status of all facilities, dispatches or assigns technicians, and maintains the file of active job status documents (JSD).

The JSD is the document used by job control to monitor and direct most maintenance actions. The JCN serves as a unique identifier for each job. It is the means by which work is controlled and resources accounted for.

Materiel control. The people in materiel control see that proper parts, tools, and equipment are available to the maintenance shops in the required quantities at the right time. They must forecast supply requirements for each maintenance activity. In addition, the materiel control personnel coordinate with the supply management branch, in conjunction with the chief of maintenance or maintenance supervisor and work center supervisors, for the establishment of bench stocks, prepositioned spares, special levels, and supply points. They also procure time compliance technical orders (TCTOs) kits and control the issue of tools.

Plans and scheduling. Plans and scheduling produces the maintenance plan from known requirements and maintenance resource information. This plan guides the production effort toward efficient and high-quality maintenance by a schedule of activity balanced against resources. The plan is made up of a schedule of preventive maintenance inspections (PMIs) with a separate listing of TCTOs, QC inspections, and evaluations to be done. The format of the plan and additions to it are left up to the chief of maintenance.

Quality Control. Quality control, or QC, as it is more commonly known, serves as the primary technical advisor to the maintenance complex. QC is concerned with the quality of the maintenance performed within the activity and controls it through various monitoring programs. These programs do not relieve the maintenance supervisor from the responsibility of continually seeking higher quality maintenance. A coordinated team effort between the chief of maintenance, QC personnel, and supervisors is essential for an effective QC program. The QC effort involves the elements of MSEP, analysis and reporting of deficiencies, maintenance training, and technical publications.

Maintenance standardization. This is accomplished through the maintenance standardization and evaluation program (MSEP) which is explained in these paragraphs. Briefly, MSEP is used to determine technical competency through personnel evaluations. Three types of inspections are also done under MSEP. These are the technical, activity, and special inspections.

Technical inspections provide an overall indication of the quality of maintenance being performed on assigned hardware. They also produce data useful in identifying training deficiencies and potential problem areas.

QC activity inspections are used to evaluate management effectiveness, the condition of equipment and systems, and the technical competence of personnel. These inspections will be done once each year, at the least, for each work center. The results of these inspections give the commander, the chief of maintenance, and supervisors objective and factual information on how well an activity is meeting mission requirements.

Technical publications. QC maintains a complete file of TOs, TCTOs, inspection workcards, and a work unit code manual on each type of equipment maintained by the maintenance complex. The major consideration is to be sure that TOs are available for the people who use them most. QC, in conjunction with work centers, will also develop inspection workcards required for equipment that is bought "off the shelf."

Maintenance training. This QC activity makes sure that the maintenance complex has a continuous, well-organized training program. The goal is to have a sufficient number of people in all skills, at the right skill level, to support the maintenance mission. The parts of the program include: (1) job proficiency, (2) qualification, and (3) special training.

Job proficiency training and qualification training are explained in the module on OJT included in this volume. Special training is done to qualify personnel on the operation and maintenance of equipment that is not a requirement of the AFSC. An example would be learning how to start a generator or learning the use of special-purpose vehicles.

Supervisors, production analysis, and the results of MSEP evaluations are sources used for identifying training needs. The primary goal of the maintenance training effort within QC is to provide the training that will eliminate any deficiencies discovered.

Deficiency analysis and reporting. The deficiency analysis process gives the chief of maintenance and supervisors the means of finding problem causes and ways of correcting them. The process involves the elements of identification, analysis, and reporting.

Problem areas can be identified through the use of MDC data and MSEP products. Once identified, the individual most knowledgeable of the problem area should perform an in-depth study and analysis. Corrective actions recommended should be accomplished by the responsible work center. Reporting is done locally for deficiencies identified through MSEP.

Materiel deficiencies are identified and reported in accordance with TO 00-35D-54, *USAF Materiel Deficiency Reporting and Investigating System.* Technical publication errors are reported using AFTO Form 22. QC will review, process, and monitor the TO improvement system.

Workcenter. The C-E maintenance workcenters are the production elements and are responsible for all maintenance. Each workcenter supervisor is responsible for management of a specific area of responsibility.

Exercises (041):

1. What unit is responsible for determining and authorizing the expenditure of manpower and materiel in the maintenance activity?

2. What part does the administration function play in the maintenance management program?

3. What is the purpose of the production analysis function?

4. What three types of training come under the training function of QC?

5. Name the three sections that make up the maintenance control function.

6. State the function of the job control section.

7. What is the function of the materiel control section?

5-4. Other Management Concepts

There are two other areas of management which you should understand. First is the maintenance standardization and evaluation program which insures that all maintenance technicians perform each job by proven methods. The second area deals with a structure for the maintenance organization that is different from the normal communication-electronics maintenance management structure.

042. State the objectives of the maintenance standardization and evaluation program and how these objectives are met.

Maintenance Standardization and Evaluation Program. The objective of standardization is to improve maintenance quality and capability. This objective can be achieved through the application of the maintenance management system and through MSEP. The objective of MSEP is to improve your technical competence, as well as the quality of maintenance you perform. These objectives can be met by training you, via the OJT program, to use standard maintenance practices and to comply with technical data. Your supervisor and quality control personnel evaluate you periodically to insure the adequacy of the work center's training program, to check your technical proficiency, and make sure technical and procedural data are accurate. Additionally, quality control personnel conduct activity and technical inspections to find out the quality of maintenance production and management.

Personnel Evaluations. The supervisor identifies all tasks performed within a work center and sets up a training program for each person as needed. When a trainee has proven that he or she can perform a given task, the supervisor certifies the individual on that task. Both the supervisor and quality control personnel later evaluate the trainee's performance on these tasks. If the trainee fails on a test for which certified, the individual is decertified and retrained to eliminate the deficiency.

The selection of individuals for the evaluation process under MSEP is based on factors such as the number of newly assigned personnel, equipment and training problems that develop, and the different types of equipment to be maintained.

All maintenance personnel that have been certified on specific tasks are subject to an evaluation. The evaluations are normally done during a quality control activity inspection. You may also be evaluated anytime after 3 months from the time that new or modified equipment, which you maintain, becomes operational. If you were decertified on a particular task and then recertified, you must be reevaluated no more than 3 months from the date of decertification.

Specific details on how to conduct evaluations and how results are recorded are contained in AFR 66-1, Volume 5, and attachment 1 to that volume. Major air commands may also set up MSEP personnel evaluation criteria on their own.

Exercises (042):

1. What are the objectives of MSEP?

2. List two ways the objectives of MSEP can be met.

3. Who may certify a trainee proficient on a task?

4. Who may decertify task proficiency?

043. State the objectives of production oriented maintenance organization and cross utilization training.

Production Oriented Maintenance Organization (POMO). In most cases you will find the C-E maintenance organized under the centralized maintenance concept; however there may be times when maintenance is organized under POMO. This concept restructures the organization from the centralized maintenance format. Just as in the centralized maintenance management concept, POMO plans, schedules, controls, and directs all maintenance resources. One significant difference in the two concepts is that POMO generally decentralized the maintenance shops and assigns both people and equipment to smaller maintenance shops. On-equipment and off-equipment maintenance may be performed by separate shops, each shop using personnel with two or more AFSCs. This decentralized maintenance concept is designed to meet the peculiar combat needs of the Tactical Air Force (TAC).

Cross Utilization Training (CUT). POMO relies on cross utilization training to provide individuals the ability to perform, with little or no supervision, selected maintenance tasks that are not part of their primary AFSC. This consists of practical training and may also include training conducted by the field training detachment (FTD). CUTs is available under the centralized maintenance concept, but it is not the intricate part of the training program as it is in POMO.

Exercises (043):

1. What are the two management concepts?

2. What are the differences between the two management concepts?

3. What is CUT?

Maintenance Documentation

6-1. Maintenance Data Collection System

A functional system for collecting and maintaining data is mission essential. Required data must show individual responsibility and time completion of work.

044. State what kinds of information are provided by the maintenance data collection system and how the information is used.

Data Collection. The maintenance data collection system provides management with information as to what job was performed, who did the work, and when it was performed. The system further provides such data as how many direct man-hours were consumed on each job (unit of work), why each repair was required (how malfunctioned), when the malfunction was discovered, and what workcenter performed the work. All maintenance jobs are recorded in this way so that comprehensive data is available for analysis. (NOTE: A unit of work, within the maintenance area, is defined as a "job which has a definite beginning and end; the accomplishment of which requires the expenditure of direct labor.")

The summary data compiled in the various types of reports are used at all levels of supervision. From these reports, administrators and supervisors are able to analyze and evaluate their operations to make intelligent decisions for performing their missions. A workcenter supervisor can use this information to increase management efficiency at the shop level. Your chief of maintenance and staff use this information for personnel planning, forecasting tool and equipment needs, budget computations, and cost analysis. The Air Force Logistics Command uses this data for inspection and maintenance requirements analysis, life expectancy, time change requirements, justification for modification programs, master repair schedules, deficiency analysis, and costs. The primary source for all this is the paperwork you turn in daily — namely the AFTO Form 349, Maintenance Data Collection Record.

Exercises (044):

1. What information does the maintenance data collection system provide and to whom?

2. What is a unit of work?

3. List the different levels of supervisors and administrators who use maintenance data and give the reasons why each uses the data.

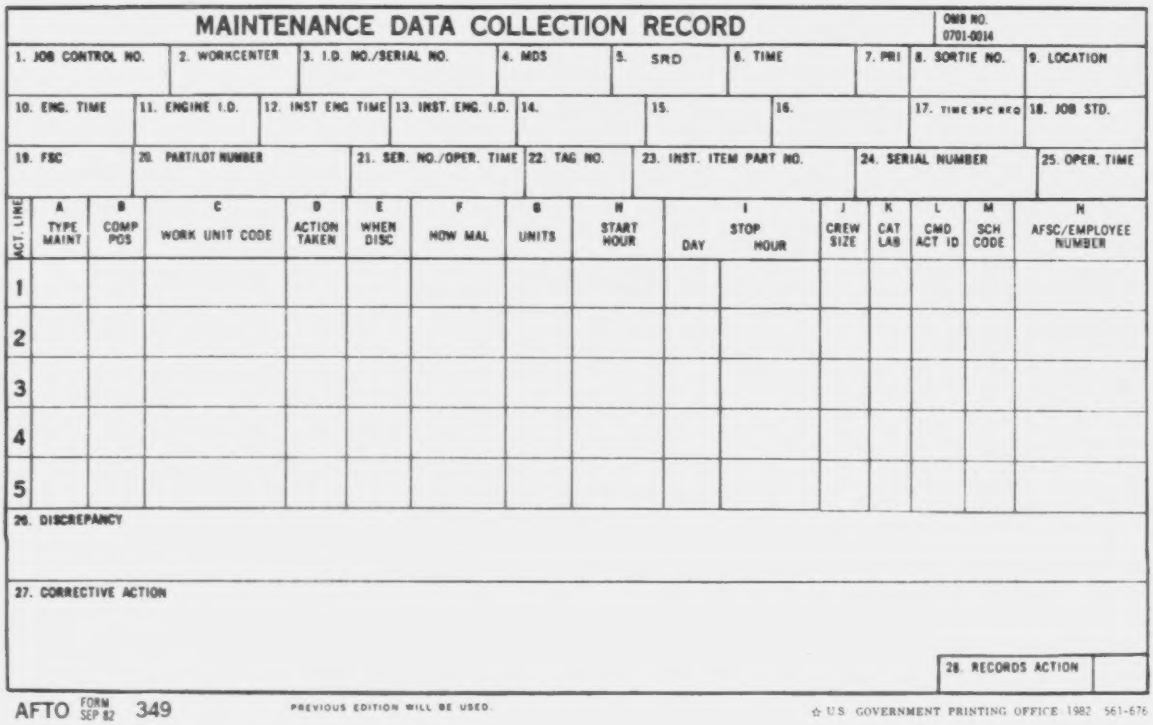
045. List the forms used to record maintenance action, and specify entries to be made in selected blocks.

General Recording Procedures. The management of the maintenance effort requires recording and reporting of all maintenance actions. The AFTO Form 349, Maintenance Data Collection Record, shown in figures 6-1A and 6-1B are used to report all on-equipment and off-equipment maintenance actions and all work directed by TCTOs. Basically, work performed on a complete item of equipment is considered on-equipment work. This kind of work includes support general work, removal and installation of components, and fix-in-place actions. In-shop maintenance performed on a subassembly or part that is removed from a piece of equipment and returned to the shop for repair is considered off-equipment work. When an item is removed from a piece of equipment and taken to the shop or repair depot, an AFTO Form 350, Reparable Item Processing Tag, is completed and attached to the item. The AFTO Form 350, shown in figure 6-2, remains with the item during the whole repair process, since it serves to identify the item as well as furnish information for a second AFTO Form 349 that must be completed by shop personnel. The first AFTO Form 349 is considered on equipment and shows removal of the item. The second 349 shows the off-equipment repair action.

You must use specific codes for recording maintenance data because your information must be converted into language that electronic accounting machines can read. When the maintenance forms are complete, they are sent to data services where the information is punched into accounting machine cards.

As a maintenance specialist, you are responsible for completing your own maintenance data forms. Your work center supervisor is responsible for the accuracy of the forms you complete. Both the specialist and the supervisor must know the reporting system from A to Z.

Since the AFTO 300 series forms are used Air Force-wide, it is only logical that certain adaptations or modifications must be made to them in specialized areas to document the maintenance data pertinent to that field. Therefore, you must understand the modifications re-



MAINTENANCE DATA COLLECTION RECORD

OMB NO. 0701-0014

1. JOB CONTROL NO.	2. WORKCENTER	3. I.D. NO./SERIAL NO.	4. MDS	5. SRD	6. TIME	7. PRI	8. SORTIE NO.	9. LOCATION

10. ENG. TIME	11. ENGINE I.D.	12. INST ENG TIME	13. INST. ENG. I.D.	14.	15.	16.	17. TIME SPC REQ	18. JOB STD.

19. FSC	20. PART/LOT NUMBER	21. SER. NO./OPER. TIME	22. TAG NO.	23. INST. ITEM PART NO.	24. SERIAL NUMBER	25. OPER. TIME

ACT. LINE	A TYPE MAINT	B COMP POS	C WORK UNIT CODE	D ACTION TAKEN	E WHEN DISC	F HOW MAL	G UNITS	H START HOUR	I STOP DAY	 HOUR	J CREW SIZE	K CAT LAB	L CMD ACT ID	M SCH CODE	N AFSC/EMPLOYEE NUMBER
1															
2															
3															
4															
5															

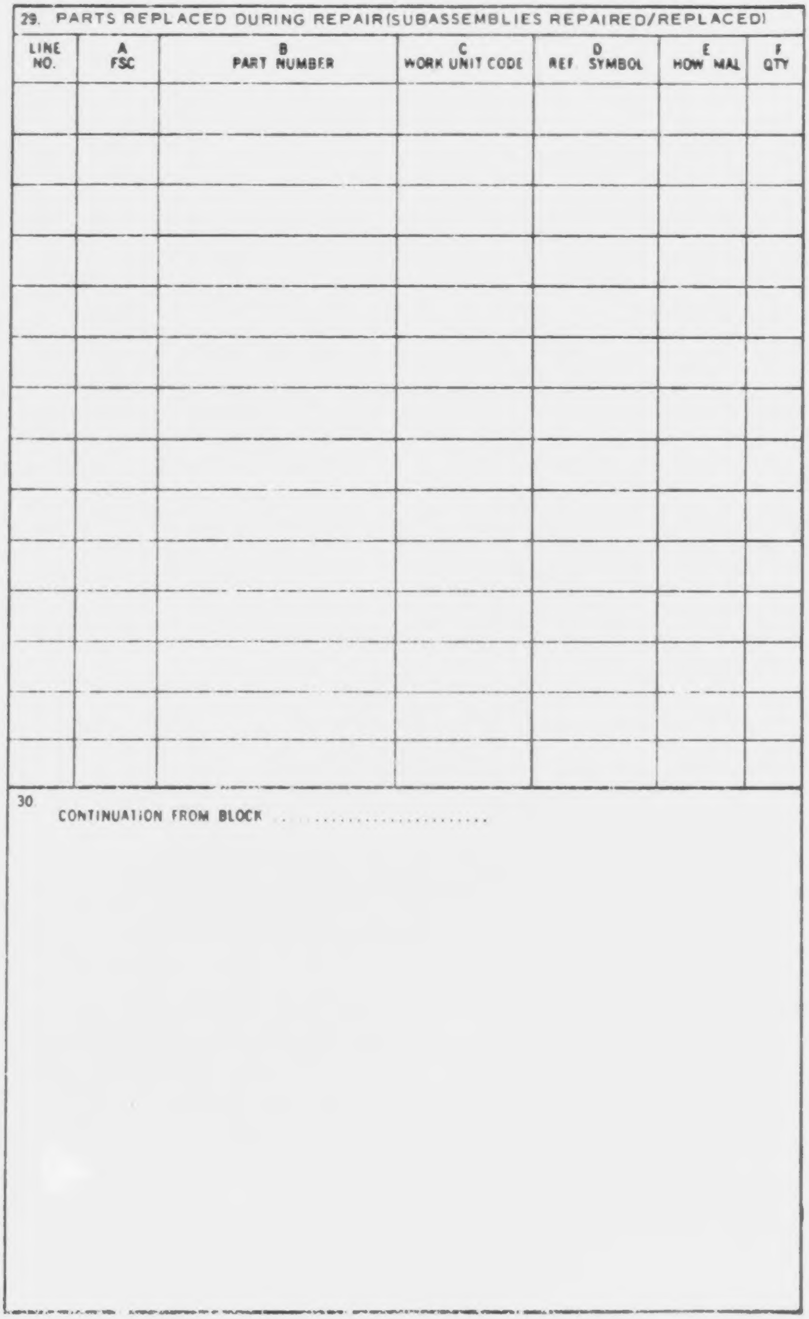
26. DISCREPANCY

27. CORRECTIVE ACTION

28. RECORDS ACTION

AFTO FORM SEP 82 349   PREVIOUS EDITION WILL BE USED.   ☆ U.S. GOVERNMENT PRINTING OFFICE 1982 561-676

Figure 6-1A. AFTO Form 349 (front).

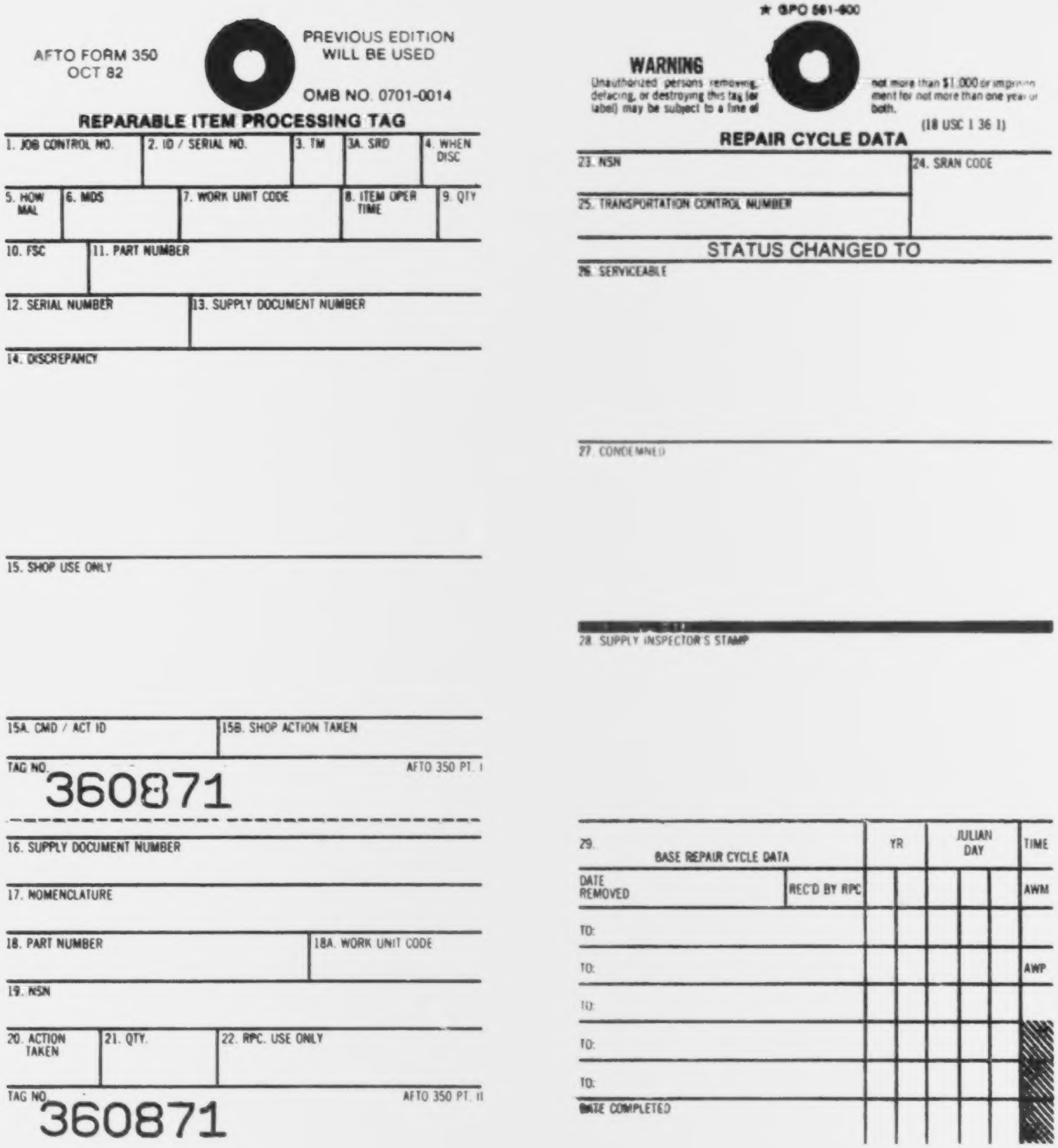


29. PARTS REPLACED DURING REPAIR(SUBASSEMBLIES REPAIRED/REPLACED)

LINE NO.	A FSC	B PART NUMBER	C WORK UNIT CODE	D REF. SYMBOL	E HOW MAL	F QTY

30. CONTINUATION FROM BLOCK ....

Figure 6-1B. AFTO Form (back).



AFTO FORM 350
OCT 82

PREVIOUS EDITION
WILL BE USED

OMB NO. 0701-0014

REPARABLE ITEM PROCESSING TAG

1. JOB CONTROL NO.	2. ID / SERIAL NO.	3. TM	3A. SRD	4. WHEN DISC

5. HOW MAL	6. MDS	7. WORK UNIT CODE	8. ITEM OPER TIME	9. QTY

10. FSC	11. PART NUMBER
12. SERIAL NUMBER	13. SUPPLY DOCUMENT NUMBER

14. DISCREPANCY

15. SHOP USE ONLY

15A. CMD / ACT ID	15B. SHOP ACTION TAKEN

TAG NO. 360871 AFTO 350 PT. I

16. SUPPLY DOCUMENT NUMBER

17. NOMENCLATURE

18. PART NUMBER	18A. WORK UNIT CODE

19. NSN

20. ACTION TAKEN	21. QTY.	22. RPC. USE ONLY

TAG NO. 360871 AFTO 350 PT. II

★ GPO 561-600

WARNING

Unauthorized persons removing, defacing, or destroying this tag (or label) may be subject to a fine of not more than $1,000 or imprisonment for not more than one year or both.

(18 USC 1 36 1)

REPAIR CYCLE DATA

23. NSN	24. SRAN CODE
25. TRANSPORTATION CONTROL NUMBER	

STATUS CHANGED TO

26. SERVICEABLE

27. CONDEMNED

28. SUPPLY INSPECTOR'S STAMP

29. BASE REPAIR CYCLE DATA		YR		JULIAN DAY			TIME
DATE REMOVED	REC'D BY RPC						AWM
TO:							
TO:							AWP
TO:							
TO:							
TO:							
DATE COMPLETED							

Figure 6-2. AFTO Form 350 (front and back).

quired for your work before you can use one of these forms effectively. There is some information that is fairly standard so let's briefly examine some of the blocks on the AFTO Form 349.

Job control number (JCN). The JCN consists of seven characters and is used in block 1. You use this number to control and identify maintenance actions. Only authorized maintenance tasks can be assigned a JCN; maintenance is not authorized without a JCN or the knowledge that a JCN will be assigned. The first three characters of the JCN are the Julian date, such as 041 for 10 February. The last four characters are used to identify jobs. They normally consist of a daily or monthly job sequence number such as 0001 for the first job of the day or month. Using the examples just given the JCN would be 0410001.

Workcenter code. The workcenter code goes in block 2. The workcenter number is a 5-digit code and will be the workcenter for the individual performing the work.

Item identification number (ID No.). The ID number is used in block 3 and identifies either specific groups or individual items on which the maintenance actions have been performed. The ID numbers are assigned and published locally. A list of the identification numbers assigned to the equipment maintained by your organization is filed with work unit code manuals and copies of AFR 300–4, *Classified Data Elements and Codes*, that are furnished for your use when reporting maintenance work.

In establishing identification numbers for groups of items, like equipment is grouped according to type and service provided. For example, all end instruments having the same work order prefix/suffix or the same work unit code are assigned the same identification number. The identification number is always a six-character code. The first character, which is also the first digit of the work center code number, identifies the work center responsible for the maintenance of that particular equipment. The second character of the identification number is the first character of the equipment classification code. The four remaining positions, assigned locally, identify the grouped items according to equipment type and service provided. In items that need to be identified by an individual identification number, the last four digits of the item's serial number are used for the last positions (digits) of the identification number. If the item does not have a serial number the last four digits of the identification number are assigned locally.

Use of columns. Codes for columns a, c, d, e, and f are found in the TO–06, *Work Unit Code Manual.* The work unit code tells what unit or subassembly failed and the other columns require codes for indicating how and when the unit failed and the required action for its repair.

Column G is the units of work completed. For example, troubleshooting is a job in itself. The removal of an item, replacement of a component, and similar jobs are considered complete jobs. Each such job has an action taken code of its own.

The job-beginning and job-ending times are recorded in column H and I are self-explanatory.

The last column we will discuss is column N, employee number. This code consists of the technician's first letter of the last name, followed by the last four digits of that person's Social Security number. Under maintenance management information and control system (MIMICS) the employee number consists of a five-digit number assigned to the individual. In case of more than one technician (column J) the senior person's code will be used. The remaining blocks are easy. Enter a brief description of the trouble or the work to be performed in block 26. Block 27 is used for a brief description of the work required (action taken) to correct the trouble. If any parts are required to complete the repair action you are recording on the AFTO Form 349, list them in block 29 on the back of the form.

The AFTO Form 350 is a two-part form required on removed items that need maintenance shop processing or actions that will be documented as off-equipment maintenance. These items include components, subassemblies, and units removed from end items. A completed AFTO Form 350 serves to identify the origin of an item and contains certain key data elements needed to document shop actions on a shop-generated AFTO Form 349. Part I of the AFTO Form 350 is the repair cycle processing tag and Part II serves as the production scheduling document.

The AFTO Form 350 is made up in tag form, as shown in figure 6-2, and has information code blocks printed on both sides. When you initiate an AFTO Form 350, you complete blocks 1 through 14 on the front of the tag and block 27 on the back of the tag. Obtain entries for blocks 1 through 12 and block 14 from the AFTO Form 349 completed at the time of the removal action. When a demand is made for a replacement item, obtain the supply document number from the supply activity. Enter it in block 13. Block 27 is just as easy. You enter the date on which the part was removed from the unit of equipment or the end item in block 27. The remaining blocks on both the front and the back of the tag are the responsibility of the production control section and shop personnel.

When making up an AFTO Form 350, follow the same procedures that you use to record a fix action on an AFTO Form 349. Always use extra care in selecting the work unit code for block 7 on an AFTO Form 350, because it is important that the defective part is identified correctly. You should always select the proper "when discovered" and "how malfunctioned" codes from your code manual and enter them in blocks 4 and 5, respectively. Support general codes are not used on the AFTO 350.

Exercises (045):

1. List the forms used to record maintenance actions.

2. State what each form is used for.

3. What does a job control number consist of?

4. Where can you find the codes used in columns A through F on an AFTO Form 349?

5. What makes up the employee number?

6. What information is recorded on the back of the AFTO Form 349?

7. What are the two parts of the AFTO Form 350 used for?

8. How many and what type of forms are required for off-equipment repair action?

046. Identify proper procedures for processing and controlling repairable items.

Repairable Item Processing. Because a reparable item may be the only source of supply, a reparable item is as important as a serviceable item. Therefore, reparable items are repaired at base level, whenever possible. Thus, replenishment items from the depot are furnished only to replace items that are condemned or cannot be repaired at base level, or to furnish items that are needed to adjust stock levels.

To provide a positive control of reparable items routed through intermediate maintenance, the Air Force has established the repair cycle asset control system. This system controls the reparable item throughout its repair cycle. A reparable item can also be called a repair cycle asset or a due-in from maintenance (DIFM) asset. In essence, DIFM means that you must turn the item in for exchange with a serviceable item.

For control purposes, maintenance activities route a reparable item along with the AFTO Form 350, which is initiated at the time the item was removed from equipment, through the reparable processing center (RPC) or the reparable asset control center (RACC). This activity schedules the item into the shop for repair and for subsequent turn-in to supply or for return to maintenance for reinstallation. RPC is the production control activity responsible for controlling repair cycle assets in the maintenance activity. RACC is an integrated activity consisting of RPC (a production control activity) and the repair cycle support unit (a base supply activity). Normally, when you turn in an item for repair, you request a like item from supply. However, if a replacement item is not available from supply, production control gives priority to the repair of the turned in item. Priorities in repair are given to items according to their urgency of need or to those that are in critically short supply ("critical" items).

Remote data link (when available) used in conjunction with the supply system computer, provides production control with a means of updating the current location and condition status of each repair cycle asset. A computer product known as the DIFM Listing, provides production control with a current inventory of all DIFM items, including each item's location and status.

If intermediate maintenance (shops) cannot repair an item that you turn in, they either condemn it or declare it "not reparable this station" (NRTS). Then they process these items through production control to base supply for disposition.

Exercises (046):

Indicate whether each statement below is true (T) or false (F). Correct any false statements.

_____ 1. To the optimum extent possible, reparable items are repaired commercially.

_____ 2. DIFM means that a part classified as a due-in from maintenance asset must be sent to the depot before a replacement can be received.

_____ 3. The reparable processing center (RPC) is the production control activity that controls the flow of repair cycle assets through intermediate maintenance.

_____ 4. A reparable item that intermediate maintenance repairs is returned through production control either (1) to supply or (2) to maintenance for reinstallation.

_____ 5. You can determine the location and status of each DIFM item being repaired by referring to the supply system computer produced DIFM listing.

_____ 6. NRTS means "not replaceable this station."

6-2. Maintenance Management Information and Control System

The maintenance management information and control system (MMICS) is a computerized on-line information system designed to give timely information to maintenance managers for management decisions. The information once recorded by hand is now entered into the computer, where management can retrieve it at will, in a variety of formats.

047. State how information is provided by the maintenance management information and control system.

The MMIC Subsystems. Procedures for use of MMICS are located in AFM 66-278, *Maintenance Management Information and Control System,* and AFP 66-10, *Maintenance Management Information and Control System (MMICS) Guide for Maintenance Managers.*

MMICS is made up of the following subsystems which are used by C-E maintenance: Operational events; inspection and time changes; time compliance technical orders (TCTO); C-E equipment status and inventory reporting, and maintenance personnel.

Operational Events. This subsystem allows the COM to plan, execute, and evaluate the effectiveness of the unit's mission on-line. The inquiries available to the COM allow: monitoring of the current status of an event, including its start and stop times, delays, and reasons for delays; listing of TCTO inspections and time change items required for equipment; listing of all training scheduled; listing of all historical events for equipment; and providing utilization reports.

Inspection and Time Changes. This subsystem lets the maintenance activity automate its records for inspections and time changes. C-E units must first establish inspection records for all end items of equipment that require preventive maintenance inspections (PMIs). Once these records are established in MMICS, it updates them automatically without user intervention. The inspection program can print PMI schedules, arranged by either owning or performing workcenter, up to 90 days in advance. If maintenance data collection (MDC) data are required for either scheduled or unscheduled maintenance, you can enter them through this subsystem and have them forwarded to the MDC batch system automatically. All MDC data are edited when entered, and errors can be corrected immediately. Entering MDC data from scheduled inspections updates the inspection records. Also, entering MDC data from scheduled inspections, and from maintenance "on" and "off" equipment, can close the appropriate status records and generate transactions for the MAJCOM status reporting system.

Time Compliance Technical Orders. This subsystem is an on-line information system for managing TCTOs. It provides the information on each TCTO for each item of equipment including: Title, number, location of accomplishment, type, date received, date expires, kits required, status, estimated work hours, list of equipment to be completed, list of equipment already completed, and the work schedule for completion of the TCTOs.

C-E Equipment Status and Inventory Reporting. This subsystem gives on-line access to a data base with information about organization, mission, equipment and status. It is used to keep the data base up to date when events affect assigned equipment and mission.

Maintenance Personnel. This subsystem provides a computerized method to monitor personnel resources. It provides updated list for: workcenter roster, workcenter listings, organizational manning, training requirements, training schedule, task coverage, training status of individuals, training forecast, on-the-job training (OJT) status, special certification roster, job proficiency guide certification on each individual, and workcenter assigned tasks.

Exercises (047):

1. Which MMICS subsystem is used by the COM to monitor the effectiveness of the organization?

2. Which subsystem provides the maintenance shop with PMI schedules?

3. Under MMICS where a job proficiency guide (JPG) certification monitored?

4. Where is information on the status of TCTO modification of a particular equipment item found?

6-3. C-E Maintenance and Inspection System

Maintenance is defined as the process of "keeping equipment in a state of repair or efficiency." This requires the proper application of established maintenance procedures. The best type of maintenance is preventive in nature.

048. Specify the concepts and procedures for making and reporting CEM inspections.

Preventive Maintenance. Preventive maintenance is defined as those measures taken periodically or when

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they are needed to achieve maximum efficiency in performance, to insure continuity of service, to reduce major breakdowns, and to lengthen the useful life to the equipment or system. This form of maintenance consists principally of inspecting, cleaning, and lubricating equipment during periodic inspections. Preventive maintenance is aimed at discovering and fixing conditions that could lead to malfunctions requiring major repair. Thorough repetitive inspections and effective repair actions result in the highest possible percentage of equipment in a mission-ready status.

Maintenance Inspections. Planned maintenance and inspections always fall under the heading of scheduled maintenance. When speaking of scheduled maintenance, we are referring to such things as inspection and TCTO accomplishment; unscheduled maintenance refers to fixing such emergencies as a blown fuse, a damaged circuit card, or a power failure.

The basic principle of periodic inspections is that they should be made in accordance with a prearranged plan, using a fixed number of people, each of whom has a definite work assignment within a specific period of time. To be thorough, an inspection must follow a carefully planned pattern with each step performed in the proper sequence so that nothing is missed. This requirement necessitates some type of instruction or guidelines.

Inspection Workcards. Each complete preventive maintenance action is prepared as a detailed job procedure and is called a routine. Each routine contains the following:

a. A statement of the job purpose.

b. A listing of all required tools, test equipment, or other materiel.

c. A step-by-step work picture of each action required of the specialist to complete the job, together with the resulting visible or measurable reactions.

d. The measurable equipment performance tolerances essential for determining satisfactory equipment operation.

The inspection cards are designed to provide each specialist with a convenient guide to use while performing an inspection. The requirements listed on the cards are arranged by work areas and are sequenced for the most logical and practical order of accomplishment. This arrangement makes it convenient for the maintenance supervisor to assign each specialist of a crew to a specific job or series of jobs. The result is greater speed, higher quality of maintenance, better training, and more efficient work habits.

The workcards contain other pertinent information to indicate the frequency of the routing time allotted to complete the work and whether a power-on or power-off condition is required to accomplish the inspection requirements.

Inspection Intervals. Inspection time intervals in the inspection workcards are the maximum allowed, thus should not be exceeded. They may, however, be shortened by the chief of maintenance to compensate for difficulties due to geographic location or climactic conditions. All activities using the Air Force equipment are expected to determine whether items are being over inspected or under inspected.

Quality Control (QC) Inspections. QC inspections were listed earlier in the text. At this time, we will go into these inspections in detail to explain areas covered by the technical, activity, and special inspections.

Technical inspections. Quality control technical inspections provide an overall indication of the quality of maintenance being performed on assigned hardware. They also provide data useful in identifying training deficiencies and potential problem areas. Technical inspections must be accomplished in sufficient depth to determine whether the system or equipment is being maintained to meet technical order specifications. Technical inspections must be scheduled to insure that all maintained systems, equipment, aerospace ground equipment, and vehicles are inspected annually.

a. Minimum areas of coverage:

(1) Corrosion control.

(2) Cleanliness, oil leaks, grime, and so forth.

(3) Safety.

(4) Equipment configuration and completeness.

(5) Equipment operational performance in accordance with technical specifications.

(6) Availability and condition of technical data, tools, and test equipment required for the equipment inspected.

(7) Equipment historical file.

(8) Standard maintenance practices.

b. Responsibilities of quality control during technical inspections:

(1) Make recommendations for corrective actions, as required, to the appropriate supervisor.

(2) Insure that proper management action has been taken on all deferred maintenance involving the item inspected.

Activity inspections. QC activity inspections provide the commander, chief of maintenance, and supervisors with factual and objective evaluations of the maintenance management program. Quality control must inspect each staff function and work center at least annually

a. Minimum areas of coverage:

(1) Equipment status reporting and maintenance data collection.

(2) Currency and condition of technical order and publication files.

(3) Effectiveness of maintenance training and MSEP.

(4) Use and applicability of technical data.

(5) Compliance with prescribed safety rules and procedures.

(6) Supply discipline, bench stock management, and reparable processing.

(7) Tools and test equipment availability and condition.

(8) General condition of equipment.

b. Responsibilities of quality control during activity inspections:

(1) Inspect subject areas in sufficient depth to insure that the result is indicative of the whole activity being inspected. Observations should be related to mission accomplishment, when possible.

(2) Determine why the discrepancy exists and include recommendations for correction and applicable references or rationale.

(3) Brief activity supervisory personnel on the inspection findings before the formal inspection report is written.

Special Inspections. QC inspections of this type are requested by the work center supervisor or directed by the COM, commander, or higher headquarters. Special inspections may be either administrative or technical.

Some minimum areas of coverage are as follows:

a. Identification of problem areas and corrective actions required to restore equipment to technical specifications after unsatisfactory checks or evaluations.

b. Insuring, upon initial issue, that incoming precision measurement equipment (PME) meets technical order configuration and physical serviceability requirements.

c. Evaluating the quality of maintenance being performed on alternate equipment. Equipment such as power generators must be evaluated as to its capability of being put into safe and sustained operation immediately.

d. Determining if newly installed, overhauled, modified, or modernized equipment and systems meet technical requirements and if technical data is adequate.

e. Verifying, through spot checks, the accomplishment of in-process inspections.

Inspection Reporting. QC must render complete, accurate, and impartial reports with sound recommendations that will aid in the correction of discrepancies or irregularities and their cause. QC inspections with discrepancies will be documented on AF Form 2420, Quality Control Inspection Summary. The use of AF Form 2420 for documenting activity inspections is an option of the chief of maintenance. All inspection reports are routed through supervisory channels to QC Deficiency Analysis using AF Form 2419, Routing and Review of Quality Control Reports. Additionally, all activity inspection reports are routed through QC and the chief of maintenance to the commander.

All man-hours expended and work accomplished during a maintenance inspection are recorded on AFTO Form 349. The AFTO Form 349 may also be used as the work order (control document) to direct the performance of the inspection routines.

Exercises (048):

1. What is preventive maintenance aimed at?

2. Planned inspections are what type of maintenance?

3. List four types of information included on the workcards for each routine.

4. Who may change the intervals at which maintenance inspections are made?

5. List three types of inspections made by quality control and state the purpose of each.

6. What is the routing for quality control inspection reports?

7. What documentation is required for work done during maintenance inspections?

6-4. Materiel Deficiency Reporting and Investigating System

No system is perfect. We are familiar with the recall of automobiles to correct their deficiencies. The Air Force is no different. From time to time, a piece of equipment is found to have contributed to an accident or incident or created a safety hazard. Materiel deficiencies result in maintenance deficiencies for your work center. Some of these items are caught through an analysis of the maintenance data collection system. The Air Force also depend upon each individual to make materiel deficiency reports (MDRs). If you ever have to make out one of these reports, check TO 00-35D-54, *USAF Materiel Deficiency Reporting and Investigating System,* to make sure you have the latest information. The responsibility for clearance and control of MDRs is assigned to QC. Be sure you check with QC for up-to-date advice on using the reporting system. Now, what is a materiel deficiency?

049. Define materiel deficiency and maintenance deficiency, and state the purpose of the MDR system.

Materiel Deficiency and Maintenance Deficiency. The materiel deficiency reporting and investigating system is set up to feed back deficiency data on hardware and computer programs to the people responsible for the procurement or development of these items, so action can be taken to correct and prevent deficiencies in the design or quality of materiel. For example, suppose an integrated circuit failed on two occasions in a critical piece of communications gear used in the Nation's air defense system. An MDR should be made to correct this materiel deficiency which, in turn, may have caused a maintenance deficiency. The combination of these effects, if not corrected, could result in a declaration of National emergency when there wasn't any.

A material deficiency, as defined by TO 00–35D–54, is "the failure of an end item which was attributable to neither the repair nor the manufacturing process, but was due to an unpredictable failure of an internal component or subassembly." The integrated circuit (IC) in our example was failing. The technician didn't know when it would fail but it did, and as a result, the equipment failed and the mission suffered.

When this IC failure first occurred, it probably resulted in many hours of maintenance to find and correct the problem. Because of this, operational capability of the equipment was reduced. Subsequent failures would increase the number of maintenance hours expended and a maintenance deficiency would exist. The primary factors involved in determining whether a maintenance deficiency is present are reliability, accessibility, simplicity, supportability, standardization, and interchangeability of components and end items.

Exercises (049):

1. What is a materiel deficiency?

2. Define maintenance deficiency.

3. What is the purpose of the MDR system?

050. Identify the report used for a given deficiency and specify methods for reporting MDRs.

Category I Materiel Deficiency Report (MDR). This category of MDR is a report on emergency conditions that may affect equipment, systems, and computer programs. These conditions have a potential of being unacceptable in terms of safety, operations, or maintenance. The specific conditions are listed in TO 00–35D–54 and consist of Air Force mishaps, nuclear safety deficiencies, critical deficiencies, and explosive safety deficiencies.

Air Force mishaps. This is an unplanned incident or accident that damages personnel or property and is not caused by enemy action.

Nuclear safety deficiency. Any computer program, materiel, or design deficiency that could cause a nuclear accident, incident, or deficiency.

Critical deficiency. The TO defines this condition, as it applies to electronic and electrical equipment as: "Any malfunction or design deficiency (including safety devices) that could result in exposure of maintenance or operating personnel to lethal voltages, excessive radiation, or other danger, by either direct or indirect action."

Explosive safety deficiency. This condition is present when malfunctions or detonations of explosives occur during use, handling, or storage.

Category II MDR. This type of report concerns itself with quality deficiencies, design, and maintenance materiel deficiencies and problems that result from embedded computer system programs.

Quality deficiencies have to do with materiel that does not conform to specifications or workmanship in the manufacture, repair, or modification process.

Design and maintenance materiel deficiencies do not have a safety impact, but if they are not corrected, prolonged usage could have a negative impact on operational efficiency; reduce tactical or tactical support ability; reduce operational life or general service utilization of equipment; or create economic problems with manpower and money. These criteria apply to nonwork unit coded items. Work unit coded items with this type of deficiency are reported if they are new systems and equipment for which limited MDC data exists.

A Category II MDR is generated on embedded computer system programs if related to errors occurring during design and production. An embedded computer system is a digital computer or system physically incorporated into a larger system whose primary function is not data processing.

Once a deficiency is determined to exist as a Category I or I MDR, it must be reported and routed according to the procedures established under TO 00–35D–54.

Methods of Reporting MDRs. All MDRs are prepared on DD Form 173, Joint Messageform, and submitted by electrical transmission. Category I MDRs are prepared for submission by priority message within 72 hours after discovery of the deficiency.

Category II MDRs are submitted by routine message within 15 workdays after discovery of the deficiency. SF Form 368, Quality Deficiency Report (Category II), is also prepared when reporting hardware and computer program deficiency data.

Only minor defects are not reported under this system. A minor defect is classified as a defect that does not alter how an item is used. The item still operates normally for its intended purpose.

Exercises (050):

1. What type of materiel deficiency report is turned in to report a deficiency caused by an error in workmanship?

2. What deficiencies are not reported under the MDR system?

3. An emergency condition that causes a Category I MDR will be submitted by what means and in what time period?

4. What category of MDR is prepared for work unit coded items of new equipment?

6-5. Supply Documentation

To accomplish the mission of the Air Force, we buy many thousand items. Among these are spare parts, special tools, maintenance equipment, pencils, paper clips, and other items. The cost runs into billions of dollars. This property is stored, issued, turned in, and shipped. This cycle may be repeated several times before an item is no longer usable and is sold for scrap. At this moment there are items in your shop that need to be repaired or condemned. Condition tags are used to reflect the status of these items.

051. State the purpose of the DD Form 157X series condition tags; and for given situations, state the proper tag to use and the proper way to fill it out.

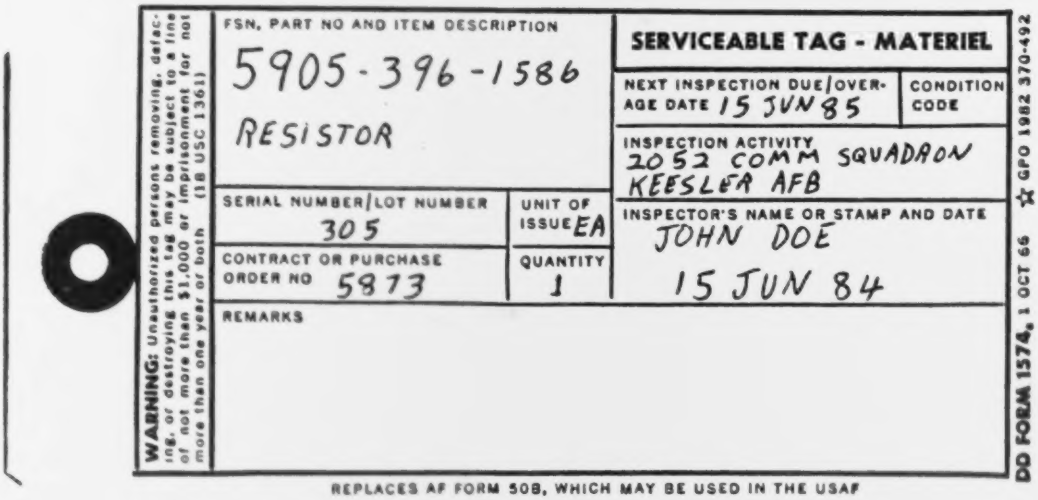
Condition Tags. The purpose of the DD Form 157X series tags is to show the condition of USAF property. As a maintenance person, you are required to fill out these tags and to know what condition the tags reflect.

When a part is removed from the equipment, you will fill out an AFTO Form 350, Reparable Item Processing Tag, and attach it to the part. This part is then routed to the responsible shop for repair. The exact action taken at the ship, i.e., whether it is tested, repaired, or sent to a higher echelon for maintenance action, depends on the setup of your particular organization. Nevertheless, somewhere along the line, the part is tagged with the appropriate DD Form 157X series tags. Once again, your main concern with these tags is knowing what condition they reflect. Therefore, we will discuss the condition tags with this in mind.

DD Form 1574 (yellow tag). The DD Form 1574, Serviceable Tag — Materiel, and 1574-1, Serviceable Label-Materiel, are yellow and have the same format; their only difference is that the 1574 form is a tag, and the 1574-1 form is a gummed label. A properly completed 1574 is shown in figure 6-3. The presence of one of these forms on a piece of equipment denotes that the equipment is in a serviceable condition. They may be placed on used as well as new equipment to indicate the equipment is in a serviceable condition and good for the purpose in which it was intended.

Most of the entries made in the blocks are self-explanatory by their titles. However, a few words should be said about the Serial Number/Lot Number and the Contract or Purchase Order No. blocks. Normally the serial number is entered in the Serial Number/Lot Number block. If no serial number is given for the part, the part number is entered. The contract or purchase number is entered by supply personnel when the number is available.

DD Form 1577-2 (green tag). The DD Form 1577-2, Unserviceable (Reparable) Tag — Materiel (fig. 6-4) is



WARNING: Unauthorized persons removing, defacing, or destroying this tag may be subject to a fine of not more than $1,000 or imprisonment for not more than one year or both (18 USC 1361)

SERVICEABLE TAG - MATERIEL

FSN, PART NO AND ITEM DESCRIPTION
5905-396-1586
RESISTOR

NEXT INSPECTION DUE/OVERAGE DATE 15 JUN 85

CONDITION CODE

INSPECTION ACTIVITY
2052 COMM SQUADRON
KEESLER AFB

SERIAL NUMBER/LOT NUMBER 305

UNIT OF ISSUE EA

INSPECTOR'S NAME OR STAMP AND DATE
JOHN DOE
15 JUN 84

CONTRACT OR PURCHASE ORDER NO 5873

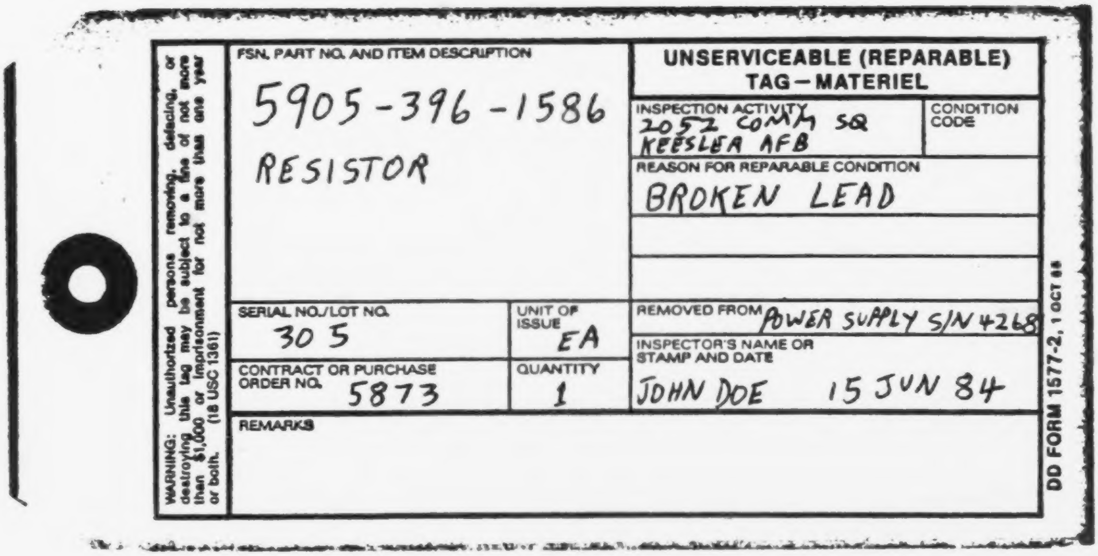
QUANTITY 1

REMARKS

DD FORM 1574, 1 OCT 66 ☆ GPO 1982 370-492

REPLACES AF FORM 508, WHICH MAY BE USED IN THE USAF

Figure 6-3. Sample, DD Form 1574 (yellow).



WARNING: Unauthorized persons removing, defacing, or destroying this tag may be subject to a fine of not more than $1,000 or imprisonment for not more than one year or both. (18 USC 1361)

UNSERVICEABLE (REPARABLE) TAG – MATERIEL

FSN, PART NO. AND ITEM DESCRIPTION: 5905-396-1586 RESISTOR

INSPECTION ACTIVITY: 2052 COMM SQ KEESLER AFB

CONDITION CODE:

REASON FOR REPARABLE CONDITION: BROKEN LEAD

SERIAL NO./LOT NO.: 30 5

UNIT OF ISSUE: EA

CONTRACT OR PURCHASE ORDER NO.: 5873

QUANTITY: 1

REMOVED FROM: POWER SUPPLY S/N 4268

INSPECTOR'S NAME OR STAMP AND DATE: JOHN DOE 15 JUN 84

REMARKS:

DD FORM 1577-2, 1 OCT 88

Figure 6-4. Sample, DD Form 1577-2 (green).

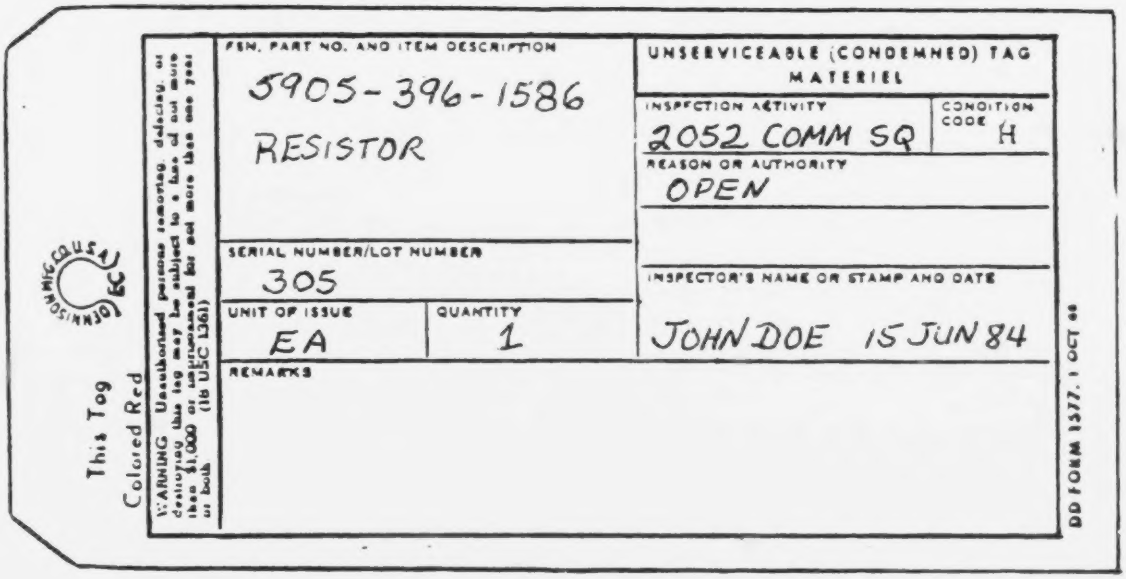
green and is used to indicate that the item requires work to restore it to a serviceable condition; in other words, the item is reparable. This means that items which are removed from service, but which still appear serviceable, are tagged with a 1755–2, form whenever a reasonable doubt exists as to their serviceability. However, when items are obviously not serviceable, they are inspected to ascertain their repair cost; and if the cost is within the prescribed allowance, they are "green tagged" and processed through the proper repair channel to be restored to a serviceable condition. The entries made in the block either have been previously discussed or are self-explanatory by the titles of the blocks.

DD Form 1577 (red tag). The DD Form 1577, Unserviceable (Condemned) Tag — Materiel (fig. 6-5), is in sharp contrast to the foregoing forms. This tag is used to indicate either that the article to which it is attached is unsuitable for restoration to a serviceable condition, or that it is of no further use to the Air Force in the function for which it was manufactured or authorized. We can say that equipment is placed in a condemned category either because of its condition or by administrative action. When equipment is condition condemned, the decision is made by a qualified inspector and is the result of one of two situations: either the article cannot be repaired, or the cost of repair would exceed the established maximum repair allowance. When equipment is administratively condemned, the personal judgment of an inspector does not enter into the situation, since this action is taken by AFLC or higher authority. Administrative condemnation exists to prevent further use of inadequate equipment. It is applied when equipment is no longer required, when it becomes obsolete, when parts must be removed and replaced by technical order change (TOC) items, or when a batch of equipment or consumable materiel is found defective. Like those on the green tag, the block entries have been discussed previously, or they are self-explanatory by their titles.

Exercises (051):

1. State the purpose of the following three DD Form 157X series condition tags:
    a. DD Form 1574 (yellow tag).
    b. DD Form 1577–2 (green tag).
    c. DD Form 1577 (red tag).
2. If you repaired a unit that had a serial number, what tag should you use and how should you fill it out?
3. If you bench checked a serial numbered unit and had to order a carbon resistor, what tag should you use and how should you fill it out?
4. If you are directed by AFLC to condemn a unit but the unit is serviceable, what tag should you use?

052. State the purposes of forward supply points and bench stocks.



This Tag Colored Red

WARNING Unauthorized persons removing, defacing, or destroying this tag may be subject to a fine of not more than $1,000 or imprisonment for not more than one year or both (18 USC 1361)

FSN, PART NO. AND ITEM DESCRIPTION
5905-396-1586
RESISTOR

SERIAL NUMBER/LOT NUMBER
305

UNIT OF ISSUE
EA

QUANTITY
1

REMARKS

UNSERVICEABLE (CONDEMNED) TAG
MATERIEL

INSPECTION ACTIVITY
2052 COMM SQ

CONDITION CODE
H

REASON OR AUTHORITY
OPEN

INSPECTOR'S NAME OR STAMP AND DATE
JOHN DOE 15 JUN 84

DD FORM 1577, 1 OCT 66

Figure 6-5. Sample, DD Form 1577 (red).

Requisition Supplies/Parts. Supply customers are an integral part of the base-level supply system. To a large degree, your actions determine the ability of the base supply organization to support your demands. Organization commanders must, therefore, insure that designated supply representatives are thoroughly familiar with the contents of AFR 67-23, *Standard Base Supply Customers Guide.* The chief of supply should assist organization commanders in this effort as much as possible. Close liaison between them will contribute to a mutual understanding and resolution of problems that affect their ability to meet assigned missions.

When reparable parts are needed, you first check to see if the parts are located in the forward supply point. If the parts are expendable, you first check your bench stock. If the parts you need are not available at either location, then you order the parts from Base Supply.

Supply Point. Supply points are established in coordination between the chief of supply and the chief of maintenance. Items stocked in the supply point normally are assets that are peculiar to the needs of the supported activity and have a high rate of usage. The purpose of the supply point is to make these assets immediately available to the using activity.

The supported activity must submit to the supplies management office a list of items to be placed in the supply point. The following information is required:

a. Stock number.
b. Part number.
c. Noun.
d. End item application.
e. Whether functional check calibration is required before being stored in the supply point.

A list of items stocked in the supply point is provided to the supporting materiel control and other activities as required.

All supply point issues are over the counter. At the time of issue, you should provide the stock number, the quantity required, and the organization/shop codes.

Bench Stock. Bench stock consists of low-cost expendable items which, due to repetitive consumption, are placed at the point of use before actual need. The most obvious advantage to this system is that the items are immediately available to the user. There are certain disadvantages. From a customer's viewpoint, the most important of these if the fact that, with few exceptions, bench stock assets are funded items and must be paid for by the organization before actual use. The organizational commander must be aware of the dollar value of bench stock items to insure that adequate money is available to support requirements. The commander should also review any request for special levels.

The initial establishment of a bench stock is a coordinated effort between the organization and the supplies management office (SMO). This may be accomplished by submission of a letter to the SMO citing the organization and shop code, stock numbers and units of issue of the requested items, and the recommended 30-day level. This method also can be used to add or delete an item on an existing bench stock. If there has been no previous consumption on the requested items, or if past consumption is not sufficient to support the requested levels, a minimum operating level should be established. In this event contact the SMO for assistance.

Exercises (052):

1. State the purpose of bench stock.

2. State the purpose of supply points.

053. State the purpose of AF Form 2413, Supply Control Log, and give the meaning of selected entries on this form.

AF Form 2413, Supply Control Log. AF Form 2413 is a running account of all parts and supplies that have been ordered by your section. If properly maintained, it shows the status of all parts, whether they have been received, whether they are on back order, or whether they have been canceled.

The AF Form 2413 is divided into 16 columns. A line entry is made for each item ordered with information about the item provided in each column on that line. The heading line at the top has entries for your unit and the page number.

The columns are filled in as follows:

(1) A, DLVR DESTN Code — Where part is to be delivered (quite often the building number is used).

(2) B, Requested by — Self-explanatory.

(3) C, Stock-Part-Quick Reference List Number — Stock and part number is self-explanatory. The basic purpose of a quick reference list (QRL) is to provide maintenance personnel with a speedy identification and communication capability for placing a demand on Supply. Additionally, the listings aid Supply by eliminating repetitive research. When a base elects to use the QRL, Maintenance Supply Liaison coordinates with Supply for the initial selection of QRL items by the use of Supply computer programs to identify high-usage items. This coordination may include the requirement for Supply to assume responsibility for revision and final publication of quick reference lists. Final selection of items on the QRL is made by the Maintenance Supply Liaison.

(4) D, Unit of Issue — Self-explanatory.

(5) E, QNTY — Self-explanatory.

(6) F, Noun — Self-explanatory.

(7) G, Job Control Number — Job control number is the same one that is on your AFTO Form 349 or AFTO Form 350.

(8) H, Document Number — Most of the transaction you process with Base Supply are assigned an organizational document number consisting of 14 alphanumeric characters. It is a control or reference number that is used to identify a specific transaction. For example: R622HS-41670019.

R = Activity code (1 alpha)
622 = Organization code (3 numeric)
HS = Shop code (2 alpha)
4167 = Julian date (4 numeric)
0019 = Serial number (4 numeric)

a. Activity Code — This code identifies the method or location used by an organization in processing an issue or turn-in request to Base Supply. In some cases, it further identifies the type of item; for example, bench stock and war reserves materiel. The codes you normally use are:

B = Bench stock
E = Equipment
L = Bulk issue
M = Mission support kits
P = Non-EAID equipment
R = Routine
S = Supply point
U = War-readiness spares kit
X = Expedite

b. Organizational Code — This code is used to specifically identify your unit or subordinate activities. These codes are assigned by Base Supply in specific series for various types of activities, as directed by AFM 67-1. These same codes also are used by the base comptroller to maintain dollar data on the supplies and equipment drawn from or turned in to Base Supply.

c. Shop Code — This code further identifies the shop or office within your organization.

d. Julian Date — This is the standard Julian date; for example, 4167 is 15 June 1984. It indicates the date the document serial number was assigned.

e. Serial Number — These numbers are assigned beginning with 0001 daily for each activity code. They are manually assigned, normally by Base Supply.

(9) J, Demand Code — "R" for recurring or "N" for nonrecurring type items.

(10) K, PROJ Code — This block is seldom used.

(11) L, Priority — This is the delivery priority and you can find the legend for this in the lower right block of AF Form 2413.

(12) M, UJC — Urgency justification code (UJC) is a two-character code used to indicate urgency of need.

(13) N, Mark For — This is used to indicate the equipment for which the item is ordered.

(14) P, TO, Figure, and Index — These are from the Illustrated Parts Breakdown TO.

(15) Q, Time — Ordered is time only and received is both time and date.

(16) R, Remarks — This block is for remarks such as back ordered, request killed, request canceled, etc.

Exercises (053):

1. State the purpose of AF Form 2413.

2. What is a QRL?

3. What is the purpose of a QRL?

4. What are the five parts of a document number?

5. What is the purpose of the activity code?

6. What are the meanings of activity codes "R" and "X"?

7. What is a UJC?

8. Where would you get the information for column P?

054. State when the selected entries should be made on AF Form 2005, Issue/Turn-in Request.

AF Form 2005, Issue/Turn-in Request. The following information is required when submitting AF Form 2005, Issue/Turn-In Request. Review the entries made on the AF Form 2413 (fig. 6-6) for identical entries of these items:

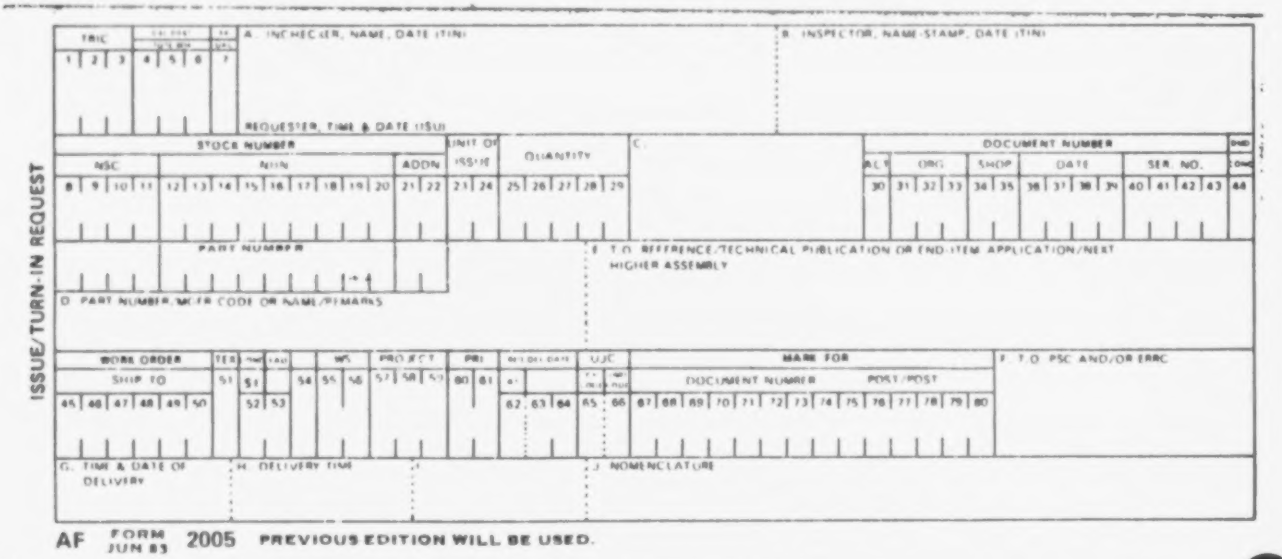
a. Name of requesting individual.
b. Delivery destination.
c. National Stock Number (NSN). If NSN is not available, furnish the manufacturer's part number and TO reference. If the item is nonlisted (no NSN is assigned), DD Form 1348-6, Non-NSN Requisition, also must be submitted.
d. Unit of issue.
e. Quantity.
f. Organization and shop code.
g. Demand code.
h. FAD (force activity designator) is used when the required item is for direct support of an organization having a higher priority FAD.
i. UJC.
j. Mark for.

If the requirement is for an NMCS (not mission capable — supply) or PMCS (partially mission capable — supply) reportable item, furnish the type, model, series, and serial number of the applicable equipment.

When the item is a first-time request, Materiel Control verifies the requirement and determines whether the item is recurring or nonrecurring. This action is taken before back order by the supplies management officer. When the action is determined to be recurring, Materiel Control recommends an anticipated stock level to assist the supplies management officer in establishing a stock level.

Exercises (054):

1. When is an FAD entry required?



ISSUE/TURN-IN REQUEST
TRIC
A. INCHECKER, NAME, DATE (TIN)
B. INSPECTOR, NAME-STAMP, DATE (TIN)
REQUESTER, TIME & DATE (ISU)
STOCK NUMBER
NSC
NIIN
ADDN
UNIT OF ISSUE
QUANTITY
C.
DOCUMENT NUMBER
ACT
ORG
SHOP
DATE
SER. NO.
PART NUMBER
E. T.O. REFERENCE/TECHNICAL PUBLICATION OR END-ITEM APPLICATION/NEXT HIGHER ASSEMBLY
D. PART NUMBER/MCFR CODE OR NAME/REMARKS
WORK ORDER
SHIP TO
WS
PROJECT
PRI
UJC
MARK FOR
DOCUMENT NUMBER
POST/POST
F. T.O. PSC AND/OR ERRC
G. TIME & DATE OF DELIVERY
H. DELIVERY TIME
J. NOMENCLATURE

AF FORM JUN 83 2005 PREVIOUS EDITION WILL BE USED.

Figure 6-6.

2. When are the type, model, series, and serial number entries required?

055. State the procedures for ordering supplies and parts through the demand processing section of Base Supply.

Supply Request Procedures. Demands will normally be made by telephone or radio for supply delivery priorities 1 through 4. When the volume of issue requests would restrict call-in to Demand Processing or when workload dictates, AF Form 2005 may be prepared and handcarried to Supply. Demands for items stored in the supply points may be placed over the counter or through Demand Processing. Where call-in to Demand Processing is available, it should be used.

The requestor will complete the line entry on AF Form 2413 and provide the information from columns A through P (with a few exceptions) in sequence for demand call-in. The exceptions are:

a. Column B--also give telephone number.

b. Column G--not applicable for call-in.

c. Column H--The document number's Julian date is already known by Supply and they will give you the serial number.

To complete the call-in entries, the document number, as provided by Supply, will be entered and the time ordered.

The AF Form 2413 is retained by the requesting organization or shop for verification of the daily document register (DO4). The organizational maintenance activity verifies only those issue requests created for their organization and the shop codes on the daily document register.

Routine parts request for non-NSN items are delivered to Demand Processing accompanied by a DD Form 1348-6, *Non-NSN Requsition (Manual).* These forms are prepared as outlined in AFM 67-1.

Exercises (055):

1. What procedure should you use for demand call-in?

2. What procedure should you use for routine non-NSN items?

056. State the purpose of AF Form 601, Equipment Action Request.

AF Form 601, Equipment Action Requestion. You cannot order equipment, such as test equipment, by the same method that you use for supplies/parts. You, as the equipment custodian (the person responsible for all equipment), must order your equipment through the equipment management office (EMO).

The custodian uses the AF Form 601 to request allowance and authorization change and/or issue and turn-in of equipment. The EMO also uses this document to notify custodians of action taken on requests.

Before submitting a request, carefully screen the custody receipt listing to insure that the desired item or a suitable substitute is not on hand.

The custodian obtains the signature of the organization commander or designated representative, retains one copy, and forwards the remaining copies to EMO.

Exercises (056):

1. What type of items are ordered on AF Form 601?

2. Who is authorized to order equipment on a AF FORM 601?

Bibliography

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AFR 0-2, *Numerical Index of Standard and Recurring Air Force Publications.*

AFR 0-9, *Numerical Index of Departmental Forms.*

AFR 5-1, *Air Force Publications Management Program.*

AFR 5-4, *Numbering Publications.*

AFR 8-2, *Air Force Technical Order System.*

AFR35-1, *Military Personnel Classification Policy (Officers, Warrant Officers, Airmen).*

AFR 39-1, *Airman Classification Regulation.*

AFR 50-38, *Field Evaluation of Education and Training Programs.*

AFR 66-1, *Maintenance Management Policy.*

AFP 66-10, *Maintenance Management Information and Control System (MMICS) Guide for Maintenance Managers.*

AFR 66-278, *Maintenance Management Information and Control System (MMICS) DSD: GO73/RF, Users Manual.*

AFR 67-23, *Standard Base Supply Customer's Guide.*

AFR 125-37, *The Resources Protection Program.*

AFR 127-12, *Air Force Occupational Safety and Health Program.*

AFR 205-1, *Information Security Program.*

AFR 207-1, *The Air Force Physical Security Program.*

AFM 300-4, *Classified Data Elements and Codes.*

Air Force Occupational Safety and Health Standards

AFOSH Standard 127-50, *Ground Communication-Electronics (C-E) Systems.*

Department of Defense Publications

DOD 5200.1-R, *Information Security Program.*

Answers for Exercises

CHAPTER 1

References:

001 – 1. Career field, skill level, and specific specialty.
001 – 2. Most highly trained and qualified to perform.

002 – 1. AFR 39–1.
002 – 2. High speed, general-purpose, and special electronic computer and switching systems.

003 – 1. Modifications.
003 – 2. Operational testing procedures.
003 – 3. Work; reviews.

004 – 1. AFR 39–1.
004 – 2. Physics and mathematics.
004 – 3. (1) Installing, (2) repairing, (3) testing, or (4) modifying.
004 – 4. AFR 205–32.

005 – 2. Field evaluation visits and direct correspondence questionnaires.
005 – 2. The Specialty Training Standard.
005 – 3. AF Form 1284, Training Quality Report.
005 – 4. To pinpoint the ability of graduates to perform the tasks they were trained to do.

CHAPTER 2

006 – 1. DOD 5200.1–R, *Information Security Program.*
006 – 2. AFR 205–1, *Information Security Program.*
006 – 3. AFR 207–1, *The Air Force Physical Security Program.*

007 – 1. Security classification guides.
007 – 2. Security classification guides.
007 – 3. When prepared by supervisors and tailored for use in individual workcenters.
007 – 4. A listing of sensitive information that should be protected.

008 – 1. To regulate the protection of classified government information in the hands of industry.
008 – 2. The contractor must adhere to the same security practices followed for protecting, marking, and controlling the same category of information still in USAF possession.
008 – 3. It helps protect classified Government information by prescribing uniform security practices to be used in industrial plants, educational institutions, and other facilities used by contractors with access to or possession of classified information.

009 – 1. To deter hostile actions; to provide the right quality and quantity of protection for resources.
009 – 2. Priority A, priority B, and priority C.
009 – 3. (1) Restricted area; land where priority resources are under the control or jurisdiction of DOD; and (2) National defense area: land where priority A resources are located without the land being under the control or jurisdiction of DOD.

010 – 1. (1) c.
(2) a.
(3) e.
(4) d.

011 – 1. Detection of hostile acts and security violations, sounding an alarm (notifying CSC), and responding to prevent or limit damage, stop the person(s) involved, and/or keep the situation from getting worse.
011 – 2. By being alert to everything going on around you on your job; by shouting HELPING HAND or COVERED WAGON, as appropriate; by notifying CSC; and by Responding in any way you can to control the situation.
011 – 3. A possible hostile event occurring against priority A or B resources.
011 – 4. An actual or probable hostile act occurring against priority A or B resources.
011 – 5. (1) a.
(2) b.
(3) a.

012 – 1. Investigations or studies of compromising emanations.
012 – 2. To deny enemy access to the information we transmit.
012 – 3. When that equipment is processing classified information.

013 – 1. Measures taken to reduce enemy attempts at intercepting and analyzing information emanating from equipment.
013 – 2. All panels secure, all screws installed, built in tempest protection not defeated, all grounds connected, TO was followed for maintenance, test equipment disconnected, and no radio receivers near equipment.
0113 – 3. Supervisor or tempest representative only.

CHAPTER 3

014 – 1. Report the condition, using AF Form 457.
014 – 2. All supervisors and employees will be given safety and health training.
014 – 3. To develop and enforce standards to insure safe and healthy working conditions for all Air Force personnel.

015 – 1. The current capacity to kill or produce nasty burns by heating ring, etc.
015 – 2. Do not short with probe tips; discharge before working around them and keep them discharged by connecting a resistor across them.
015 – 3. Do not short with metal objects (rings, probes, screwdrivers, etc); no smoking or open flame near batteries.

016 – 1. Eye protection, heavy-canvas apron, and gauntlet-type gloves.
016 – 2. To prevent electrical shock.
016 – 3. The high vacuum inside the glass envelope.
016 – 4. It may cause it to fracture and implode.

017 – 1. Set up a work area for regular soldering, use a holder, and do not leave it on and unattended.
017 – 2. To make your work easier and prevent either dropping the work or burning yourself.
017 – 3. Use eye protection in the form of prescription glasses, safety glasses, or face shields.

018 – 1. Your reaction to electrical shock.
018 – 2. Sharp edges.
018 – 3. Wear long sleeves, keep clear of sharp edges, leave yourself plenty of room, don't overreach, and do use shields.

019 – 1. a. Use correct-sized blade.
b. Use the correct type.
c. Use the correct size and type.
d. Use an iron or gun with a low enough wattage to do the job and watch out for accidental burns.
e. Wear goggles.

f. Use gloves.
g. Do not stick the metal nozzle into energized equipment.
019 – 2. Make sure you are using the correct piece of test equipment; insure the instrument is correctly connected in the circuit; and when possible, connect the test instrument used prior to turning the power on.
019 – 3. By using the proper test leads on test equipment, we reduce the possibility of shock or accident to the technician and damage to the equipment.

020 – 1. Make sure the materials are stored properly; be sure the storage areas are properly ventilated; and be sure to place NO SMOKING signs in the storage area.
020 – 2. No smoking is ever permitted in an area containing volatile solutions or fuels.
020 – 3. Do not spray it into your eyes.
020 – 4. Be extremely careful not to get any of the liquid in your eyes.

021 – 1. To protect the equipment and to prevent a slipping or tripping hazard.
021 – 2. Danger of fire.
021 – 3. Paper tape residue could cause an accident.

(1) f.
(2) c.
(3) d.
(4) g.
(5) e.
(6) a.
(7) b.

CHAPTER 4

023 – 1. Departmental publications are issued by Headquarters USAF; field publications are issued at major command or below.
023 – 2. a. Departmental.
b. Departmental.
c. Field.
d. Field.
e. Field.

024 – 1. (1) d.
(2) e.
(3) b.
(4) a.
(5) c.

025 – 1. Operating instructions.
025 – 2. Visual aids.
025 – 3. Regulations.
025 – 4. Pamphlets.
025 – 5. Manuals.

026 – 1. Identifies the broad area of Air Force publications.
026 – 2. The specific area within the broad area indicated by the first number.
026 – 3. To index and categorize all publications in an orderly fashion.

027 – 1. AFR 0–2, *Numerical Index of Standard and Recurring Air Force Publications.*
027 – 2. AFR 0–9, *Numerical Index of Departmental Forms.*
027 – 3. AFR 0–2, *Numerical Index of Standard and Recurring Air Force Publications.*

028 – 1. The AFR 0–2 for your file.
028 – 2. A minus (–) in the left margin in front of the listing.
028 – 3. By checking the date on the publication against the listing in AFR 0–2.

029 – 1. TO 00–5–1 and TO 00–5–2.
029 – 2. Preliminary TOs.
029 – 3. Index TOs.
029 – 4. (1) TMs, (2) TCTOs, (3) abbreviated TOs, (4) indexes, (5) preliminary TOs, and (6) commercial manuals.

030 – 1. An abbreviated TO in the form of workcards.
030 – 2. The digits indicate an Illustrated Parts Breakdown/Parts catalog TO.
030 – 3. The preface of each NI&RT explains TO numbering.

031 – 1. TO 0–1–01.
031 – 2. NI&RT TO 0–1–33–2.

032 – 1. The activity responsible for the TO file.
032 – 2. The NI&RT.
032 – 3. TO 00–5–2.
032 – 4. It must be mission essential.

031 – 1. Illustrated parts breakdown (IPB).
031 – 2. Servicing instructions.
031 – 3. Operating instructions.

034 – 1. Immediate, Urgent, and Routine.
034 – 2. All affected personnel must be notified within 4 hours.
034 – 3. Permits rapid dissemination of unsafe condition information to units until a formal Immediate Action TCO is distributed.
034 – 4. Action is taken to stop the use of equipment or system affected.

035 – 1. Work simplification devices to aid in carrying out instructions contained in other types of technical orders.
035 – 2. Demands are listed in sequence in the left column, responses are listed in the right column.
035 – 3. Inspection workcards.

036 – 1. The individual who discovers the deficiency.
036 – 2. Typographical errors or misspelled words.
036 – 3. TO 00–561.
036 – 4. After 90 days.

CHAPTER 5

037 – 1. The element of an organization responsible for insuring that Air Force materiel is serviceable, safely operable, and configured to meet mission requirements.
037 – 2. Inspection, repair, overhaul, modification, preservation, testing, and analysis of condition or performance.

038 – 1. On-equipment maintenance is performed on the computer or equipment; off-equipment maintenance is performed on units which were removed from the computer or equipment.
038 – 2. Tasks which require special equipment or skills that are not available at the mission-oriented unit.
038 – 3. On-equipment and off-equipment tasks using the equipment and skills available in the unit.

039 – 1. Deputy commander for maintenance (DCM).
039 – 2. Operations, maintenance, and resources management.
039 – 3. Provide leadership and management for their wing or unit, and consolidate functions.

040 – 1. Manager of the maintenance complex.
040 – 2. Staff functions plan, control, and schedule maintenance.

041 – 1. Maintenance control.
041 – 2. Prepares and maintains reports, correspondence, and local maintenance directives in support of the maintenance effort.
041 – 3. Serves as the source for statistical data used in managing maintenance.
041 – 4. Job proficiency, qualification, and special training.
041 – 5. Plans and scheduling, job control, and materiel control.
041 – 6. Controls the jobs that are initiated and done.

041 – 7. Provides maintenance personnel with the materiel resources necessary for job completion.

042 – 1. Improve quality of maintenance and technical competency of personnel.
042 – 2. Training and personnel evaluations.
042 – 3. The supervisor.
042 – 4. Quality Control or supervisor.

043 – 1. Centralized maintenance management and production oriented maintenance.
043 – 2. Under the centralized maintenance management concept, specialist are dispatched under central direction and control, and specialists perform only those duties that are directly related to their AFSC. Under POMO, the maintenance shop are decentralized, and both people and equipment are assigned to smaller shops. Maintenance personnel may have to perform selected maintenance tasks that are not part of their AFSC.
043 – 3. Cross utilization training which is for individuals to perform simple maintenance tasks, with little or no supervision, that aren't part of their AFSC.

CHAPTER 6

044 – 1. Information such as what job was done, who did the work, when it was done, number of direct man-hours consumed for a job, why the job was necessary, when the malfunction was discovered, and what workcenter performed the work is provided to management.
044 – 2. A job that has a definite beginning and end, the accomplishment of which requires expenditure of direct labor.
044 – 3. a. Administrators and supervisors are able to analyze and evaluate their operations.
b. Workcenter supervisors are helped in managing their shops and in increasing their efficiency.
c. The COM and his staff use this information for personnel planning, for forecasting tool and equipment needs, for budget computations, and for cost analysis.
d. AFLC uses this data for inspection and maintenance requirements analysis, and determining cost.

045 – 1. AFTO Form 349 and AFTO Form 350.
045 – 2. AFTO Form 349 is used to report all on-equipment and off-equipment maintenance actions, and all work-directed time compliance TOs. AFTO From 350 is attached to the item when it is removed and taken to the shop or repair depot.
045 – 3. A three-digit Julian date followed by a four-digit number sequenced by day or month.
045 – 4. TO –06, Work Unit Code Manual.
045 – 5. A technician's first letter of the last name, followed by the last four digits of the Social Security number or the assigned five-digit number.
045 – 6. Parts replaced during the repair action.
045 – 7. Part I is the repair cycle processing tag; Part II is used for production scheduling.
045 – 8. One AFTO Form 349 for on-equipment work — used to show removal; a second AFTO Form 349 to show repair action; and one AFTO Form 350 to identify an assembly removed from the end item.

046 – 1. F; they are repaired at base level, if possible.
046 – 2. T.
046 – 3. T.
046 – 4. T.
046 – 5. T.
046 – 6. F; "Not reparable this station."

047 – 1. Operational events.
047 – 2. Inspection and time changes.
047 – 3. Maintenance personnel subsystem.
047 – 4. Time compliance technical order subsystem.

048 – 1. Discovering and fixing conditions that could lead to malfunctions requiring major repair.
048 – 2. Scheduled maintenance.
048 – 3. Statement of job purpose; a listing of all required tools, test equipment, and materials required; step-by-step instruction for doing the job; frequency of the routine, time needed, and power condition; and the measurable equipment performance tolerances.
048 – 4. Chief of maintenance.
048 – 5. (1) Technical, (2) activity, and (3) special. Technical inspections are made to determine if the equipment is being maintained to meet TO specifications. Activity inspections are made to determine the quality of management of the maintenance activity. Special inspections are made to provide maintenance supervisors or managers information on one-time situations of either administrative or technical nature.
048 – 6. Quality control inspection reports are routed through supervisory channels to QC Deficiency Analysis; all activity inspection reports will be routed through the COM.
048 – 7. A completed AFTO Form 349.

049 – 1. Failure of an end item due to an unpredictable failure of an internal component or subassembly.
049 – 2. Equipment capability is reduced due to excessive man-hours expended in the maintenance of the equipment.
049 – 3. Feedback of data to correct or prevent deficiencies in the design or quality of materiel.

050 – 1. Category II MDR.
050 – 2. Defects that don't affect the usability of an item.
050 – 3. Submitted by electrical transmission within 72 hours.
050 – 4. Category II MDR.

051 – 1. a. Indicates serviceable condition of item.
b. Indicates repairable condition of item.
c. Indicates item is condemned or not repairable.
051 – 2. Use DD Form 1574 and fill in the self-explanatory blocks. Enter the serial number in the Serial Number/Lot Number block and leave the Contract or Purchase Order No. block blank.
051 – 3. Use DD Form 1577 – 2, fill in the self-explanatory blocks, and enter the serial number in the Serial Number/Lot No. block.
051 – 4. Use DD Form 1577.

052 – 1. To provide immediate availability of low-cost expendable items subject to repetitive consumption.
052 – 2. To provide assets that are peculiar to the needs of the support activity and that have high rates of usage.

053 – 1. It is a running account of all parts and supplies that have been ordered.
053 – 2. Quick Reference List.
053 – 3. To provide maintenance personnel with speedy identification of assets and a communication capability for placing demands on Supply.
053 – 4. Activity code, organization code, shop code, Julian date, and serial number.
053 – 5. It identifies the method or location used by an organization in processing an issue or turn-in request to Base Supply.
053 – 6. "R" means a routine transaction and the "X" means an expedite transaction.
053 – 7. It is a two-character code used to indicate urgency of need.
053 – 8. The Illustrated Parts Breakdown TO.

054 – 1. When the required item is for direct support of an organization having a higher priority FAD.
054 – 2. When the requirement is for an NMCS or PMCS reportable item.

055 – 1. Fill out AF Form 2413, call in appropriate columns to Demand Processing, and record the document number, serial number, and time on the AF Form 2413.

055 - 2. For hand-carried request, they will be accompanied by DD Form 1348-6, Non-Nsn Requisition. For call-in, you must furnish the information over the phone so they can fill out DD Form 1348-6.

056 - 1. Equipment items.
056 - 2. Equipment custodian.

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STOP- 1. MATCH ANSWER SHEET TO THIS EXERCISE NUMBER.
2. USE NUMBER 2 PENCIL ONLY.

EXTENSION COURSE INSTITUTE
VOLUME REVIEW EXERCISE

30554 01 25

MAINTENANCE ORIENTATION

Carefully read the following:
DO's:

1. Check the "course," "volume," and "form" numbers from the answer sheet address tab against the "VRE answer sheet identification number" in the righthand column of the shipping list. If numbers do not match, return the answer sheet and the shipping list to ECI immediately with a note of explanation.
2. Note that item numbers on answer sheet are sequential in each column.
3. Use a medium sharp #2 black lead pencil for marking answer sheet.
4. Write the correct answer in the margin at the left of the item. (When you review for the course examination, you can cover *your* answers with a strip of paper and then check your review answers against your original choices.) After you are sure of your answers, transfer them to the answer sheet. If you *have* to change an answer on the answer sheet, be sure that the erasure is complete. Use a clean eraser. But try to avoid any erasure on the answer sheet if at all possible.
5. Take action to return entire answer sheet to ECI.
6. Keep Volume Review Exercise booklet for review and reference.
7. If *mandatorily* enrolled student, process questions or comments through your unit trainer or OJT supervisor. If *voluntarily* enrolled student, send questions or comments to ECI on ECI Form 17.

DON'Ts:

1. Don't use answer sheets other than one furnished specifically for each review exercise.
2. Don't mark on the answer sheet except to fill in marking blocks. Double marks or excessive markings which overflow marking blocks will register as errors.
3. Don't fold, spindle, staple, tape, or mutilate the answer sheet.
4. Don't use ink or any marking other than a #2 black lead pencil.

NOTE: **NUMBERED LEARNING OBJECTIVE REFERENCES ARE USED ON THE VOLUME REVIEW EXERCISE.** In parenthesis after each item number on the VRE is the *Learning Objective Number* where the answer to that item can be located. When answering the items on the VRE, refer to the *Learning Objectives* indicated by these *Numbers*. The VRE results will be sent to you on a postcard which will list the *actual* VRE *items you missed*. Go to the VRE booklet and locate the *Learning Objective Numbers* for the items missed. Go to the text and carefully review the areas covered by these references. Review the entire VRE again before you take the closed-book Course Examination.

Name	Grade/Rank	SSN	Date

MULTIPLE CHOICE

Note to Student: Consider all choices carefully and select the *best* answer to each question.

1. (001) In the Air Force Speciality Code (AFSC) coding method, the fourth digit identifies the

   a. career field.
   b. career field subdivision.
   c. skill level of the AFS.
   d. specific specialty.

2. (001) What AFSC is used as a management tool for assignment against authorized manning requirements?

   a. CAFSC.
   b. DAFSC.
   c. TAFSC.
   d. PAFSC.

3. (002) What regulation provides a description of the duties of an Electronic Computer and Switching Systems Specialist?

   a. AFR 35-1.
   b. AFR 39-1.
   c. AFR 39-6.
   d. AFR 39-11.

4. (002) Which of the following jobs will most likely be performed by a 5-level specialist?

   a. The repair of an electronic switching system component.
   b. Modification of a computer terminal keyboard.
   c. Inspect the repair of a minicomputer.
   d. Evaluate personnel under MSEP.

5. (003) Which of the following responsibilities belong to a 30554 specialist?

   a. Advise and direct all personnel.
   b. Establish and monitor training programs.
   c. Align and adjust computer and switching systems.
   d. Repair and monitor precision measurement equipment.

6. (004) Which of the following requirements is mandatory for the award of AFSC 30554?

   a. Completion of a basic electronic computer or switching system maintenance course.
   b. Knowledge of radar and communications principles.
   c. Experience in programming large computer systems.
   d. Completion of high school physics.

7. (004) Which of the following is *not* a mandatory requirement for AFSC 30554?

   a. A Secret security clearance.
   b. A knowledge of oscilloscope operation.
   c. Operational experience in the use of test equipment.
   d. Completion of a high school course in mathematics.

8. (005) The field evaluation program provides a source of information in determining the

   a. need to update the JPG.
   b. need to revise the approved STS.
   c. extent of on-the-job training effectiveness.
   d. result of formal training.

9. (005) In evaluating graduates of technical schools, a supervisor should prepare an AF Form 1284, Training Quality Report, when

   a. a graduate does not meet an STS performance level.
   b. a graduate has not has a chance to perform an STS task.
   c. a particular task is not required in your unit.
   d. an STS item is not required.

10. (006) Which directive provides guidance for safeguarding classified information?

   a. DOD 5200.1-R, *Information Security Program*.
   b. AFR 125-37, *Protection of USAF Resources*.
   c. AFR 200-1, *Air Force Intelligence Mission Responsibilities and Functions*.
   d. AFR 300-5, *Air Force Data Elements Standardization Program*.

11. (006) What is the purpose of AFR 205-1, *Information Security Program?*

   a. Replaces DOD 5200.1-R.
   b. Supplements DOD 5200.1-R.
   c. Implements Privacy act of 1974.
   d. Provides policies for safeguarding computers.

12. (007) Who is responsible for furnishing you with security classification guidance when you handle classified information?

   a. Classified Information Officer.
   b. Plans and Program Security Manager.
   c. Each individual commander or supervisor.
   d. Commander responsible for initial classification.

13. (007) Which of the following is *not* an Essential Element of Friendly Information?

   a. Status of tactical training.
   b. Personnel deficiencies.
   c. Itinerary of the General's visit.
   d. Phone number of an individual.

14. (008) On a contract involving classified materials or information, the Industrial Security Program covers

   a. an agreement to abide by DOD rules for labor.
   b. all aspects of the contract activity.
   c. an agreement to abide by USAF rules for labor.
   d. controls to prevent strikes and labor disputes.

15. (009) Which of the following would be a priority A operational resource?

   a. Resources most vital to the United States war-making ability.
   b. Non-nuclear alert aircraft.
   c. High-value aircraft systems.
   d. Operational aircraft which can be generated to alert status in a short period of time.

16. (009) Those operational resources on an Air Force base that have a priority assigned are placed in which security area?

   a. Controlled area.
   b. National defense area.
   c. Restricted area.
   d. Fenced area.

17. (010) A civilian employee was discharged from his job. After having several beers, he slashed the tires of five AF vehicles. His action characterizes

a. espionage.	c. vandalism.
b. sabotage.	d. larceny.

18. (011) For which three progressive steps under the Air Force Physical Security Program are you responsible?

a. Detect, alarm, and respond.	c. Detect, challenge, and report.
b. Alarm, challenge, and report.	d. Challenge, identify, and report.

19. (011) What form of report should you transmit if you see a person fire a rifle at alert aircraft?

a. Safe Wind.	c. Broken Arrow.
b. Helping Hand.	d. Covered Wagon.

20. (012) Tempest is concerned with emanations from

a. computers processing data.
b. electronic equipment used for data storage.
c. printers typing classified data.
d. radio transmitters used on base.

21. (013) What emission security steps should you take when the equipment is processing classified information?

a. Connect grounds and connect an approved oscilloscope.
b. Follow the TO and use a digital voltmeter.
c. Connect grounds and install screws.
d. Secure panels and connect approved oscilloscope.

22. (014) Policy for the Air Force Occupational Safety and Health (AFOSH) Program is established by

a. AFR 127-101.	c. AFR 127-3.
b. AFR 127-12.	d. AFR 127-1.

23. (014) Which of the following is *not* a specific individual responsibility under the AFOSH program?

a. To comply with AFOSH standards.
b. To report unsafe or unhealthy conditions.
c. To report injuries or illnesses sustained on or off the job.
d. To wear or use all required protective clothing, eye protection, hard hats, or other equipment.

24. (015) The minimum amount of electrical current required to kill an average person is

a. .01 ampere.	c. 0.5 ampere.
b. 0.1 ampere.	d. 1 ampere.

25. (015) What additional hazard does a storage battery have that a power supply does not?

a. Explosive gas.
b. Current capacity to electrocute.
c. Produces arc weld sparks when shorted.
d. High current capable of making a ring red hot.

26. (016) Why are gloves, face shield, and an apron necessarv when handling a cathode ray tube?

a. The glass tube has sharp edges.
b. The tube could implode.
c. The connector pins may have high voltage.
d. The tube contains phosphorus.

27. (016) Concerning cathode ray tubes, which of the following is *not* a hazard?

a. High voltage charge.
b. High current.
c. Implosion.
d. X-ray.

28. (017) Which of the following is the proper use of a tool?

a. Using a screwdriver to obtain extra leverage.
b. Using a wrench to check an electrical circuit.
c. Using a 20-40 watt soldering iron to remove a capacitor from a circuit board.
d. Using pliers as a punch.

29. (017) Which item should *not* be part of your soldering area?

a. A small vice to hold articles.
b. A fire extinguisher, just in case.
c. A metal can to flick solder into.
d. A holder for the soldering iron.

30. (018) Which of the following is *not* recommended when working near sharp edges within equipment cabinet?

a. Avoid electrical shock.
b. Wear short sleeves.
c. Maintain balance.
d. Keep hands and arms clear.

31. (019) When using test equipment on computer or switching equipment that uses a power supply that is isolated from the ground, what must be used to power the test equipment?

a. Three-phase AC.
b. Equipment power supply.
c. A step-up transformer.
d. An isolation transformer.

32. (020) Which of the following does not leave an oily residue and is normally used for cleaning printed circuit boards?

a. Freon.
b. Alcohol.
c. Contact cleaner.
d. Hydrocarbol solvent.

33. (020) Which of the following is regarded as the all-purpose cleaner in ground electronics?

a. Isopropyl alcohol.
b. Freon.
c. Contact cleaner.
d. Trichloroethylene.

34. (020) Concerning the storage of chemicals or diesel fuel, NO SMOKING signs must be posted stating that no smoking is permitted within

a. 25 feet.
b. 50 feet.
c. 75 feet.
d. 100 feet.

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35. (021) When exercising good housekeeping practices, you should

a. provide a professional appearance in your work area.
b. properly use equipment dust covers.
c. provide a safe work area.
d. do all of the above.

36. (022) When working on equipment capable of producing 50 volts and 100 milliamperes AC, what safety practice must be followed?

a. Keep one hand in your pocket.
b. Discharge all power supply capacitors.
c. Use the two-man concept.
d. Deactivate safety interlocks.

37. (022) What are fuses and circuit breakers *not* designed to do?

a. Protect people.
b. Turn power on/off.
c. Open when overloaded.
d. Prevent equipment damage.

38. (023) What are the two general classes of Air Force publications?

a. Departmental and field.
b. Headquarters and field.
c. Departmental and major command.
d. Air Force and major command.

39. (023) Who issues departmental publications for use by Air Force personnel?

a. Department of Defense.
b. Headquarters USAF.
c. Major command.
d. Wing headquarters.

40. (024) Standard publications are issued by

a. Headquarters USAF.
b. major commands.
c. commanders.
d. all of the above.

41. (024) The technical order system is an example of which category of Air Force publication?

a. Standard.
b. Specialized.
c. Non-Air Force.
d. Periodical.

42. (025) Which type of standard publication contains directives and policy material for *all* Air Force personnel?

a. Regulations.
b. Technical orders.
c. Operating instructions.
d. Staff digests.

43. (026) Details of the subject and numbering system used to identify Air Force publications are contained in

a. AFR 5-4.
b. AFR 39-1.
c. AFR 50-2.
d. AFR 205-1.

44. (026) The first number in a standard publication identifying number indicates a

a. level of command.
b. sequence number.
c. specific subject area.
d. broad subject area.

45. (027) What AF directive would you use to find standard publications concerning maintenance?

a. AFR 0-2.
b. AFR 0-4.
c. AFR 0-6.
d. AFM 0-2.

46. (027) Where can you find the first part of a publication number if you know the subject?

a. Front of AFR 0-9.	c. Back of AFR 0-9.
b. Front of AFR 0-2.	d. Back of AFR 0-2.

47. (028) To verify that a publication is up to date, use

a. AFR 8-2.	c. AFR 0-9.
b. AFR 5-31.	d. AFR 0-2.

48. (028) What does a minus sign (-) in the left margin beside a publication reference listed in AFR 0-2 indicate?

a. Publication is obsolete.	c. Publication is on loan.
b. Publication is not required.	d. Publication is on order.

49. (029) A purpose of index type technical orders is to

a. record TOs on hand and on order.
b. show the availability of TOs.
c. list all Air Force publications.
d. list all forms used by the TO system.

50. (029) How are commerical manuals filed for Air Force use?

a. They are not used.	c. A publication number is assigned.
b. A TO number is assigned.	d. Alphabetically by manufacturer's name.

51. (030) What type of information is found in a technical order ending in number -3, -13, -23, etc., through -493?

a. Illustrated parts breakdown.	c. Service instructions.
b. Alignment procedures.	d. Circuit diagrams.

52. (030) Which of the following identifies a time compliance technical order (TCTO)?

a. 31P5-2MPN-522.	c. 31P5-2MPN-13-6.
b. 31P4-2GPX-9-4.	d. 31P5-2MPN-13-9.

53. (030) Preventive maintenance routines are found in which of the following technical order series?

a. -2.	c. -6.
b. -4.	d. -8.

54. (031) Which of the following publications should you use to determine whether a TO is up to date?

a. The alphabetical index.
b. The list of applicable publications.
c. The numerical index and requirement table.
d. AFR 8-2.

55. (031) Which of the following TOs provides an easy means of locating the correct TO category when the type of equipment is known?

a. TO 0-2-1.	c. TO 00-5-1.
b. TO 0-1-01.	d. TO 0-1-31-6.

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56. (032) Policy and procedures for maintaining TO files is contained in

a. TO 00-5-1.
b. TO 00-5-2.
c. TO 00-5-15.
d. TO 00-20-1.

57. (032) A maintenance organization operational file is *normally* authorized how many copies of a particular TO?

a. One.
b. Two.
c. Three.
d. Four.

58. (033) What is the function of the technical manual in a TO series?

a. It outlines PMIs to be accomplished.
b. It acts as a guide to find other TOs of the same series.
c. It provides guidance on installation, operation, servicing, and overhaul of equipment and material.
d. It contains a detailed list of all PMIs, TCTOs, emergency operating instructions, and historical records.

59. (033) Technical manuals for operating instructions, servicing instructions, and illustrated parts breakdown

a. are always printed as one manual.
b. are never printed as one manual.
c. are all given the same TO number.
d. provide information for maintenance.

60. (034) Because of the urgent nature of TCTOs, you must become familiar with

a. TO 00-5-1.
b. TO 00-5-2.
c. TO 00-5-15.
d. TO 00-5-20.

61. (034) Instructions given in a TCTO prescribe a

a. single task element.
b. variety of equipment to be changed.
c. number of equipment changes.
d. modification of equipment.

62. (034) Which type of TCTO requires compliance within 1 to 10 days?

a. Immediate Action.
b. Urgent Action.
c. Routine Action.
d. Record Type.

63. (035) Inspection sequence charts are used

a. for unscheduled inspections.
b. as a guide for preparing work schedules.
c. to perform scheduled inspections.
d. to provide demand-response format.

64. (035) Which abbreviated technical orders provide tasks arranged in a demand-response format?

a. Checklists.
b. Inspection workcards.
c. Inspection sequence charts.
d. All of the above.

65. (036) What type of report is *not* submitted on an AFTO Form 22?

a. Minor.
b. Urgent.
c. Routine.
d. Emergency.

66. (036) What technical order provides detailed instructions on completing AFTO Form 22?

a. TO 0-2-1.
b. TO 0-1-01.
c. TO 00-5-1.
d. TO 00-5-2.

67. (037) In accordance with AFR 66-1, *Maintenance Management Policy*, maintenance personnel must keep equipment

a. properly configured, in original design, and safely operable.
b. properly configured, in original design, and serviceable.
c. serviceable, safely operable, and in a clean condition.
d. serviceable, safely operable, and properly configured.

68. (038) A mission-oriented unit will perform

a. only on-equipment maintenance.
b. only off-equipment maintenance.
c. only tasks using skills and equipment in the unit.
d. all tasks related to that mission.

69. (038) How is remove and replace action categorized if performed at an operational site?

a. On-equipment, depot maintenance.
b. On-equipment, mission-oriented unit maintenance.
c. Off-equipment, depot maintenance.
d. Off-equipment, mission-oriented unit maintenance.

70. (039) Who is responsible for consolidating the functions of the maintenance complex?

a. Unit commander.
b. Chief of maintenance.
c. Deputy commander for maintenance.
d. Major command.

71. (039) Who is the deputy commander for maintenance?

a. Unit commander.
b. Chief of maintenance.
c. A junior manager for C-E maintenance.
d. None of the above.

72. (040) What office has overall responsibility for the maintenance mission?

a. Staff functions.
b. Chief of Maintenance.
c. Maintenance control.
d. Support functions.

73. (041) The support function under the COM that examines maintenance reports is

a. production analysis.
b. training management.
c. programs and mobility.
d. administration.

74. (041) Which of the following is *not* a function of quality control?

a. Technical publications.
b. Maintenance training.
c. Deficiency analysis.
d. Production analysis.

75. (042) A standardized method that improves maintenance quality and capability is the

a. management system and equality program.
b. maintenance systems and evaluations program.
c. management supervisor and evaluation plan.
d. maintenance standardization and evaluation program.

76. (042) If you fail a maintenance personnel evaluation on a job task you were previously certified on, who will now decertify you?

a. Quality control.
b. Supervisor.
c. Quality control or supervisor.
d. Supervisor or trainer.

77. (043) What would result if a unit were reorganized under POMO?

a. Larger shops.
b. Centralized maintenance.
c. More than one AFSC in a shop.
d. Each individual works within his or her AFSC.

78. (044) Data entered on an AFTO Form 349, Maintenance Data Collection Record, is used by

a. supervisors.
b. the chief of maintenance.
c. the Air Force Logistics Command.
d. all of the above.

79. (045) Which listed form is used to control items flowing to and from maintenance shops?

a. AFTO Form 346.
b. AFTO Form 349.
c. AFTO Form 350.
d. AFTO For 444.

80. (045) When more than one person takes part in a maintenance action, what employee number code is entered in Column N of an AFTO Form 349?

a. The last technician to leave the job.
b. The technician completing the form.
c. The technician who opened the JCN.
d. The senior technician.

81. (046) Which of the following means ''not reparable this station''?

a. DIFM.
b. RACC.
c. RPC.
d. NRTS.

82. (046) When an unserviceable item is turned in to base supply in exchange for a serviceable item, this supply asset is designated

a. NRTS.
b. DIFM.
c. RACC.
d. RPCM.

83. (047) The maintenance management information and control system (MMICS) is used to

a. forward MDC data for batch processing.
b. replace the maintenance data collection system.
c. replace AF Form 623, On The Job Training Record.
d. update manual entries on the job proficiency guide (JPG).

84. (047) Which listed maintenance management information and control system (MMICS) subsystem, if any, allows editing of MDC data when it is entered?

a. Inspection and time changes.
b. C-E equipment status and inventory reporting.
c. Operational events.
d. None of the above.

85. (048) The action taken to determine equipment configuration and completeness is

a. an activity inspection.
b. a primary evaluation.
c. a special evaluation.
d. a technical inspection.

86. (049) What kind of deficiency results from the unpredictable failure of a transistor in computer or switching equipment?

a. Poor workmanship.
b. Materiel.
c. Maintenance.
d. Reliability.

87. (049) If a piece of electronic equipment requires excessive time to maintain and is not reliable, what kind of deficiency does this represent?

a. Design.
b. Material.
c. Maintenance.
d. Accessibility.

88. (050) The procedures to use when reporting equipment deficiencies are outlined in

a. AFR 66-1, Volume 5.
b. AFR 66-1, Volume 1.
c. TO 00-20-2-8.
d. TO 00-35D-54.

89. (050) The form to use when making a quality deficiency report on a Category II deficiency is

a. Standard Form 368.
b. AFTO Form 350.
c. DD Form 173.
d. AF Form 2411.

90. (051) Which condition tag is attached to a condemned item?

a. AFTO Form 350.
b. DD Form 1577-2 (Green tag).
c. DD Form 1577 (Red tag).
d. DD Form 1574 (Yellow tag).

91. (052) Items placed in a supply point are normally

a. expendable and peculiar to the activity.
b. expendable and low cost.
c. reparable and peculiar to the activity.
d. reparable and low cost.

92. (052) Which type items are placed in a bench stock?

a. Calibrated items.
b. Low consumption items.
c. Repaired items.
d. Expendable items.

93. (053) How is AF Form 2413, Supply Control Log, used?

a. By supply to list items ordered.
b. By a section to list parts on order.
c. Sent to supply to order parts.
d. Sent to section to confirm parts on order.

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94. (053) Concerning AF Form 2413, the document number for a part ordered from supply indicates the

a. equipment ordered for and activity code.
b. shop code and date ordered.
c. urgency justification code and serial number.
d. delivery destination code and quick reference list number.

95. (054) The force activity designator (FAD) on AF Form 2005, Issue/Turn-In Request, will

a. indicate the activity to receive the part.
b. indicate the organization that ordered the part.
c. be the same as used on AF Form 2413.
d. contain the demand code.

96. (054) If a part does *not* have a national stock number listed, submit

a. AF Form 2005 only.
b. DD Form 1348-6 only.
c. AF Form 2413 and AF Form 2005.
d. DD Form 1348-6 and AF Form 2005.

97. (055) When call-in demand processing is used to order parts from base supply, which form is used?

a. AF Form 2005, Issue/Turn-In Request.
b. AF Form 2413, Supply Request Log.
c. Neither AF Form 2005 nor AF Form 2413.
d. Both AF Form 2005 and AF Form 2413.

98. (056) What is ordered by using AF Form 601?

a. Parts.
b. Supplies.
c. Equipment.
d. Expendable items.

99. (056) Which form is used by the equipment management office (EMO) to notify sections of actions taken on equipment requests?

a. AF Form 2005, Issue-Turn-In Request.
b. DD Form 1348-6, Non-NSN Requisition.
c. AF Form 601, Equipment Action Requisition.
d. AF Form 2413, Supply Control Log.

END OF EXERCISE

MAIL TO: ECI, GUNTER AFS AL 36118-5643

STUDENT REQUEST FOR ASSISTANCE

PRIVACY ACT STATEMENT

AUTHORITY: 10 USC 8012. PRINCIPAL PURPOSE: To provide student assistance as requested by individual students. ROUTINE USES: This form is shipped with ECI course package. and used by the student, as needed, to place an inquiry with ECI. DISCLOSURE: Voluntary. The information requested on this form is needed for expeditious handling of the student's inquiry. Failure to provide all information would result in slower action or inability to provide assistance to the student.

I. CORRECTED OR LATEST ENROLLMENT DATA

1. THIS REQUEST CONCERNS COURSE (1-6)	2. TODAY'S DATE	3. ENROLLMENT DATE	4. AUTOVON NUMBER

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CDC 30554

ELECTRONIC COMPUTER AND SWITCHING SYSTEMS SPECIALIST

(AFSC 30554)

Volume 2

Electronic Principles and Digital Techniques

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Preface

A KNOWLEDGE OF numbering systems, discrete logic circuits, integrated circuits, and electronic computer and switching system components is required of all personnel holding AFSC 305X4. This volume of CDC 30554 reviews these basics and also presents state-of-the-art information on current technologies.

Chapter 1 reviews basic information about solid-state theory and the devices used to implement various logic circuits. You will be referred to Module 10008, *Semiconductors and Semiconductor Devices,* and supplement to it (which are included in your course package), for objectives 200–210. Chapter 2 gives a capsule history of digital electronics and explains the numbering systems used to symbolize and manipulate data in logic circuits. You will be referred to Module 10005, *Digital Techniques,* Unit 1 (which is included in your course package), for objectives 217 through 234. Chapter 3 details the building blocks used to create a logic circuit. Boolean algebra gives us a method of defining a logic circuit. You will be referred to Module 10005, *Digital Techniques,* Unit 2 (which is included in your course package), for objectives 235 through 258. Chapter 4 describes the basic timing generators needed to cause digital logic circuits to operate in the proper sequence. Also discussed here are the time-based methods of getting information transmitted within a computer or switching system. You will be referred to Module 10005, *Digital Techniques,* Unit 3 (which is included in your course package), for objectives 259 through 281. Chapters 5 and 6 explain the sequential and combinational logic circuits used to process data. You will be referred to Module 10005, *Digital Techniques,* Units 4 and 5 (which are included in your course package), for objectives 282 through 316. Chapter 7 covers the equipment used in a digital system to process, store, and display data. You will be referred to Module 10005, *Digital Techniques,* Unit 6 (which is included in your course package), for objectives 317 through 348.

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This volume is valued at 87 hours (29 points). These hours and points include those assigned to the modules that you will study in conjunction with this volume.

Material in this volume is technically accurate, adequate, and current as of April 1981.

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CHAPTER 1

NOTE: In this volume, the subject matter is developed by a series of student-centered objectives. Each of these carries a three-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see whether your answers match those in the back of this volume. If your response to an exercise is incorrect, review the objective and its text.

Solid-State Theory and Devices

THE OBJECTIVES in this chapter seek to satisfy part of the basic knowledge requirements for any electronic maintenance specialist. The basics mastered by these objectives are the building blocks upon which all circuits are based. An understanding of the transistor, the field-effect transistor (FET), and the integrated circuit is a necessity if we are to effectively analyze the problems that develop in electronic computer and switching systems.

At one time or another, you will be exposed to discrete circuits that will require the identification and replacement of individual components. You will be faced with the repair of equipment that only requires replacement of a module or printed circuit card containing numerous integrated circuits. The effective use of the information and technologies discussed in this and succeeding chapters will contribute significantly to your ability to be a successful maintenance specialist or technician.

NOTE: For objectives 200–210, study objectives 001–011 in Module 10008, *Semiconductors and Semiconductor Devices,* and the supplement to it which accompany this volume. When you complete Module 10008 and the supplement to it, return to the text.

Module 10008

Semiconductors and Semiconductor Devices

CDC 30554-2 Objectives	*Module 10008 Objectives*
200	001
201	002
202	003
203	004
204	005
205	006
206	007
207	008
208	009
209	010
210	011

1-1. Field-Effect Transistors (FETs)

FETs derive their names from the fact that current through the device is determined by an electric field within the FET. Therefore, the FET is a voltage-controlled device similar in operation to the triode-vacuum tube. The idea of a device using this field-effect principle was first worked on in 1925 by Julius Lilienfield. Although the FET is a very simple device, the technology to develop it was not available until after

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the invention of the transistor in 1948. The FET is a unipolar device in that it has only one type of semiconductor material in which current flows, whereas the transistor, a bipolar device, has two. There are two types of FETs being used at present; they are the junction FET (JFET) and the insulated gate FET (IGFET). The IGFET is more commonly referred to as a metal-oxide semiconductor FET, or MOSFET.

211. Specify the operational characteristics of a junction field-effect transistor.

Junction Field-Effect Transistor (JFET). The basic construction of the JFET appears in figure 1-1. The body of the FET is represented by a block of N-type material. This body or channel can be either an N or a P channel. To each end of this semiconductor block ohmic connections are made. The two connections are metal plates that serve to bring external voltages into contact with the semiconductor. Instead of emitter and collector, these ohmic contacts are named "source" and "drain" respectively. P-N junctions are formed on either side of the channel to provide a "gate" connection for the FET. The gate of the FET is analogous to the base of a transistor. In most cases, the P region in our example goes completely around the body.

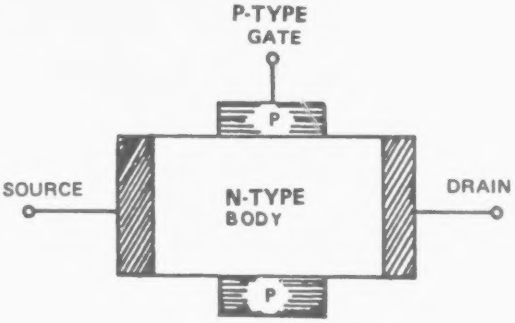

Figure 1-1. Field-effect transistor.

In the FET, the bias on P-N junctions is still used to control current, but current never flows across the P-N junctions. Figure 1-2 illustrates two symbols for the FET. An N-type FET is shown in figure 1-2,A. For an FET consisting of a P-type block with an N-type gate, the arrow on the symbol is reversed, as shown in figure 1-2,B. The reasons for choice of the terms "source," "gate," and "drain" should become apparent in the insuing discussion.

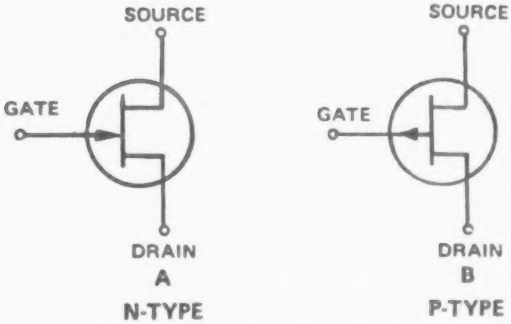

Figure 1-2. FET schematic symbol.

With reference to figure 1-3, we will consider the DC voltages applied to the FET. Battery V_D (Drain voltage) is the source-to-drain voltage supply and causes electron current to flow through the N-type material from the source to the drain. This voltage is dropped across the internal resistance of the N-type block, setting up a potential gradient from left to right. Battery V_Q is the gate bias voltage and is applied to both P-type gates. It is easily seen that the gates are at some negative potential with respect to the source. The potential at any point in the block is positive with respect to the source. The potential at any point in the block is positive with respect to the gate. This consititutes a reverse-bias condition. Progressing across the block from source to drain, the voltage becomes increasingly positive. As a result, the potential difference between the gate and block is less at the end of the block near the source than it is at the drain end. Hence, the shape of the depeletion regions is as shown in the figure. Since the two depletion areas are devoid of current carriers, the electrons flowing through the block are directed, or *channeled,* into the area between the depletion regions. This is referred to as the conduction channel.

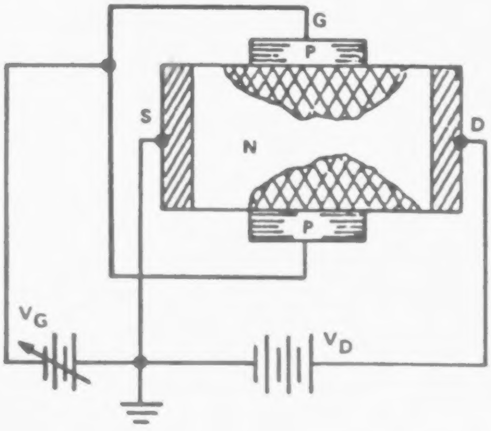

Figure 1-3. FET biasing.

Assuming a zero-volt gate potential (V_G) as the drain voltage is increased, drain current increases up to a point. At this point a further increase in drain voltage does not produce an appreciable increase in drain current. The potential at which this occurs is referred to as the pinch-off voltage. The reason for this behavior is that increasing the drain voltage increases the strength of the source-to-drain field, drawing more current through the block until a point of maximum current is reached. At the same time, the gradient potential opposite the gate becomes increasingly positive, increasing the reverse bias and widening the depletion regions. Maximum drain current flows with the gates at the same potential as the source. If, however, the gates are made negative with respect to the source by increasing the potential of battery V_G, the size of the depletion regions is increased. The result is that the FET now reaches a constant value of drain current at a much lower value of drain voltage. As gate voltage is increased further, lower values of drain voltage become necessary to reach a constant drain current. Finally, if the gate potential equals the value of pinch-off voltage described earlier, current through the device is at a minimum, negligible for most purposes. The depletion regions are enlarged to such an extent that they effectively close, or "pinch off," the conduction channel. Careful thought reveals that the gate voltage is analogous to the emitter-base voltage on a transistor in that it controls the amount of current flowing between the two end elements. Since a small change in gate voltage causes a rather large change in drain current, the device is capable of amplification.

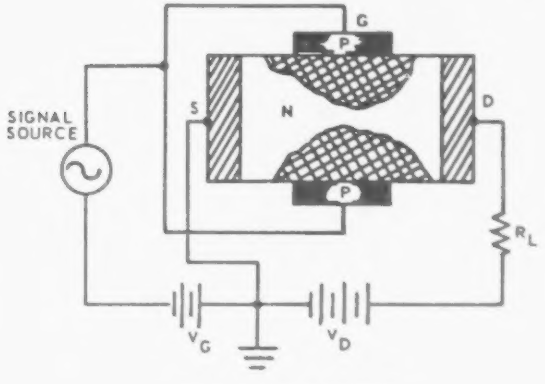

Figure 1-4. FET amplifier.

Consider now the insertion of a signal in series with V_G as in figure 1-4. Obviously, the effect of the signal is to vary the gate potential. The positive half-cycle opposes the biasing potential of V_G, making the gates less negative. This decreases the size of the depletion areas and allows more current to flow to the drain. The increased current flowing through R_L causes the voltage across R_L to increase greatly, producing an amplified output signal. The negative half-cycle has the opposite effect, allowing less drain current to flow. Thus, the input signal controls, or modulates, the output current. Because the input signal is applied to a reverse-biased junction, the input impedance of the FET is very high, at least a megohm. For the same reason, the only gate current that flows is minority carrier current, which is very small. The current and power gains are determined by that ratio of change in gate current to a change in drain current and, hence, are very high. Notice that in this device the only concern is with one type of current carrier (electrons in this example). In this respect, the FET is similar to a triode-vacuum tube.

Examination of the high-frequency characteristics reveals several advantages of the FET over conventional transistors. Recall that transit time is the time it takes carriers to travel across the base from emitter to collector. By our definition, there is no transit time in the FET. The input signal is merely used to narrow or widen the conduction channel, not to vary the rate of travel of the current carriers. For this reason, we need not concern ourselves with transit time from source to drain. Since this device has no base, two of our determinants (base width and base resistance) are eliminated. There are certain shunting capacitances in the FET which limit frequency of operation. These, however, are not quite as significant as they are in conventional junction transistors.

FETs are used as amplifiers and switches in both the discrete and integrated circuit forms. Understanding basic JFET operation is necessary to understand MOSFET operation in the next section. The MOSFET is the workhorse of semiconductor memories which will be covered later in this volume.

Exercises (211):

1. When does maximum drain current flow?

2. How does increasing the gate voltage affect the amount of drain voltage required to reach a constant drain current?

3. The potential at which drain current cannot be increased is known as the ______ ______ ______ .

4. Name the three elements of an FET.

5. In text figure 1-3, why is the electron flow directed between the depletion regions?

6. Why is the FET gate voltage analogous to the emitter-base voltage on a transistor?

7. In what respect is an FET similar to a triode vacuum tube?

8. Why do we consider the FET to have no transit time?

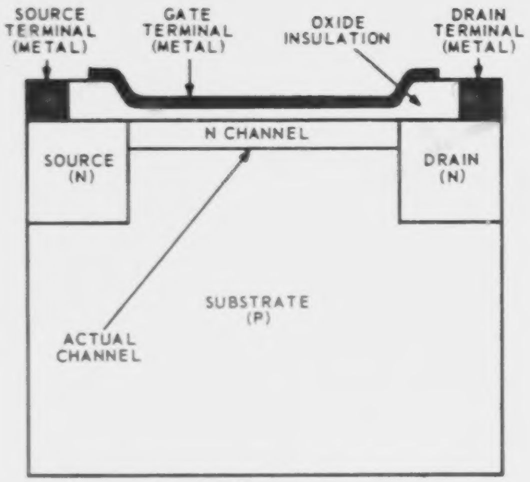

Figure 1-5. MOSFET physical construction, depletion type.

212. Identify types and specify the characteristics of metal oxide semiconductor FETs (MOSFETs).

MOSFETs. The insulated-gate FET (IGFET), or metal oxide semiconductor FET (MOSFET), is so named due to the presence of a silicon dioxide insulating layer between the metal contacts and the semiconductor body. An important characteristic that results from this combination is that a capacitor is formed by the metal, silicon dioxide, and P or N material. A capacitor can charge to a voltage level and will, therefore, hold information. This fact will be used later to explain the operation of MOSFET semiconductor memories.

MOSFETs are divided into two primary categories: the P or N channel, depletion and enhancement mode devices. Each will be explained as to their schematic representations, biasing requirements, and particular characteristics.

Depletion-type MOSFETs. Figure 1-5 shows a depletion-type MOSFET. The example chosen for the illustration is an N-channel device. We could just as easily have used a P-channel device by reversing the N and P materials. Ohmic contacts are made to a section of N-type material to form source and drain connections. An insulator consisting of an oxide layer is placed between the source and drain. The gate connection is then made to the oxide layer. This is why MOSFETs are referred to as *insulated gate* FETs. Notice that the gate or oxide layer extends across the top of the N-type material. Current normally flows from the source to the drain through a "channel" immediately below the gate. The amount of current depends on the number of carriers (electrons) in the channel, the voltage between source and drain, and gate bias. If the N-type channel has many carriers (highly doped), a relatively small drain-source voltage will cause a large current.

A negative voltage on the gate with respect to the source will create an electrostatic field which will reduce drain current. This action is similar to the effect of grid bias on the conduction of a triode vacuum tube. The N-channel depletion MOSFET will have a positive drain voltage with respect to the source. The use of a positive gate voltage will enhance the flow of drain current. If a gate bias is not used, drain to source voltage will determine drain current.

The depletion mode MOSFET is a normally on device and, therefore, consumes power at all times unless gate bias is negative enough to stop channel conduction. The device is normally operated with reverse or negative bias for linear operation.

Enhancement-type MOSFETs. The distinguishing characteristic of this device is that a channel doesn't exist until you apply a positive gate voltage to *enhance* a channel to form. This gate voltage must be at a specific threshold level before a channel will start to form. Increasing the positive bias above threshold will increase the channel current. Refer to figure 1-6 for a diagram of the N-channel enhancement MOSFET.

The enhancement MOSFET is a normally off device and, therefore, consumes very little, if any, power until it is turned on. The input signal will alternately add to and subtract from the gate voltage and cause current to vary accordingly. Using digital pulses as the input with no gate bias, the device turns on only when a pulse is present. With that fact in mind, and remembering that the gate is one plate of a capacitor internal to the FET, a one or a zero could be stored.

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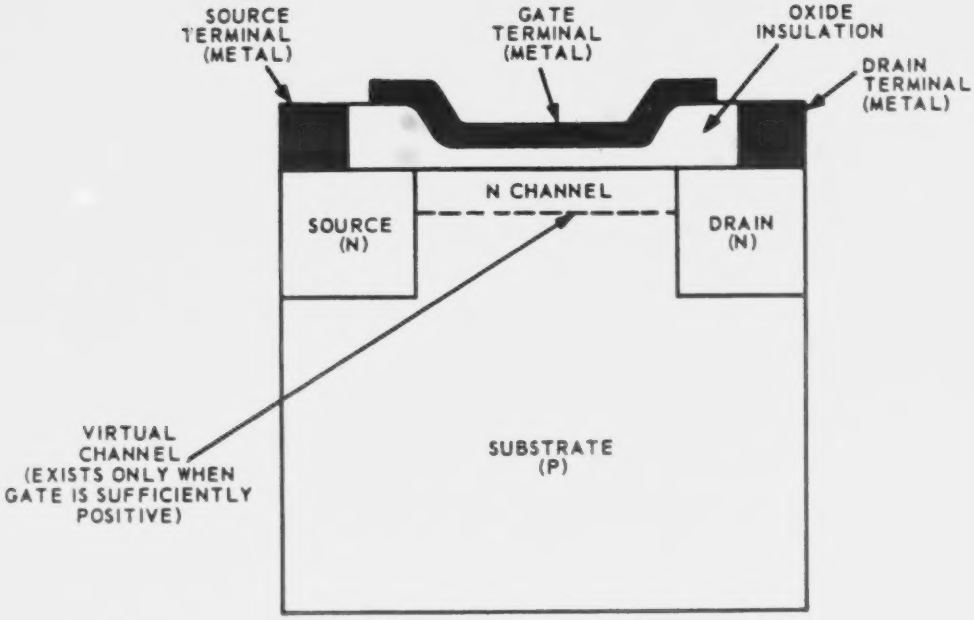
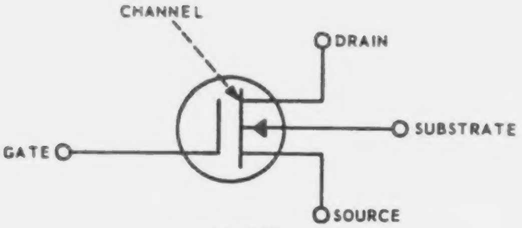

SOURCE TERMINAL (METAL)
GATE TERMINAL (METAL)
OXIDE INSULATION
DRAIN TERMINAL (METAL)
N CHANNEL
SOURCE (N)
DRAIN (N)
VIRTUAL CHANNEL (EXISTS ONLY WHEN GATE IS SUFFICIENTLY POSITIVE)
SUBSTRATE (P)

Figure 1-6. MOSFET physical construction, enhancement type.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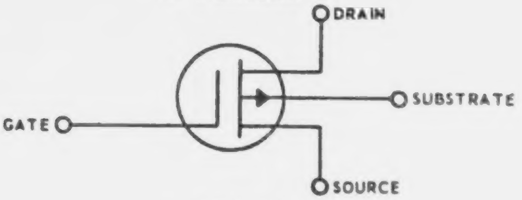
A. N CHANNEL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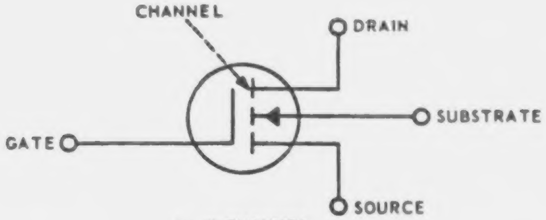
B. P CHANNEL

Figure 1-7. MOSFET schematic symbol, depletion type.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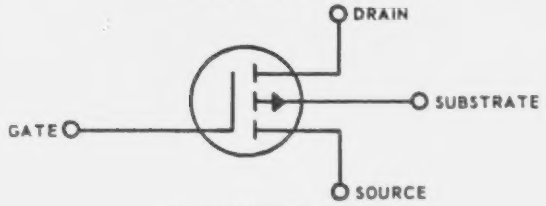
A. N CHANNEL


DRAIN
SUBSTRATE
GATE
SOURCE

B. P CHANNEL

Figure 1-8. MOSFET schematic symbol, enhancement type.

The schematic symbols of MOSFETs are shown in figures 1-7 and 1-8. The arrow pointing out represents a P-channel (the hole is majority carrier). A solid line between the source and drain represents a depletion type, and a broken line between the source and drain represents the enhancement type. In neither case does the gate touch the source-drain line; the space between the gate and channel indicates that the device is an insulated gate or MOSFET.

Diode-Protected MOSFETs. Because of the very thin insulating layer of silicon dioxide and the high-input impedance of the FET, static charges developed on the input leads are sufficient to puncture the oxide layer. Laboratory experiments indicate that the human body acts as a static source with a capacitance ranging from 100 to 200 picofards and a resistance typically greater than 1,000 ohms. Further measurements suggest that the potential stored by the human body is usually less than 1,000 volts but can be much higher. Experience has also indicated that the likelihood of damage to an MOS transistor as a result of static discharge is greater during handling than during operation. To guard against static discharge damage, two systems of protection have found general usage. First, the device may come from the factory with a shorting strap on the leads, or it will be inserted into a piece of conductive foam. If it has the strap, do not remove it until the device is soldered in place. When removing it from the conductive foam, do not let your fingers touch the leads until the MOSFET is inserted into the circuit. A second method of protection is that protective diodes will be used inside the device.

The equivalent schematic symbol is shown in figure 1-9. The diodes do not conduct unless the gate to source voltage exceeds ±10 volts typically. The transistor, therefore, can handle a very wide dynamic signal swing without significant conductive shunting effects by the diodes. If either diode conducts to short out any static discharge, the diode could be destroyed. MOSFETs must be handled with care, and special soldering techniques must be used.

Exercises (212):

1. What are the two basic types of MOSFETs?

2. Using a depletion MOSFET with no voltage on the gate will result in a (current/voltage) from source to drain.

3. What distinguishes the MOSFET from the JFET?

4. Which type of MOSFET is the normally off device?

5. What is the significance of the gate capacitance?

6. How do static discharges harm the MOSFET?

7. In diode-protected MOSFETS, what do the diodes protect against?

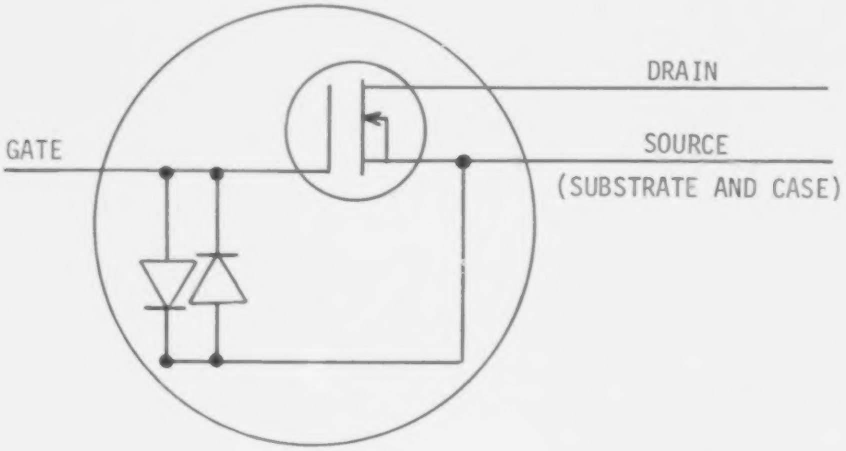


Figure 1-9. Diode protected MOSFET.

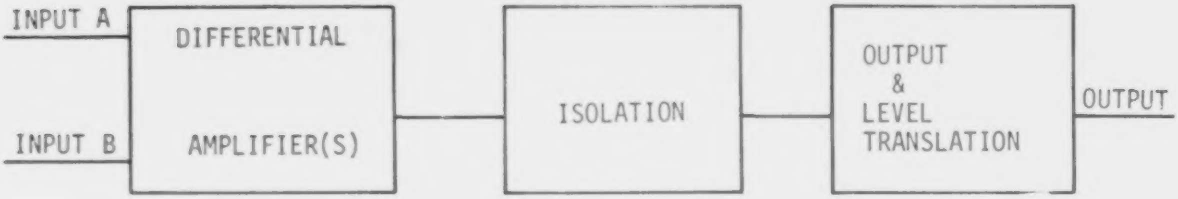


Figure 1-10. Block diagram of an OP AMP.

1-2. Operational Amplifiers

One of the more important circuit techniques available to analog and digital electronics is the operational amplifier. It was originally designed in 1938 by G. A. Philbrick for use as an electronic integrator and differentiator circuit. It later got its present name because it was used in analog computers for performing mathematical operations, hence the name "operational amplifier," or "OP AMP." It is used today throughout the analog world, and is predominant in the digital area for use as an interface circuit technique. OP AMPs are used for the four common math functions and as the primary element in digital-to-analog conversions and vice-versa.

213. Define the term "operational amplifier," categorize the modes of operation, and specify the characteristics of each mode.

The "operational amplifier" is a direct-coupled high-gain amplifier which uses feedback to control its performance characteristics. Figure 1-10 is a block diagram of the stages that an OP AMP usually consists of. The first two or three stages are differential amplifiers to provide amplification and elimination of noise. Next is an isolation stage, such as the common collector circuit discussed in a later chapter. The last stage is for output of the signal and level translation. Level translation is similar to what's done by line drivers and receivers in computer interface circuits, namely, changing logic levels.

Single-Ended Input Operation. The schematic diagram of an operational amplifier is shown in figure 1-11. The lead coming off the point of the triangle is the output lead. The other two leads are the inputs. The + input lead is called the *noninverting* lead and the — lead is the *inverting* input. The + and — signs do not indicate polarity; instead, they indicate whether or not signal inversion takes place between the input and output.

One characteristic of the OP AMP is the *open loop* voltage gain. This term identifies the voltage gain of the operational amplifier without any feedback connected. As an example, a type 709, high-performance operational amplifier has an open-loop gain of 70,000. This means that when a signal is applied to one of the input leads and the output signal is observed, the output will be 70,000 times larger than the input signal. This is only possible, however, if the power supply is capable of supporting that large a signal. For example, if the input signal were 0.1 volt and the power supply voltage were 20 volts, the limit of the output voltage swing would be something less than ±20 volts, not the 7,000 volts the open-loop gain figure would indicate!

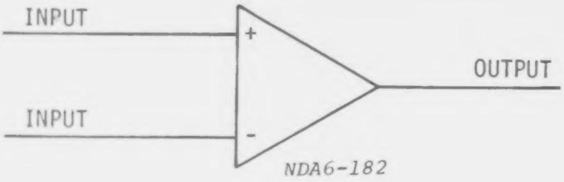


Figure 1-11. OP AMP schematic symbol.

Differential or Common Mode Operation. Using this mode of operation, the OP AMP amplifies the difference between the two input signals. When the two signals are equal in amplitude and in phase, there will be no difference and the output of the operational amplifier will be zero. When the two input signals are equal in amplitude but out of phase, the difference between the two signals is determined by their phase relationship. When they are 180° out of phase, their difference will be maximum. Further, if one signal is 10 millivolts, the other signal is 15 millivolts, and they are in phase, the difference between the two is 5 millivolts. This is what the operational amplifier will amplify.

Other OP AMP Characteristics. Ideally, the input resistance should be infinitely large (an open), and the output resistance should be infinitely small (a short). In actual operational amplifiers this is not possible. However, the input resistance is very high and the output resistance is very low in most commercial OP AMPS. For example, the type 709 has an input resistance of 700 kilohms and an output resistance of 150 ohms. A type 777 has an input resistance of 10 megohms and an output resistance of 100 ohms. These are typical values for most OP AMPS.

One of the limitations of operational amplifiers is their instability over a wide range of input frequencies. Because of their high-voltage gain characteristics, and because of phase shifting problems at the higher frequencies, some operational amplifiers break into oscillations at various times, primarily when they are used in the open-loop configuration. To obtain a high degree of stability, and to provide certain other desirable features, most operational amplifiers are connected in a *closed-loop* configuration. A closed-loop configuration refers to the fact that degeneration is present in the circuit (feeding a portion of the output signal back to the input so that it opposes the input signal).

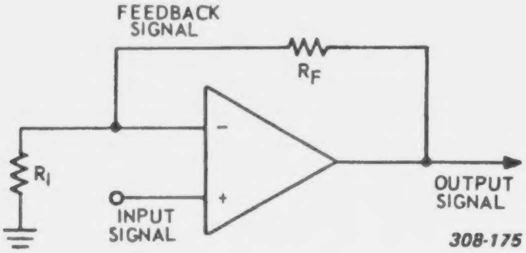


Figure 1-12. Noninverting mode of operation.

Noninverting Mode. The normal noninverting mode of operation is shown in figure 1-12. The input signal to the circuit is applied to the noninverting lead. A portion of the output signal is applied through R_F (feedback resistor) and developed across R_I (input resistor) and is applied to the inverting input lead. The feedback signal has the same frequency and same phase as the original input signal on the noninverting lead. In fact, the only difference between the two signals is their amplitude, and that is controlled by the feedback network, R_F and R_I. Since this is degenerative feedback, the voltage gain of the circuit will be less than the open-loop gain of the operational amplifier, but the circuit will now be very stable. Further, the gain of the circuit is not entirely dependent upon the gain of the operational amplifier. To illustrate this condition, an example problem will be worked.

First, consider an operational amplifier that has an open-loop voltage gain of 250,000. This operational amplifier is placed in a circuit with no feedback. The output of the circuit will be 250,000 times larger than the input signal as long as the operational amplifier is performing properly. However, if something happens to the operational amplifier that reduces its voltage gain to, say, 125,000 (due to aging, component values changing, etc.), the gain of the circuit will also decrease to that value. A circuit like this (open loop) is entirely dependent upon the active device (operational amplifier) for the circuit gain. In this problem the circuit gain decreased 50 percent.

Second, consider the same operational amplifier (open-loop voltage gain of 250,000) connected in the noninverting mode of operation (as shown in fig. 1-12) with 0.0004 percent of degenerative feedback (the percent of degenerative feedback is controlled by the size of R_F and R_I). This circuit is not entirely dependent on the operational amplifier for the circuit voltage gain. Some of the circuit gain is determined by the degenerative feedback. This produces the following situation:

- A circuit that still has a large voltage gain.
- A very stable amplifier circuit.
- A circuit that is not entirely dependent on the active device for the voltage gain of the circuit.

As more and more degenerative feedback is used, the stability of the circuit increases and the voltage gain becomes more dependent on the feedback network.

Inverting Mode. Another configuration that an operational amplifier can be connected in is the *inverting* mode of operation, shown in figure 1-13. Notice once again that degenerative feedback is present. The amount of degeneration will be controlled by the size of R_F and R_I. Also notice that the input signal is applied through R_I to the inverting input lead. The voltage gain of this circuit, inverting mode of operation, can be determined by using the formula $A_V = R_F/R_I$. Suppose R_F is 100 kilohms and R_I is 1 kilohm. The voltage gain in this example is 100. This means that the input signal will be amplified by a factor of 100 and the output signal will be inverted by 180° from the input signal. As another example, when R_F is 500 kilohms and R_I is 500 ohms, the voltage gain of the circuit is 1,000.

Voltage Follower. Another possible configuration for the operational amplifier is in a circuit that provides a voltage gain of one and that does not shift the phase of the signal. This connection is called *voltage follower* (shown in fig. 1-14). In this circuit the input signal is applied to the noninverting input lead and the degenerative feedback is present on the inverting lead. This provides a voltage gain of one and no inversion of the signal. Circuits like this are used where a high-input resistance is required, a low-output resistance is required, and no phase shift is wanted. This can be used as a line driver, or in any place where a common-collector configuration would normally be used.

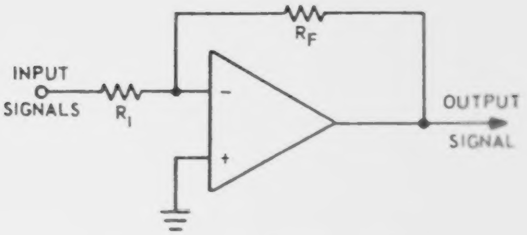

INPUT
SIGNALS
R_1
R_F
OUTPUT
SIGNAL

Figure 1-13. Inverting mode of operation.

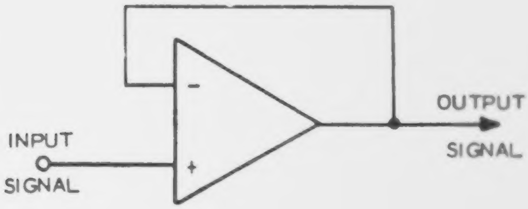

INPUT
SIGNAL
OUTPUT
SIGNAL

Figure 1-14. Voltage follower: noninverting, gain of one.

Another circuit which is very similar is shown in figure 1-15. This is the basic inverting mode of operation, but R_F is now equal to R_1. In this arrangement, the voltage gain is one (using the previous formula for the inverting mode of operation) and the output signal is inverted. This circuit also provides a high-input resistance and a low-output resistance.

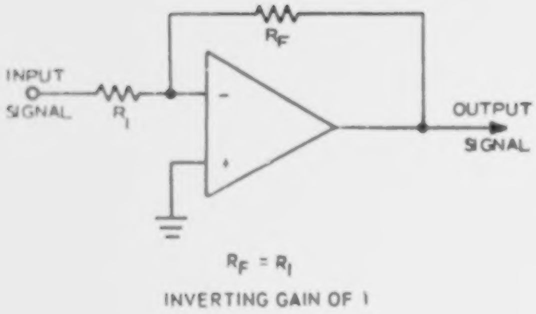

INPUT
SIGNAL
R_1
R_F
OUTPUT
SIGNAL
$R_F = R_1$
INVERTING GAIN OF 1

Figure 1-15. Inverting mode of operation, gain of one.

Differential Mode Example. When an operational amplifier is connected to receive two input signals at the same time, it is said to be in a differential or common mode configuration. A typical circuit is shown in figure 1-16.

For this example, the voltage gain is assumed to be the same for both input signals. R^1 is 1 kilohm, R^2 is 1 megohm, R^3 is 1 kilohm, and R^4 is 1 megohm. From input 1 to the output, the gain will be equal to the ratio of R^2/R^1, or 1,000. From input 2 to the output, the gain will be equal to the attenuation of the input resistors:

$$\frac{R^4}{R^3 \pm R^4} = \text{approximately } 0.999$$

multiplied by the gain of the noninverting mode of operation.

$$\frac{F^1 \pm R^2}{R-} = 1001$$

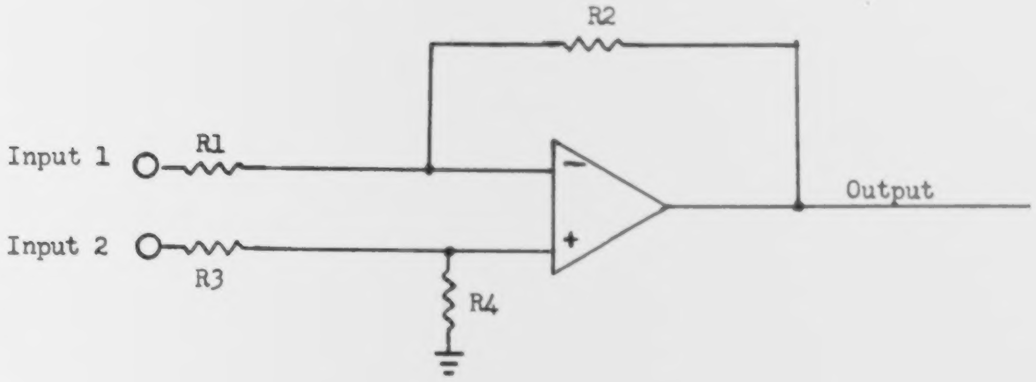

R2
Input 1
R1
Input 2
R3
R4
Output

Figure 1-16. Common mode input (differential input).

which equals a voltage gain of 1,000. So the voltage gain for each input signal is the same. Of course, the input signal number 1 is inverted and signal 2 is not.

When input signals 1 and 2 are equal in amplitude and in phase with each other, the output is zero (the difference between the two input signals times the voltage gain).

When input 1 is 2 millivolts peak to peak and input 2 is 1.5 millivolts peak to peak, and the two inputs are in phase, the output will be the difference between the two input signals (0.5 millivolts peak to peak) times the gain (1,000), which produces an output voltage of 500 millivolts peak to peak.

In summary, the output of an operational amplifier that is connected for common-mode operation is equal to the difference between the two input signals multiplied by the gain of the circuit. When the two signals are equal in amplitude and in phase, the output is zero. The output amplitude increases as the two input signals shift out of phase, and is maximum when the two signals are 180° out of phase.

Exercises (213):

1. What is an operational amplifier?

2. Name the three basic stages of an OP AMP.

3. The input lead of an operational amplifier that provides inversion is marked with what symbol?

4. If an OP AMP has two signals at the input but no output, what mode of operation is being used?

5. What is the primary purpose of the closed loop configuration?

1-3. Integrated Circuits

The first silicon transistor was made in 1954. Subsequent developments permitted the production of a number of transistors on a single wafer or chip of semiconductor material. Each transistor was cut from the wafer and then packaged. The idea of leaving a chip intact, and connecting the transistors together to perform a function, was first conceived and accomplished in 1959. The integrated circuit had become a reality.

Integrated circuits (ICs) permitted the increased complexity of circuits without the high cost associated with interconnecting discrete components. The IC has been primarily responsible for the tremendous growth in all areas of electronics, especially in the digital world. The military has been a prime mover in these developments due to aircraft, missile, and space electronics requirements.

214. Specify types and distinguishing characteristics of integrated circuits.

An integrated circuit is a piece of semiconductor material on which transistors, resistors, and capacitors are etched to form an electronic circuit. An IC is also termed "monolithic" because of its one piece construction. A transistor or FET is often used in ICs to take the place of a resistor because of their variable resistance characteristic. Diodes in an IC can serve as small value capacitors when reverse biased, operating as varactors. Large value capacitors and inductors must be added externally to ICs if they are required for proper operation. ICs can be made to simulate inductors or capacitors electrically. Integrated circuits are classified as either digital or linear (analog).

Linear Integrated Circuits (LICs). LICs are used for analog circuits such as oscillators, amplifier, comparators, filters, and voltage regulators. The operational amplifier is probably the most predominant of the general-purpose linear integrated circuits. OP AMPs are used to a great extent in analog-to-digital and digital-to-analog conversion circuits. Special-purpose LICs are used in circuits such as AM detectors and FM stereo decoders in radios or as a video detector/amplifier IC in a television set. System interface ICs are frequently analog chips that are used as line drivers/receivers or peripheral drivers. The linear IC of both the special- and general-purpose types is used in a great many peripheral devices for processing digital data that has been converted into analog form.

Digital Integrated Circuits (DICs). This type of IC is usually the simplest as far as construction and operational requirements are concerned. The DIC is only required to handle two voltage or current levels. Circuit requirements are normally just input, output, and power supply connections. The types of logic used within the digital IC consists of several different families. These logic families are the transistor-transistor logic (TTL), emitter-coupled logic (ECL), diode-transistor logic (DTL), and others that will be discussed later in this section. Normally, several logic gates or circuits are usually built on each IC. DICs are normally low-power devices consuming about 10–15 milliwatts per gate using TTL logic. We will look at digital integrated circuits and logic in much greater detail later in this course.

Exercises (214):

1. What is the distinguishing characteristic between the functions accomplished by digital and linear integrated circuits?

2. Which is probably the most used of all the LICs?

3. Capacitors can be formed in an IC by using the characteristics of what semiconductor device?

215. Define IC terms and specify the characteristics of each logic family.

IC Terms and Definitions. The following terms are used when talking about integrated circuits. The definitions will enable you to better understand the operation and use of digital integrated circuits.

Chip. A piece of semiconductor material on which electronic components have been formed (usually transistors and resistors), to produce an integrated circuit. May also be called a die or substrate.

DIP (dual-in-line package). An integrated circuit package type, made of plastic or ceramic, with two rows of leads along either side. It is rectangular in shape and usually has from 8 to 40 leads. The leads extend vertically from each side and permit easy insertion of the DIP into printed circuit boards.

Fall time. A measure of the time required for the voltage at the trailing edge of a pulse to drop from 90 percent to 10 percent of the original amplitude. Also called *decay time.*

Fan-in. The number of logical inputs to a circuit.

Fan-out. The number of logical outputs from a circuit or the number of gates that a given output gate can drive.

Flat-pack. Another type of integrated circuit package that is thinner than the DIP, with the leads extending horizontally from the sides. Like the DIP, it is made of plastic or ceramic.

IGFET. Insulated-gate field-effect transistor. See the definition of MOSFET.

LSI (large-scale integration). A digital IC with between 100 and 1,000 logic gates with in the package.

Monolithic. A microcircuit in which transistors, diodes, resistors, and capacitors are formed on and within a single-crystal semiconductor substrate.

MOSFET (metal-oxide silicon field-effect transistor). A high-impedance input device which can be used as an amplifier or switch. Charge carriers within the transistor are of only one type, N or P; therefore, the MOSFET is a unipolar device. The MOSFET is classified as an enhancement type (normally off) or the depletion type (normally on).

MSI (medium-scale integration). A digital integrated circuit that has from 12 to 100 gates within.

SSI (small-scale integration). A digital integrated circuit that has 10-12 gates or less.

Pull-down resistor. A resistor tied to logic 0 or ground and the input of a gate to keep that input at a logic low.

Pull-up resistor. A resistor connected to a logic 1 level and tied to the input of a gate to keep the input at the logic 1 level.

Rise time. The time required for a pulse to rise from a specific lower limit to a specific upper value, usually from 10 to 90 percent of its final value.

VLSI. Very large-scale integration. VLSI means that a digital integrated circuit will have more than 1,000 gates on a chip. These chips are responsible for the "computer on a chip," the microprocessor.

Logic Families. A variety of digital logic circuits are available, dependent on the circuit to be used for them and its electrical requirements. Integrated circuits may use bipolar transistor, MOSFET or CMOS technology to implement a logic circuit. Each will have its own advantages and disadvantages and special characteristics. A brief exlanation of several logic families follows along with a table of characteristics for three of the more prominent logic types.

Current mode logic (CML). CML is also referred to as current steering logic. The circuit uses a transistor for each input and an additional transistor for biasing. Both the OR and NOR outputs are available from the circuit. Because the transistors in this logic don't saturate during switching transistions, the speed of this logic is greater than some others.

Complementary MOS logic (CMOS). This type of logic is built on a chip using the MOSFET as its primary active device. An N-channel MOSFET will be complemented by a P-channel device, and both are of the enhancement or normally off type. If either device is turned on, the other will be off, and the only time current will be drawn from the power supply will be during the transition period when the N-channel is turning off or the P-channel is turning on. This will also be true during the reverse situation. Therefore, CMOS logic requires very little power during operation.

Direct-coupled transistor logic (DCTL). DCTL was one of the first types of logic to be put in IC form. Each emitter and collector of the transistors in a gate are tied together. Input signals are connected to the bases of the individual transistors that are part of the gate circuit. Because of the inherent differences between each transistor, if one has lower voltage requirements for bias than the others, it will tend to hog the current available. To remedy this, resistors are put in the base lead of each transistor to lessen the effects of the base-emitter voltage.

Diode-transistor logic (DTL). The input of DTL will consist of diodes for each input to a gate. The output of the diode gate is fed through another diode and then to the base of an inverter transistor gate. A capacitor may be used across the series diode to speed up the gate.

Emitter-coupled logic (ECL). ECL is the fastest available logic family, capable of over 500 megahertz. Logic in the ECL IC is similar to th at in CML. Complimentary outputs are availble from the ECL gate.

High threshold logic (HTL). The HTL circuit is similar to the DTL except that a zener diode replaces the coupling diode.

Integrated injection logic (I^2L). The I^2L logic is another IC development that came about after modifying the DCTL device. Modification involved the elimination of resistors and the use of multiple collector transistors. The unit may have both AND and NAND outputs, or OR and NOR outputs.

Resistor-transistor logic (RTL). This type of logic is equal to the DCTL after base resistors are installed. This prevents the current hogging effects of DCTL but slows the speed of the device.

Transistor-transistor logic (TTL). TTL or T^2L is the most common and popular logic used today. A multiemitter transistor is normally used as the input to this type of gate, the output of which is directly coupled to a pull-up transistor which provides the drive to switch the output on and off. TTL logic is available in standard, low-power, high-speed, and the nonsaturating or Schottky versons.

The following table indicates some typical characteristics of three of the most used types of logic. The propagation delay indicates the time for a digital pulse to get through a gate. Power is in milliwatts.

	Supply Voltage	*Speed (MHz)*	*Propagation Delay (ns)*	*Power Dissipated Per Gate (mW)*	*Fan Out*
CMOS	3-18	5	70	1	50
ECL	—5.2	30-500	2	40	25
TTL	5.0	35	3-12	20	10

Exercises (215):

1. Match each term in column B with the statement in column A that is most appropriate. Column B items will be used only once.

	Column A		*Column B*
____	(1) Also called die or substrate.	a.	LSI.
____	(2) A digital IC with 100 to 1,000 logic gates.	b.	Flat pack.
____	(3) Leads extend horizontally from the sides.	c.	DIP.
____	(4) The number of logical inputs to a circuit.	d.	Chip.
____	(5) A digital IC that has fewer than 12 gates.	e.	MSI.
____	(6) Fastest logic family.	f.	Fan-out.
____	(7) Current steering logic.	g.	SSI.
____	(8) One of the first logics put in IC form.	h.	Fan-in.
		i.	ECL.
		j.	CML.
		k.	DCTL.

2. In which category would an IC device containing 150 gates be listed?

3. What is the most common logic family in use?

4. What is the fastest logic family available?

5. What logic family uses the multiemitter transistor as an input?

6. MOSFET devices are used to implement what logic family?

7. What type logic could handle a fan out of 40?

8. Which logic family is available in high-speed and low-power versions?

216. List the three types of IC packages and specify advantages of ICs over normal solid-state devices.

Benefits of the IC and Its Packaging. There is no question of the influence circuitry has had on electrons today — in missiles, computers, television, radio, portable calculators, automobiles, and many more. Of course, where size and weight are important, as they are in missiles, satellites, or computers, integrated circuits are highly desirable. To these factors add the inherent characteristics of high reliability and lower cost; it is easy to understand why ICs have been so widely accepted.

In transistorized circuitry, the trend has been to replace tube functions with a transistor that would do the job. This resulted in overall reduction in the size of various circuits, but in most cases the passive elements (resistors, capacitors, etc.) were retained pretty much intact. In the case of the monolithic integrated circuit, though, it not only replaces both multiple active elements within a circuit (transistors and tubes). However, the monolithic integrated circuit includes most all of the passive elements within one envelope, which is a totally encapsulated silicon wafer of approximately 1/10 inch square or less. The resultant weight and space-saving qualities of the IC are spectacular in comparison to discrete techniques. Factors such as these resulted in a tremendous savings in the space program. After all, each pound saved in payload will reduce the costs of getting the vehicle in orbit. Additionally, more space is available for the primary functions of experimentation, data gathering, and a host of other requirements.

Currently, there are three major types of integrated circuit package styles. These are shown in figure 1-17. The dual-in-line package or DIP shown in figure 1-17,A, is the predominant package used for digital ICs. The majority of linear chips made in the past few years are of this type also. It is available in plastic or ceramic. Plastic is the cheaper of the two, but ceramic may be required due to the temperature requirements of some equipment. The ceramic package is usually rated for much greater temperature extremes. The standup characteristics of the DIP make it easier to use in printed circuit boards. It may use a socket or be soldered to the board, although the use of a socket makes the end item more expensive. For the maintenance specialist, repair and replacement of a chip is much easier if an IC is plugged in. The DIP is available is packages of 8 to 40 pins, depending on the complexity of the IC. Standard digital ICs are usually in packages of 14 or 16 pins.

The TO-5 IC package is shown in figure 1-17,B, and is a multilead unit similar to that used for some transistors. Early RTL and DTL logic ICs were packaged this way, and today some MOSFET storage registers use this style of package.

The flat pack IC, shown in figure 1-17,C, is not used as much today, although its reliability is very good. The leads are sealed glass to metal protrusions, and the unit is hermetically sealed. Flat packs are usually soldered into the circuit, and special soldering techniques must be used for their installation and removal.

Lead identification methods for the three IC packages mentioned are shown in figure 1-18. Standardization of IC packages by manufacturers has been, for the most part, successful.

Exercises (216):

1. What are the three types of IC packages available? Which type is most used?

2. From the list of statements given below, identify those statements which are true and which are false when comparing the value of integrated circuits to those of discrete devices.

____ a. They require a less space, which saves in equipment size.

____ b. They are made of totally different materials.

____ c. They are capable of only one circuit function.

____ d. They contain both active and passive circuit elements.

____ e. They are difficult to replace during maintenance.

____ f. They operate on lower supply voltages.

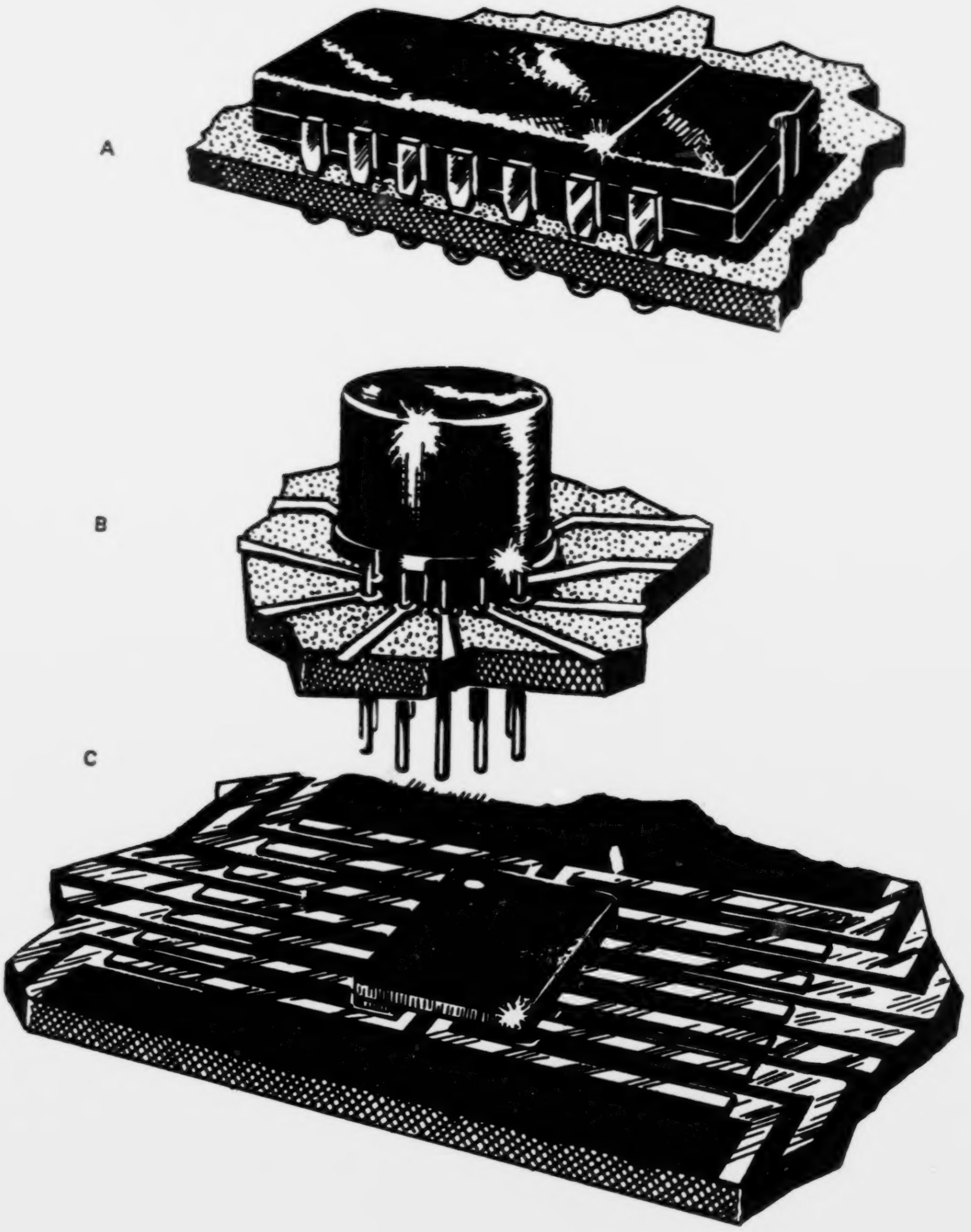


Figure 1-17. Integrated circuit packaging.

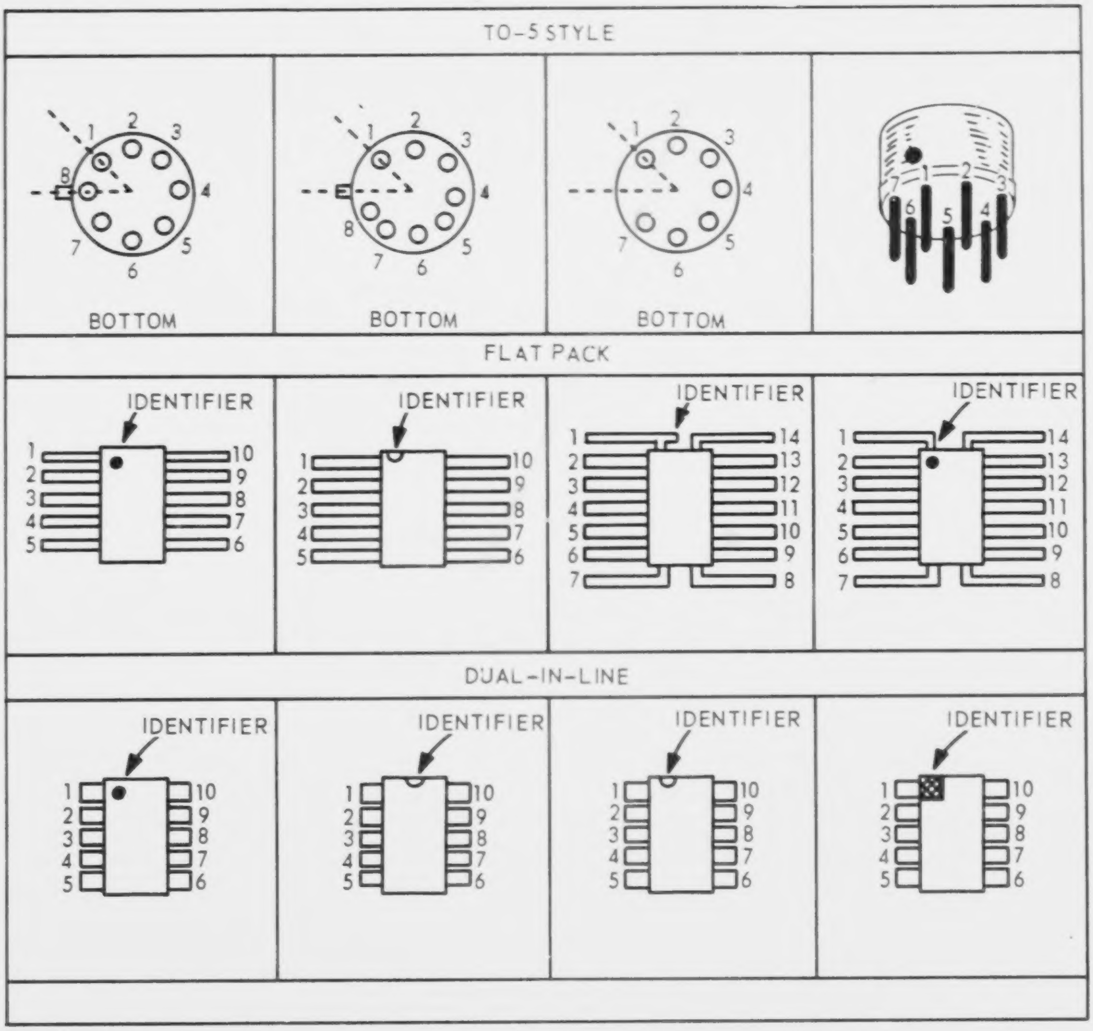

TO-5 STYLE
1
2
3
4
5
6
7
8
BOTTOM
BOTTOM
BOTTOM
FLAT PACK
IDENTIFIER
1
2
3
4
5
6
7
8
9
10
11
12
13
14
DUAL-IN-LINE
IDENTIFIER
1
2
3
4
5
6
7
8
9
10

Figure 1-18. Integrated-circuit package pin identification.

CHAPTER 2

Introduction to Digital Techniques and Numbering Systems

NOTE: For objectives 217-234, study objectives 005-022 in Module 10005, *Digital Techniques*, Unit 1, which accompanies this volume. When you complete Unit 1 of Module 10005, return to the text.

Module 10005

Unit 1

CDC 30554-2 Objectives	*Unit 1 Objectives*
217	005
218	006
219	007
220	008
221	009
222	010
223	011
224	012
225	013
226	014
227	015
228	016
229	017
230	018
231	019
232	020
233	021
234	022

Digital Logic and Boolean Algebra

NOTE: For objectives 235-258, study objectives 001-024 in Module 10005, *Digital Techniques,* Unit 2, which accompanies this volume. When you complete Unit 2 of Module 10005, return to the text.

Module 10005

Unit 2

CDC 30554-*2 Objectives*	*Unit 2 Objectives*
235	001
236	002
237	003
238	004
239	005
240	006
241	007
242	008
243	009
244	010
245	011
246	012
247	013
248	014
249	015
250	016
251	017
252	018
253	019
254	020
255	021
256	022
257	023
258	024

Clock/Pulse Generators

NOTE: For objectives 259-281, study objectives 001-023 in Module 10005, *Digital Techniques,* which accompanies this volume. When you complete Unit 3 of Module 10005, return to the text.

Module 10005

Unit 3

CDC 30554-2 Objectives	*Unit 3 Objectives*
259	001
260	002
261	003
262	004
263	005
264	006
265	007
266	008
267	009
268	010
269	011
270	012
271	013
272	014
273	015
274	016
275	017
276	018
277	019
278	020
279	021
280	022
281	023

CHAPTER 5

Sequential Logic

NOTE: For objectives 282–298, study objectives 001–017 in Module 10005, *Digital Techniques,* Unit 4, which accompanies this volume. When you complete Unit 4 of Module 10005, return to the text.

Module 10005

Unit 4

CDC 30554-2 Objectives	Unit 4 Objectives
282	001
283	002
284	003
285	004
286	005
287	006
288	007
289	008
290	009
291	010
292	011
293	012
294	013
295	014
296	015
297	016
298	017

Combinational Logic and Converters

NOTE: For objectives 299-316, study objectives 001-018 in Module 10005, *Digital Techniques,* Unit 5, which accompanies this volume. When you complete Unit 5 of Module 10005, return to the text.

Module 10005

Unit 5

CDC 30554-2 Objectives	Unit 5 Objectives
289	001
300	002
301	003
302	004
303	005
304	006
305	007
306	008
307	009
308	010
309	011
310	012
311	013
312	014
313	015
314	016
315	017
316	018

CHAPTER 7

Computers, Peripherals, and Storage Media

NOTE: For objectives 317-348, study objectives 001–032 in Module 10005, *Digital Techniques,* Unit 6, which accompanies this volume. When you complete Unit 6 of Module 10005, return to the text.

Module 10005

Unit 6

CDC 30554-2 Objectives	Unit 6 Objectives
317	001
318	002
319	003
320	004
321	005
322	006
323	007
324	008
325	009
326	010
327	011
328	012
329	013
330	014
331	015
332	016
333	017
334	018
335	019
336	020
337	021
338	022
339	023
340	024
341	025
342	026
343	027
344	028
345	029
346	030
347	031
348	032

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ANSWERS FOR EXERCISES

CHAPTER 1

Reference:

See Module 10008 and supplement to it for answers to objectives 200-210.

211 - 1. When the gate is at the same potential as the source.
211 - 2. Lower values of drain voltage are necessary to reach a constant drain current.
211 - 3. Pinch-off voltage.
211 - 4. Source, drain, and gate.
211 - 5. The depletion regions are devoid of current carriers.
211 - 6. It controls the amount of current flowing between the source and drain. Source and drain are analogous to the emitter and collector respectively.
211 - 7. It is a voltage-controlled, high-impedance input with only one type of current carrier.
211 - 8. There is no base junction.

212 - 1. Depletion and enhancement types.
212 - 2. Current.
212 - 3. The gate is insulated from the body of the device.
212 - 4. Enhancement.
212 - 5. It can store a charge (information).
212 - 6. They can puncture the insulating layer and destroy the MOSFET.
212 - 7. They guard against static discharge damage.

213 - 1. A high-gain DC coupled amplifier.
213 - 2. Differential input stage, isolation stage, and an output stage.
213 - 3. A minus (—) sign.
213 - 4. Differential or common mode.
213 - 5. To obtain a high degree of stability.

214 - 1. Linear ICs work with analog voltages and currents, whereas the DIC uses only two voltage or current levels.
214 - 2. The operational amplifier IC.
214 - 3. The diode.

215 - 1. (1) d.
(2) a.
(3) b.
(4) h.
(5) g.
(6) i.
(7) j.
(8) k.
215 - 2. Large-scale integration (LSI).
215 - 3. TTL.
215 - 4. ECL.
215 - 5. TTL.
215 - 6. CMOS.
215 - 7. CMOS.
215 - 8. TTL.

216 - 1. The TO-5, flat pack and DIP. The DIP is most common.
216 - 2. a. T.
b. F.
c. F.
d. T.
e. F.
f. T.

CHAPTER 2

See Module 10005, Unit 1 for answers to objectives 217-234.

CHAPTER 3

See Module 10005, Unit 2 for answers to objectives 235-258.

CHAPTER 4

See Module 10005, Unit 3 for answers to objectives 259-281.

CHAPTER 5

See Module 10005, Unit 4 for answers to objectives 282-298.

CHAPTER 6

See Module 10005, Unit 5 for answers to objectives 299-316.

CHAPTER 7

See Module 10005, Unit 6 for answers to objectives 317-348.

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MODULE 10005

DIGITAL TECHNIQUES

Unit 1

Introduction to Digital Techniques

and

Numbering Systems

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Preface

THIS UNIT to Module 10005, *Digital Techniques,* contains material that may be useful in portions of several digital electronics career fields. The unit may be of use in any subject area that includes a general introduction to computers and numbering systems. After a look at the decimal system, an "in-depth" study is made of the binary, octal, and hexadecimal numbering systems used in digital electronics.

Code numbers appearing on figures are for preparing agency identification only and should be of no concern to the student.

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This unit is valued at 12 hours (4 points).

Material in this unit is technically accurate, adequate, and current as of March 1981.

Acknowledgment

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NOTE: In this unit, the subject matter is developed by a series of student-centered objectives. Each of these carries a three-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see whether your answers match those in the back of this unit. If your response to an exercise is incorrect, review the objective and its text.

History and Introduction to Computers

THE ELECTRONIC computer has expanded people's ability to store and retrieve vast amounts of information. It can rapidly complete calculations that would require weeks for a mathematician to accomplish. By feeding engineering data into computers, designs can be tested and improved before they leave the drawing board. In many ways, the computer is one of the human race's greatest achievements. It is a tremendous aid in peacetime and in war.

In other words, "computers are here to stay." They are designed and built by people for their use. Computers are machines; therefore, they are no better and no worse than the motives driving their designers, programmers, and operators.

1-1. Classification and History

Since we are becoming more and more dependent on computers, it is helpful for you to understand the classifications used for computers. This section is a study of computer classifications and a brief history of their development.

001. Identify the generally accepted major classifications of computers, and state the difference between analog and digital operation.

Classification of Computers. There are many ways used to classify computers. One method will place them in groups according to their circuitry and technological state of development. Vacuum-tube computers are referred to as *first generation*, and transistorized computers are said to be *second generation*. The *third generation* of computers is not easily defined. Companies that build computers and base their product on microminiature integrated circuits use this technology to set them apart from others as third generation computers. But other manufacturers who have improved the performance, reliability, internal memory, and programming capabilities, using discrete components, insist that these improvements place them into the third generation of computers. At other times, computers are grouped according to their use, such as scientific, business, or military. A more common method is to class computers according to the "electronic way" in which they solve problems. This method will class computers into the major groups of *analog*, *digital*, and *hybrid*.

Analog computers solve problems electronically by comparison. For computation, data are not converted into digits but into a physically measurable quantity such as length, voltage, or current. The analog computer solves problems by causing these physical quantities to vary proportionately to the way in which the variables in the problem change. These variables can be continuously changed while the computer is at work. This means that the analog computer can give a continuing answer to a constantly changing problem. Stress on a missile, for example, can be continually updated with an analog computer.

A digital computer performs a series of arithmetic operations (addition, subtraction, multiplication, and division) using data expressed as digits or numbers. In the case of a digital computer, the data are expressed in terms of the binary numbering system. The digital computer performs operations in a sequence of distinct steps determined by certain mathematical rules and according to the programmed instructions. The major advantages of a digital computer are the speed that these arithmetic operations can be performed and the fact that the computer can be programmed to make logical decisions by examining, comparing, and testing, as well as performing mathematical operations. Digital computers are used to solve complex scientific problems, prepare payrolls, control air traffic, and guide a missile in flight.

Hybrid computers use a combination of analog and digital equipment. They are often used in scientific and technical applications, such as simulation, medical systems, and aerospace operations. Hybrid systems combine the advantages of the analog computers, such as continuity, and the advantages of the digital computer, such as speed and precise calculating ability.

A final method of classifying computers is according to their purpose or versatility—*special purpose* and *general purpose*. A special-purpose computer is one designed for a specific job or a specific class of jobs. It will usually have a sequence of operations permanently or semipermanently "wired in." For this reason it lacks the flexibility of being "reprogrammed" to perform a different type of job. General-purpose computers are made to solve a wide variety of problems. Flexibility is achieved by the fact that instruction changes to the computer are made by just loading a different program into the memory. Most of the commercial computers being acquired by the Air Force are of the general-purpose digital and stored-program type.

Exercises (001):

1. The major groupings that computers may be classified under are ________ and ________.

2. Which type of computer may compare quantities and represent the results with a voltage level?

3. Which type of computer detects the presence or nonpresence of information?

002. Identify some of the major technical advances leading to the development of the electronic computer.

History. Let's look at the history of computers by defining two words: "compute" and "computer."

(1) *Compute*—a verb from the Latin word *computare* meaning to define or reckon, especially by numerical means.

(2) *Computer*—derived from compute and meaning a person or device that computes.

Naturally, in the beginning, the only computer was the human brain, but people soon began devising means to simplify computing chores.

Probably the first indicating device for computation was a person's finger. Later sticks, stones, or other objects may have been used to indicate quantity. As previously stated, these things were only indicators; they made the job easier, but the brain was still the computer. Relatively little information is known about the very early stages of human life, but clay tablets dating around the year 2000 B.C. have been found containing information and computations concerning business transactions.

The first known device for counting was the *abacus*, invented sometime before 300 B.C. It is still widely used throughout the world. Although a skilled person may make rapid calculations using an abacus, it is not a true calculator but merely a more sophisticated indicating device (see fig. 1-1).

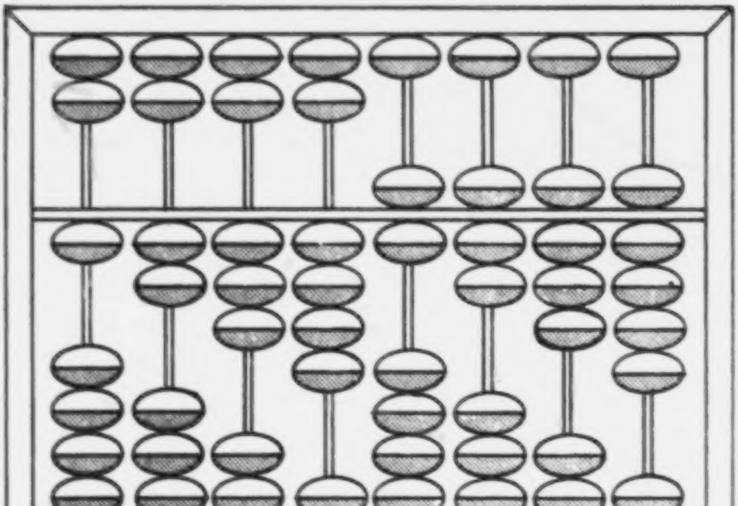

Figure 1-1. Abacus.

After the abacus, and a refinement of it, which is called a *Soraban*, little further advancement in computating devices is recorded until the year 1642. In that year a French mathematician, named Pascal, invented the first machine able to add and carry the next higher order. The next noteworthy development came in 1673 when a German mathematician, Leibnitz, designed a unit that could multiply as well as add. The German's ideas were an advancement, but the machine did not work well enough to be of wide value. In 1801, in France, probably the first major step toward computers was made. Jacquard developed the idea of having a series of punched cards containing information to control machinery. He used this system very successfully to control the weaving patterns of looms in a fabric mill. In 1820, Thomas, an American inventor, refined the principles of Leibnitz's machine and came up with the first desk calculator. Improved models of this calculator were used well into the 20th century. Charles Babbage, a brilliant mathematician, received funds from the English Government in the early 1800's to develop a machine that would calculate mathematical tables to 20 decimal places. He called his invention the *difference engine*. His design was a good one, but the inability to manufacture many precision parts caused repeated failures in attempts to produce a working model. The Government withdrew its support of the project and "Babbage's Difference Engine" died on the drawing board.

Around 1840, Babbage presented a new proposal to the British Government, requesting funds to build an *analytical engine*. Despite his earlier failures, funding was granted. He began work on a computing machine consisting of three sections: a *storage unit*, an *arithmetic unit*, and a *control unit*. He planned to use an adaptation of the punched card, designed by Jacquard, to enter information into the *analytical engine*. Babbage had plans for a machine that would store a thousand numbers of up to 50 digits each and make computations automatically by following stored instructions. Again, his ideas were far too advanced for the technology of the time. After many failures to produce a working prototype, the British Government withdrew its backing and this second endeavor was also abandoned. Despite his failures, Charles Babbage's ideas were sound and many of his principles are used in modern computers.

In 1886, Dr. Herman Hollerith, head of the U.S. Bureau of Census, set out to develop a faster means of compiling census data. He made a major contribution to the field of computer technology with his method of coding information on punched cards. This "Hollerith code" is still used in the data processing industry.

The first general-purpose computer project was begun in 1939 and completed in 1944 when IBM built the Mark I computer for Harvard University. It was built from "in stock" parts and was of electromechanical design. This computer is believed to be a direct representation of Babbage's "analytical engine."

The first "electronic" computer was the *Electronic Numerical Integrator and Calculator* known as the ENIAC. This was the first use of vacuum tubes, rather than relays, for storing information. The concept increased the speed of operations by about 1500 percent and was a tremendous step forward.

Another great step forward took place in the 1950's, when the operational amplifier ushered in the era of fully electronic analog computers. Also taking place during this time period was the perfection of magnetic-core technology. Magnetic cores offered large, fast, and economical memories to computer designers. Once developed, core memories revolutionized the growth of the computer.

One of the greater marketing events of the 1950's was the delivery of the first universal automatic computer (UNIVAC I). This system used mercury delay lines for storage and, for the first time, used metal-based magnetic tape. The first real production, full-sized computer, using magnetic drum storage, was the IBM 650 in 1954. The growth of computers was revolutionized in 1958 when RCA introduced the BIZMAC, the first commercial core memory system. That year, IBM modified their model 701 to a magnetic core memory system. Table 1-1 lists some historic events in the development of computers as we know them today.

The computer industry has not been alone in the influence of advancing technology. The emphasis of solid-state electronics has also been felt by other industries. For example, in 1964, the telecommunications industry felt the first effect with the introduction of the *No. 1 Electronic Switching System* (ESS-1). This opened the era of electronic switching, in which high-speed computers run systems that can perform more services faster, more reliably, and with greater flexibility.

A key to the high speed of today's computers is the number of circuits involved and their physical size. The more circuits, the more the computer can do—and the closer they are to each other, the faster the computer can perform. In 1959, Texas Instruments and Fairchild Semiconductor announced that they had produced integrated circuits (ICs)—single semiconductor chips containing several complete electronic circuits. Since that announcement, the speed and capabilities of computers have increased, as their physical size has decreased. By 1970, large scale integration (LSI) of circuitry was placing thousands of integrated circuits onto a single quarter-inch square chip. Today 100,000 transistors can be integrated on a single chip, making this chip more powerful than the ENIAC computer of 1946, which used 18,000 vacuum tubes.

Further technology advances in the 1970's saw the development of the *microprocessor* and *minicomputer*. In 1974, RCA introduced the first complementary metal oxide semiconductor (CMOS) microprocessor. With the advancement of ICs, chip makers saw that some of the peripheral functions could be integrated

TABLE 1-1
CHRONOLOGY OF IMPLEMENTATION OF MAJOR STORAGE TECHNOLOGIES/COMPUTERS

~~TABLE~~ 1 ~~1~~ ~~Chronology~~ of Implementation of Major Storage Technologies/Computers

Date Major System Operating[a]	Storage Technology	System Identification or Implementor	Module Size	Speed	Comments
BC	Mud tablets; ink on papyrus	Malasians; Egyptians and Greeks		Minutes	
1623	Mechanical positions; cogs on wheels	Schickard's semiautomatic calculator			Probably first mechanical calculator; not extant
1642	Mechanical positions; cogs on wheels	Pascal's calculator	10 digits/wheel 8 wheels	Seconds	First mechanical calculator still extant
1812	Punched cards	Jacquard weaving loom			First use of punched card storage
1890	Electromechanical dials, punched cards	Hollerith census machine	40 dials, 10K decimal digits per dial	Seconds per card (operator dependent)	First electrical calculator; mechanical storage electrically activated
1940	Capacitors on rotating durm	Atanasoff		1 rev/sec	Precursor to other circulating types of memory
1942	Electrical resistance on cards (analog)	Western Electric electrical director			Analog storage of functions

TABLE 1-1(Contd)

1943, 1944	Electromechanical relays, punched tapes (papers)	Mark I IBM-Harvard U	Internal counter 2204 positions		First fully automatic calculator
1946	Vacuum tube flip-flop Resistor array	ENIAC (University of Pennsylvania	20, 10 decimal digit numbers 4Kbits (100 numbers)		First large-scale electronic storage
1948	Cathode ray (Williams) tube, magnetic drum	Manchester University (England) miniature machine (not full computer)	CRT (1) 1024 bits (2) 1280 bits		First CRT storage; one of the earliest operational drums
1949	Mercury delay lines	EDSAC (Cambridge University, England)	576 bits/tube 18K bits total	1.1 msec circulation time	First fully operational delay line memory
1951	Magnetic tape (commercial)	UNIVAC I	1.44M bits max 1500 ft, 128 char./in.	100 in./sec	First commercial tape (and computer)
1953	Magnetic cores (coincident selection)	MIT memory test computer		20 sec access	First operational core memory
1955	Magnetic cores (coincident selection)	RCA BIZMAC			First commercial core memory
1956	Magnetic disk, movable heads	IBM 350 RAMAC	40M bits on 100 surfaces	0.5 sec access	First commercial movable head system

TABLE 1-1 (Contd)

1962	Thin magnetic films	UNIVAC 1107	128 words 36 bits/word (scratch-pad memory)	0.3 sec	First commercial thin film memory
1965	Plated rods	MCR 315			First commercial system
1968	Transistor (bipolar), integrated circuits	IBM buffer memory S360/M85, M25	512 words 18 bits/word 64 bits/chip	60 nsec cycle	First mass-produced integrated circuit memory; First cache (M85)
1971	Transistor (bipolar) main memory	IBM main memory S370 M145	128 bits/chip	0.54 sec cycle	First integrated circuit main memory
1973 FCS (announced 1972)	MOS FET	IBM main S370/M158, M168	1024 bits/chip		First mass-produced MOS memory

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[a]FCS=first customer shipment

on the same chip as the microprocessor. This is how the minicomputers and microcomputers "computer on a chip" were born. Becoming increasingly more popular, the microcomputer has opened a whole new spectrum of controller functions.

Today, computers are used, in some way, in practically every aspect of your daily life. They are found in the toys and games used to entertain and educate children. They are used as electronic controls for defense systems, industry, and in the home. Microcomputers are found in appliances, television, and in your automobile. The advances and applications of computers are only limited by the imagination of designers and the physical limitations of the very large scale integration (VLSI) process.

Exercises (002):

1. Computations concerning business transactions have been found on clay tablets believed to be from around the year ________ .

2. The first known mechanical aid in calculating is the ________ .

3. The first calculating machine with ability to carry to the next higher order was invented by a French mathematician, ________ .

4. Who designed the first machine capable of multiplying as well as adding?

5. Jacquard's major contribution to data processing is the ________ ________ .

6. Charles Babbage is noted for designing two calculating machines. He called his second machine his ________ ________ .

7. In 1886, the head of the U.S. Bureau of Census developed the ________ code.

8. The IBM Mark I was the first ________ ________ computer.

9. The increased operating speed of the ENIAC is attributed to its use of ________ ________ for storing information.

10. Computer and data processing units have become smaller, lighter, less expensive, and consume less power. This is due largely to the development of ________ ________ ________ .

1-2. The Basic Computer and Computer Applications

The purpose of the next section is to describe the five units used to form a basic computer, the function of each unit, and the general applications of the computer as a whole.

003. Relate each of the five basic computer units to its general function.

The Basic Computer. Let's continue our introduction to computers by learning the basic units that make up any digital computer. Figure 1-2 shows the five basic blocks making up all digital computers.

Input unit. All information used by a computer must be entered through the input unit. The information may be presented to the input in a number of ways, such as punched cards or tape, magnetically recorded, or by use of a manual keyboard. No matter what the method of entry is, the input unit translates the information into machine language. It also adjusts the logic level (voltage) to that required by the computer.

Control unit. The control unit of a digital computer directs the operation of all other units. It implements a series of instructions called a *program*. This program

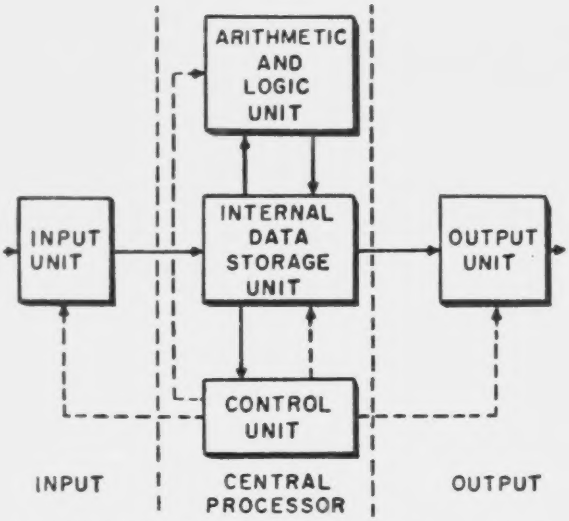


Figure 1-2. Representative digital data processor, block diagram.

insures that all steps of a computer's operation are done in proper sequence.

Memory unit. The computer program, as well as interim results of computer operations, must be stored within the computer. Not all information fed into a computer can be used at once, so a method of storing this information is required. This is done by the memory unit.

Arithmetic unit. The arithmetic unit accomplishes all mathematical and logical functions within the computer. Basically, it can only perform addition; but by proper manipulation of addition, problems in higher mathematics can be solved. When performing logic operations of the arithmetic unit, it renders *yes* or *no* decisions based upon instructions from the program.

Output unit. After being processed by the computer, information is transferred to the output unit. There it is transformed to meet the necessary requirements and is punched, printed, or recorded for future use.

Exercise (003):

1. Column A is a list of general computer functions. Relate each to the appropriate unit listed in column B. Units in column B may relate to more than one function from column A.

Column A

___ (1) Information is transformed to meet requirements for punching.
___ (2) Performs mathematical functions.
___ (3) Stores information until it is needed.
___ (4) Receives information after it has been processed.
___ (5) Insures that proper sequence is followed.
___ (6) Accepts information from a keyboard.
___ (7) Adjusts logic levels to those required by the computer.

Column B

a. Input unit.
b. Control unit.
c. Memory unit.
d. Arithmetic unit.
e. Output unit.

004. State the two general types of computer applications, and identify some of the uses for each type.

Applications for Computers. Computers are used in nearly every field where large quantities of information are processed. Computers are categorized as data processing (general-purpose) computers or scientific (special-purpose) computers. Digital computers are capable of being programmed to perform either function. You may sometimes hear reference to a third category of computers. These are called *military computers*; however, while they *are* used to process scientific or general information for military use, they still fall into one of the *two* basic categories. A few areas where computers are used are:

Data processing:

a. Accounting.
b. Dispatching.
c. File and record maintenance.
d. Inventory control.
e. Research studies.
f. Sales analysis.
g. Education.

Scientific:

a. All branches of engineering.
b. Statistics.
c. Physics.
d. Biology.
e. Chemistry.
f. Medicine.
g. Meteorology.

Military: The military services use computers to perform all of the same functions that are performed by computers in the civilian community. These functions include the following:

a. Accounting.
b. Dispatching.
c. File and record maintenance.
d. Inventory control.
e. Research studies.
f. Sales analysis.
g. Education.
h. All branches of engineering.
i. Statistics.
j. Physics.
k. Biology.
l. Chemistry.
m. Medicine.
n. Meteorology.

In addition, many operations, such as weapons control, classified as having "only military application," are controlled by computers.

This is only a *very* small sample of the applications to which computers can be applied. In fact, the versatility of the computer is limited only by the inherent limitations of the programmer and operator.

Exercises (004):

1. The two general categories of computer applications are ________ ________ and ________.

2. Military computers are applied in which type of application?

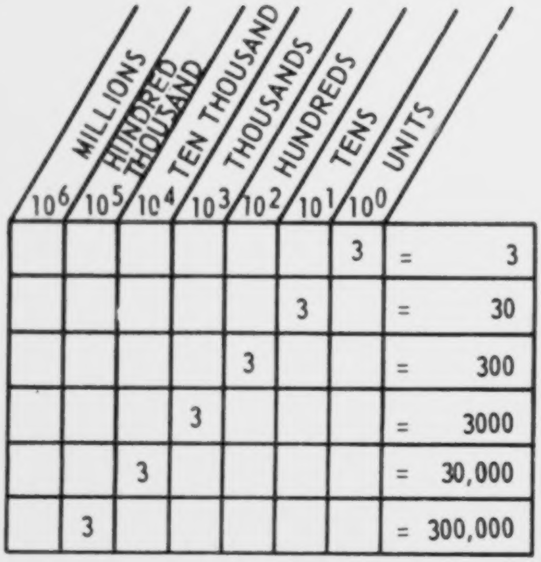
3. Identify three areas where data processing (general-purpose) computers are used and three areas where scientific computers are used.

Numbering Systems and Mathematical Computations

SINCE A DIGITAL computer deals directly with numbers, we must study numbering systems. The decimal system, using 10 different symbols, is the most common systems in use today.

Many different numbering systems are possible and are available for use. The number of different symbols or digits used in a numbering system is called the base, or radix, of the system. In addition to the 10-digit decimal system, digital techniques use the binary (with a base of 2), the octal (with a base of 8), binary coded decimal (with a modified base of 10), and hexadecimal (with a base of 16). This module presents some important facts about the most frequently used numbering systems along with their arithmetic operations.

Although computers can be designed to operate with any numbering system, the octal, binary, and hexadecimal systems are commonly used. Each system has its own advantages, and each is used in a different type of computer. Sometimes, two or more numbering systems are used in the same equipment. When this is done, a facility is incorporated to convert from one numbering system to the other.



MILLIONS 10^6	HUNDRED THOUSAND 10^5	TEN THOUSAND 10^4	THOUSANDS 10^3	HUNDREDS 10^2	TENS 10^1	UNITS 10^0	
						3	= 3
					3		= 30
				3			= 300
			3				= 3000
		3					= 30,000
	3						= 300,000

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Figure 2-1. Decimal PLACE values.

2-1. Decimal Numbering System

The decimal numbering system is the most understood system, and we use it daily. Most of the rules and terms used with the decimal system are also used with the other systems you will study. In this section, we will review the decimal numbering system.

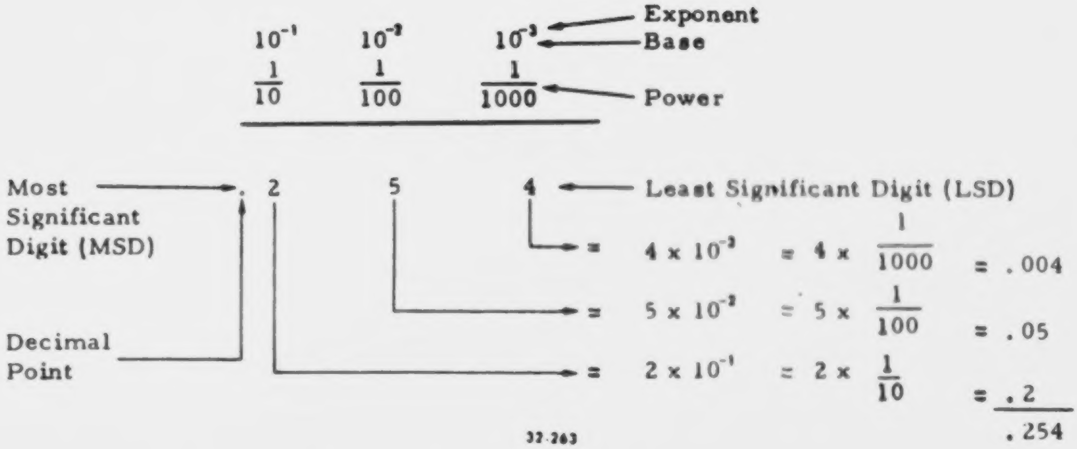
005. Identify PLACE values, radix, integral portion, fractional portion, placeholder, MSD, LSD, and powers, as they apply to the decimal numbering system.

Decimal Numbering System. The decimal numbering system uses 10 different basic symbols: 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. These symbols are called digits. In order to represent a number larger than 9, PLACE VALUE must be used. PLACE, in this case, is the position of the symbol with respect to the decimal point. It determines the power of 10 by which the digit in the PLACE will be multiplied.

In figure 2-1, the 3 written in the units column stands for three, but the 3 written in the tens column stands for 30. Thus, in a number system, the VALUE of a digit depends upon its PLACE in the number.

In figure 2-1, moving a digit to the left from one column to the next has the effect of multiplying the number by 10. The digit 3 in the units column stands for three. Moving the 3 one column to the left signifies 30. If moved one more column, it indicates 300. You can see that in the decimal system, PLACE represents the power of 10 by which the digit must be multiplied.

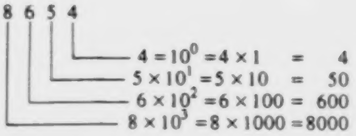
When the system of using PLACE value was first developed, a space was used to indicate that no number appeared in that position. For example, 106 was written 1 6 and 1006 was written 1 6. It is easy to see that this system led to confusion. Does 1 6 represent 10006 or 100006? It is difficult to decide with certainty. This difficulty led to the development of a PLACEHOLDER or the use of the zero.



10^{-1}
10^{-2}
10^{-3}
Exponent
Base
$\frac{1}{10}$
$\frac{1}{100}$
$\frac{1}{1000}$
Power
Most Significant Digit (MSD)
. 2 5 4
Least Significant Digit (LSD)
$= 4 \times 10^{-3} = 4 \times \frac{1}{1000} = .004$
$= 5 \times 10^{-2} = 5 \times \frac{1}{100} = .05$
$= 2 \times 10^{-1} = 2 \times \frac{1}{10} = .2$
.254
Decimal Point
32-263

Figure 2-2. Example of decimal fraction PLACE value.

You have learned how to write numbers as powers of 10. Recall that 10^4 is $10 \times 10 \times 10 \times 10$. The number 4 tells how many times to use 10 as a factor. In the equality $10^4 = 10{,}000$, 10 is the BASE and 4 is the EXPONENT. The number 10^4 can be read as "10 to the fourth power." Therefore, in the decimal system, one speaks of POWERS of 10. Powers of 10 are also illustrated in figure 2-1. Remember, always, that any number to the zero power is equal to one. Here is another way to expand a number to show both PLACE value and powers of 10.



8 6 5 4
$4 = 10^0 = 4 \times 1 = 4$
$5 \times 10^1 = 5 \times 10 = 50$
$6 \times 10^2 = 6 \times 100 = 600$
$8 \times 10^3 = 8 \times 1000 = 8000$

$8654_{(10)}$

The decimal number $305.84_{(10)}$ consists of seven different parts. The following shows the name and relationship of each part.

Integral portion	305
Fractional portion	84
Placeholder	0
Decimal point	.
LSD (least significant digit)	4
MSD (most significant digit)	3
Radix	(10)

The integral portion (305) is left of the decimal point, while the fractional portion (84) is to the right of the decimal point. The LSD (4) has the smallest value and MSD (3) has the greatest value because of their relative positions to the number. The radix indicates which numbering system is being used and is written as a subscript to a number. Normally, the radix is omitted in decimal numbers. Because binary numbers consist of only two digits, the radix 2 is often omitted. If any possible confusion may arise, the radix should be included.

So far, we have dealt with a whole number; that is, one in which all discrete characters (digits) are to the left of the decimal point. A fractional number has the discrete characters to the right of the decimal point. The first digit to the right of the decimal point is the MSD, while the last digit to the right is the LSD. Figure 2-2 illustrates fractional PLACE values. Notice that the exponents are negative.

Of course, much more might be said about the decimal system. Later, we shall refer to certain rules and procedures for manipulating decimal numbers. For the present, this brief review should aid you in understanding certain characteristics of the binary numbering system.

Exercises (005):

1. Use figure 2-3 and expand the decimal number 2532.

10^3	10^2	10^1	10^0	POWER OF RADIX
1000	100	10	1	PLACE VALUE
			2	=
		3		=
	5			=
2				=

NDA13-2

Figure 2-3. Expanding decimal numbers (objective 005, exercise 1).

2. Identify the portion of the number 706.4 to which each of the following terms are related. Write the letter of the correct term on the line drawn to the right of the number.
   a. LSD of the integral portion.
   b. Least significant digit (LSD).
   c. Most significant digit (MSD).
   d. Placeholder.
   e. Decimal point.

7 ______

0 ______

6 ______

. ______

4 ______

3. Identify the portion of the number $509_{(10)}$ to which each of the following terms is related. Write the letter of the correct term on the line drawn to the right of the number.
   a. Least significant digit (LSD).
   b. Most significant digit (MSD).
   c. Placeholder.
   d. Radix or base.

5 ______

0 ______

9 ______

(10) ______

4. In the statement $10^3 = 1000$, what number is called the base? the power? the exponent?

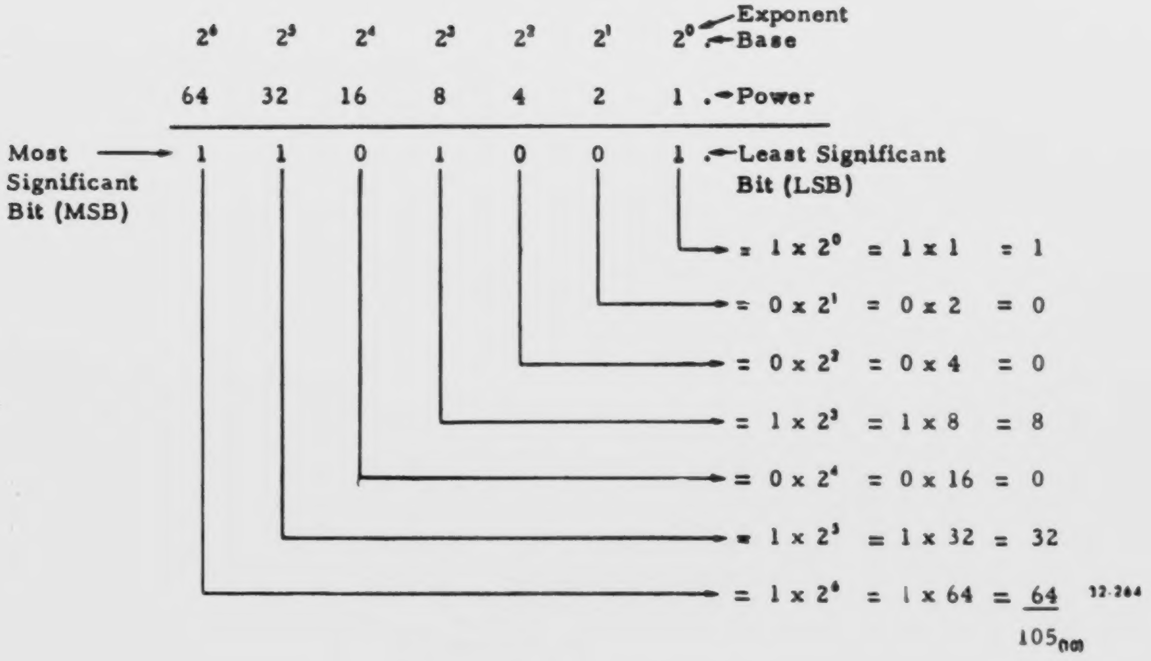
5. The power of a number is equal to what?

6. In the number 6178, what number is the MSD and what number is the LSD?

7. In the number .6178, what is the MSD and what number is the LSD?

2-2. Binary Numbering System

Since computers operate using the symbols 0 and 1, using the binary numbering system has many advantages. The purpose of this section is to provide a thorough study of the binary numbering system and binary mathematics.



2^6 2^5 2^4 2^3 2^2 2^1 2^0
Exponent
Base
64 32 16 8 4 2 1
Power
Most Significant Bit (MSB)
1 1 0 1 0 0 1
Least Significant Bit (LSB)
$= 1 \times 2^0 = 1 \times 1 = 1$
$= 0 \times 2^1 = 0 \times 2 = 0$
$= 0 \times 2^2 = 0 \times 4 = 0$
$= 1 \times 2^3 = 1 \times 8 = 8$
$= 0 \times 2^4 = 0 \times 16 = 0$
$= 1 \times 2^5 = 1 \times 32 = 32$
$= 1 \times 2^6 = 1 \times 64 = 64$
$105_{(10)}$
12-264

Figure 2-4. Examples of binary whole number PLACE value.

006. Identify the essential elements of the binary number system, and compare decimal numbers to binary numbers.

Binary System. Six of the seven different parts of a number apply to any numbering system that uses the PLACE value concept. The exception is the term "DECIMAL POINT." Octal numbers have an OCTAL POINT, and binary numbers have a BINARY POINT. In the number $320.61_{(8)}$ the point (.) is referred to as the OCTAL POINT. When you are working with a binary number, such as $1101.11_{(2)}$, you must refer to the point (.) as the BINARY POINT.

Three important features of numbering systems are: (1) PLACE value for the symbols positioned in the number, (2) a point (.) which is used to separate the fractional part of a number from the whole part, and (3) a radix, or base, of a number system.

Most present-day digital computers use the binary numbering system. One advantage of this binary numbering system is that it uses only two symbols. These symbols are 0 and 1. Since only two symbols are used, a computer using the binary system needs only two different conditions to represent them. This arrangement simplifies computer design and improves its accuracy. Many electronic components can be operated as two state (on-off) devices; for example, each digit of a binary number can represent a logic situation of yes or no, a relay energized or deenergized, a transistor conducting or cut off, a switch open or closed. To express numbers other than 0 and 1 in the binary system, the symbols are arranged in sequence. The PLACE of each symbol in the sequence has a designated VALUE based on the powers of 2.

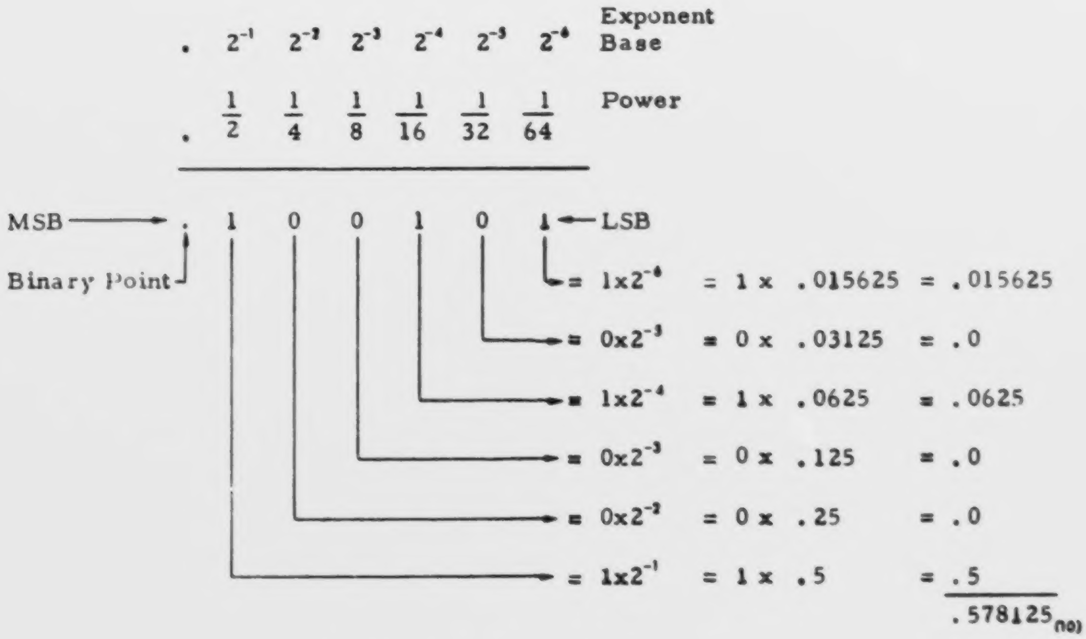
The binary system uses the radix two (2). It has only two symbols, 0 and 1. You can write any number using these two symbols. Zero is the PLACEHOLDER for the system. One stands for 1, unity, or a single unit. As an example, let's find the decimal equivalent of the binary number 1101001 using the powers of 2, as shown in figure 2-4. After multiplying each of the bits by the power of the PLACE the bit occupies, and then adding these values together, we see that 1101001_2 is equal to 105_{10}. Note in figure 2-4 that as the exponent increases by 1, the power doubles; this is characteristic of the base two system.

As shown in figure 2-5, the representation of fractional numbers, those numbers whose bits lie to the right of the binary point (decimal point in base 10), is also similar to the decimal method. Note that as the negative exponent decreases by 1 (for example, from 2^{-2} to 2^{-3}, or from $2P^4$, to 2^{-5}) the power is halved.

When we used the powers of 2 in figures 2-4 and 2-5, we actually converted a binary number to its decimal equivalent. This method of converting from binary to decimal is called the addition method. You will study this and other binary-to-decimal conversion methods later.

Exercises (006):

1. State essential characteristics of the binary number system.



. 2^{-1} 2^{-2} 2^{-3} 2^{-4} 2^{-5} 2^{-6}
Exponent
Base
. $\frac{1}{2}$ $\frac{1}{4}$ $\frac{1}{8}$ $\frac{1}{16}$ $\frac{1}{32}$ $\frac{1}{64}$
Power
MSB
. 1 0 0 1 0 1
LSB
Binary Point
= 1x2^{-6} = 1 x .015625 = .015625
= 0x2^{-5} = 0 x .03125 = .0
= 1x2^{-4} = 1 x .0625 = .0625
= 0x2^{-3} = 0 x .125 = .0
= 0x2^{-2} = 0 x .25 = .0
= 1x2^{-1} = 1 x .5 = .5
$.578125_{(10)}$

Figure 2-5. Examples of binary fraction PLACE value.

0	+	0	=	0	&	CARRY 0
0	+	1	=	1	&	CARRY 0
1	+	0	=	1	&	CARRY 0
1	+	1	=	0	&	CARRY 1

NDA13-30

Figure 2-6. Truth table for binary addition.

2. In the base two system, as the exponent increases by 1, what happens to the power?

3. What happens to the power when the negative exponent decreases by 1 (from 2^{-2} to 2^{-3})?

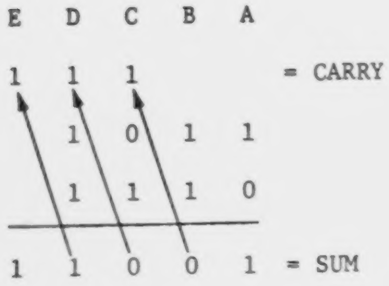
007. Solve binary mathematical problems using addition, subtraction, multiplication, and division.

Binary Mathematics. Binary mathematics is extremely simple since we are dealing with only 0 and 1. In binary addition, the most complex problem we encounter is 1 + 1 + 1. The truth table for all possible combinations for addition is shown in figure 2-6. Let us apply these rules to a binary addition problem. Add 1110 to 1011. The proper procedure is illustrated in figure 2-7. The alphabetic letters identify the columns.

Steps: (Begin at the right-hand column and work to the left.)

A. 0 + 1 = 1, with no carry.
B. 1 + 1 = 0, with a carry of 1 to the C column.
C. 1 + 0 + 1 (the carry from B) = 0, with a carry of 1 to D.
D. 1+ 1 + 1 (the carry from C) = 1, with a carry of 1 to E.

Bring the carry of 1 in E down and it becomes the MSD of the final sum. Practice problems and solutions:



NDA13-31

Figure 2-7. Steps for binary addition.

$$\begin{array}{r} 1010 \\ \underline{0101} \\ 1111 \end{array} \qquad \begin{array}{r} 111 \\ \underline{11} \\ 1010 \end{array} \qquad \begin{array}{r} 10011 \\ 0010 \\ \underline{1001} \\ 11110 \end{array} \qquad \begin{array}{r} 1011101010 \\ \underline{1000111001} \\ 10100100011 \end{array}$$

For an even number of 1's (including carries) in each column, the sum will always be 0. For an odd number of 1's (including carries) in each column, the sum will always be 1. For every two 1's in a column (excluding carries), 1 is carried to the next column.

Example:

$$\begin{array}{r} 1111 \leftarrow \\ 111111 \leftarrow \\ 11111 \\ 1010 \\ 10101 \\ \underline{11111} \\ 1011101 \end{array} \text{carries}$$

Addition Examples:

$$(1)\begin{array}{r} 1 \\ \underline{0} \\ 1 \end{array} \quad (2)\begin{array}{r} 0 \\ \underline{1} \\ 1 \end{array} \quad (3)\begin{array}{r} 0 \\ \underline{0} \\ 0 \end{array} \quad (4)\begin{array}{r} 1 \\ \underline{1} \\ 10 \end{array} \quad (5)\begin{array}{r} 11 \\ \underline{00} \\ 11 \end{array}$$

$$(6)\begin{array}{r} 10 \\ \underline{01} \\ 11 \end{array} \quad (7)\begin{array}{r} 11 \\ \underline{01} \\ 100 \end{array} \quad (8)\begin{array}{r} 11 \\ \underline{11} \\ 110 \end{array} \quad (9)\begin{array}{r} 101 \\ \underline{010} \\ 111 \end{array} \quad (10)\begin{array}{r} 111 \\ \underline{11} \\ 1010 \end{array}$$

$$(11)\begin{array}{r} 1111 \\ \underline{0101} \\ 10100 \end{array} \quad (12)\begin{array}{r} 1111 \\ \underline{1111} \\ 11110 \end{array}$$

Binary subtraction is just the reverse of addition. It is performed the same as in decimal numbers as illustrated in the truth table in figure 2-8.

Example:

$$\begin{array}{r} 1 \\ 01 \\ 10110 \\ \underline{-\ 1010} \\ 1100 \end{array}$$

Since the MSD of the minuend is worth 16, two binary 1's must be used to represent it in the next lower position, which is worth only 8. Thus, there is a remainder of 1.

0	-	0	=	0	NO BORROW
0	-	1	=	1	BORROW 1
1	-	0	=	1	NO BORROW
1	-	1	=	0	NO BORROW

NDA13-32

Figure 2-8. Truth table for binary subtraction.

0	X	0	=	0
0	X	1	=	0
1	X	0	=	0
1	X	1	=	1

NDA13-33

Figure 2-9. Truth table for binary multiplication.

Perhaps the simplest way to perform binary subtraction is to subtract as in decimal subtraction; that is, by treating the bits as decimal digits. When a borrow is necessary in any number system, its value is equal to the radix of that system. The borrow is then added decimally to the minuend bit of that particular column, and the subtrahend is subtracted decimally.

Example:

```
 02  borrow
 10  minuend
 -1  subtrahend
 --
  1
```

Subtraction Examples:

```
(1)  1    (2)  0    (3)  10    (4)  11
    -1        -0        -01         -1
    --        --        ---         --
     0         0         01         10

(5)  111   (6)  111   (7)  110   (8)  1110
    -010       -110       -011       -0111
    ----       ----       ----       -----
     101        001        011        0111
```

Binary multiplication is the same as decimal multiplication, but the multiplication table is composed entirely of 0's and 1's. This is shown in the truth table of figure 2-9.

Multiplication Examples:

```
(1)  1    (2)  0    (3)  0    (4)  1    (5)  11
    ×1        ×1        ×0        ×0        ×01
    --        --        --        --        ---
     1         0         0         0         11

(6)   111    (7)  101    (8)   1010    (9)    1101
     ×11         ×10          ×101           ×110
    -----       ----        ------        -------
      111         000         1010           0000
     111         101         0000           1101
    -----       ----        1010           1101
    10101       1010        ------        -------
                             11010        1001110
```

Binary division is a bit tricky because division by zero has never been defined. We have no truth table for this operation, but it is simply a matter of thinking in binary terms.

Division Examples:

```
        10             10              10
(1) 10/100     (2) 11/110     (3) 100/1000
       10             11             100
       --             --             ---
       00             00              00
       00             00              00
       --             --              --

           111                11
(4) 101/100011     (5) 011/001001
        101                011
        ---                ---
         111                011
         101                011
         ---                ---
          101
          101
          ---
```

Exercises (007):

1. Write the binary count next to the following decimal numbers.

   1—
   2—
   3—
   4—
   5—
   6—
   7—
   8—
   9—
   10—
   11—
   12—
   13—
   14—
   15—
   16—
   17—
   18—
   19—
   20—

2. Add:

```
a.  1110101
    1011010
    -------

b.  11011
    01010
    -----

c.  0100111
    1011101
    -------
```

3. Subtract:

```
a.  110101
      1011
    ------

b.  101101
     10111
    ------

c.  1110101
     111111
    -------
```

4. Muitiply:

a. $$\begin{array}{r} 11111 \\ \underline{11} \end{array}$$

b. $$\begin{array}{r} 1011 \\ \underline{101} \end{array}$$

c. $$\begin{array}{r} 100010 \\ \underline{111} \end{array}$$

5. Divide:

a. $110/\overline{101101}$.

b. $101/\overline{101000}$.

c. $100/\overline{110100}$.

008. Solve binary subtraction problems using complements and end-around carry.

Binary subtraction may also be accomplished using complements and end-around carry. There are two types of number complements, the radix complement and the radix −1 complement. In the binary numbering system, the radix complement is commonly called the *2's complement,* while the radix −1 complement is known as the *1's complement.* The radix complement is simply the difference between a number and the radix of that numbering system. For example, the radix complement of $1_{(2)}$ is 2 − 1 or 1. The radix −1 is the difference between a number and highest symbol in that numbering system. For example, the radix −1 complement of $1_{(2)}$ is 0 and of $0_{(2)}$ is 1.

Numbers complement is widely used in computers, and the value far exceeds that indicated by the simplicity of the operation. Inside the computer, all numbers are binary; and, it is common practice to store all negative numbers in the complement form. More important, the use of complements enables the computer to add, subtract, multiply, and divide by a process of simple addition. This results in a fantastic reduction in the required computer circuitry.

Let's try a few examples of complements. Extract the radix complement and the radix −1 complement of these binary numbers: 01, 101, and 1010.

Largest symbol	11	111	1111
Subtract	01	101	1010
Radix − 1 complement	10	010	0101
Add 1 to LSD	1	1	1
Radix complement	11	011	0110

Subtraction by addition: It is obvious that multiplication can be accomplished by a series of addition. 5 × 5 = 25, but 5 + 5 + 5 + 5 + 5 is also 25. Division can be performed by a series of subtractions. 25 divided by 5 = 5, but 25 − 5 − 5 − 5 − 5 − 5 = 0 and the number of operations is 5.

Now if we can subtract by adding, the only arithmetic function needed in the computer for basic arithmetic is addition. So let's see how it subtracts by adding with binary numbers. Let's subtract $011\ 111_{(2)}$ from $101\ 010_{(2)}$. Step by step, using the 2's complement, it goes like this:

Largest symbol	111 111
Subtract	011 111
Radix − 1 complement	100 000
Add 1 to LSD	1
Radix complement	100 001
Add minuend	101 010
Discard end carry 1	① 001 011

In other computer systems, the radix −1 (1's complement) complement and end-around carry are used. Using the same numbers, the end-around carry goes like this:

```
Minuend   101 010       101 010
Subtract  011 111       100 000—add radix − 1 complement
                   ①    001 010
                          └────→1   add end carry to LSD
                        001 011
```

Exercise (008):

1. Perform the following subtractions by complements and end-around carry:

a. $$\begin{array}{r} 110\ 011_{(2)} \\ -\underline{011\ 111}_{(2)} \end{array}$$

b. $$\begin{array}{r} 111\ 101_{(2)} \\ -\underline{100\ 000}_{(2)} \end{array}$$

c. $$\begin{array}{r} 100\ 000_{(2)} \\ -\underline{011\ 000}_{(2)} \end{array}$$

009. State a fundamental division method rule, and convert decimal whole numbers to binary whole numbers by the division method.

Decimal-to-Binary Conversion. There are several methods of converting decimal numbers to binary

Position	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
Binary number	1	0	0	0	1	1	1	0	. binary point
	MSB							LSB	

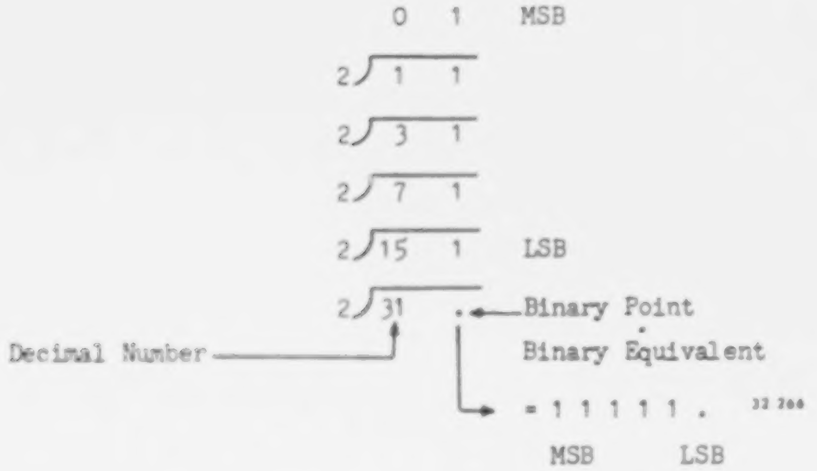


Figure 2-10. Division method—decimal-to-binary conversion.

form, but we shall consider only two of them: the division method of converting whole numbers and the multiplication method of converting fractions.

Division method (whole numbers). This is a versatile, easily used method, which works well on a decimal whole number of any size. It merely involves repeatedly dividing the decimal number by the radix (2) of the binary system, according to the following three rules for the division method of conversion (see fig. 2-10).

(1) Divide the decimal number by 2. The remainder (0 or 1 when dividing by 2) becomes the LSB of the binary number.

(2) Divide the quotient of the first division by 2. The remainder becomes the next bit in the binary number.

(3) Continue to divide by 2 until the final quotient is 0. The remainder of each division step will become a bit in the binary number.

The final remainder is the MSB of the binary equivalent number. Let's apply these rules and convert 142_{10} to its binary equivalent in a step-by-step process, as outlined in figure 2-11.

Step 1. Following rule 1, we divide 142 by 2. The remainder (0) becomes the LSB of the binary number.

Step 2. Following rule 2, we divide the quotient of the first division (71) by 2. The remainder (1) becomes the next bit in the binary number. The following steps are directed by rule 3.

Step 3. Dividing 35 by 2 gives a quotient of 17 and a remainder of 1. The remainder (1) becomes the next bit in the binary number.

Step 4. Dividing 17 by 2 gives us a quotient of 8 and a binary bit of 1.

Step 5. Dividing 8 by 2, we get a binary bit of 0.

Step 6. Dividing 4 by 2 gives us a binary bit of 0.

Step 7. Dividing 2 by 2 gives us a binary bit of 0.

Step 8. Dividing 1 by 2 gives us a final quotient of 0 and a remainder of 1. This remainder (1) becomes the MSB of the binary number equivalent of 142_{10}.

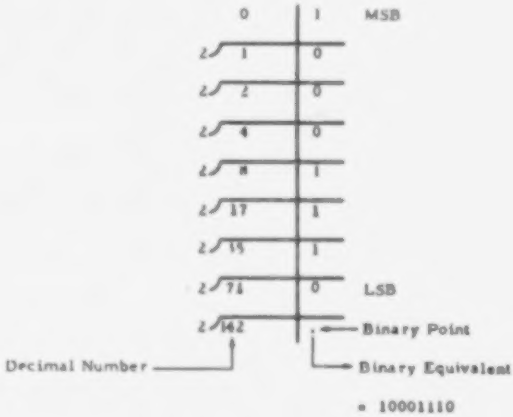


Figure 2-11. Examples of decimal-to-binary conversion—whole number.

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25

Figure 2-12. Powers of 2.

This completes the conversion process. To check our answer, we write the binary number 10001110 and, above each bit, indicate the position held by the bit as shown below. Since this is a whole number, the LSB occupies the 2^0 position; the next bit occupies the 2^1 position, and so on. The MSB occupies the 2^7 position. Now, referring to figure 2-12, table of powers of 2, we add together the power of each position that is occupied by a binary 1. Since 0's are merely placeholders, we ignore them. The 2^7 position has a power of 128. This will be one of the powers that we shall add together. Positions 2^6 through 2^4 are occupied by 0's, so we ignore tham. Position 2^3 is occupied by a 1 and has a power of 8. Position 2^2 is occupied by a 1 and has a power of 4. Position 2^1 is also occupied by a 1 and has a power of 2. Position 2^0 is occupied by a placeholder and may be ignored. Adding together the powers of the position that are occupied by 1's, we find that $128 + 8 + 4 + 2 = 142_{10}$. This tells us that we made a correct conversion.

Exercises (009):
In the exercises below are some problems on which you can use the division method of converting from decimal to binary. Convert these numbers to binary form and check your answers, as we did in the preceding paragraph. If your answers do not agree with the correct answers, rework the problems, carefully following the rules, and pay close attention to the arithmetic involved. Many wrong solutions result not from procedural errors but from simple arithmetic mistakes.

1. What is the rule when converting decimal numbers to binary numbers using the division method?

2. When converting decimal numbers to binary numbers by the division method, what number do we use to divide by?

3. Using the division method, convert the following numbers to binary numbers:
   a. 76_{10}

   b. 212_{10}

   c. 63_{10}

   d. 21_{10}

   e. 1409_{10}

   f. 855_{10}

010. State basic principles of the multiplication method, and convert decimal fractional numbers to binary fractional numbers by use of this method.

Multiplication method (fractional numbers). This method, adaptable to fractions of all sizes, consists of a series of multiplication steps. The decimal fraction is repeatedly multiplied by 2, and the digit (1 or 0 when multiplying by 2) generated to the left of the decimal point in the product becomes a bit in the equivalent binary number. The example in figure 2-13 shows the conversion of the decimal fraction .4375 to binary form. The following three rules are used for the multiplication method of conversion:

(1) Multiply the decimal fraction by 2. If the product is greater than 1, the whole part of the product (1 or 0 when multiplying by 2) becomes the MSB of the binary equivalent and is dropped from the product. If the product is less than 1, a 0 becomes the binary MSB.

(2) Multiply the fractional part of the product of the first multiplication by 2. If a whole number (1 when multiplying by 2) is generated to the left of the decimal point, it becomes the next bit of the binary number and is dropped from the product. If no 1 was generated, the binary bit will be a 0.

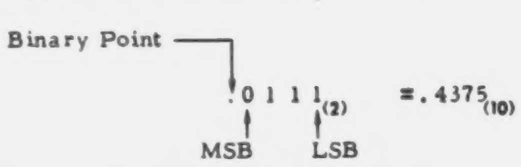


Figure 2-13. Multiplication method—decimal-to-binary conversion.

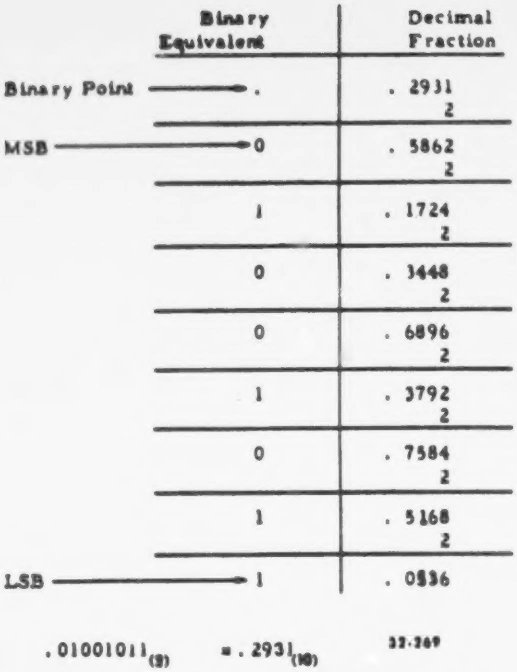


Figure 2-14. Decimal-to-binary conversion—fraction.

(3) Continue multiplying the fractional portion of the products by 2. The digit to the left of the decimal point of each product will be the binary bit for that step. The degree of accuracy desired will determine the number of multiplication steps to be performed. The binary bit generated by the last multiplication step is the LSB.

To clarify the use of these rules, let's convert the decimal fraction .2931 to binary form in a step-by-step process. Figure 2-14 illustrates these steps.

Step 1. Following rule 1, we multiply the decimal fraction (.2931) by 2. Since the product (.5862) is less than 1, the digit to the left of the decimal point is a 0. This 0 becomes the MSB of the binary equivalent.

Step 2. Following rule 2, we multiply the fractional part of the first product (.5862) by 2. This time, the product (1.1724) is greater than 1; therefore, the 1 to the left of the decimal point becomes the next bit of the binary number.

Step 3. We now multiply the fractional part (.1724) of the current product by 2. Since the product (0.3448) of this multiplication step is less than 1, the 0 to the left of the decimal point becomes the next binary bit.

Step 4. Multiplying the fractional part (.3448) of the current product by 2, we get a product of 0.6896. The 0 to the left of the decimal point becomes the next binary bit.

Step 5. Multiplying .6896 by 2 gives us a product of 1.3792. The 1 becomes a binary bit.

Step 6. Multiplying .3792 by 2 gives us a product of 0.7584 and a binary bit of 0.

Step 7. Multiplying .7584 by 2 gives us a product of 1.5168 and a binary bit of 1.

Step 8. Multiplying .5168 by 2 gives us a product of 1.0336 and a binary bit of 1.

At this point, our conversion is accurate to eight binary places, since we have 8 binary bits. We shall stop here, and following rule 3, the digit (1) to the left of the decimal point in the final product (1.0336) will be designated the LSB of the binary number. We could continue the multiplication steps until we attain any desired degree of accuracy. However, the binary equivalent will never be exactly equal to the decimal fraction unless the fractional portion of the final product consists of all zeros, as shown in figure 2-12. To check our conversion and see just how closely $.01001011_2$ compares to $.2931_{10}$, we shall use figure 2-12. First, we write the binary number (.01001011) and indicate the positions occupied by each bit. This is a fractional number, so the MSB will occupy the 2^{-1} position as shown below:

Position:	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
Binary number:	0	1	0	0	1	0	1	1

Now we add together the powers of each position occupied by a 1 in the binary number. Since zeros are placeholders, we ignore them. Figure 2-12 shows that position 2^{-2} has a power of .25; 2^{-5} has a power of .03125; 2^{-7} has a power of .0078125; and 2^{-8} has a power of .00390625. Adding these powers together, we find that $.01001011_{(2)}$ equals $.29296875_{(10)}$:

$$
\begin{array}{r}
.25 \\
.03125 \\
.0078125 \\
\underline{.00390625} \\
.29296875
\end{array}
$$

Subtracting .29296875 from the decimal fraction .2931, which we initially converted to binary equivalent, we find that the inaccuracy is only slightly more than .0001.

$$
\begin{array}{r}
.2931 \\
\underline{-.29296875} \\
.00013125
\end{array}
$$

We haven't yet discussed converting mixed decimal numbers (numbers that have a whole part and a fractional part) to binary. To convert a mixed number to binary, you must first separate the number into its whole and fractional parts. For instance, in the decimal number 16.25, the whole part (16) is converted to $10000_{(2)}$ by using the division method. Then, the fractional part is converted to $.01_{(2)}$ by using the multiplication method. The conversion is completed by adding together these two binary parts: $10000_{(2)} + .01_{(2)} = 10000.01_{(2)}$. The equivalent of $16.25_{(10)}$ is $10000.01_{(2)}$.

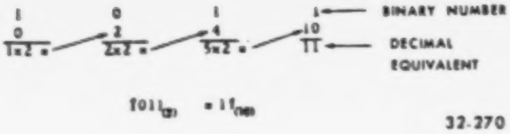


Figure 2-15. Double-dabble method binary-to-decimal conversion.

Exercises (010):

1. When converting decimal fractional numbers to binary fractional numbers, what method should you use and what number should you use as the multiplier?

2. How are mixed decimal numbers converted to their equivalent binary form?

3. Convert the following fractions and whole numbers to binary numbers:
   a. $.436_{(10)}$

   b. $.75_{(10)}$

   c. $23.125_{(10)}$

   d. $175.789_{(10)}$

   e. $69.963_{(10)}$

   f. $928.441_{(10)}$

011. Convert binary whole numbers to decimal whole numbers by the double-dabble method.

Binary-to-Decimal Conversion. For converting binary numbers to decimal form, there is again a choice of several methods. The two methods that we shall discuss, double-dabble (whole numbers) and addition (fractional numbers), are the methods that are most easily adapted to binary numbers of all sizes.

Double-dabble method (whole numbers). The double-dabble method, sometimes called synthetic division, is a repeated series of addition and multiplication steps. While studying the following six rules, refer to the example shown in figure 2-15.

(1) Add 0 to the MSB of the number that is to be converted.

(2) Multiply the sum (from rule 1) by the base of the number being converted.

(3) Add the product (from rule 2) to the next lower significant bit of the number.

(4) Multiply the sum (from rule 3) by the base.

(5) Add the product (from rule 4) to the next lower significant bit, and repeat the add-multiply progression until all bits except the LSB have been acted on.

(6) The final step is to add the product of the last multiplication step to the LSB. This sum will be the decimal equivalent of the number being converted.

To apply the double-dabble rules in a step-by-step process, let's convert the binary number 110100 to its decimal equivalent, as shown in figure 2-16.

Step 1. Add 0 to the MSB. This gives a sum of 1.

Step 2. Multiplying this sum (1) by 2 gives a product of 2.

Step 3. Adding the product (2) to the next lower significant bit (1), gives a sum of 3.

Step 4. Again we multiply the sum (3) by 2.

Step 5. The product (6) added to the next lower bit (0) gives a sum of 6.

Step 6. Continuing the process, we multiply 6 × 2.

Step 7. When we add the product (12) to the next lower significant bit (1), we derive a sum of 13.

Step 8. Multiplying 13 by 2 gives a product of 26.

Step 9. Adding the product (26) to 0 gives a sum of 26.

Step 10. Multiplying the sum (26) by 2 gives a product of 52. We have now operated on all bits except the LSB.

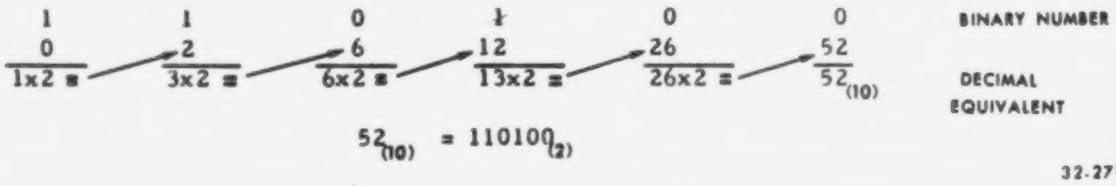


Figure 2-16. Example of binary-to-decimal conversion—whole numbers.

Step 11. According to rule 6, the last step will be to add the final product (52) to the LSB (0), which gives a sum of 52. This sum is the decimal equivalent of 110100_2.

Exercises (011):

1. Using the double-dabble method, convert the following binary numbers to decimals:
   a. $1101_{(2)}$

   b. $1000_{(2)}$

   c. $10111_{(2)}$

   d. $101100_{(2)}$

   e. $111111_{(2)}$

012. State a fundamental rule for converting mixed numbers, and convert binary whole and fractional numbers to decimal fractional numbers by the addition method.

Addition method (fractions). As you have seen, this method requires only that you add together the powers of the positions that are occupied by 1's in the binary number. The powers may be found by referring to figure 2-12. You might find that writing the binary number and indicating above each bit the position occupied by the bit will help to eliminate errors. As an example, we shall convert the binary fraction .10011 to decimal form by following the steps given below:

Position:	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}
Binary number:	1	0	0	1	1

Step 1. First write the binary number and indicate bit positions.

Step 2. From the table of powers of 2, we find that 2^{-1} has a power of .5.

Step 3. Again using the table, we find that 2^{-4} has a power of .0625.

Step 4. We find that 2^{-5} has a power of .03125.

Step 5. Now we add together the powers we have extracted from the table: $.5 + .0625 + .03125 = .59375$. Therefore, $.59375_{10} = .110011_2$. The conversion is now complete.

Exercises (012):

The exercises below will provide you with practice in converting binary whole and fractional numbers to decimal form. Remember, to convert the mixed numbers, treat each part (whole and fractional) separately; then add the results to complete the conversion.

1. When converting binary whole and fractional (mixed) numbers to decimal form, what must you do?

2. Convert the following binary numbers to their decimal form:
   a. $.110001_2$

   b. $.00011_2$

   c. 11.11010_2

   d. 1011.01000_2

2-3. Octal Numbering System

The octal numbering system is used in many computers to reduce the number of digits required to represent binary numbers. The conversion from binary to octal is easily accomplished and reduces the possibility of errors when you are working with large binary numbers.

013. State the chief difference between the decimal, binary, and octal number systems; and state key octal system characteristics.

Octal Numbering System. The computer uses the binary numbering system to do its calculations. The binary system has the disadvantage of requiring 3 to 4 times as many digits in a row to represent a number as does the decimal system. Chances for human error are much greater with an increase in the number of digits.

To reduce human errors, the octal numbering system is often used in digital computer input and output units. The octal system requires only one-third as many digits as the binary system. The octal system is more convenient than decimal for representing binary numbers, because it is very easy to convert from binary to octal and octal to binary.

The octal numbering system, sometimes called the octonary system, is similar to the decimal and binary system.

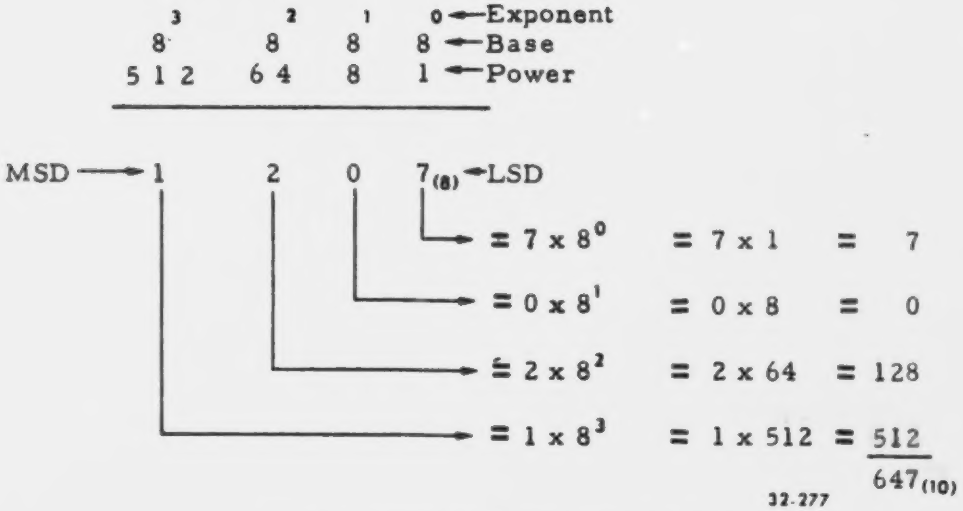


Figure 2-17. Example of octal whole number PLACE value.

Octal System Elements. The major difference between the octal system and the decimal and binary systems is the base. The octal system uses eight symbols (0, 1, 2, 3, 4, 5, 6, and 7) to represent numbers and is therefore, a base (radix) 8 system. An octal number is identified by a subscript (8). Octal numbers can be written in powers of 8. An exponent tells how many times to use 8 as a factor. Thus, $8 \times 8 \times 8 = 512$ may be written $8^3 = 512$. The value of a digit in an octal number is equal to the digit multiplied by the power of the PLACE it occupies. To illustrate, let's find the value in the decimal system of the number 1207_8, using the powers of 8, shown in figure 2-17. Figure 2-18 contains a more comprehensive table of powers of 8.

Exercises (013):

1. What is the difference between the octal number system and the binary and decimal number system?

8^n	n	8^{-n}
1	0	1.0
8	1	0.125
64	2	0.015 625
512	3	0.001 953 125
4 096	4	0.000 244 140 625
32 768	5	0.000 030 517 578 125
262 144	6	0.000 003 814 697 265 625
2 097 152	7	0.000 000 476 837 158 203 125
16 777 216	8	0.000 000 059 604 644 775 390 625

34-297

Figure 2-18. Powers of 8.

0	1	2	3	4	5	6	7
1	2	3	4	5	6	7	10
2	3	4	5	6	7	10	11
3	4	5	6	7	10	11	12
4	5	6	7	10	11	12	13
5	6	7	10	11	12	13	14
6	7	10	11	12	13	14	15
7	10	11	12	13	14	15	16

NDA13-36

Figure 2-19. Octal addition matrix.

2. The base or radix of the octal number system is ________ .

3. What is the value of a digit in an octal number?

014. Solve octal mathematical operations using addition and subtraction.

Octal addition. Octal addition also uses the sum-and-carry technique. A carry to the next higher order column is produced each time a sum equals or exceeds the radix.

The main point to remember is that there are only eight octal symbols, 0-7. Thus, 7 + 1 = 10, 17 + 1 = 20, 27 + 1 = 30, etc. Until you form a habit of thinking in octal, the matrix in figure 2-19 will help you in adding and subtracting octal numbers.

The matrix functions like this for addition:

(1) Locate one number on the left margin.

(2) Locate the other number on the top margin.

(3) Project a line from both numbers until the lines intersect.

(4) The number at the intersection is the sum of the two numbers.

Example: A line from 4 on the left and 5 on the top intersect at 11; the sum of 4 + 5 = 11.

Octal addition examples:

$$(1)\ \begin{array}{r} 7 \\ \underline{1} \\ 10 \end{array} \qquad (2)\ \begin{array}{r} 5 \\ \underline{3} \\ 10 \end{array} \qquad (3)\ \begin{array}{r} 6 \\ \underline{4} \\ 12 \end{array} \qquad (4)\ \begin{array}{r} 7 \\ \underline{6} \\ 15 \end{array} \qquad (5)\ \begin{array}{r} 2 \\ \underline{7} \\ 11 \end{array}$$

$$(6)\ \begin{array}{r} 7654 \\ \underline{1426} \\ 11302 \end{array} \qquad (7)\ \begin{array}{r} 1234567 \\ \underline{7273747} \\ 10530536 \end{array}$$

Octal subtraction. Octal subtraction is performed in much the same manner as decimal and binary subtraction. When a borrow is necessary in any number system, its value is equal to the radix of that system. The borrow is then added to the minuend digit of that particular column and the subtrahend is subtracted. For example, subtract $45_{(8)}$ from $54_{(8)}$.

$$\begin{array}{lrrl} \text{Borrow: } 8 + 4 \longrightarrow & & & \\ & 4 & 12 & \\ & 5 & 4 & \text{minuend} \\ & \underline{-4} & \underline{5} & \text{subtrahend} \\ & & 7 & \end{array}$$

$$\text{Proof: } \begin{array}{r} 45_{(8)} \\ \underline{+\ 7_{(8)}} \\ 54_{(8)} \end{array}$$

Another example of octal subtraction using three digits is shown in the following example: Subtract $565_{(8)}$ from $704_{(8)}$.

$$\begin{array}{rrrl} & 7 & & \\ 6 & 8 & 12 & \\ 7 & 0 & 4 & _{(8)} \\ \underline{-\ 5} & \underline{6} & \underline{5} & _{(8)} \\ 1 & 1 & 7 & _{(8)} \end{array}$$

Borrow one from the 7 (MSD of $704_{(8)}$). Then borrow one from column two's minuend. Thus, the minuend becomes: 6 7 $12_{(8)}$.

The answer $117_{(8)}$ is now apparent.

The matrix in figure 2-19 is used in this manner for subtraction:

(1) Locate subtrahend on left margin.

(2) Project a line into the matrix to the minuend.

(3) Turn 90° and come out to the top margin.

(4) The number at the exit point is the difference between the two numbers.

Use figure 2-19 as you study the following example: 14 − 5 = 7. Locate 5 on the left margin, project in to 14, and project upward to 7 on the top margin.

Octal subtraction examples:

$$(1)\ \begin{array}{r} 7 \\ \underline{-4} \\ 3 \end{array} \qquad (2)\ \begin{array}{r} 5 \\ \underline{-2} \\ 3 \end{array} \qquad (3)\ \begin{array}{r} 10 \\ \underline{-2} \\ 6 \end{array} \qquad (4)\ \begin{array}{r} 100 \\ \underline{-76} \\ 02 \end{array} \qquad (5)\ \begin{array}{r} 5432 \\ \underline{-3254} \\ 2156 \end{array}$$

$$(6)\ \begin{array}{r} 7776 \\ \underline{-6777} \\ 777 \end{array} \qquad (7)\ \begin{array}{r} 76543210 \\ \underline{-01234567} \\ 75306421 \end{array}$$

Complements Method. Subtraction using complements and end-around carry may also be applied to the octal numbering system. In the octal numbering system, the radix complement is sometimes called the 8's complement, and the radix − 1 complement is referred to as the 7's complement. Let's take a step-by-step look at this method. Suppose you wish to subtract $3452_{(8)}$ from $4761_{(8)}$. You would first complement the subtrahend.

Largest symbol	7777	
Subtract	3452	
Radix − 1 comp	4325	
Add 1 to LSD	1	
Radix comp	4326	
Add minuend	4761	
	11307	**discard the end carry = 1307**

You can accomplish the same thing by adding the radix − 1 complement and using end-around carry. In this case, the end carry is brought around and added to the LSD of the answer. Using the same numbers, you have:

Minuend	4761	4761	
Subtract	−3452	+4325	←add radix − 1 complement
		①1306	
		1	←add end carry to LSD
		1307	

Exercises (014):

1. For each of the following terms identify the portion of the number $703_{(8)}$ to which each term is related. Write the letter of the correct term on the line drawn to the right of the number.
   a. Radix or base.
   b. Least significant digit.
   c. Most significant digit.
   d. Placeholder.

7_______

0_______

3_______

(8)_______

2. For each of the following terms identify the portion of the number $405.1_{(8)}$ to which each term is related. Write the letter of the correct term on the line drawn to the right of the number.
   a. MSD.
   b. LSD.
   c. Placeholder.
   d. Radix or base.
   e. Octal point.

4_______

0_______

0_______

._______

1_______

(8)_______

3. Add:

a. $54_{(8)}$
$45_{(8)}$

b. $367_{(8)}$
$455_{(8)}$

c. $4577_{(8)}$
$3211_{(8)}$

4. Subtract:

a. $63_{(8)}$
$34_{(8)}$

b. $523_{(8)}$
$434_{(8)}$

c. $5327_{(8)}$
$1456_{(8)}$

d. $4513.72_{(8)}$
$1372.36_{(8)}$

e. $537.01_{(8)}$
$426.10_{(8)}$

f. $3.1416_{(8)}$
$1.5710_{(8)}$

g. $1.37765_{(8)}$
$.24313_{(8)}$

5. Perform the indicated subtractions by complements and end-around carry. Show your work.

a. $643_{(8)}$
$-452_{(8)}$

b. $756_{(8)}$
$-654_{(8)}$

c. $\begin{array}{r} 6741_{(8)} \\ \underline{-0777_{(8)}} \end{array}$

015. Convert decimal numbers to octal and octal to decimal, and convert octal numbers to binary and binary to octal.

Decimal-to-Octal Conversion. You use the multiplication-division method to convert from a decimal number to an octal number. The same rules apply as in converting decimal to binary, except you use 8 instead of 2.

This method of conversion has two parts, treating the integral and fractional parts of the number separately. The integral portion uses a dividing process, and the fractional portion uses a multiplying process. We will work with whole numbers only.

To convert the integral portion of the decimal number to octal, follow these rules:

(1) Divide the integral number by 8.

(2) Write the remainder of the first division as the LSD of the octal number.

(3) Divide the quotient of the first division by 8, and use the remainder or zero as the next digit of the octal number.

(4) Continue division by 8 until the quotient is zero.

(5) Write the remainder as the digits of the octal number, and the MSD is generated last.

Problem: Convert $3844_{(10)}$ to its octal equivalent.

Decimal Number	*divided by*	*Octal Radix*	=	*Quotient*	+	*Remainder (Octal Digit)*
3844	divided by	8	=	480	+	4 LSD
480	divided by	8	=	60	+	0
60	divided by	8	=	7	+	4
7	divided by	8	=	0	+	7 MSD
$3844_{(10)}$			=	$7404_{(8)}$		

Let's work one more problem: Convert $204_{(10)}$ to its octal equivalent.

Decimal Number	*divided by*	*Octal Radix*	=	*Quotient*	+	*Remainder (Octal Digit)*
204	divided by	8	=	25	+	4 LSD
25	divided by	8	=	3	+	1
3	divided by	8	=	0	+	3 MSD
$204_{(10)}$			=	$314_{(8)}$		

Octal-to-Decimal Conversion. Accomplish octal-to-decimal conversion in the following manner. Convert the octal number $227_{(8)}$ to a decimal number. Use figure 2-17 for octal place values.

$$\begin{aligned} 227_{(8)} &= (2 \times 8^2) + (2 \times 8^1) + (7 \times 8^0) \\ &= (2 \times 64) + (2 \times 8) + (7 \times 1) \\ &= 128 + 16 + 7 \\ &= 151_{(10)} \end{aligned}$$

Another method which may be used to convert a number of any base to a decimal number is synthetic division. Convert the integral portion of the octal number to a decimal using the following rules.

(1) Multiply the MSD by the radix (8 for octal).

(2) Add the product to the next lower digit of the number being converted.

(3) Multiply the sum of the two numbers in rule 2 by the radix.

(4) Repeat rules 2 and 3 for all digits of the number being converted except the LSD. For the LSD, repeat only rule 2.

(5) The final sum is the converted number. For example: Convert $234_{(8)}$ to decimal; the underlined number is the converted result.

$$\begin{array}{lrrr} \text{MSD} & 2 & 3 & 4 \\ & & 16 & 152 \\ \hline & & 19 & \enclose{circle}{156} \end{array}$$

$$234_{(8)} = \underline{156_{(10)}}$$

Octal-to-Binary Conversion. A requirement often exists for octal-to-binary conversion. The substitution method of conversion takes advantage of a natural relationship between octal and binary numbers. The base of the octal system is 8; the base of the binary system is 2, and 2^3 equals 8. One octal digit may be expressed by three binary digits (bits); for example count to 7 in each system.

Octal No.	*Binary No.*	*Octal No.*	*Binary No.*
0	000	4	100
1	001	5	101
2	010	6	110
3	011	7	111

Convert an octal number to its binary equivalent by direct substitution. Replace each octal digit by its corresponding three binary digits. By substitution, for example, the number $23_{(8)}$ equals 010 $011_{(2)}$. For another example, convert $56{,}473_{(8)}$ to binary.

$$\begin{array}{cccccc} 5 & 6 & 4 & 7 & 3 & (8) \\ \wedge & \wedge & \wedge & \wedge & \wedge & \\ 101 & 110 & 100 & 111 & 011 & (2) \end{array}$$

In the last example, the groupings are separated to call attention to the equivalence. In actual practice, there is no spacing between groups. To check for equivalence, convert both the binary and octal numbers to decimal numbers. Both equal $23{,}867_{(10)}$.

Binary-to-Octal Conversion. Binary-to-octal conversion also uses substitution. To make this conversion, arrange the binary digits in groups of three, proceeding to the left and to the right from the binary point. Fill out the extreme left or right group with zeros if necessary. Then directly substitute for each binary group its octal digit equivalent. For example, convert $11100_{(2)}$ to an octal number.

$$\begin{array}{lcc} 11100 = & 011 & 100 \\ & \vee & \vee \\ & 3 & 4 \end{array}$$

$11100_{(2)} = 34_{(8)}$

Exercises (015):

1. Convert $38_{(10)}$ to its equivalent octal value.

2. Convert $122_{(10)}$ to its equivalent octal value.

3. Convert $2143_{(10)}$ to its equivalent octal value.

4. Convert $347_{(8)}$ to its equivalent binary and decimal value.

5. Convert $573_{(8)}$ to its equivalent binary and decimal value.

6. Convert $2135_{(8)}$ to its equivalent binary and decimal value.

7. Convert $1011_{(2)}$ to its octal equivalent.

8. Convert $1101_{(2)}$ to its octal equivalent.

2-4. Hexadecimal Numbering System

Like the octal numbering system, the hexadecimal system reduces the number of binary bits used to represent a decimal number. This system requires only one-fourth as many digits as the binary system, making it very common for use in microprocessors.

016. State the chief advantage, general features, and writing method of the hexadecimal number system.

The Hexadecimal System. The big disadvantage of the binary number system is that it requires three to

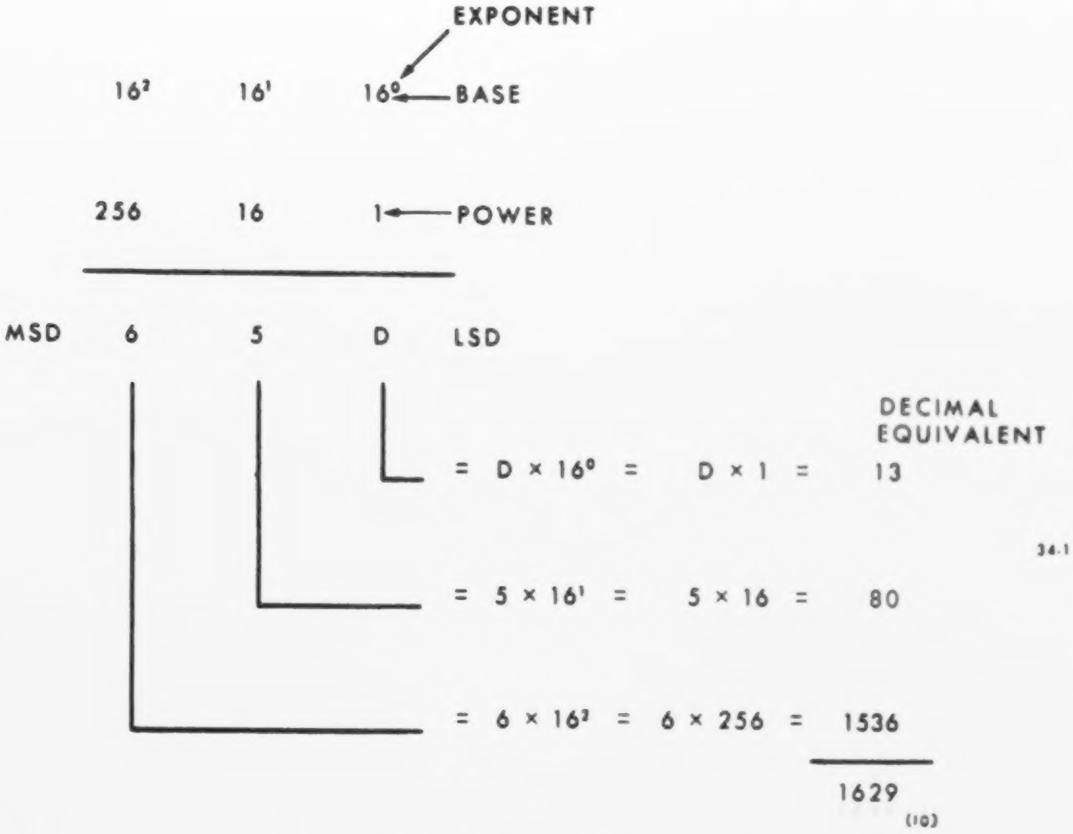

EXPONENT
16^2 16^1 16^0
BASE
256 16 1
POWER
MSD 6 5 D LSD
DECIMAL EQUIVALENT
$= D \times 16^0 = D \times 1 = 13$
$= 5 \times 16^1 = 5 \times 16 = 80$
$= 6 \times 16^2 = 6 \times 256 = 1536$
$1629_{(10)}$
34.1

Figure 2-20. Hexadecimal whole number PLACE value.

four times as many bits to represent a numerical value as does the decimal system. The large number of 1's and 0's make it hard to handle. Also, the chance of error is much greater than when one number or letter is used to represent a group of 4 binary bits.

To reduce errors, the hexadecimal (HEX) number system is used in some digital computers. Binary bits are divided into groups of fours. They are divided into groups in both directions from the binary point (radix point). The HEX (radix) point is used to divide the whole numbers from the fractions.

The HEX system is more convenient than the decimal system, since it represents the binary numbers in a more compact way. It requires only one-fourth as many digits as does the binary system. HEX numbers and letters, which represent binary bits, are used externally by the computer programmer. All computations are performed internally by the computer use of binary bits.

The hexadecimal system is similar to decimal, binary, and octal systems of numbers. The major difference between this system and the other three is the radix (base). Radix of the HEX system is 16. Therefore, the system uses 16 symbols (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F) to represent numbers.

The HEX count starts at zero (0) and goes to nine (9), just as in the decimal system. However, the number 10 in decimal is an "A" in HEX. In other words, decimals 10 through 15 are represented by "A" through "F" in the HEX system. Operational progress from one column to another column is the same as in the decimal system. But keep in mind that you are working with a radix of 16, not a radix of 10.

When writing a hexadecimal number, you use a slightly different method. When writing the number in octal, you used the base of 8 as the subscript; and likewise, when writing decimal or binary numbers, you also used the base of the number system as a subscript. Hexadecimal numbers are preceded by the symbol X', with a prime mark after the HEX characters. Let us write a number in HEX. AF94 base 16 is written X'AF94'. AF94 is the number, and the X' signifies that it is a base 16 number. Sometimes the subscript 16 is also used, so you must be familiar with both systems of notation.

The HEX number system, like all others, is a system of digit magnitude and position. Each position in a number represents a different power of the base. The position to the left of the radix point is the zero position. The base is raised to the zero power for this

16^n	n	16^{-n}					
1	0	0.10000	00000	00000	00000	x	10
16	1	0.62500	00000	00000	00000	x	10^{-1}
256	2	0.39062	50000	00000	00000	x	10^{-2}
4 096	3	0.24414	06250	00000	00000	x	10^{-3}
65 536	4	0.15258	78906	25000	00000	x	10^{-4}
1 048 576	5	0.95367	43164	06250	00000	x	10^{-6}
16 777 216	6	0.59604	64477	53906	25000	x	10^{-7}
268 435 456	7	0.37252	90298	46191	40625	x	10^{-8}
4 294 967 296	8	0.23283	06436	53869	62891	x	10^{-9}
68 719 476 736	9	0.14551	91522	83668	51807	x	10^{-10}
1 099 511 627 776	10	0.90949	47017	72928	23792	x	10^{-12}
17 592 186 044 416	11	0.56843	41886	08080	14870	x	10^{-13}
281 474 976 710 656	12	0.35527	13678	80050	09294	x	10^{-14}
4 503 599 627 370 496	13	0.22204	46049	25031	30808	x	10^{-15}
72 057 594 037 927 936	14	0.13877	78780	78144	56755	x	10^{-16}
152 921 504 606 846 976	15	0.86736	17379	88403	54721	x	10^{-18}

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Figure 2-21. Powers of 16 expressed as decimal numbers.

10^n	n	10^{-n}		
1	0	1.0000 0000 0000 0000		
A	1	0.1999 9999 9999 999A		
64	2	0.28F5 C28F 5C28 F5C3	×	16^{-1}
3E8	3	0.4189 374B C6A7 EF9E	×	16^{-2}
2710	4	0.68DB 8BAC 710C B296	×	16^{-3}
1 86A0	5	0.A7C5 AC47 1B47 8423	×	16^{-4}
F 4240	6	0.10C6 F7A0 B5ED 8D37	×	16^{-4}
98 9680	7	0.1AD7 F29A BCAF 4858	×	16^{-5}
5F5 E100	8	0.2AF3 1DC4 6118 73BF	×	16^{-6}
3B9A CA00	9	0.44B8 2FA0 9B5A 52CC	×	16^{-7}
2 540B E400	10	0.6DF3 7F67 5EF6 EADF	×	16^{-8}
17 4876 E800	11	0.AFEB FF0B CB24 AAFF	×	16^{-9}
E8 D4A5 1000	12	0.1197 9981 2DEA 1119	×	16^{-9}
918 4E72 A000	13	0.1C25 C268 4976 81C2	×	16^{-10}
5AF3 107A 4000	14	0.2D09 370D 4257 3604	×	16^{-11}
3 8D7E A4C6 8000	15	0.480E BE7B 9D58 566D	×	16^{-12}
23 8652 6FC1 0000	16	0.734A CA5F 6226 F0AE	×	16^{-13}
163 4578 5D8A 0000	17	0.B877 AA32 36A4 B449	×	16^{-14}
DE0 B6B3 A764 0000	18	0.1272 5DD1 D243 ABA1	×	16^{-14}
8AC7 2304 89E8 0000	19	0.1D83 C94F B6D2 AC35	×	16^{-15}

34-302

Figure 2-22. Powers of 10 in hexadecimal notation.

position. The powers increase by 1 for each succeeding position to the left and decrease by 1 for each succeeding position to the right. A number in this system may be written in powers of 16. Figure 2-20 illustrates the value in the decimal system of the HEX number X'65D', using the power 16. Figures 2-21 and 2-22 contain a more comprehensive table of powers 16 and 10.

Exercises (016):

1. What is the big advantage of the hexadecimal number system as compared to the decimal, binary, and octal number systems?

2. Describe the characteristics of the hexadecimal number systems.

3. What method is used for writing hexadecimal numbers to signify that they are hexadecimal?

017. Convert decimal numbers to their hexadecimal (HEX) equivalents and "HEX" numbers to their decimal equivalents.

Decimal-to-Hexadecimal Conversion Rule. The appropriate method for converting from decimal to hexadecimal is by DIVIDING SUCCESSIVELY BY THE BASE of the HEX number system. This procedure has been explained before in this unit. To convert a decimal whole number into its hexadecimal equivalent, divide successively by 16 and record the remainder in each case. Continue this process until the original number is reduced to 0. The first recorded remainder is the LSD, and the last remainder is the MSD of the hexadecimal number equivalent.

Example: Convert $942_{(10)}$ to its HEX equivalent.

Step 1.

$$\begin{array}{r} \underline{58} \\ 16/942 \\ \underline{80} \\ 142 \\ \underline{128} \\ 14 \end{array}$$

= remainder = E = LSD of answer

Step 2.

$$16\overline{)58}\quad \text{quotient } 3$$
$$\begin{array}{r} 58 \\ \underline{48} \\ 10 \end{array}$$

10 = remainder = A = middle digit

Step 3.

$$16\overline{)3}\quad \text{quotient } 0$$
$$\begin{array}{r} 3 \\ \underline{0} \\ 3 \end{array}$$

3 = remainder and is the MSD of the HEX number

NOTE: 3 is the quotient from step 2; 3 cannot be divided by 16 and give a quotient that is a whole number. Therefore, 3 is the remainder of step 3, and becomes the MSD.

Answer: $942_{(10)}$ is equal to $3AE_{(16)}$

Summary of decimal-to-hexadecimal (HEX) conversion:

(1) For decimal whole number to HEX conversion, the procedure is to divide the decimal number by 16.

(2) The first recorded remainder is the LSD of the HEX number.

(3) Continue the procedure until the original number equals 0.

(4) The last recorded remainder is the MSD of the HEX equivalent.

Hexadecimal-to-Decimal Conversion. Conversion of HEX numbers to equivalent decimal numbers is accomplished by either of the following methods:

(1) Assigning weight to digit position.

(2) Synthetic division.

These two methods should be very familiar, because they were used in converting binary and octal numbers to their decimal equivalent.

In the hexadecimal numbering system, each digit to the left of the HEX point is worth 16 times the value of the digit to its right. Weights can be assigned to all digit positions as follows:

16^4	16^3	16^2	16^1	16^0	.	16^{-1}	16^{-2}
65536	4096	256	16	1	.	1/16	1/256

Rules:

(1) Place HEX digits under the appropriate weights.

(2) If any parts of the HEX number are alpha characters, place their decimal equivalent in parentheses under the alpha character.

(3) Place the decimal equivalent of the HEX power under the digit or character of the HEX number to be converted.

(4) Multiply each positional value separately.

(5) Add the products.

(6) The resultant sum is the decimal equivalent of the hexadecimal number.

Example: Convert $FA2_{(16)}$ to its decimal equivalent.

Step 1.	256 16 1	List the weight of the bit positions.
Step 2.	F A 2	Place the HEX number under the weight positions.
Step 3.	(15) (10)	Place the decimal equivalent in parentheses under each alpha character.
Step 4.	256 × 15 = 3840 16 × 10 = 160 1 × 2 = 2 Decimal answer = 4002	Multiply the HEX digit or decimal equivalent times the weight position of that digit. Add up the products of each position.

Summary: Assigning weight to bit positions.

(1) Each bit to the left of the HEX point is worth 16 times the value of the bit to its right.

(2) Assign weights to all bit positions as follows: 65536, 4096, 256, 16, 1.

(3) To convert from HEX to decimal, place the bits under the appropriate weights.

(4) Then multiply the digit times the weight.

(5) Add the products.

(6) The resultant sum is the decimal equivalent of the HEX number.

Synthetic Division (Double Dabble) Method. The synthetic division method of converting hexadecimal to decimal is the result of repeated multiplication and addition. It is exactly the same as previously discussed for binary to decimal and octal to decimal. For whole numbers, the multiplier for hexadecimal is 16^1 or 16, and the addition is to add the digit in the next lower place value to the product obtained in the multiplication step.

Rules:

(1) If any parts of the HEX number are alpha characters, place their decimal equivalent in parentheses under the alpha character.

(2) Multiply the MSD by 16.

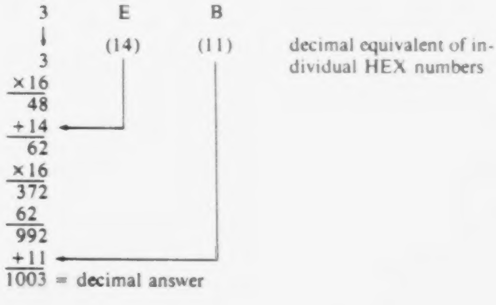
(3) Add the product obtained by rule 2 to the decimal equivalent of the next lower digit.

(4) Multiply the sum obtained in step 3 by 16.

(5) Repeat the process of adding and multiplying with all digits EXCEPT THE LSD.

(6) The final step is to add the LSD to the last product. This results in the decimal equivalent of the HEX number.

Example: Convert HEX 3EB to decimal using synthetic division.



Exercises (017):

1. Convert the decimal numbers in a. and b. to their HEX equivalents.
   a. 934.

   b. 2716.

2. Convert the HEX numbers in a. through d. to their decimal equivalents.
   a. 7CD.

   b. FA2.

   c. FAB.

   d. BCE.

018. State relationships between binary and hexadecimal systems, and convert binary numbers to hexadecimal and hexadecimal numbers to binary numbers.

Binary-Hexadecimal-Binary Conversion. The best and simplest way to convert binary numbers to HEX form, and HEX numbers to binary form, is by the inspection method. A number in any number system whose radix is a power of 2 can be directly converted to its equivalent value in another system, whose radix is also a power of 2. Because 16 equals 2^4, HEX digits can be represented by 4 binary bits representing the 2^0, 2^1, 2^2, and 2^3 positions.

Therefore, when you convert from a binary number to HEX, separate the binary bits into groups of fours, starting at the radix point, and convert each 4-bit group into its hexadecimal equivalent. (See fig. 2-23,A.)

When converting from a HEX number to a binary number, you separate the HEX digits and replace each digit with 4 binary bits. Arrange them so that their value is equal to the HEX digit. Figure 2-23,B, shows how this method works.

Exercises (018):

1. What is the relationship between hexadecimal and binary number systems?

2. Convert the following binary numbers to their hexadecimal equivalent form:
   a. $011011110011_{(2)}$

   b. $111100000101_{(2)}$

   c. $1110.00111100_{(2)}$

   d. $11101101101011_{(2)}$

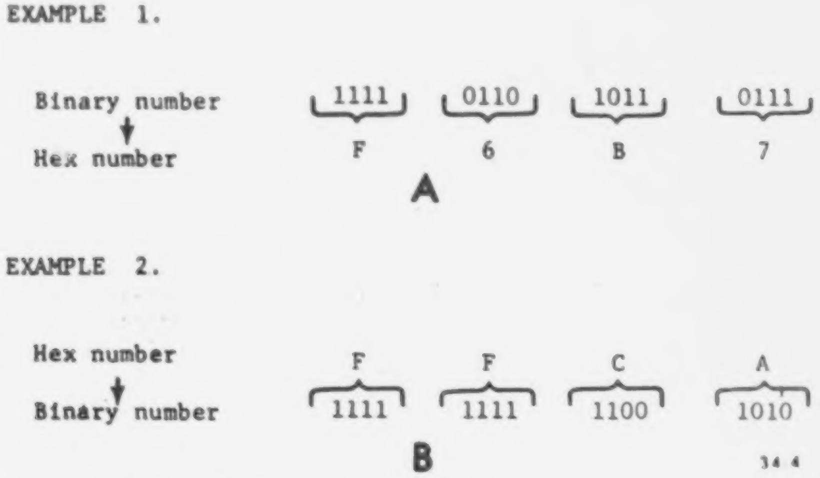


Figure 2-23. Binary-to-hexadecimal and hexadecimal-to-binary conversion.

e. $11010100_{(2)}$

f. $101010101010_{(2)}$

3. Convert the following hexadecimal numbers to their equivalent binary number form:
   a. $54D_{(16)}$
   b. $F6B7_{(16)}$
   c. $AB.CD_{(16)}$
   d. $ACD43_{(16)}$
   e. $BE728_{(16)}$
   f. $A4CD0_{(16)}$

019. Perform hexadecimal addition and subtraction.

Hexadecimal Addition. You have learned from adding binary and octal numbers that the basic rules of addition are the same, no matter which base you are working with; hexadecimal is no different. Until you can remember the decimal equivalents of the alpha numbers in the hexadecimal system, it might be helpful to jot them down on the scratch paper you are working on. A = 10 . . . F = 15. To add hexadecimal numbers, use the sum-and-carry method, generating a carry whenever the radix is exceeded in a column.

Rules:

(1) Add the LSD column as in decimal addition.

(2) Divide the column total by the radix of the hexadecimal system (16).

(3) Enter the QUOTIENT of the division as a carry to the next higher column.

(4) Enter the REMAINDER of the division as the sum of the column just added.

(5) Repeat rules 1 through 4 for each higher column until addition is complete.

Example: Add the following hexadecimal numbers:

$$\begin{array}{ccc} 8 & A & C \\ 2 & B & 5 \\ F & 7 & 4 \\ D & 6 & E \end{array}$$

A = 10
B = 11
C = 12
D = 13
E = 14
F = 15

Step 1. First column added decimally is: 12 + 5 + 4 + 14 = 35.

$$\begin{array}{rl} 2 & \text{carry to second column} \\ 16\overline{)35} & \\ \underline{32} & \\ 3 & \text{LSD of answer} \end{array}$$

Step 2. Second column added decimally is: 2 (carry from last column) + 10 + 11 + 7 + 6 = 36.

$$\begin{array}{rl} 2 & \text{carry to third column} \\ 16\overline{)36} & \\ \underline{32} & \\ 4 & \text{second digit to answer} \end{array}$$

Step 3. Third column added decimally: 2 (carry from last column) + 8 + 2 + 15 + 13 = 40.

$$\begin{array}{rl} 2 & \text{carry to 4th column—MSD of answer} \\ 16\overline{)40} & \\ \underline{32} & \\ 8 & \text{third digit of answer} \end{array}$$

Final sum is $2843_{(16)}$

Hexadecimal Subtraction. You have learned three methods of subtraction with numbering systems and have noted that the basic rules of subtraction remain the same regardless of which base you are working with. The three methods are:

(1) Direct method (subtract and borrow).
(2) End-around carry method.
(3) Base complement method.

Direct method. This is the subtract and borrow routine. When a borrow is necessary, its value is equal to the radix of the base of the system, in this case, 16.

Rules:

(1) Beginning with the LSD column, subtract the subtrahend digit from the minuend digit, if the minuend digit is equal to or larger than the subtrahend digit.

(2) If the minuend digit is smaller, borrow the BASE from the first higher column which contains a significant digit. Reduce the value of the digit you borrowed from by one.

(3) Decimally add the radix (16) to the minuend digit already in the column.

(4) Decimally subtract the subtrahend digit from the adjusted minuend digit.

(5) Repeat rules 1 through 4 for each higher column until subtraction is complete.

Example:

$$\begin{array}{rccc} & A & D & 2 \\ - & 9 & 3 & E \\ \hline \end{array}$$

Step. 1. Subtract E from 2. This cannot be done until the radix has been borrowed from the next higher place value digit. Borrow 1 from D, leaving it a C. Add 16 to the 2, making the new minuend 18. Subtract E from 18, leaving 4.

$$\begin{array}{rccrl} & & C & 18 & \\ & A & D & 2 & \\ - & 9 & 3 & E & \\ \cline{1-4} & & & 4 & \text{difference after first digit has been subtracted} \end{array}$$

Step 2. Decimally subtract 3 from C.

$$\begin{array}{rccrl} & & C & 18 & \\ & A & D & 2 & \\ - & 9 & 3 & E & \\ \cline{1-4} & & 9 & 4 & \text{difference after second digit has been subtracted} \end{array}$$

Step 3. Decimally subtract 9 from A.

$$\begin{array}{rccrl} & & C & 18 & \\ & A & D & 2 & \\ - & 9 & 3 & E & \\ \cline{1-4} & 1 & 9 & 4 & \text{final difference—hexadecimal answer} \end{array}$$

End-around carry method. Fifteen's complement works for hexadecimal the same way the 1's complement works for binary and the 7's complement works for octal. The subtrahend is 15's complemented and added to the minuend with end-around carry.

To obtain the 15's complement of a number, subtract each digit in the number being complemented from the highest symbol in the hexadecimal system (F).

Example:

$$\begin{array}{rcccccl} & F & F & F & F & F & \\ - & A & 3 & F & 6 & 2 & \\ \cline{1-6} & 5 & C & 0 & 9 & D & \text{15's complement of A 3 F 6 2} \end{array}$$

Now that the procedure for 15's complementing a number is understood, we will discuss the method of subtraction using this. The following rules should be followed. (Note that they are the same rules for end-around carry using 7's complement and 1's complement. Only the radix has changed.)

Rules:

(1) If the subtrahend contains fewer digits than the minuend, fill the subtrahend columns with zeros.

(2) Obtain the 15's complement of the subtrahend.

(3) Hexadecimally add the complemented subtrahend to the minuend.

(4) If the end-around carry bit is a 1 (example 1), perform the end-around carry and you obtain the final result. If the end-around carry bit is a 0 (example 2), this means the subtrahend was larger than the minuend and you must perform rule 5.

(5) When the end-around carry bit is a 0, RECOMPLEMENT the number, using 15's complement. This is a NEGATIVE result and must have a minus sign preceding it. This complemented answer with a minus sign in front of it is the final result.

Example 1:

Step 1. Original subtraction problem:

$$\begin{array}{rccccccl} & 5 & A & E & 9 & F & 1 & \text{minuend} \\ - & & 8 & B & 2 & E & 4 & \text{subtrahend} \\ \cline{1-7} \end{array}$$

Step 2. Adding:

$$\begin{array}{rccccccl} & 5 & A & E & 9 & F & 1 & \text{minuend} \\ & F & 7 & 4 & D & 1 & B & \text{subtrahend} \\ \cline{2-7} \text{End-around carry bit } 1 & 5 & 2 & 4 & 7 & 0 & C & \end{array}$$

NOTE: Remember to add hexadecimally.

Step 3. Perform an end-around carry with the end-around carry bit and add.

$$\begin{array}{lccccccl} \textcircled{1} & 5 & 2 & 3 & 7 & 0 & C & \text{result in step 2} \\ \multicolumn{5}{l}{\longrightarrow} & & + \; 1 & \text{end-around carry bit} \\ \cline{2-7} & 5 & 2 & 3 & 7 & 0 & D & \text{final result in hexadecimal} \end{array}$$

The end-around carry bit was a 1, so the final result has been obtained.

Example 2:

Step 1. Original subtraction problem:

$$\begin{array}{rccccc} & 3 & 2 & B & 0 & 9 \\ - & C & F & B & 7 & D \\ \cline{1-6} \end{array}$$

Step 2.

$$\begin{array}{rcccccl} & 3 & 2 & B & 0 & 9 & \\ + & 3 & 0 & 4 & 8 & 2 & \text{15's complement of subtrahend} \\ \cline{2-6} \text{End-around carry bit } 0 & 6 & 2 & F & 8 & B & \text{sum} \end{array}$$

When the MSD column was added, there was no carry bit generated. This makes the end-around carry bit a 0. The sum obtained in the addition must be recomplemented using 15's complement and a minus sign placed in front of the final result to indicate that the answer is negative.

Step 3.

$$\begin{array}{rcccccl} & 6 & 2 & F & 8 & B & \text{sum in step 2} \\ & 9 & D & 0 & 7 & 4 & \text{15's complement} \\ \cline{2-6} - & 9 & D & 0 & 7 & 4 & \end{array}$$

Base complement method. Subtraction using the 16's complement works the same way the 2's complement and the 8's complement work.

Rules:

(1) Find the 16's complement of the subtrahend.

(2) Add the minuend to the complemented subtrahend.

(3) If the overflow bit is 1, the answer is positive (example 1). Eliminate the overflow bit, and the final result has been obtained. If the overflow bit is 0 (example 2), perform rule 4. The term "overflow" as used here is the bit that is carried after adding the MSD of the hexadecimal problem. In other words, it is the same bit we used as the end-around carry bit when we worked with the 15's complement.

(4) If the overflow bit is a 0 (no carry from the MSD column):

(a) Find the 16's complement for the answer.

(b) Place a minus sign in front of the recomplemented answer, and the final result has been obtained. This is a negative answer.

Example 1:

Step 1. Original subtraction problem:

```
   E B 8 0 A   minuend
 -   2 D 4 A   subtrahend
```

Include zeros in subtrahend to size of minuend.

Step 2. Adding:

```
   E B 8 0 A   minuend
 + F 0 2 B 6   16's complemented
               subtrahend
 ___________
 1 E 8 A C 6
Overflow bit
```

Step 3. Since the overflow bit is 1, the final result has been obtained when the overflow bit is eliminated. $E8AC0_{(16)}$ final result.

Example 2:

Step 1. Original problem:

```
   A 2 7 C 1   minuend
 - D E 3 9 B   subtrahend
```

Step 2. Adding:

```
   A 2 7 C 1   minuend
 + 2 1 C 6 5   16's complemented
 0 C 4 4 2 6     subtrahend
Overflow bit understood
```

Step 3. Since the overflow bit is 0, recomplement the sum obtained and place a minus sign in front of it.

```
   C 4 4 2 6   sum from step 2
   3 B B D 9   15's complement
         + 1
 ___________
 - 3 B B D A(16)  final result
```

Exercises (019):

1. Perform HEX addition, as indicated, on exercises a and b.

a. 1F2B
3CEF
2594

b. 2F9A
8EBC
ABCD
FADE

2. Perform HEX subtraction, as indicated, on exercises a, b, and c.

a. FBB
−032

b. ACD
−ABF

c. 5AE9F1
−08B2E4

2-5. Number Coding System

You should be familiar with number coding systems used in particular computer systems. This section describes the binary coded decimal, Excess-three code and Gray code systems.

020. Convert decimal numbers to their binary coded decimal (BCD) equivalents and BCD numbers to their decimal equivalents.

Binary Coded Decimal (BCD). It is possible to group symbols to get a workable system such as the binary coded decimal (8421) system. This system derives its name from the fact that the symbols 8, 4, 2, and 1 are the first four PLACE values of the digits in a four-digit binary number. Instead of a true conversion to binary, this system codes each of the 10 Arabic numerals into a four-digit binary code as follows:

Decimal Number	*Binary Coded Decimal*	*Binary Number*
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
6	0110	0110
7	0111	0111
8	1000	1000
9	1001	1001
10	0001 0000	1010
15	0001 0101	1111
18	0001 1000	10010

The chart shows that BCD and binary ARE NOT THE SAME. BCD will never go above 1001, decimal 9, in a group of four binary digits. BCD cannot be converted to binary in the same manner as binary to octal or hexadecimal, because BCD and binary are not the same. That is, $00\ 100\ 101_{(2)}$ is not equal to $0010\ 0101_{(BCD)}$. However, decimal can be converted directly to BCD and BCD directly to decimal.

Decimal-to-BCD conversion. To convert decimal to BCD, start at the fractional point and work out. Write out the 8421 for each decimal digit as an aid.

Example: Convert 970.31 decimal to BCD.

Step 1. Write down the 8421 code for each decimal digit. Treat each decimal bit separately.

9	7	0	3	1	Decimal number
8421	8421	8421	8421	8421	BCD bit position weights

Step 2. Treat each 8421 as the first 4 bits in the assigning weights to bit position method of decimal-to-binary conversion. Treat each decimal bit separately and convert it to BCD, always using 4 bits in each BCD code.

9	7	0	3	1	Decimal number
8421	8421	8421	8421	8421	BCD bit position weights
1001	0111	0000	0011	0001	BCD number

Therefore, 1001 0111 0000.0011 0001 BCD is equal to 970.31 decimal.

BCD-to-decimal conversion. To convert from BCD to decimal, remember that each BCD group can only go from 0 through 9 decimal. BCD-to-decimal conversion is just the reverse of the process of converting from decimal to BCD. Each group of 4 bits is weighted the same as the first four positions in the assigned weight to bit positions in the binary system. One use of the BCD system is to convert from computer language to keyboard printout. In this system, each decimal digit is coded separately to a binary form. It *must* be understood that the decimal number is not converted to the binary form. *While the 8421 code is commonly used, it is apparent that an infinite number of special codes are possible.* In order to interpret these special codes, you must know the system being used.

Example: Convert 101 0100 0111 0000 1 BCD to decimal.

Step 1. Separate binary bits into groups of 4-bits, beginning at the fractional point. Add zeros as necessary to the fractional LSD and whole number MSD sides to make each group 4 bits.

0101 0100 0111 0000 1000

Step 2. Assign the weights of the binary weight table to each group of bits. Add the position weights for each group. The result is the decimal equivalent of the BCD number.

8421	8421	8421	8421	8421	
0101	0100	0111	0000	1000	
5	4	7	0	8	Decimal equivalent of BCD number

Exercises (020):

1. Convert the decimal numbers in exercises a and b to their BCD equivalents.
   a. 1753.68.

   b. 1590.

2. Convert the BCD numbers in exercises a and b to their decimal equivalents.
   a. 111 1000 0101. 0100 011.

   b. 0111 1001 1000 0010.

021. Specify the formation and disadvantage of the Excess-three code; and convert decimal numbers to Excess-three code, and vice versa.

Excess-Three Code. This code is formed simply by adding 3 to each decimal digit and then substituting a group of 4 binary bits for each digit of the resultant decimal number, just as in the 8, 4, 2, 1 code. For example, to form the Excess-three code of the decimal number 6, first add 3 to 6, yielding 9. Then as in the 8, 4, 2, 1 code, substitute 4 binary bits for the 9:

$$\begin{array}{r} 6 \\ +3 \\ \hline 9 \end{array}$$

$$9_{(10)} = 1001_{(2)}$$

	4	2	$6_{(10)}$	
Plus	3	3	3	
Equals	7	5	9	
Equals	0111	0101	1001	excess-three code
Complementing equals	1000	1010	0110	
Equals	8	10	6	
Minus	3	3	3	
Equals	5	7	3	= 9s complement of $426_{(10)}$ 34-296

Figure 2-24. Excess-three code.

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Therefore, $6_{(10)} = 1001_{(2)}$ in the Excess-three code.

To convert an Excess-three coded number back to decimal form, merely substitute the proper decimal digit for each group of 4 binary bits and then subtract 3 from each digit.

Let's take the decimal number 426; from the Excess-three code equivalent; complement the code; and convert back to decimal to see whether we derive the 9's complement of 426. Refer to figure 2-24.

You have seen how the Excess-three code compensates for the disadvantage of the 8, 4, 2, 1 code. Both of these codes, however, share a characteristic that is inconvenient in certain circumstances. This undesirable trait is that, in changing the count represented by 4 binary bits, more than 1 bit can change value at the same time. For instance, in increasing a count from 0000 to 0001, only the LSB changed. But in changing from 0001 to 0010, both the LSB and the next bit changed. Again, "necessity being the mother of invention," a code was developed to compensate for this drawback. Complete the following exercises and then we'll take a look at the Gray code.

Exercises (021):

1. How is the Excess-three code formed?

2. Convert the following decimal numbers to their Excess-three code equivalents:
   a. 37.
   b. 249.
   c. 112.
   d. 873.
   e. 1102.
   f. 614.

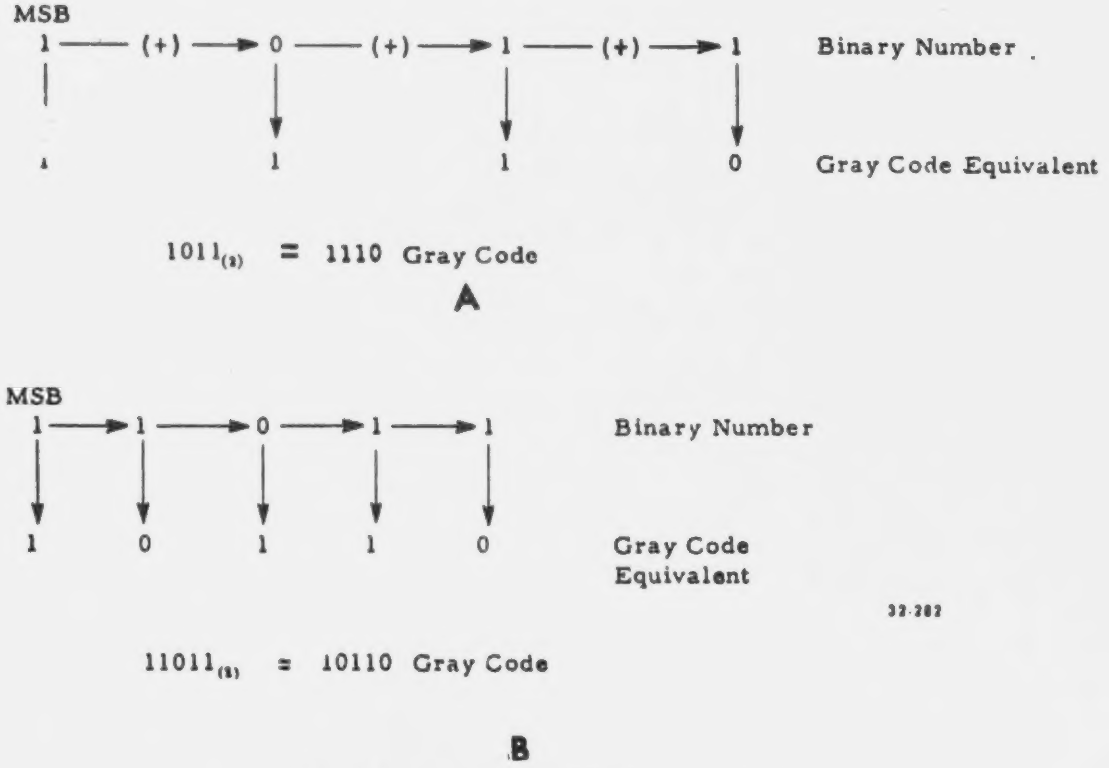
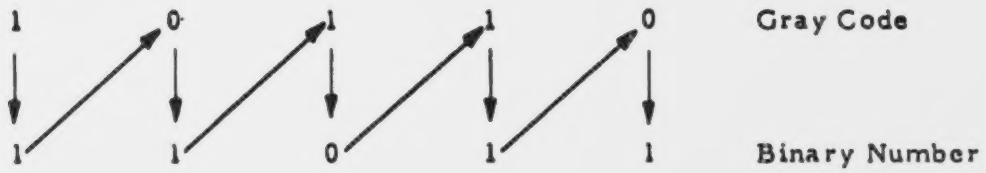

MSB
1 (+) 0 (+) 1 (+) 1
Binary Number
1 1 1 0
Gray Code Equivalent
1011(2) = 1110 Gray Code
A
MSB
1 1 0 1 1
Binary Number
1 0 1 1 0
Gray Code Equivalent
32-282
11011(2) = 10110 Gray Code
B

Figure 2-25. Examples of binary-to-Gray code conversion.



33-203

10110 Gray Code = $11011_{(2)}$

Figure 2-26. Gray code to binary conversion.

3. Convert the following Excess-three codes to their equivalent decimal numbers:
   a. 11000110.
   b. 11000110.
   c. 101011001010.
   d. 100000110101.
   e. 1011010010010011.
   f. 11000100100101101011.

4. What undesirable trait does the Excess-three code, along with the 8, 4, 2, 1 code, have?

022. State the main characteristics of the Gray code; and convert binary numbers to Gray code numbers, and vice-versa.

The Gray Code. The Gray code is known as a cyclic code. A cyclic code has the unique characteristic that only 1 bit changes value when proceeding from one number to the next successive number. This trait is used to advantage in counters and analog-to-digital conversion units in some computers.

Converting binary numbers to Gray code. Binary numbers can be converted to Gray code by applying the following three rules. (The examples in fig. 2-25 illustrate the use of these rules.)

(1) Make the MSB of the binary number the MSB of the Gray code.

(2) Add the binary bits, laterally, from left to right, two at a time. Drop all carries.

(3) Make the sum of each 2 bits a bit in the Gray code equivalent.

Converting Gray code to binary numbers. Figure 2-26 shows examples of converting a Gray coded number to its binary form. The following three rules are used to perform this conversion:

(1) Make the MSB of the Gray code the MSB of the binary number.

(2) Add the second Gray code bit to the first binary bit (MSB); the sum becomes the next binary bit. Drop any carry.

(3) Continue adding successive Gray code bits to the preceding binary bits until each Gray code bit has been added to a binary bit. The sum of the last addition is the LSB of the binary number.

Exercises (022):

1. The Gray code is known as a ______ code.

2. What is the unique characteristic of this type (exercise 1, above) code?

3. Convert the following binary numbers to Gray code:
   a. 110101101.
   b. 1100010.
   c. 111001.
   d. 10000001.

4. Convert the following Gray code numbers to binary form:
   a. 1101101.
   b. 101011.
   c. 111100.
   d. 1010111.

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Answers for Exercises

CHAPTER 1

Reference:

001 - 1. Analog; digital.
001 - 2. Analog.
001 - 3. Digital.

002 - 1. 2000 B.C.
002 - 2. Abacus.
002 - 3. Pascal.
002 - 4. Leibnitz.
002 - 5. Punched card.
002 - 6. Analytical engine.
002 - 7. Hollerith.
002 - 8. General-purpose.
002 - 9. Vacuum tubes.
002 - 10. Solid-state electronics.

003 - 1. (1) e.
(2) d.
(3) c.
(4) c and e.
(5) b.
(6) a.
(7) a.

004 - 1. Data processing; scientific.
004 - 2. Both.
004 - 3. a. Data processing: accounting, dispatching, inventory, etc.
b. Scientific: engineering, physics, biology, etc.

CHAPTER 2

005 - 1. 2 5 3 2

$$\begin{array}{lr} 2 + 10^0 = 2 \times 1 = & 2 \\ 3 \times 10^1 = 3 \times 10 = & 30 \\ 5 \times 10^2 = 5 \times 100 = & 500 \\ 2 = 10^3 = 2 \times 1000 = & \underline{2000} \\ & 2532_{(10)} \end{array}$$

005 - 2. 7 c.
0 d.
6 a.
. e.
4 b.

005 - 3. 5 b.
0 c.
9 a.
(10) d.

005 - 4. 10 is called the base, 1000 is called the power, and 3 is called the exponent.

005 - 5. The product of the base used as a factor a number of times equal to the exponent.
005 - 6. The 6 is the MSD and the 8 is the LSD.
005 - 7. The 6 is the MSD and the 8 is the LSD.

006 - 1. The binary number system, like the decimal, uses zero as a PLACEHOLDER and the PLACE value method of representing numbers. The binary system uses powers of 2 and the base, or radix, of the binary number system is 2.
006 - 2. The power doubles.
006 - 3. The power is halved.

007 - 1.
1—1
2—10
3—11
4—100
5—101
6—110
7—111
8—1000
9—1001
10—1010
11—1011
12—1100
13—1101
14—1110
15—1111
16—10000
17—10001
18—10010
19—10011
20—10100

007 - 2. a. 10001111.
b. 100101.
c. 10000100.
007 - 3. a. 101010.
b. 10110.
c. 110110.
007 - 4. a. 1011101.
b. 110111.
c. 11101110.
007 - 5. a. 111.1.
b. 1000.
c. 1101.

008 - 1. a.

$$\begin{array}{rcr} 110\ 001_{(2)} & = & 110\ 011 \\ \underline{-011\ 111}_{(2)} & 11 & \underline{+100\ 000} \\ & 1 & 010\ 011 \\ & & \underline{1} \\ & & 010\ 100 \end{array}$$

b.

$$\begin{array}{rcr} 111\ 101_{(2)} & = & 111\ 101 \\ \underline{-100\ 000}_{(2)} & & \underline{+011\ 111} \\ & 1 & 011\ 100 \\ & & \underline{1} \\ & & 011\ 101 \end{array}$$

c.

$$\begin{array}{rcr} 100\ 000_{(2)} & = & 100\ 000 \\ \underline{-011\ 000}_{(2)} & & \underline{+100\ 111} \\ & 1 & 000\ 111 \\ & & \underline{1} \\ & & 001\ 000 \end{array}$$

009 - 1. Divide by 2. The first remainder 1 or 0 becomes the LSD of the binary number. Continue to divide by 2 until the final quotient is 0.

009 - 2. 2.

009 - 3. a. 1001100.
b. 11010100.
c. 111111.
d. 10101.
e. 10110000001.
f. 1101010111.

010 - 1. The multiplication method; 2.

010 - 2. By first treating them as two different numbers (whole number to the left of the decimal point and fractional number to the right of the decimal point), and then combining the two binary numbers together.

010 - 3. a. 0.011011.
b. 0.11.
c. 10111.001.
d. 10101111.110010.
e. 1000101.111101.
f. 1110100000.011100.

011 - 1. a. 13.
b. 8.
c. 23.
d. 44.
e. 63.

012 - 1. Treat each part (whole and fractional) separately; then add the results to complete the conversion.

012 - 2. a. 0.765625.
b. 0.09375.
c. 3.8125.
d. 11.25.

013 - 1. The base.

013 - 2. 8.

013 - 3. The digit multiplied by the power of the PLACE it occupies.

014 - 1. 7 c.
0 d.
3 b.
(8) a.

014 - 2. 4 a.
0 c.
0 c.
e.
1 b.
(8) d.

014 - 3. a. $121_{(8)}$
b. $1044_{(8)}$
c. $10010_{(8)}$

014 - 4. a. $27_{(8)}$
b. $67_{(8)}$
c. $3651_{(8)}$
d. $3121.34_{(8)}$
e. $110.71_{(8)}$
f. $1.3506_{(8)}$
g. $1.13452_{(8)}$

014 - 5. a.

$$\begin{array}{rcr} 643_{(8)} & = & 643 \\ \underline{-452_{(8)}} & & \underline{+325} \\ & 1 & 170 \\ & & \underline{1} \\ & & 171 \end{array}$$

b.

$$\begin{array}{rcr} 756_{(8)} & = & 756 \\ \underline{-654_{(8)}} & & \underline{+123} \\ & 1 & 101 \\ & & \underline{1} \\ & & 102 \end{array}$$

a.

$$\begin{array}{rcr} 6741_{(8)} & = & 6741 \\ \underline{-0777_{(8)}} & & \underline{+7000} \\ & 1 & 5741 \\ & & \underline{1} \\ & & 5742 \end{array}$$

015 - 1. 38 divided by 8 = 4 R 6 LSD
4 divided by 8 = 0 R 4 MSD
$38_{(10)} = 46_{(8)}$

015 - 2. 122 divided by 8 = 15 R 2 LSD
15 divided by 8 = 1 R 7
1 divided by 8 = 0 R 1 MSD
$122_{(10)} = 172_{(8)}$

015 - 3. 2143 divided by 8 = 267 R 7 LSD
267 divided by 8 = 33 R 3
33 divided by 8 = 4 R 1
4 divided by 8 = 0 R 4 MSD
$2143_{(10)} = 4137_{(8)}$

015 - 4. $347_{(8)} = 231_{(10)} = 11\ 100\ 111_{(2)}$

015 - 5. $573_{(8)} = 379_{(10)} = 101\ 111\ 011_{(2)}$

015 - 6. $2135_{(8)} = 1117_{(10)} = 10\ 001\ 011\ 101_{(2)}$

015 - 7. $1011_{(2)} = 13_{(8)}$

015 - 8. $1101_{(2)} = 15_{(8)}$

016 - 1. It requires fewer digits than the other systems.

016 - 2. The hexadecimal number system has a radix, or base, of 16. The system uses 16 symbols (0 through 9, and A through F) to represent numbers.

016 - 3. Hexadecimal numbers are preceded by the symbol X, with a prime mark (') after the HEX characters.

017 - 1. a. 3A6.
b. A9C.

017 - 2. a. 1997.
b. 4002.
c. 4011.
d. 3022.

018 - 1. Both the hexadecimal and the binary number systems use the power of 2 or a multiple of the power of 2.

018 - 2. a. X'6F3'
b. X'F05'
c. X'E.3C'
d. X'3B6B'
e. X'D4'
f. X'AAA'

018 - 3. a. $010101001101_{(2)}$
b. $1111011010110111_{(2)}$
c. $10101011.11001101_{(2)}$
d. $10101100110101000011_{(2)}$
e. $10111111001110010100O_{(2)}$
f. $10100100110011010000_{(2)}$

019 - 1. a. 80AE.
b. 28391.

019 - 2. a. F89.
b. 10E.
c. 52370D.

020 - 1. a. 10111 0101 0011.0110 1.
b. 10101 1001 0000.

020 - 2. a. 785.46.
b. 7982.

021 - 1. By adding 3 to each decimal digit and then substituting a group of 4 binary bits for each digit of the resultant decimal number.

021 - 2. a. 01101010.
b. 010101111100.
c. 010001000101.
d. 101110100110.
e. 0100010000110101.
f. 100101000111.

021 - 3. a. 67.
b. 93.
c. 797.
d. 502.
e. 8160.
f. 91638.

021 - 4. In changing the count represented by 4 binary bits, more than 1 bit can change value at the same time.

022 - 1. Cyclic.

022 - 2. Only 1 bit changes value in proceeding from one number to the next successive number.

022 - 3. a. 101111011.
b. 1010011.
c. 100101.
d. 11000001.

022 - 4. a. 1001001.
b. 110010.
c. 101000.
d. 1100101.

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DIGITAL TECHNIQUES

Unit 2

Digital Logic and Boolean Algebra

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Preface

IN THE DIGITAL electronics arena, the electronic switch is the basic element of all logic circuits. The electronic switch, or gate, opens or closes only when it has a logical (or correct) combination of inputs. We can define this combination of inputs and the resultant output using Boolean algebra.

This module describes the different kinds of logic gates used to make binary decisions. We will deal with both the discrete and integrated circuit forms of digital logic gates. We'll then use Boolean algebra to explain how a given circuit output is derived.

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Figure No.	*Title*
1-81.	Hex inverter buffers/drivers with open-collector high-voltage outputs.
1-82.	SN54H04, SN74H04 hex inverters.
1-83.	SN7402 quadruple two-input positive NOR-gates.
1-84.	SN54H30, SN74H30 eight-input positive NAND-gates.
1-85.	SN5426, SN7426 quadruple two-input high-voltage interface NAND-gates.
1-86.	Quadruple two-input positive NAND buffer.
1-87.	SN5486, SN7486 quadruple two-input EXCLUSIVE OR-gates.

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CHAPTER 1

NOTE: In this unit, the subject matter is developed by a series of student-centered objectives. Each of these carries a three—digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see whether your answers match those in the back of this volume. If your response to an exercise is incorrect, review the objective and its text.

Digital Logic and Boolean Algebra

DIGITAL LOGIC refers to the electonic circuits that use voltage or current levels to represent a 1 or 0 in the binary number system. We'll describe the discrete circuits that make up a logic gate and show the logic symbol which represents that gate. The use of logic symbols, instead of repetitious circuit schematics, enables us to trace or troubleshoot logic circuits much easier.

The mechanization of more complex circuits, including flip-flops, will be covered in a later module. Only the more basic circuits are considered in this module, and, in order to simplify explanation of their operation, ideal operating conditions are assumed. That is, circuit losses due to such factors as inductance, capacitance, resistance, and transit time are ignored. Also, signal excursions are, in most cases, assumed to start at 0 volts and go either positive or negative. Thus, the waveforms actually appearing in theses circuits will, due to circuit losses, be distorted versions of the idealized waveforms. For signal excursions, the voltage used to represent the various logic levels (both positive and negative) will be determined primarily by circuit design.

1-1. Discrete Digital Logic

The inputs and outputs of logic circuits consist of voltage or current values which are two-state. This means we're dealing with two finite values that represent the binary 1 or 0. If we use a high (H) level of voltage to represent a binary 1 and a low (L) value to represent binary 0, we are using *positive logic.* If we use a low (L) value of voltage as a binary 1 and a high (H) level of voltage as a binary 0, we are using *negative logic.* For example, if +5 volts is binary 1 and 0 volt is binary 0, then we are using positive logic. On the other hand, if binary 0 is set at +12 volts and binary 1 is set at −12 volts, then we are using negative logic.

There are basically two kinds of circuit elements used to implement digital circuits. These are the gates, that provide an output from a logical combination of inputs and the sequential circuits that provide a storage or memory function. When gates are connected together to perform some mathematical or logical function necessary to process digital data, the circuitry is called *combinational logic.* The digital circuits used to implement storage or memory functions are called *sequential logic.* Individual gates and their symbols are important because they are the building blocks for combinational and sequential logic circuits used in digital electronics applications.

001. Construct truth tables, draw circuits, identify logic symbols, and determine correct inputs and outputs for resistor-diode logic AND- and OR-gates.

RDL Gates. A logic gate is a switch. The output of this switch is determined by the logic designer. A switch (gate) opens or closes depending on whether or not its input requirements are met. A way to do this in the case of AND- and OR-gates is to use a simple network of diodes with a load resistor. This resistor-diode logic (RDL) is useful for explaining how basic AND- and OR-gates work.

OR logic. One of the common logic operations is the alternative or choice called the OR function. This comes into play whenever any one of two or more alternate possibilities can bring about a specified result.

The symbol in figure 1-1 represents the OR function. The symbol indicates that OR is the relationship between its "inputs," which are, of course, the arrival of George, Pete, or Joe. Another way of

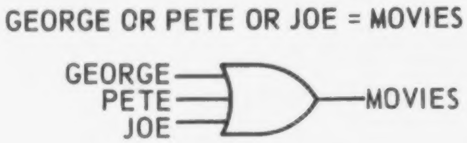


Figure 1-1. OR function.

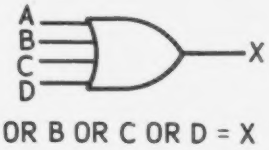


Figure 1-2. Four-input OR function.

thinking of it (more accurate when dealing with equipment) is that the symbol applies the OR function to its inputs. The circuit produces an "output" only when the inputs meet the OR requirements; in other words, when at least one of the inputs appears. Figure 1-1 can be altered, as in figure 1-2, to illustrate the general case—any OR situation. Four inputs are shown (A, B, C, and D) although any number of inputs other than one is possible (one input offers no alternative, hence no OR).

The OR function produces a specified result, X, when any one of its input conditions (A or B, or C or D) is satisfied. Notice that if any one, two, three, or even all of the inputs appear together, the output X is still produced. The OR in this case includes all combinations as well as one-at-a-time inputs, so it is called an inclusive OR. In digital logic circuits, the OR function is always "inclusive" unless otherwise specified.

RDL OR-circuit. The RDL OR-circuit consists of two or more diodes connected in the manner shown in figure 1-3. The load resistor is connected to a negative potential. The presence of information is represented by a high, while the absence of information is represented by a low.

Figure 1-4 shows waveforms of the OR-circuit. At time T0 to T1, all diodes are cut off and the output is low (−6V). At time T1 to T2, CR1 (fig. 1-4,A) conducts and the output goes high (OV). At time T2 to T3, CR1 cuts off but CR2 (fig. 1-4,B) conducts, so the output remains high. From T3 to T4, CR3 (fig. 1-4,C) conducts and the output is high. All inputs must be low to have a low output; one or more diodes conducting make a high output.

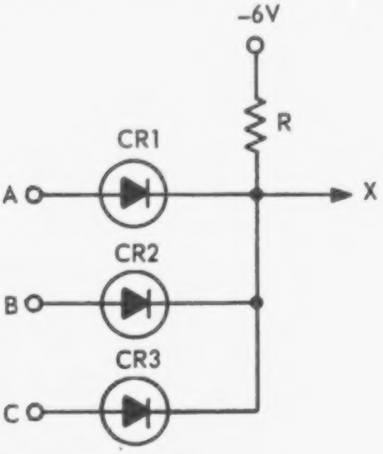


Figure 1-3. Diode OR-circuit.

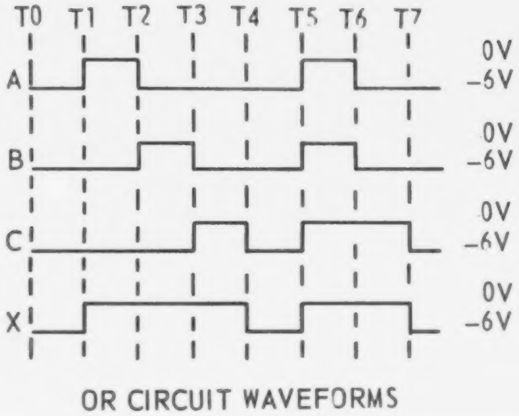


Figure 1-4. OR-circuit waveforms.

Figure 1-5 shows a two-diode OR-circuit. With one diode anode at 0 volt (high) and the other diode anode at −6 volt (low), the output is high (OV). Assume no voltage drop across conducting CR1. The output is clamped to 0 volt. This clamping action causes a zero potential to be felt on the cathode of CR2. Thus, the cathode of CR2 is positive with respect to its anode, causing CR2 to be reverse biased, and the diode will not conduct. This operation occurs when one input is high and the other is low; the output is high. If both inputs are at 0 (high), then both diodes will conduct and the output is high, as can be seen in figure 1-6.

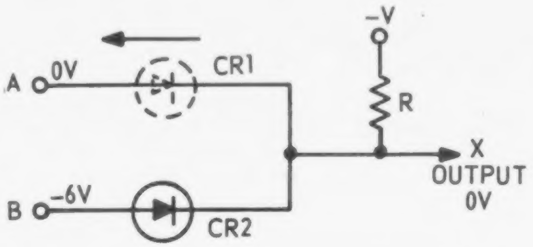


Figure 1-5. OR-circuit with two-inputs high.

Figure 1-7 is the truth table which relates all of the important features of the OR-gate. In this truth table,

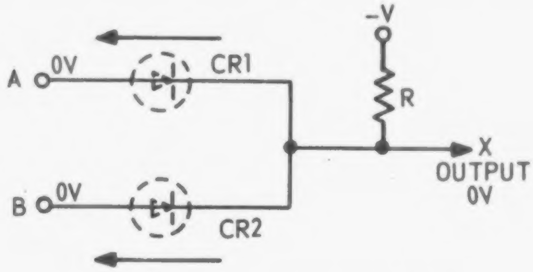
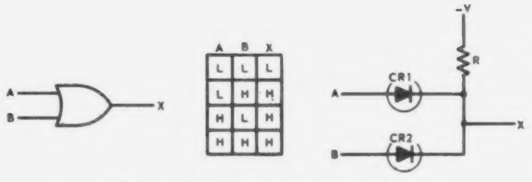


Figure 1-6. OR-circuit with two-inputs high.



A	B	X
L	L	L
L	H	H
H	L	H
H	H	H

Figure 1-7. OR-gate and truth table.

the low (L) represents 0 volt. Verify the truth table which indicates the following:

- All inputs low give a low output.
- Any one input high gives a high output.
- All inputs high give a high output.

The important feature to remember from figure 1-7 is that any, or all, high (H) inputs will produce a high (H) output.

RDL AND logic. The opposite of the OR situation is the AND-gate. It requires that all inputs be present in order to obtain the specified output. The symbol in figure 1-8 represents the AND function. The symbol indicates that AND is the relationship between its "inputs" which are the combination of pigment, lead, and linseed oil. Another way of thinking of it more accurately, when dealing with equipment, is that the symbol applies the AND function to its inputs. The circuit produces an "output" only when the inputs meet the AND requirements; in other words, when all of the inputs appear at the same time.

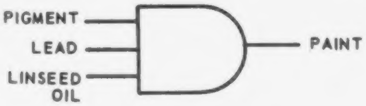
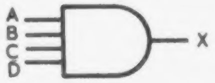


Figure 1-8. AND situation.



A AND B AND C AND D = X

Figure 1-9. Four-input AND situation.

Figure 1-8 can be altered, as in figure 1-9, to illustrate the general case for any AND situation. Four inputs are shown (A, B, C, and D) although any number of inputs are possible.

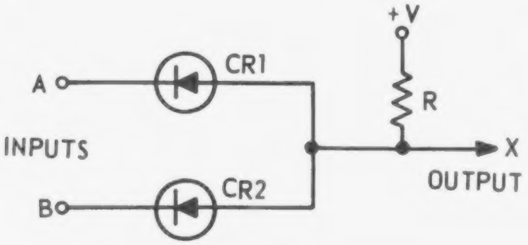


Figure 1-10. Diode AND circuitry.

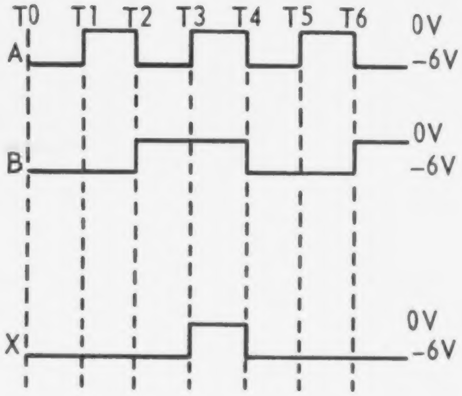


Figure 1-11. AND-gate waveforms.

Diode AND-circuit. Circuits that perform the AND function are called AND-gates. AND-gates may use diodes as shown in figure 1-10. The circuit has one output, at which a pulse appears if, and only if, pulses are applied simultaneously to BOTH inputs. If the inputs are not of the same time duration, the output will appear only during the time interval that the input pulses overlap. When both diodes have a high input, the output is "high." When either diode has a low input or if both diodes have low inputs, the output is "low." A low output is considered NO output and represents binary 0.

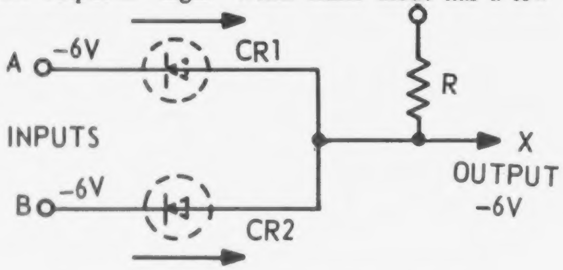


Figure 1-12. AND-gate with both diodes conducting.

Time T0 to T1 in figure 1-11 shows a −6 volts being applied to both diode inputs. Both diodes are conducting heavily and the output is −6 volts (low). Figure 1-12 shows the equivalent circuit with the

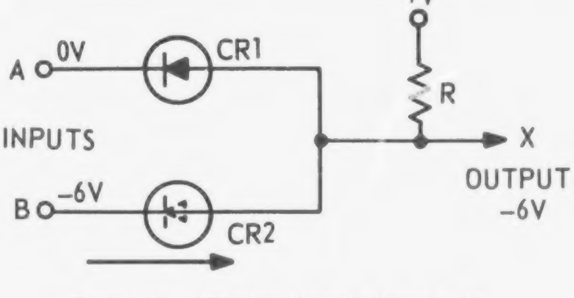
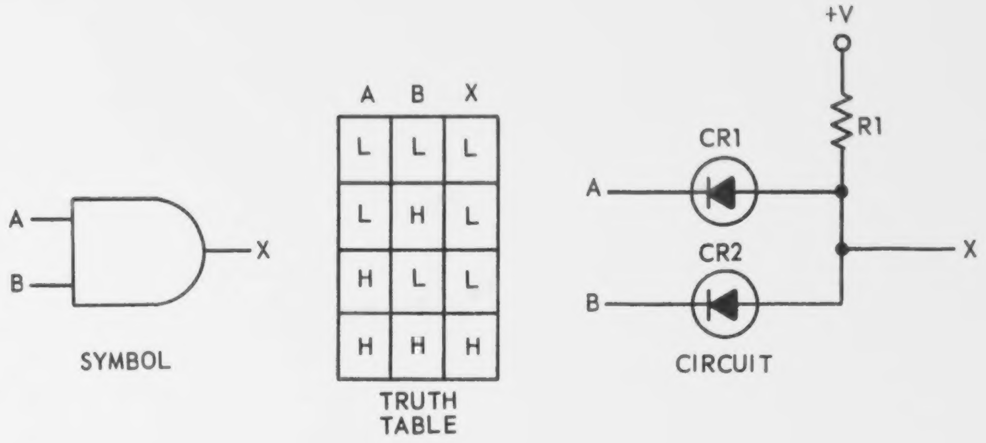


Figure 1-13. AND-gate with one diode conducting.



A	B	X
L	L	L
L	H	L
H	L	L
H	H	H

Figure 1-14. AND-gate with truth table.

diodes shorted. Times T1 and T2, figure 1-11, show one input at 0 volt (high) and the other at −6 volts (low). CR2 is forward biased and conducts heavily, clamping the output and the anode of CR1 to −6 volts. CR1 is reverse biased and does not conduct.. Figure 1-13 shows the equivalent circuit with CR2 shorted. The −6 volt (low) output is identified as no output.

In the explanation of AND-circuits, the logic levels are the numeric values of the high or low outputs. If the outputs are 0V and −6V, 0 volt represents a high and −6 volts represents a low. The most positive value is high and the most negative value is low. The high represents binary 1, and low represents binary 0.

A truth table shows all the possible input conditions and the output of each case. Figure 1-14 is a truth table which relates all the important features of AND-gates. In this truth table, the low (L) represents −6 volts and the high (H) represents 0 volt. Compare each line of the truth table with specific conditions as follows:

(1) In figure 1-12 when both diodes have a −6V input (L), the output is −6V (L).

(2) Figure 1-13 shows either diode input −6 volts (L) with the other diode input 0 volt (H); the output is −6 volts (L).

(3) Figure 1-15 shows 0 volt (H) on both diodes; this is the AND condition which provides an output (H).

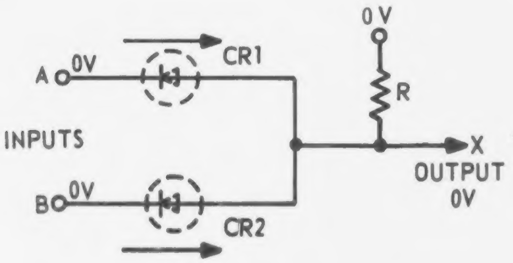


Figure 1-15. Satisfied "AND."

The important feature to remember about an AND-gate (fig. 1-14) is that all inputs must be high (H) before the output (X) will be high.

Exercises (001):
Use figure 1-16 to answer questions 1 and 2.

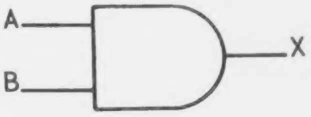


Figure 1-16. Figure for objective 001, exercises 1 and 2.

1. Write the correct output (X) for the gate if A is low and B is high.

2. Write the correct ouput (X) for the gate when A is high and B is high.

3. Draw the correct diode circuitry for the logic symbol in figure 1-17.

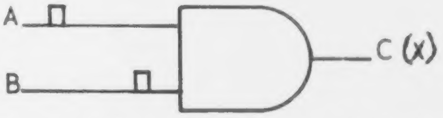
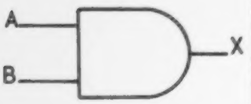


Figure 1-17. Figure for objective 001, exercises 3 and 4.

4. The AND-gate shown in figure 1-17 will have an output at C when the inputs to A and B are as shown (observe pulse timing). (True/False)

5. Construct the truth table for the logic symbol shown in figure 1-18.



A	B	X

Figure 1-18. Figure for objective 001, exercise 5.

6. Write the correct output (C) for the gate in figure 1-19 when A is low and B is high.

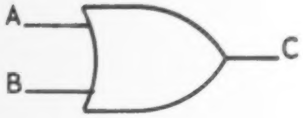


Figure 1-19. Figure for objective 001, exercise 6.

7. Write the correct output (X) for the gate shown in figure 1-20 when A is high and B is low.

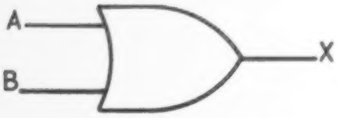


Figure 1-20. Figure for objective 001, exercise 7.

8. Write the correct output (Z) for the gate shown in figure 1-21 when X is high and Y is high.

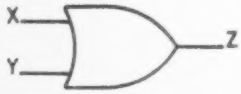


Figure 1-21. Figure for objective 001, exercise 8.

9. Draw the correct diode circuitry for the logic symbol shown in figure 1-22.

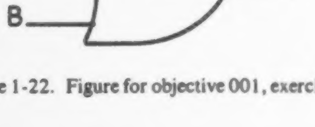


Figure 1-22. Figure for objective 001, exercise 9.

10. The OR-gate will have an output at C when the inputs to A and B (pulse inputs) are shown in figure 1-23. (True/False).

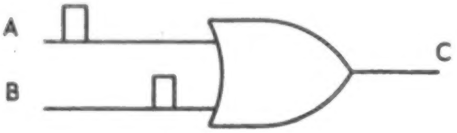
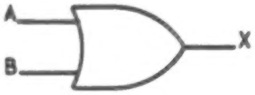


Figure 1-23. Figure for objective 001, exercise 10.

11. Construct the truth table for the logic symbol shown in figure 1-24.



A	B	X

Figure 1-24. Figure for objective 001, exercise 11.

002. State the characteristics of NOT, exclusive OR, and negative logic; determine inhibit, NAND- and NOR-gate inputs/outputs; construct truth tables and circuits for these gates.

NOT Logic. Another logic operation of importance is the NOT function, which denotes an alternate or converse value. It is also known as *inversion.* When inverted, every high becomes a low. Similarly, a low that is inverted becomes a high. A line drawn over a signal designator indicates a NOT function. NOT A is written as $\overline{A}$. If A equals a 1, the $\overline{A}$ equals a 0. If A equals 0, the $\overline{A}$ equals a 1. An inverting amplifier can be used to obtain a NOT function. The logic symbols for such an amplifier are shown in figure 1-25. The symbol for an amplifier is the triangle; the small circle represents inversion; without the circle, the amplifier has no inversion.

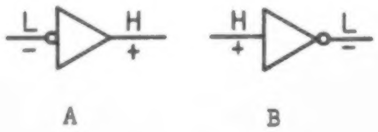
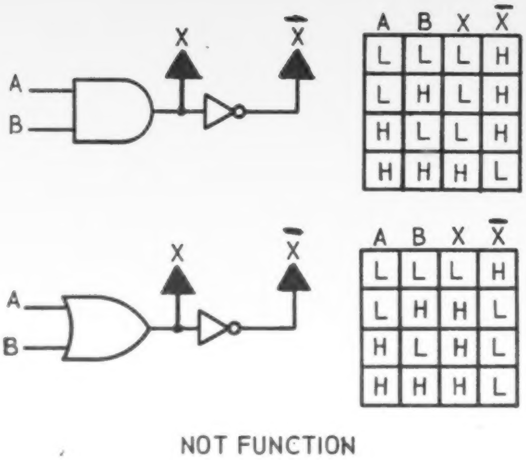


Figure 1-25. Amplifier symbols.

The small circle placed before or after the amplifier symbol is the state indicator. The circle at the input to figure 1-25 indicates that a low is required at the input



A	B	X	$\overline{X}$
L	L	L	H
L	H	L	H
H	L	L	H
H	H	H	L

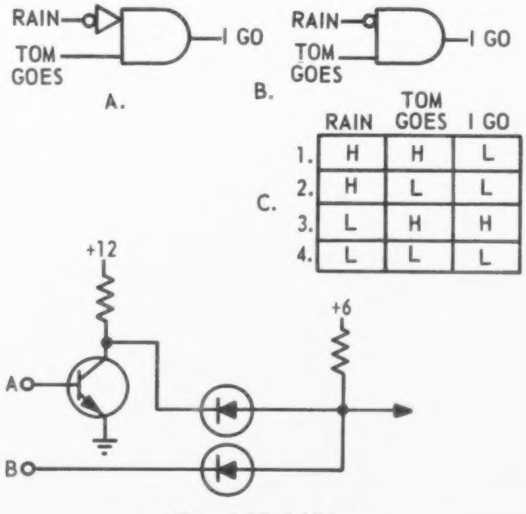
A	B	X	$\overline{X}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

Figure 1-26. NOT function.

to activate the amplifier and produce a high output. Without a low input, this function is not activated and the output is low. The absence of a circle at the input indicates that a high is required to activate the function. Without a high input, the output remains high. A high input produces a low output. The polarity signs (in addition to L and H) indicate that signal inversion occurs within the amplifier.

An amplifier such as the common-emitter circuit can be used to implement the NOT function because it inverts any signal applied to it. Common base and collector amplifier configurations, by themselves, don't invert a signal applied so are not used for the NOT function.

The output of an AND- or OR-gate can have the NOT function if an inverting amplifier is added, as shown in figure 1-26. Recall that the AND function requires all inputs to be high to get a high output. Two high inputs to a two-input AND-gate produce a high at point X, that activates the amplifier and the output at point $\overline{X}$ is low. At all other times, the output remains high. In the OR function, a high at either input (or both) produces a high at point X, that activates the amplifier and produces a low at point $\overline{X}$. Unless the amplifier is activated, the signal at $\overline{X}$ is high. Incorporating the inverting amplifier within the gate and then adding a state indicator to the output of an AND- and OR-gate will give us the NAND- and NOR-gate respectively. See figures 1-28,A, and 1-29,A.



	RAIN	TOM GOES	I GO
1.	H	H	L
2.	H	L	L
3.	L	H	H
4.	L	L	L

Figure 1-27. Inhibit-gate.

Inhibit gate. The NOT function is often used in conjunction with the input to an OR or AND circuit. For example, someone might say, "I'll go if Tom goes and it does NOT rain." Examinations show that this involves an AND function and a NOT function. This situation can be diagrammed as shown in figure 1-27,A. A more common method of diagramming is to omit the amplifier symbol and show only the state indicator in conjunction with the AND symbol, as in figure 1-27,B.

If rain is present (H), it prevents the AND circuit from producing an output. This prevention of the AND operation is called inhibiting. When a state indicator is used at the input of an AND circuit, the function is termed an inhibit function. The circuit which provides the inhibit function is called an inhibitor.

The truth table for the inhibit gate is shown in figure 1-27,C. The truth table simply means:

(1) It is raining and Tom is going but I am not going.

(2) It is raining and Tom is not going so I am not going.

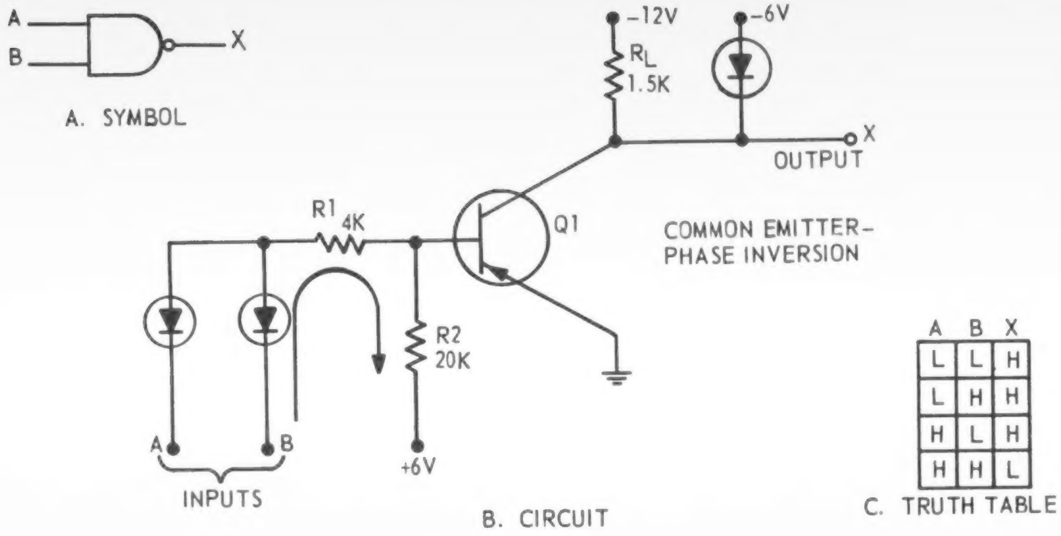
(3) It is not raining and Tom is going so I will go.

(4) It is not raining and Tom is not going so I am not going.

NAND-gate. Figure 1-28,A, shows an AND symbol with a state indicator at its output; this is called a NOT-AND (NAND) symbol. The state indicator on the output of the AND symbol indicates a relatively low-voltage level for the activated output. Thus, with two high inputs, the output will be low.

Figure 1-28,B, shows a diode-transistor logic (DTL) NAND circuit. DTL must be used to implement the NAND function since RDL will not provide inversion. An AND-gate at the inputs A and B will control the bias on the base of amplifier Q1. The potentials applied at A and B are either 0 volt, representing a high, or −6 volts, representing a low.

If a low input is applied to either diode A or B or to both simultaneously, a total of 12 volts is established across voltage divider R1-R2 and the diodes. Approximately 10 volts will be dropped across the 20 kilohm resistor, establishing a negative potential of about −2 volts for bias at the base of Q1. This forward biases the transistor into saturation which takes the output (X) to 0 volt. Note that a low input (A or B)



A	B	X
L	L	H
L	H	H
H	L	H
H	H	L

Figure 1-28. NAND-gate.

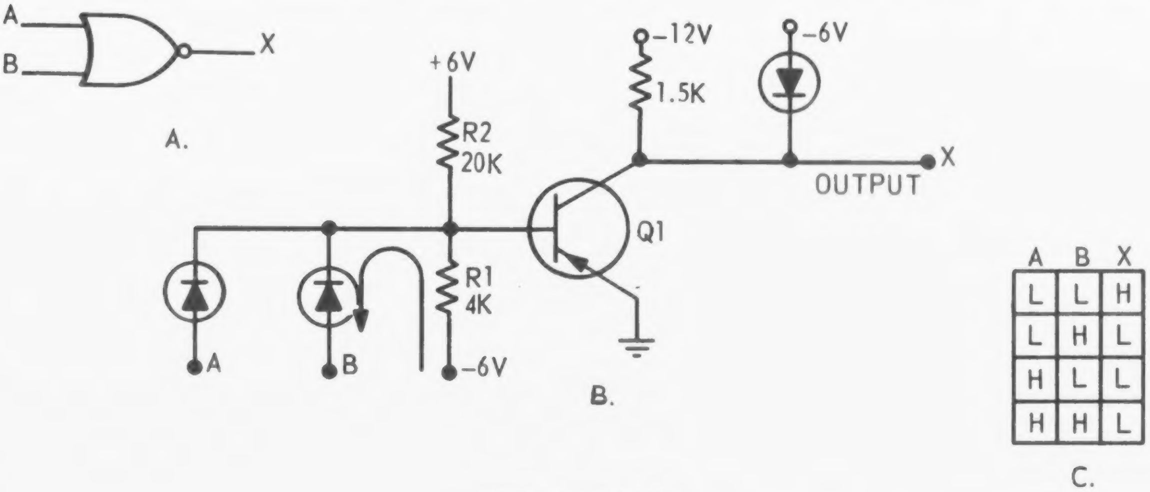
gives a high output. Now, consider the circuit with 0 volt applied to both A and B at the same instant; we have 6 volts across the voltage divider and diodes. Approximately 5 volts will be dropped across the 20 kilohm resistor, establishing a base-emitter potential of near +1 volt. This reverse biases the transistor and cuts it off. No current flow through the transistor now sets the output at −6 volts due to the diode clamp. The purpose of this diode is to establish the low-logic level. Thus, a high input at both A and B, at the same time, gives a low output.

Figure 1-28,C, shows the truth table for the NAND circuit, which you can verify. Keep in mind that the low is −6 volts and the high is 0 volt. When Q1 conducts, the output is high (0V); with Q1 cut off, the output is low (−6V). An AND function output would be high, but the NAND function output is low.

NOR-gate. An OR symbol with a state indicator at its output (fig. 1-29,A) is known as a NOT-OR (NOR) symbol. Notice that the state indicators on the output of the NOR-gate show a relatively low voltage as the activated output. Recall the normal output of an OR-gate is high with either input high. This symbol indicates the activated output will be low.

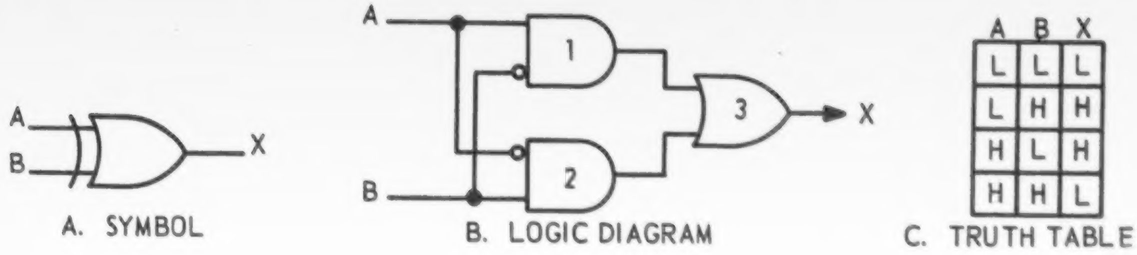
Compare the NOR circuit in figure 1-29,B, to the NAND circuit of figure 1-28,B. Note that the input diodes have been reversed and the base bias circuit has been changed. When both input diodes have −6 volts (low) applied at the same time, the 2V drop across R1 forward biases Q1. The transistor conducts and the output is 0 volt. Therefore, inputs must be low to give a high output in a NOR circuit.

Applying a high (0V) input to either diode will cause the transistor to cease conduction. The 0V input



A	B	X
L	L	H
L	H	L
H	L	L
H	H	L

Figure 1-29. NOR-gate.


A
B
X
A. SYMBOL
A
B
1
2
3
X
B. LOGIC DIAGRAM
C. TRUTH TABLE

A	B	X
L	L	L
L	H	H
H	L	H
H	H	L

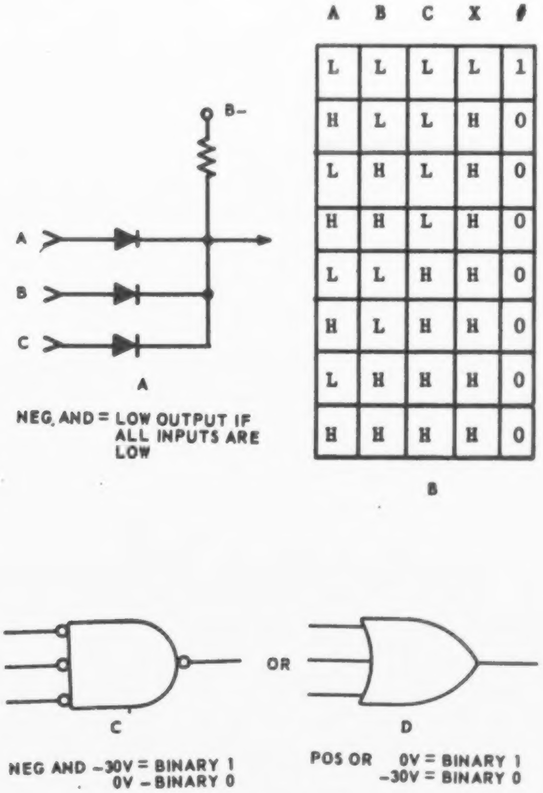
Figure 1-30. EXCLUSIVE OR Logic.

at A or B will cause the corresponding diode to conduct. Now, the voltage drop across R1 will equal 6V, making the base and emitter of Q1 at the same potential, which cuts the transistor off. The cutoff condition gives a low (−6V clamped) output. The diode at the output establishes the low-logic level. Saturation conduction of Q1 establishes the high-logic level.

Figure 1-29,C, shows the truth table for the NOR circuit, which you can verify. Notice that the two input diodes with resistors (R1 and R2) make up the OR-gate circuit. The common-emitter amplifier provides phase inversion. Any high input (A or B or both) causes a low output as represented by the NOR symbol.

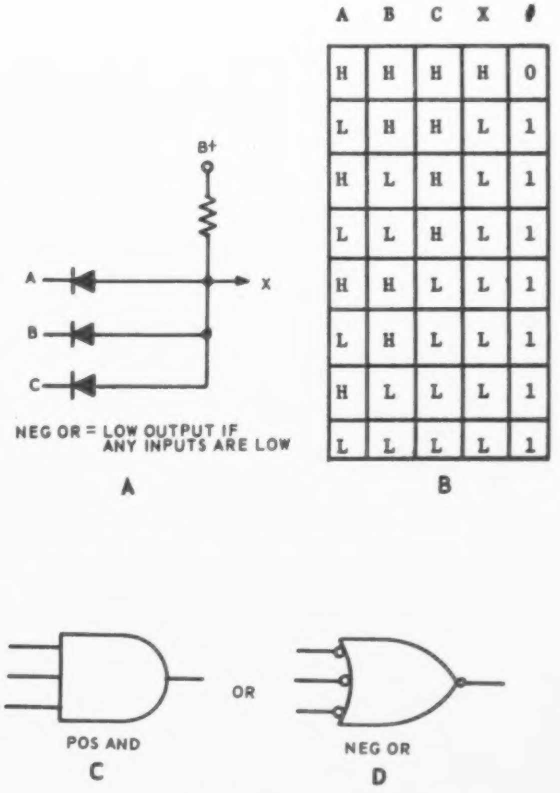
Exclusive OR Logic. Another logic function of importance is the exclusive OR. Figure 1-30,A, shows the symbol. An exclusive OR will develop an output pulse when either input A or B is high, but not when BOTH inputs are high. Figure 1-30,B, shows an example of the exclusive OR logic diagram. Notice that the exclusive OR is a combination of two inhibited ANDs and an OR symbol. Figure 1-30,C, shows the truth table which you can verify. Look back to figure 1-28,B and C, to review the conditions necessary for a high output. Then compare the truth table with the logic diagram of figure 1-30,B.

Negative Logic. In the AND- and OR-gates covered, 0 volt was used to represent high, whereas the low was represented by −6 volts.


B−
A
B
C
A
NEG. AND = LOW OUTPUT IF ALL INPUTS ARE LOW
B
C
OR
D
NEG AND −30V = BINARY 1
0V − BINARY 0
POS OR 0V = BINARY 1
−30V = BINARY 0

A	B	C	X	#
L	L	L	L	1
H	L	L	H	0
L	H	L	H	0
H	H	L	H	0
L	L	H	H	0
H	L	H	H	0
L	H	H	H	0
H	H	H	H	0

Figure 1-31. Negative AND-circuit.


B+
A
B
C
X
NEG OR = LOW OUTPUT IF ANY INPUTS ARE LOW
A
B
OR
POS AND
C
NEG OR
D

A	B	C	X	#
H	H	H	H	0
L	H	H	L	1
H	L	H	L	1
L	L	H	L	1
H	H	L	L	1
L	H	L	L	1
H	L	L	L	1
L	L	L	L	1

Figure 1-32. Negative OR-circuit.

Circuits may be designed to be activated by lows rather than highs. In this case, the AND and OR circuits used in logic systems of this type are called negative OR- and negative AND-gates.

A negative AND-circuit is one in which a low output is produced only if all the inputs are low. This condition can be met by using a circuit identical to a standard positive OR-gate. Figure 1-31 represents a negative AND-circuit. Use conditions of −30 volts for binary 1 and 0 volts for binary 0 (negative logic), and compare the circuit operation of figure 1-31,A, with the truth table of figure 1-31,B. In figure 1-31,C, note that a state indicator is used on the output terminal. This indicates that the output potential of an activated function is relatively low.

A negative OR-circuit is one in which any low input will give a low output. This condition can be met by using a standard positive AND-gate. Figure 1-32 represents a negative OR-circuit. Use the conditions −30 volts for binary 1 and 0 volts for binary 0, and compare the circuit operations with the truth table of figure 1-32.

Exercises (002):

1. A NOT function denotes ________ of a signal.

2. A gate-circuit is inhibited when the state indicator is shown in the ________.

3. Detail ________ in figure 1-33 shows an AND-gate notted.

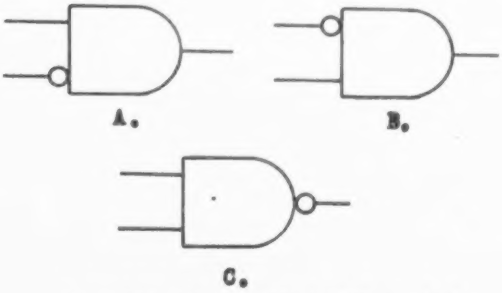


Figure 1-33. Figure for objective 002, exercise 3.

4. Write the correct output bit (X) for the gate shown in figure 1-34, when A is high and B is high.

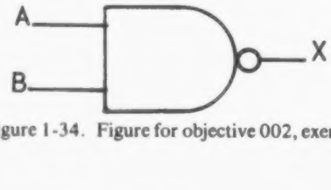


Figure 1-34. Figure for objective 002, exercise 4.

5. Draw the circuit for the gate shown in figure 1-35.

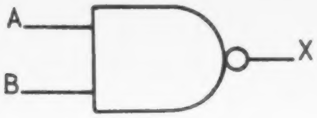
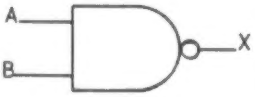


Figure 1-35. Figure for objective 002, exercise 5.

6. Construct the truth table for the logic symbol shown in figure 1-36.



A	B	X

Figure 1-36. Figure for objective 002, exercise 6.

7. Write the correct output (X) for the logic symbol shown in figure 1-37, when A and B are high.

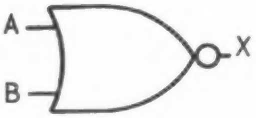


Figure 1-37. Figure for objective 002, exercise 7.

Use figure 1-38 for questions 8 through 10.

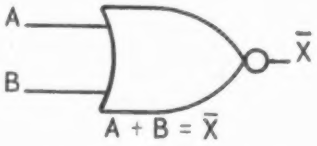
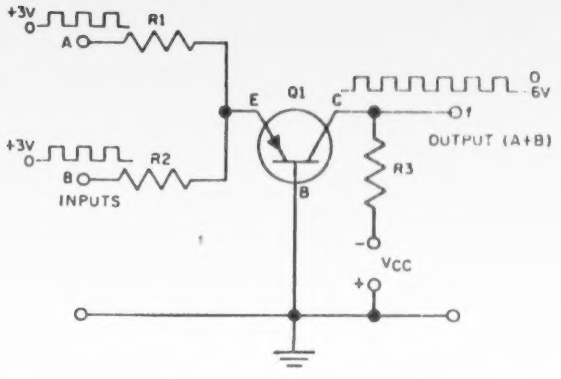


Figure 1-38. Figure for objective 002, exercises 8 through 10.

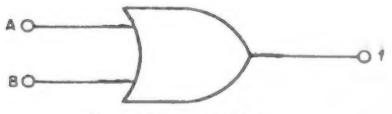
8. Write the correct output (X) for the logic symbol shown, when A and B are low.

9. Draw the correct circuit for the gate shown.

10. Construct the truth table for the gate shown.



A. CIRCUIT SCHEMATIC



B. LOGIC SYMBOL

INPUT		OUTPUT
A	B	f(A,B) = A+B
L	L	L
L	H	H
H	L	H
H	H	H

C. TRUTH TABLE

Figure 1-39. Two-input, common base, positive OR-gate.

003. Specify advantages of resistor transistor logic over diode resistor logic, and point out the major differences between the two.

Resistor Transistor Logic. Like the diode the transistor may be used to implement logic functions. By transistorizing AND and OR functions, many advantages are obtained. In addition, functions may be implemented which are not possible with diode logic. These include the NAND, NOR, and other functions using the NOT operation.

The transistor is the primary active device used in most of the digital gate circuits in use today. This is true for the discrete circuit as well as the integrated circuit. In fact, the RTL gate was one of the first to be put in integrated circuit form. Transistors function as switches by making use of an effective open or short circuit between the emitter and collector. Transistors used in gate circuits may be connected in series, parallel, or series-parallel to provide a variety of logic functions.

Properly configured, the transistor has the ability to provide an inverted version of its input signal at the output (electrical inversion), which, in turn, makes possible logic negation. Perhaps of even greater importance is the improvement in operating speed and the possibility of obtaining either a voltage or power gain through the circuit. For stages that require a heavy current output for operating relays and other electronic devices, the transistor emitter-follower connection provides power output with reduced gain. Because of the relatively higher input and output impedances possible with the transistor, the shunting effect of parallel inputs or outputs is not as great a problem as it is with diodes.

Exercises (003):

1. List four advantages of RTL over RDL.

2. Name the most important differences between RTL and RDL.

004. Identify RTL OR-gate circuit inputs with design considerations and effects.

RTL OR-Gate. Of the transistor configurations (common-emitter, common collector, and common base), only one is capable of providing a voltage gain while providing the same polarity at the output as at the input. This is the common base configuration and will be discussed first.

The schematic of a typical two-input, positive logic, single-transistor OR-gate is shown in figure 1-39,A. In this circuit the collector is reverse biased while the emitter is left floating. Thus, with no signal applied at A or B, a collector current cannot flow, and the output voltage will be the same as V_{cc}—the collector supply voltage (−6V). Assuming that proper circuit parameters have been chosen, a +3-volt signal applied at either, or both, A and B will forward bias the emitter and cause sufficient collector current to flow so as to cause the IR drop across R3 to be equal to the collector supply voltage. This condition causes the output voltage to go to 0 volts.

When the input signal is removed, the circuit returns to its quiescent state; that is, collector current cutoff and output voltage at −6 volts. Hence, a positive-going input signal of 3 volts of amplitude results in a positive-going output signal of 6 volts of amplitude, a voltage gain of two. Since, in its quiescent state, the circuit is operating at cutoff, a negative-going input signal will have little or no effect on circuit operation.

NOTE: R1 and R2 normally will have a high value of resistance in order to provide isolation between the two inputs.

Figure 1-39,B, is the logic symbol for the circuit. Figure 1-39,C, is the truth table for this circuit and indicates the possible combinations that could exist in this circuit at any given time. Note also that the output expression is shown as a Boolean function. In order for you to become familiar with this type of expression, an explanation follows.

In Boolean math, the plus sign (+) is used to indicate the OR function. The term f (A,B), means the function of A and B. The output of figure 1-39,C, is A + B which means A OR B. If it were an AND-gate, the output is expressed, A • B, the (•) stands for AND. The AND expression would be written as AB. All other truth table outputs in this module will be shown using the Boolean expression.

Exercises (004):

Use figure 1-39 to answer the following questions.

1. With no input what is the state of the collector bias?

2. With no input and V_{cc} is equal to −6 volts, what is the output?

3. What is the result of a negative input to the circuit?

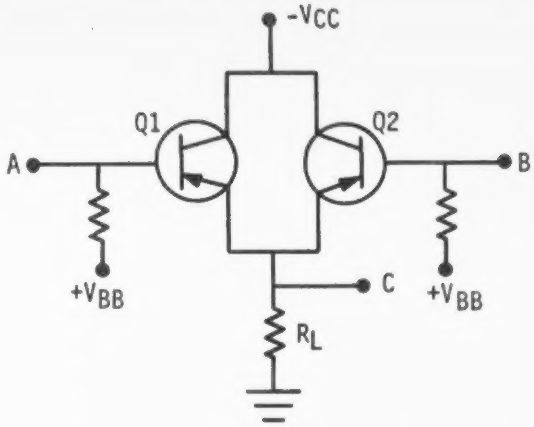
4. What is a design consideration for the value of the input resistors R1 and R2?

005. State the effects of particular operations in an RTL AND-gate circuit.

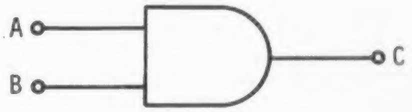
Positive Logic AND-Gates (PNP Transistors). The transistor AND-gate can be compared to a switch circuit with the switches connected in series. The positive logic AND-gate using PNP transistors is shown in figure 1-40.

Remember the conditions that control the operation of a PNP transistor? When a more positive voltage is applied to the base of a PNP transistor the emitter-base forward bias is decreased and the transistor is turned off. When a more negative voltage is applied to the base of a PNP transistor, the forward bias is increased and the transistor is turned on. Now, we will start with the conditions where inputs A and B are both more negative or a binary 0. Both Q1 and Q2 are turned on due to the increase in forward bias of the emitter-base connections. The current increase through RL renders the negative end of R_L more negative, or binary 0, and this is the output.

Let's now hold the input on A as a binary 0 and change input B to a binary 1. Q2 is now cut off due to the reduction of the emitter-base potential. Q1 is still conducting well, causing the negative end of R_L to remain very negative. This negative level is equal to a



A. CIRCUIT SCHEMATIC



B. LOGIC DIAGRAMS

INPUT		OUTPUT
A	B	f(A,B) = AB=C
L	L	L
L	H	L
H	L	L
H	H	H

C. TRUTH TABLE

NDA13-72

Figure 1–40. Two-input, common base, positive AND-gate.

binary 0, which appears on C as an output. If the input conditions are reversed, binary 1 on A and binary 0 on B, Q1 will cut off and Q2 will conduct heavily; the output remains a binary 0.

The fourth combination of inputs is when the binary 1s are applied to both inputs A and B. Both Q1 and Q2 are cut off, thereby reducing current through R_L. More positive potential is now felt on the negative end of R_L and this potential is equal to a binary 1 output. Therefore, it takes both 1's (inputs) into an AND-gate to receive a 1 out.

Exercises (005):

Use figure 1-40 to answer the following questions.

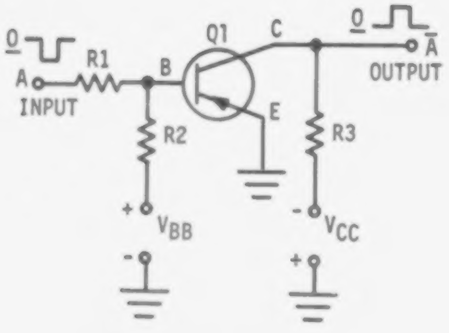
1. With a logic 0 on input A, what type of bias is present on the emitter-base junction of Q1?

2. When a logic 1 is present at point C, what is the state of Q1? Q2?

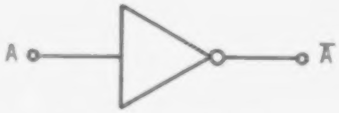
006. Define logic negation and identify an ideal characteristic of NOT-circuit operations using RTL.

RTL NOT-Circuits. When the common-emitter configuration is used, the output polarity is always inverted by an inherent action similar to that of an electron tube with a grounded cathode circuit. In logic operations it is sometimes desirable to produce an output signal that is identical to, but of opposite polarity from, the input signal. This function, which is known as logic negation, may be easily accomplished by an inverter circuit similar to the one depicted in figure 1-41,A.

When this circuit is in its quiescent state, both the emitter and collector junctions will be reverse-biased, causing the collector current to be cut off. With the collector current cut off, the IR drop across R3 will be negligible, and the output voltage will be nearly equal to the collector supply voltage. Assuming that the proper circuit parameters have been chosen, a negative-going input signal of sufficient amplitude to forward-bias the emitter junction will turn the transistor on. That is, it will cause enough current to flow so that the IR drop across R3 will equal the collector supply voltage. Since this voltage opposes the collector supply voltage, the output voltage will go to 0 volt. When the input signal is removed, the circuit returns to its quiescent state. Thus, a negative-going signal at the input results in a positive-going signal at the output. Since, in its quiescent state, the collector current is cut off, a positive-going signal at the input has little effect on the output.



A. CIRCUIT SCHEMATIC



B. LOGIC DIAGRAM

INPUT	OUTPUT
A	f (A) = Ā
L	H
H	L

C. TRUTH TABLE

NDA13-73

Figure 1-41. Single input inverter, NOT operation.

Figure 1-41,B, is the logic diagram for this circuit. Figure 1-41,C, is the truth table for this circuit and indicates the possible combinations that could exist in this circuit at a given time.

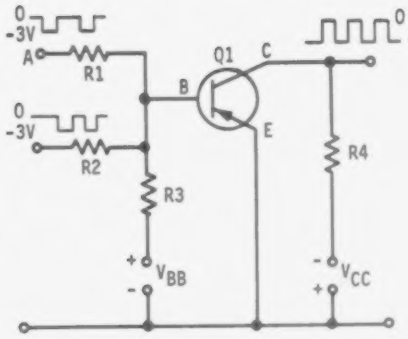
Exercises (006):

1. What is meant by the term "logic negation"?

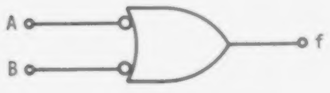
2. Why is the common-emitter circuit ideal for inverter circuits?

007. Point out the effects of particular inputs to a NOR-gate using RTL.

RTL NOR-Gate. Figure 1-42,A, is the schematic for a typical two-input, PNP-transistor NOR-gate. It is



A. CIRCUIT SCHEMATIC



B. LOGIC DIAGRAM

INPUT		OUTPUT
A	B	f (A,B) = $\overline{A+B}$
H	H	L
H	L	H
L	H	H
L	L	H

C. TRUTH TABLE

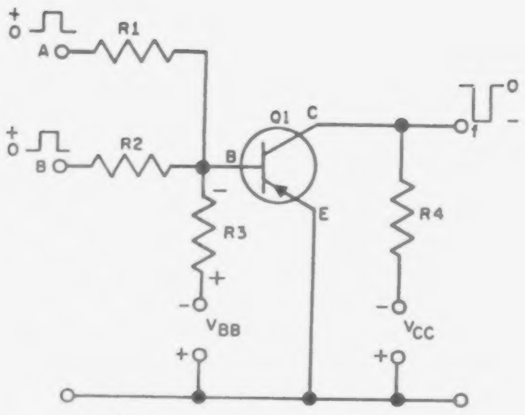
NDA13-74

Figure 1–42. Two-input, PNP transistor NOR-gate.

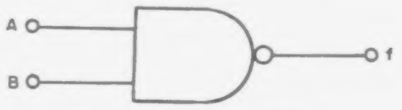
readily apparent that, with the exception of the addition of another input, this circuit is identical to the NOT-circuit just discussed. Circuit operation is also the same, except that now a negative-going signal, at either or both inputs of sufficient amplitude to forward-bias the emitter junction, will turn on the transistor.

NOTE: R1 and R2 normally will have a high value of resistance in order to provide isolation between inputs.

The logic symbols for this circuit are illustrated in figure 1-42,B. Signal (logic) inversion in the input is indicated by the small circuit adjacent to the input of the NOR symbol in the logic diagram. Common practice indicates that the logic negation indicator symbol (small circle) normally be placed adjacent to the input or output of the logic symbol for a given function, depending on whether the input or output signals are to be negated. The truth table for this circuit is illustrated in figure 1-42,C.



A. CIRCUIT SCHEMATIC



B. LOGIC DIAGRAMS

INPUT		OUTPUT
A	B	f(A,B) = AB
L	L	H
L	H	H
H	L	H
H	H	L

C. TRUTH TABLE

Figure 1-43. Two-input, PNP transistor NAND-gate.

Exercises (007):

Use figure 1-42 to answer the following questions.

1. With an input of −3V on R1, what condition will exist at R4?

2. With 0 volt signals on R1 and R2, what is the effect on the base of Q1?

008. Identify characteristics and operation of a NAND-gate using RTL.

RTL NAND-Gate. Figure 1-43,A, is the schematic of a typical two-input, PNP-transistor NAND-gate. This circuit is quite similar to the NOR circuit just discussed. The difference is that now a negative bias is applied to the base. This negative bias forward-biases the emitter junction, causing the transistor to conduct heavily. That is, with no signal applied, the emitter junction will be forward-biased to the point where the transistor operates in the saturation region. The resulting heavy collector current flow through R4 produces an IR drop across R4 that opposes the collector supply voltage and is of sufficient amplitude to reduce the output voltage to 0 volt. Assuming the parameters have been properly chosen, a positive-going signal at either, but not both, inputs will cause a certain amount of current to flow through R3. This current will produce an IR drop across R3, which opposes the base bias supply voltage. This IR drop will not, however, be of sufficient magnitude to reduce the base bias voltage to zero. Hence, the emitter junction will remain forward-biased, and the transistor will continue to operate in the saturation region with the result that there will be little or no change in output voltage. With a positive-going signal at both inputs, enough current flows through R3 so that the IR drop across R3 will be of sufficient magnitude to overcome the base bias, causing the emitter junction to be reverse-biased and cutting off the collector current. With the collector current cut off, the IR drop across R4 will be negligible, and the output voltage will now be nearly equal to the collector supply voltage.

The logic diagram for this circuit is illustrated in figure 1-43,B. With no signal or with a high at either input, but not both inputs, the output will also be high. However, should both inputs be high, the output will be low. Figure 1-43,C, is the truth table for this circuit.

In addition to providing signal inversion and the resulting logic negation, common-emitter circuits may (within practical limits) be designed to provide any amount of voltage gain desired. The primary factors in determining the maximum gain possible are the transistor characteristics and the available power supply voltage.

Exercises (008):

1. What is the primary design difference between the NOR-gate (fig. 1-42) and the NAND-gate (fig. 1-43)?

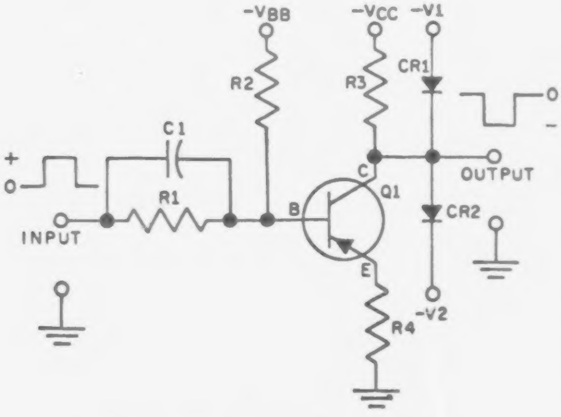


Figure 1-44. Diode transistor inverter.

2. In figure 1-43, with no applied signal, the transistor is biased to operate at ________ .

3. In figure 1-43, what is required to cut off the transistor?

009. Identify functions and characteristics of an inverter circuit operation using diode transistor logic.

Diode Transistor Logic. Computer circuits using both diodes and transistors are referred to as DTL circuits. In most cases, the diodes provide the primary logic function, while the transistors are used only to amplify and/or invert the output of the logic function. In some cases, however, the transistors provide the primary logic, while the diodes are used to control or direct the function. By combining diodes and transistors in the proper fashion, the advantages of both circuit components may be realized. That is, the diodes provide rapid switching action; and the transistors provide signal inversion, amplification, and impedance matching as needed.

Figure 1-44 is the schematic of a typical diode transistor inverter circuit. The advantage of this inverter circuit over those previously discussed is increased operating (switching) speed. Switching speed is increased by using the clamping action of the diodes to limit signal excursion in the output.

In this circuit the signal is applied to the base through R1 and C1. The purpose of Cl is to increase switching speed by increasing the slope (decreasing the rise and fall time) of the input signal. A negative bias is applied to the base via R2. R3 is the collector load resistor, and R4 is the emitter stabilization resistor. CR1 and CR2 are clamping diodes. CR1 clamps the collector voltage at the level of V1 when, as a result of a negative-going input signal, the collector voltage attempts to go positive. The values selected for V1 and V2 thus determine the amplitude of the output signal. Moreover, by making the difference between V1 and V2 quite small, the time required to switch from one level to the other is also made quite small.

In its quiescent state (with no signal applied) V_{BB} will forward-bias the emitter junction, thus permitting a large amount of collector current to flow. This collector current, in flowing through R3, produces an IR drop across R3 that opposes V_{CC} and is of sufficient amplitude to reduce the collector voltage to the point where CR2 will be forward-biased. With CR2 forward-biased, the collector voltage will be clamped at the level of V2.

If a negative-going signal is now applied at the input, it will tend to increase the forward bias on the emitter junction, and thereby increase the collector current flow. However, this increase in collector current will have little or no effect on the output voltage, since the collector and, therefore, the output are clamped at the level of V2.

With a positive-going signal applied at the input, the forward bias on the emitter junction is reduced. This, in turn, reduces the collector current flow. This reduction in collector current flow will tend to reduce the IR drop across R3 and thus increase the negative voltage appearing at the collector. However, until the collector current is reduced to the point where the resulting IR drop across R3 is less than the difference between V_{CC} and V2, there will be no change in collector voltage. Once this occurs, the negative voltage appearing at the collector will rapidly increase until a point is reached at which CR1 becomes forward-biased.

With CR1 forward-biased, the collector, and hence the output, will be clamped to the level of V1; the output will remain clamped at this level until the amplitude of the input signal is reduced below a certain level. With a reduction in amplitude of the input signal, the collector current will increase; however, there will be little or no change in the output voltage until a point is reached at which the IR drop across R3 exceeds the difference between V_{CC} and V1. At this point, the negative voltage appearing at the collector will rapidly decrease until it reaches the point where CR2 is again forward-biased.

Exercises (009):

1. How is switching speed increased in DTL as opposed to RTL?

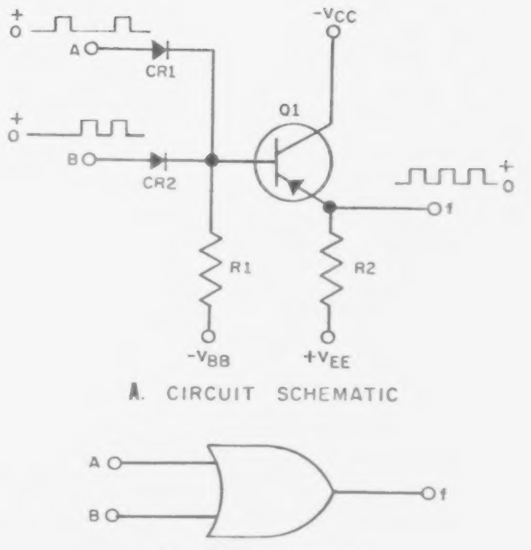
2. In figure 1-44, what is the purpose of C1?

3. An advantage of DTL over RTL is that the transistors provide signal________, ________, and ______________ as needed.

4. In figure 1-44, what is the purpose of R4?

010. State the purpose of particular components of a DTL OR-gate circuit.

DTL OR-Gate. Figure 1-45, A, is the schematic of a typical two-input, diode transistor OR-gate. CR1 and CR2, in conjunction with R1 and V_{BB}, function as the OR-gate, while Q1, which is connected in the emitter follower configuration, provides power gain and impedance matching where necessary.



A. CIRCUIT SCHEMATIC

B. LOGIC DIAGRAM

INPUT		OUTPUT
A	B	f(A,B) = A+B
L	L	L
L	H	H
H	L	H
H	H	H

C. TRUTH TABLE

Figure 1-45. Two-input, diode transistor OR-gate.

Assuming that proper parameters have been chosen, 0 volt will appear at the output when the circuit is at rest (quiescent or no signal state) because V_{BB} will, under normal operating conditions, forward-bias both diodes and the transistor emitter junction. With the diodes forward-biased and no signal (0V) applied at both inputs, 0 volt will appear at the transistor base. With 0 volt applied at the base, the emitter will be forward-biased to the point that sufficient collector current will flow to cause an IR drop across R2 of approximately the same magnitude as V_{EE}, and since it opposes V_{EE}, 0 volt will appear at the output.

A positive-going signal applied at either or both inputs will cause a positive-going signal to appear at the transistor base. This positive-going signal at the base reduces the forward-bias on the emitter junction, causing a reduction in collector current flow. With a reduction in collector current flow, the IR drop across R2 decreases, resulting in a positive-going signal of approximately the same magnitude as the input signal appearing at the output.

Figure 1-45,B, is the logic diagram for the circuit, and figure 1-45,C, is the truth table.

Exercises (010):

Use figure 1-45 to answer the following questions.

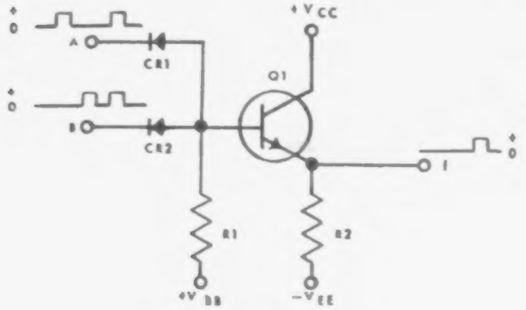
1. What is the purpose of Q1?

2. The V_{BB} provides________ bias for both the ________ and the ________ ________ .

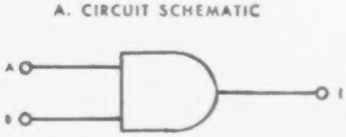
011. State the makeup and operation of a DTL AND-gate.

DTL AND-Gate. The schematic for a typical two-input, diode transistor AND-gate appears in figure 1-46,A. Like the circuit just discussed, CR1 and CR2, in conjunction with R1 and V_{BB}, perform the logic function (in this case the AND function). Q1, which is connected in the emitter follower configuration, provides power gain and impedance matching where necessary.

Assuming that proper parameters have been chosen, 0 volt will appear at the output when the circuit is at rest. This situation occurs because V_{BB} will, under normal operating conditions, forward-bias both diodes and the transistor emitter junction. With both diodes forward-biased and no signal (0V) applied at A and B, 0 volt will appear at the transistor base. With 0 volt applied at the base, the emitter junction will be forward-biased to the point that sufficient collector current will flow to cause an IR drop across R2 of approximately the same magnitude as V_{EE}. Since this IR drop opposes V_{EE}, 0 volt will appear at the output.



A. CIRCUIT SCHEMATIC



B. LOGIC DIAGRAM

INPUT		OUTPUT
A	B	1(A,B)=AB
L	L	L
L	H	L
H	L	L
H	H	H

C. TRUTH TABLE

Figure 1-46. Two-input, diode transistor AND-gate.

The application of a positive-going signal at either input (but not both) will have little effect on the output because the diode associated with the input to which no signal (0V) is applied will still be heavily forward-biased, holding the base of the transistor at approximately 0 volt. The other diode, because its anode is held at 0 volt and a positive voltage is applied to its cathode, will conduct less current.

With a positive-going signal applied at both inputs, the diodes are forward-biased to a lesser degree, causing a smaller IR drop across R1, with the result that a positive-going signal will appear at the base. The positive-going signal at the base increases the forward bias on the emitter junction, resulting in an increase in collector current flow. The increase in collector current flow causes an increase in the IR drop across R2, with the result that a positive-going signal of approximately the same magnitude as the input signal will now appear at the output.

Figure 1-46,B, is the logic diagram for the circuit, and figure 1-46,C, is the truth table.

Exercises (011):

Use figure 1-46 to answer the following questions.

1. The logic gate consists of which circuit components?

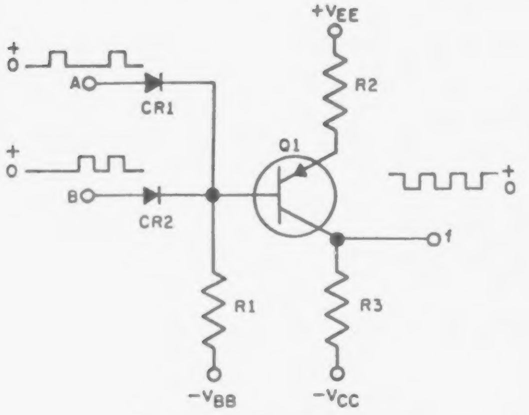
2. With the CR1 and CR2 forward-biased, what voltage is present at the base of Q1?

012. Cite operating characteristics of a NOR-gate using DTL.

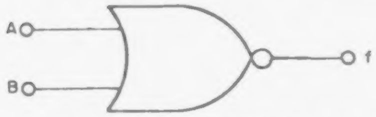
DTL NOR-Gate. Figure 1-47,A, is the schematic for a typical two-input, diode transistor NOR-gate. As you can see, the circuit is quite similar to the one in figure 1-45,A. CR1 and CR2, in conjunction with R1 and V_{BB}, still function as an OR circuit. Q1, however, is now connected in the common-emitter configuration and, hence, will function as an inverter/amplifier.

Assuming that proper parameters have been chosen, a positive voltage will appear at the output when the circuit is at rest. This situation occurs because V_{BB} will, under normal operating conditions, forward-bias both diodes and the transistor-emitter junction. With both diodes forward-biased to the point where sufficient collector current will flow so as to cause an IR drop across R3 of greater magnitude than V_{CC}, a positive voltage will appear at the output.

A positive-going signal at either or both inputs will,



A. CIRCUIT SCHEMATIC



B. LOGIC DIAGRAMS

INPUT		OUTPUT
A	B	$f(A,B) = \overline{A+B}$
L	L	H
L	H	L
H	L	L
H	H	L

C. TRUTH TABLE

Figure 1-47. Two-input, diode transistor NOR-gate.

because the diodes remain forward-biased, cause a positive-going signal to appear at the transistor base. A positive-going signal at the base reduces the forward-bias on the emitter junction, resulting in a decrease in collector current flow. With a decrease in collector current flow, the IR drop across R3 decreases, resulting in a decrease in the positive voltage appearing at the output. The output signal will thus be an amplified and inverted version of the signal appearing at the transistor base and, under the conditions established for this circuit, will switch from a predetermined positive value to zero whenever a positive-going signal is applied at either or both inputs.

The accepted logic symbols for this circuit appear in figure 1-47,B, and the truth table is shown in figure 1-47,C.

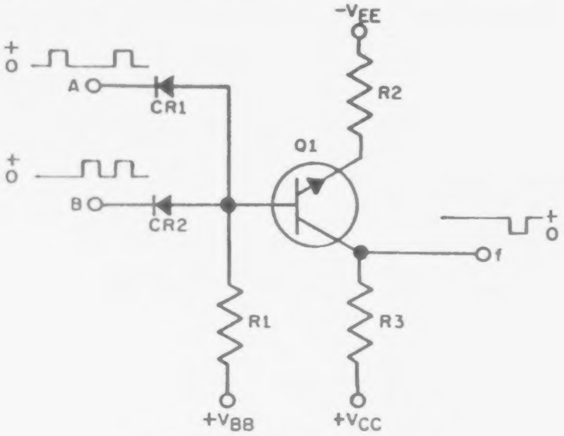
Exercises (012):

1. In order to have a DTL OR-gate function as a NOR-gate, the transistor would be reconnected in the ______ ________ configuration.
2. In figure 1-47, a decrease in collector current ________ the IR drop across R3.

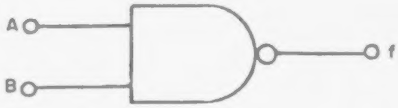
013. State the effects of a positive-going signal applied at the base of Q¹ in a DTL NAND-gate circuit.

DTL NAND-Gate. Figure 1-48,A, is the schematic of a typical two-input, diode transistor NAND-gate. As you can see, this circuit is quite similar to the AND circuit in figure 1-46,A. In fact, CR1 and CR2, in conjunction with R1 and V_{BB}, still perform the AND function. Q1, however, is now connected in the common-emitter configuration and, hence, will function as an inverter/amplifier.

Assuming that proper parameters have been chosen, a positive voltage will appear at the output when the circuit is at rest, because V_{BB} will, under normal operating conditions, forward-bias both diodes and



A. CIRCUIT SCHEMATIC



B LOGIC DIAGRAMS

INPUT		OUTPUT
A	B	f(A,B) = AB
L	L	H
L	H	H
H	L	H
H	H	L

C. TRUTH TABLE

Figure 1-48. Two-input, diode transistor NAND-gate.

the transistor emitter junction. With both diodes forward-biased and no signal (0V) applied at A and B, 0 volt will appear at the transistor base. With 0 volt applied at the base, the emitter junction will be forward-biased to the point where a certain amount of collector current will flow. This collector current, in flowing through R3, will cause an IR drop across R3 of a magnitude somewhat less than V_{CC}. This IR drop opposes V_{CC} and hence reduces the output voltage to a predetermined level.

A positive signal applied at either input (but not both) will have little effect on the output, since the diode with no signal applied is still forward-biased to the point where it will hold the base at about 0 volt. With a positive voltage on its base and 0 volt on its anode, the diode with the signal applied will be cut off and will effectively isolate the signal input from the rest of the circuit.

A positive-going signal simultaneously applied at both inputs will, because the diodes are forward-biased to a lesser degree, cause a positive-going signal to appear at the transistor base. A positive-going signal at the base increases the forward bias on the emitter junction, resulting in an increase in collector current flow. With an increase in collector current flow, the IR drop across R3 increases, resulting in a decrease in the positive voltage appearing at the output. The output signal will thus be an amplified and inverted version of the signal appearing at the transistor base and, under the conditions established for this circuit, will switch from a predetermined positive value to zero whenever a positive-going signal is simultaneously applied to both inputs.

The accepted logic diagrams for this circuit appear in figure 1-48,B, and the truth table appears in 1-48,C.

Exercises (013):

1. A positive-going signal at the base of Q1 shown in figure 1-48 ______ the ______ ________ on the emitter junction.

2. Based on the above question, the output of the NAND-gate (fig. 1-48) will be ________ and ________.

014. State one function and indicate the effects of input signals in the operation of the DTL inhibitor circuit.

DTL Inhibitor Circuit. In most number systems, including binary, subtraction is performed as follows: 0 − 0 = 0, 1 − 0 = 1, and 1 − 1 = 0. The fourth possible generation, 0 − 1, is unique in that it involves a borrow. The result will depend on the base of the number system being used. A device which will give us the correct results for the first three operations listed is the inhibitor as shown in figure 1-49. This circuit is also known as a quarter subtractor.

The circuit is essentially the basic ANd-gate in figure 1-46, with an inverter connected at input B. With an input of a logic 0 (0V) on both inputs, we would normally expect both diodes of an AND-gate to be forward-biased; however, because R1 and R2 form a voltage divider, a small negative potential is present to reverse bias Q1. With Q1 off, CR2 is reversed biased by $+V_{CC}$. With 0 volt on the cathode of CR1, it conducts heavily, creating a drop across R_L equal to the applied voltage. The voltage then is the same as on a standard AND-gate.

With a 0 on A and a 1 on B, the positive voltage on B will overcome V_{BB} and forward bias Q1. This causes CR2 to be forward-biased. With both diodes forward-biased, the output remains at 0.

With a 1 on A and 0 on B, the diodes will both, because of the inverter action of Q1, be reversed-biased (actually they are partially conducting), and the potential at R_L rises to +6V or a logic 1.

Our final possible combination is a 1 on both inputs. Although CR1 is reverse-biased, CR2 is forward-biased through Q1. Thus, the output is held to a logic 0.

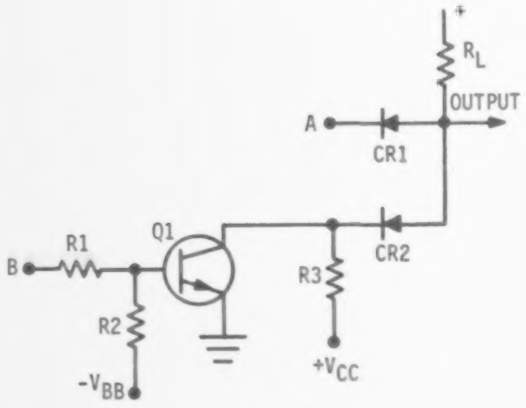
If we consider the input on A as the minuend and B the subtrahend, we see by the truth table (fig. 1-48,C) that disregarding the second operation (which in subtraction would be erroneous due to the lack of a "borrow") the inhibitor does indeed perform the subtraction function.

Exercises (014):

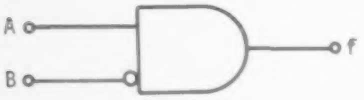
1. What inputs are required for a positive output of the inhibitor shown in figure 1-49?

2. What is another name for an inhibitor?

3. Name the combination of inputs that yield a 0 volt output.


+
R_L
OUTPUT
A
CR1
Q1
CR2
R1
B
R3
R2
-V_BB
+V_CC

A. CIRCUIT SCHEMATIC



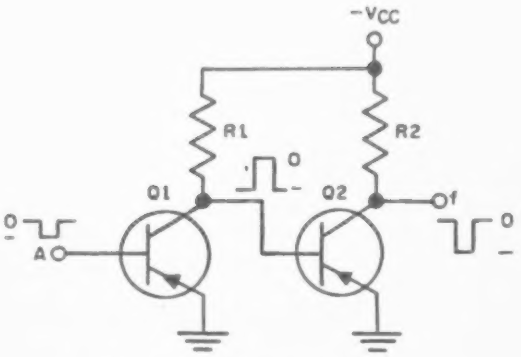
B. LOGIC DIAGRAM

INPUT		OUTPUT
A	B	f (A,B) = A$\bar{B}$
L	L	L
L	H	L
H	L	H
H	H	L

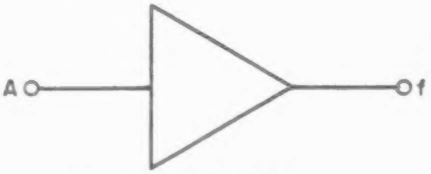
C. TRUTH TABLE

NDA13-75

Figure 1–49. The inhibitor circuit.


-V_CC
R1
R2
0
-
Q1
Q2
0
-
A
f
0
-

A. CIRCUIT SCHEMATIC



B. LOGIC DIAGRAM

INPUT	OUTPUT
A	f(A) = A
L	L
H	H

C. TRUTH TABLE

Figure 1-50. Direct-coupled transistor logic inverters.

015. State the principle of signal amplification and operation of direct-coupled transistor logic (DCTL) inverters; list advantages of direct-coupled transistors.

DCTL Amplifiers. In this type of logic mechanization, the only active elements are transistors and resistors. Coupling exists directly between the elements of successive transistors (resistors, where used, serve primarily as load resistors)–hence, the name "direct-coupled transistor logic."

Compared to transistorized logic circuits previously discussed, this type of logic mechanization generally requires fewer components and less power, while providing increased operating speeds. Power requirements are reduced for two reasons: (1) signal voltage amplitudes are on the order of millivolts; hence, power supply voltages may be reduced; and (2) fewer circuit components mean fewer circuit losses; hence, circiut efficiency is increased. Because of the lower operating voltages, the time required to switch from one level to the other is reduced, resulting in an increase in operating speed.

The schematic in figure 1-50,A, illustrates the method of coupling used in direct-coupled transistor logic circuits. Two inverter circuits are shown, with the output of one coupled directly (cascaded) to the input of the other. R1 and R2 serve only as load resistors for the transistors. Since this circuit uses two inverters, the output will be in phase (of the same polarity) as the input and thus will be an amplified version of the input.

The parameters are such that, with no signal (0V) applied at the base of Q1, it will be at or near cutoff; that is, little or no collector current will be permitted to flow. With little or no collector current flowing in Q1, the IR drop across R1 will be negligible. With negligible IR drop across R1, the voltage appearing at the collector of Q1, and hence the base of Q2, will be nearly equal to V_{CC}. This negative voltage applied at the base of Q2 will forward-bias the emitter junction of Q2, causing Q2 to conduct heavily. The collector current of Q2 in flowing through R2 produces an IR drop across R2 that is nearly equal in magnitude to V_{CC}. Since this IR drop opposes V_{CC}, the collector of Q2, and thus the output, will be at or near 0 volt.

A positive-going signal applied at the base of Q1 will have little effect on circuit operation, since it only serves to drive Q1 further into cutoff. A negative-going signal, however, will forward-bias the emitter junction, causing an increase in collector current flow; the IR drop across R1 will increase, causing the negative voltage appearing at the collector of Q1 and the base of Q2 to decrease. With a decrease in the negative voltage applied at its base, the forward-bias on the emitter junction of Q2 will decrease, causing a decrease in collector current flow. With a decrease in Q2 collector current, the IR drop across R2 decreases, resulting in a negative-going signal appearing at the collector of Q2, and hence at the output.

The logic diagram in figure 1-50,B, could be used to represent this circuit. Figure 1-50, C, is the truth table for this circuit.

Exercises (015):

1. How is signal amplification obtained in the circuit shown in figure 1-50?

2. In figure 1-50, what is the result of a positive-going signal applied to the base of Q1?

3. Name two reasons why power requirements are reduced by using DCTL.

016. Determine the affects of input signals applied to a DCTL NAND-circuits.

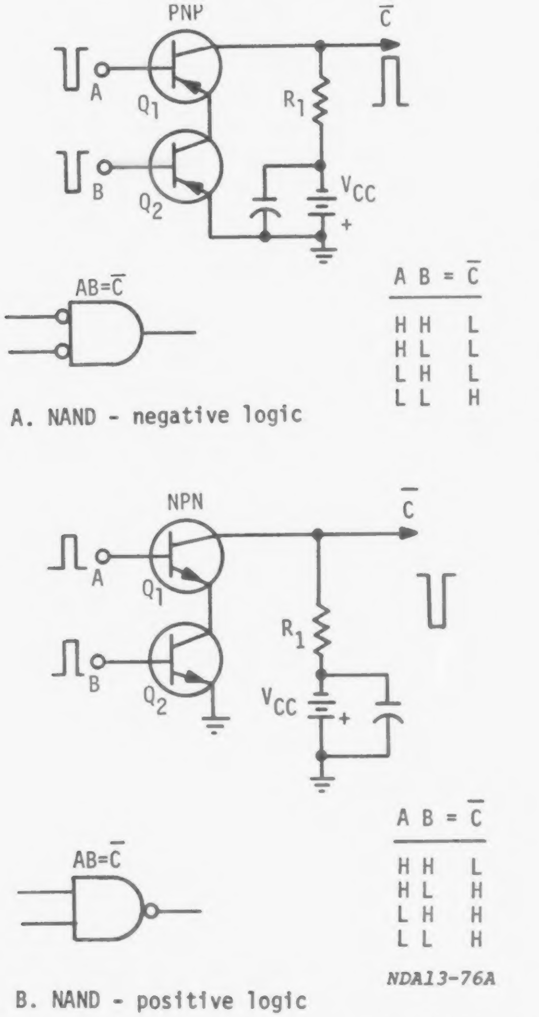
DCTL NAND-circuit. Figure 1-51 shows typical schematics for two-input NAND-gates using direct-coupled transistor logic. In figure 1-51,A, negative logic is used and in 1-51,B, positive logic is used. Compare the two schematic and logic diagrams. Q1 and Q2 are effectively connected in series between the load and ground cut off, the voltage-appearing at the collector of Q1, and thus the output C will be nearly equal to V_{CC}. Consider the circuit in figure 1-51,A. Assuming that proper parameters have been selected and no signal (0V) is applied at the inputs, both transistors will be biased at cutoff. With Q1 and Q2 both at cutoff, little or no collector current will flow, and the IR drop across R1, the voltage appearing at the collector of Q1, and hence the output, will be nearly equal to V_{CC}.

A positive-going signal applied at either or both inputs will have little effect on the output, since the effect of such a signal would be to drive the transistors further into cutoff.

A negative-going signal applied at either input, but not both inputs, also will have little effect on the output. Even though such a signal will forward-bias the emitter junction of the transistor to which it is applied, there will be no increase in collector current flow, since the other transistor will still be biased at cutoff.

The only remaining condition to be discussed is when negative-going signals are simultaneously applied at both inputs. When this occurs, the emiter junctions of both transistors will be forward-biased, and collector current will start to flow. With an increase in collector current flow, the IR drop across R1 will increase, and since this IR drop opposes V_{CC}, there will be a decrease in the negative voltage appearing at the collector of Q1 and hence the output.

The circuit in figure 1-51,B, operates in a similar manner using a positive going signal as the active input to the gate.


PNP
$\overline{C}$
A
B
Q_1
Q_2
R_1
V_{CC}
+
$AB=\overline{C}$
NPN
$\overline{C}$
A
B
Q_1
Q_2
R_1
V_{CC}
+
$AB=\overline{C}$
NDA13-76A

A	B	= $\overline{C}$
H	H	L
H	L	L
L	H	L
L	L	H

A. NAND - negative logic

A	B	= $\overline{C}$
H	H	L
H	L	H
L	H	H
L	L	H

B. NAND - positive logic

Figure 1–51. Direct-coupled transistor logic, two-input NAND-gate.

Exercises (016):

1. How would two transistors be connected to form a DTCL NAND-gate?

2. With negative-going signals applied to both A and B of the circuit in figure 1-51,A; what is the output signal?

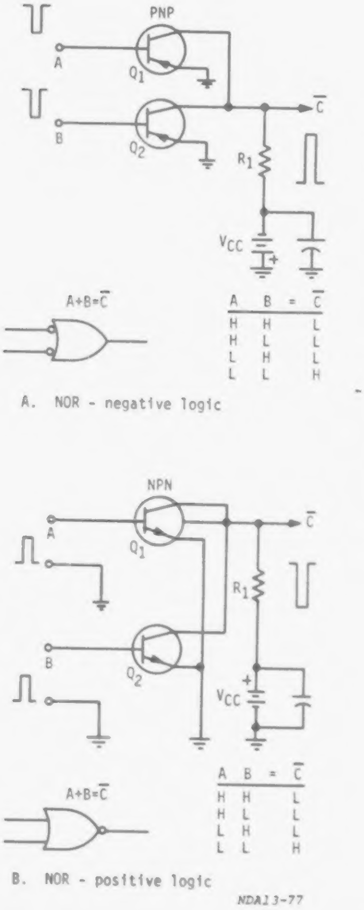
3. If the output signal of the circuit in figure 1-51,B, is a negative-going signal what are the inputs at A and B?

017. Determine the affects of input signals applied to a DCTL NOR-circuits.

DCTL NOR-circuit. In figure 1-52 are the schematic diagrams of typical two-input NOR-gates using direct-coupled transistor logic. You will note that in the case of the NOR-circuit Q1 and Q2 are connected effectively in parallel between the load and ground. Therefore, either or both transistors conducting will result in the voltage at the output being at a near 0 volts.

As we study figure 1-52,A, assume that proper parameters have been selected and no signal (0V) is applied at the inputs, both transistors will be biased at cutoff. With Q1 and Q2 both at cutoff, little or no collector current will be negligible IR drop across R1, the voltage appearing at the collectors of the transistors, and hence at the output, will be nearly equal to V_{CC}.

A positive-going signal applied at either or both inputs will have little or no effect on the output because the net effect of such a signal would be to drive either or both transistors further into cutoff. With a negative-going


PNP
A
B
Q_1
Q_2
$\overline{C}$
R_1
V_{CC}
+
$A+B=\overline{C}$
NPN
A
B
Q_1
Q_2
$\overline{C}$
R_1
V_{CC}
+
$A+B=\overline{C}$
NDA13-77

A	B	= $\overline{C}$
H	H	L
H	L	L
L	H	L
L	L	H

A. NOR - negative logic

A	B	= $\overline{C}$
H	H	L
H	L	L
L	H	L
L	L	H

B. NOR - positive logic

Figure 1–52. Direct-coupled transistor logic, two-input NOR-gate.

signal applied at either or both inputs, the emitter junction(s) of the transistor(s) to which such a signal is applied will be forward-biased. With the emitter of either or both transistors forward-biased, sufficient collector current will flow to produce an IR drop across R1 of the same magnitude as V_{CC}. Since this IR drop opposes V_{CC}, the potential appearing at the collectors of both transistors, and thus at the output, will be at or near 0 volt.

Exercises (017):

Use figure 1-52 to answer the following questions.

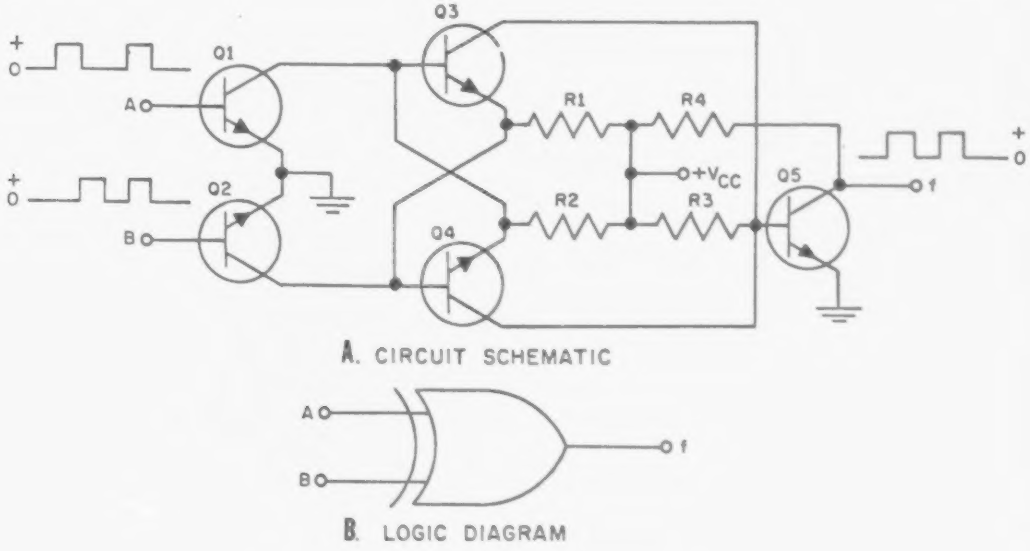
1. In the NOR circuit Q1 and Q2 are connected in ________ between the ________ and ________.

2. In the NOR circuit what is the only condition where the output will equal V_{CC}?

018. Specify the principal components and effects of applying certain input signals in the DCTL exclusive OR circuit.

DCTL exclusive OR-Circuit. Figure 1,53,A, is the schematic of an exclusive OR-gate using direct-coupled transistor logic. While it is not readily apparent, this circuit actually consists of two inhibitors and an OR-gate. Q3, in conjunction with Q1 and Q2, performs the inhibit function, f (A,B) = AB; while Q4, in conjunction with Q1 and Q2, performs the inhibit function, f (A,B) = AB. The OR function is performed by Q5 in conjunction with Q3 and Q4.

In the quiescent state, that is, with no signal (0V) applied at A and B, Q1 and Q2 will be operating at or near cutoff. Their emitter junctions will be reverse-biased, and little or no collector current will flow. With little or no collector flowing in Q1 and Q2, the IR drops across R1 and R2 will be negligible. Therefore, the voltage appearing at the bases and the emitters of Q3 and Q4 will also be operating at or near cutoff; and, with little or no collector current flow through Q3 and Q4, the IR drop across R3 will be negligible. With negligible IR drops across R3, the voltage appearing at the base of Q5 will be forward-biased and sufficient collector current will flow so as to produce an IR drop across R4 that is nearly equal in magnitude to V_{CC}. This IR drop opposes V_{CC}; hence, the output, f, will be at or near 0 volt.



A. CIRCUIT SCHEMATIC

B. LOGIC DIAGRAM

INPUT		OUTPUT
A	B	f (A,B) = A$\bar{B}$+$\bar{A}$B
L	L	L
L	H	H
H	L	H
H	H	L

C. TRUTH TABLE

Figure 1-53. DCTL OR-gate.

With a positive-going signal applied at A and no signal (0V) applied at B, the Q1 emitter junction will be forward-biased, and the Q2 emitter junction will be reverse-biased. Q1 will begin to conduct rather heavily, and Q2 will remain cut off. The Q1 collector current in flowing through R2 produces an IR drop across R2 nearly equal in magnitude to V_{CC}, and since this IR drop opposes V_{CC}, the Q4 emitter and Q3 base will be at or near 0 volt. With 0 volt on its base and a positive voltage on its emitter, Q3 remains cut off. Q4, on the other hand, will conduct rather heavily, since it will have 0 volts on its emitter and a positive voltage on its base, forward-biasing its emitter junction. The Q4 collector current, in flowing through R3, produces an IR drop across R3 nearly equal in magnitude to V_{CC}, and since this IR drop opposes V_{CC}, the base of Q5 will be at or near 0 volt. With its emitter grounded and 0 volt on its base, Q5 will be at or near cutoff. With little or no collector current flow in Q5, the IR drop across R4 will be negligible, and the voltage at the output will be nearly equal to V_{CC}.

With a positive signal at B and no signal (0V) at A, the same sort of situation will exist; only now, Q1 will be cut off and Q2 will be conducting. Q4 will be cut off and Q3 will be conducting. This condition again reduces the voltage appearing at its collector, and thus the output will be nearly equal to V_{CC}.

With a positive-going signal applied at both inputs, Q1 and Q2 will both conduct at saturation, with the result that the voltage appearing at the base of Q5 will cause it to conduct at or near saturation, thus producing an IR drop across R4 that is nearly equal in magnitude to V_{CC}. Since this IR drop opposes V_{CC}, the output will be at or near 0 volt.

The logic diagram for this circuit appears in figure 1-53,B, and the truth table in figure 1-53,C.

Exercises (018):

Use figure 1-53 to answer the following questions.

1. The exclusive OR circuit actually consists of ______ ______ and an ________ -gate.

2. With a positive-going signal applied to A and 0 volts at B, Q1 will be ______ ______ and Q2 be ______ ________ .

3. It no signal (0V) is applied to inputs A and B, the output (f) will be approximately ________ volts.

1-2. Integrated Circuit Logic

The integrated circuit (IC) logic gate is a monolithic (one-piece) circuit in which all components are etched into a tiny block of silicon. Interconnections between these component parts are made by means of metallic patterns and the individual parts are not separated from the complete circuit. Their relatively low cost, small size, and high reliability make this type of circuit ideal for applications where identical circuits are required in large quantities. This is why they are now being widely used in digital computers. The following discussion will help you understand the operation of logic ICs.

019. Define IC terms and specify the characteristics of selected logic families.

IC Terms and Definitions. The following terms are used when talking about integrated circuits. The definitions will enable you to better understand the operation and use of integrated circuits.

Chip. A piece of semiconductor material on which electronic components have been formed (usually transistors and resistors) to produce an integrated circuit. May also be called a die or substrate.

DIP (dual in line package). An integrated circuit package type, made of plastic or ceramic, with two rows of leads along either side. It is rectangular in shape and usually has from 8 to 40 leads. The leads extend vertically from each side and permit easy insertion of the DIP into printed circuit boards.

Fall time. A measure of the time required for the voltage of the trailing edge of a pulse to drop from 90 to 10 percent of the original amplitude; also called decay time.

Fan-in. The number of logical inputs to a circuit.

Fan-out. The number of logical outputs from a circuit or the number of gates that a given output gate can drive.

Flat-pack. Another type of integrated circuit package that is thinner than the DIP with the leads extending horizontally from the sides. Like the DIP, it is made of plastic or ceramic.

IGFET (insulated-gate field effect transistor). See the definition of MOSFET, which is the same as IGFET.

LSI (large-scale integration). A digital IC with between 100 and 1000 logic gates within the package.

Monolithic. A microcircuit in which transistors, diodes, resistors, and capacitors are formed on and within a single-crystal semiconductor substrate.

MOSFET (metal-oxide silicon field-effect transistor). A high-impedance input device which can be used as an amplifier or switch. Charge carriers within the transistor are of only one type, N or P, and therefore, the MOSFET is a unipolar device. The MOSFET is classified as an enhancement type (normally off) or the depletion type (normally on).

MSI (medium-scale integration). A digital integrated circuit that has from 12 to 100 gates within.

SSI (small-scale integration). A digital integrated circuit that has 10 to 12 gates or fewer.

Pull-down resistor. A resistor tied to logic 0 or ground and the input of a gate to keep the input at a logic low.

Pull-up resistor. A resistor connected to a logic 1 level and tied to the input of a gate to keep the input at the logic 1 or high level.

Rise time. The time required for a pulse to rise from a specific lower limit to a specific upper value, usually from 10 to 90 percent of its final value.

VLSI (very large-scale integration). A digital integrated circuit which will have more than 1000 gates on a chip. These chips are responsible for the computer on a chip—the microprocessor.

Logic Families. A variety of digital logic circuits are available, dependent on the circuit to be used for them and its electrical requirements. Integrated circuits may use bipolar transistor, MOSFET, or CMOS technology to implement a logic circuit. Each will have its own advantages, disadvantages, and special characteristics. A brief explanation of several logic families follows, including a table of characteristics for three of the more prominent logic types.

NOTE: Later in this section we will focus on ECL logic, which is the most common high-speed logic, and TTL, which is the most common logic used in current generation of electronic digital equipment.

Current mode logic (CML). CML is also referred to as current steering logic. The circuit uses a transistor for each input and an additional transistor for biasing. Both the OR and NOR outputs are available from the circuit. Because the transistors in this logic don't saturate during switching transitions, the speed of this logic is greater than some others.

Complementary MOS logic (CMOS). This type of logic is built on a chip using the MOSFET as its primary active device. An N-channel MOSFET will be complemented by a P-channel device, and both are of the enhancement or normally off type. If either device is turned on, the other will be off and the only time current will be drawn from the power supply will be during the transition period when the N-channel is turning off or the P-channel is turning on. This will also be true during the reverse situation. Therefore, CMOS logic requires very little power during operation.

Direct-coupled transistor logic. DCTL was one of the first types of logic to be put in IC form. Each emitter and collector of the transistors in a gate are tied together. Input signals are connected to the bases of the individual transistors that are part of the gate circuit. Because of the inherent differences between each transistor, if one has lower voltage requirements for bias than the others, it will tend to hog the current available. To remedy this, resistors are put in the base lead of each transistor to lessen the effects of the base-emitter voltage.

Diode-transistor logic. The input of DTL will consist of diodes for each input to a gate. The output of the diode gate is fed through another diode and then to the base of an inverter transistor gate. A capacitor may be used across the series diode to speed up the gate.

Emitter-coupled logic (ECL). ECL is the fastest available logic family, capable of over 500 megahertz. Logic in the ECL IC is similar to that in CML. Complementary outputs are available from the ECL gate.

High-threshold logic (HTL). The HTL circuit is similar to the DTL except that a Zener diode replaces the coupling diode.

Integrated injection logic (I^2L). The I^2L logic is another IC development that came about after modifying the DCTL device. Modification involved the elimination of resistors and the use of multiple collector transistors. The unit may have both AND and NAND outputs, or OR and NOR outputs.

Resistor-transistor logic (RTL). This type of logic is equal to the DCTL after base resistors are installed. This prevents the current hogging effects of DCTL but decreases the speed of the device.

Transistor-transistor logic (TTL). TTL, or T^2L, is the most common and popular logic used today. A multiemitter transistor is normally used as the inputs to this type of gate, the output of which is directly coupled to a pull-up transistor which provides the drive to switch the output on and off. TTL logic is available in standard, low-power, high-speed, and the nonsaturating of Schottky versions.

The table below indicates some typical characteristics for three of the most used types of logic. The propagation delay indicates the time for a digital pulse to get through a gate. Power is in milliwatts.

Supply Voltage	Speed (MHz)	Propagation Delay (ns)	Power Dissipated per gate (mW)	Fan-Out
CMOS 3-18	5	70	1	50
ECL –5.2	30-500	2	40	25
TTL 5.0	35	3-12	20	10

Exercises (019):

1. In which category would an IC device containing 150 gates be listed?
2. What is the most common logic family in use?
3. What is the fastest logic family available?
4. What logic family uses the multiemitter transistor as an input?
5. MOSFET devices are used to implement what logic family?
6. What type logic could handle a fan-out of 40?
7. Which logic family is available in high-speed and low-power versions?

020. Identify characteristics and advantages of a five-input ECL OR/NOR integrated circuit.

ECL Circuit Characteristics. The basic ECL logic gate with a fan-in of five (fig. 1-54) consists essentially of a six-transistor current-mode switch and two emitter followers coupling the signals for the collectors of the gate to the output. Five of the six switching transistors are used as input transistors, with their bases connected to input terminals; the sixth has its base connected to a fixed bias source. With no signal applied to any of the input transistors (Q1-Q5) these units are cut off, while Q6 is conducting due to the fixed bias applied. For any signal condition, there are two outputs available from the gate: one from the collector of the fixed bias transistor, the other from the common collector junction of the five input transistors. If, for example, a positive signal representing a logical 1 is applied to any of the inputs, the common collector output goes negative while that of the fixed bias transistor goes positive. These two outputs, therefore, perform an OR and NOR function. If a negative-going signal is chosen to represent a logical 1, the basic gate performs an AND and NAND operation.

It is important to note that in this circuit a desired signal and its complement are simultaneously available. This has two distinct advantages over other types of circuits where a complementary signal can be obtained only through the use of a separate inverter. First, a smaller number of stages is required for a complete system, thus increasing the speed of the system by reducing the number of stage delays; second, the interconnecting problem between logic blocks is reduced by a factor somewhere between two and three.

Signals from the gate are coupled to the output terminals through emitter followers Q7 and Q8 which serve as DC translators to make the outputs comparable with the DC level requirements of subsequent input stages. Moreover, the emitter followers, due to their low output impedance, provide a large fan-out capability. In a ECL system, the input resistance is approximately 63 kilohms and the output impedance about 30 ohms. It is evident, therefore, that a design fan-out of 100 or more is entirely practical.

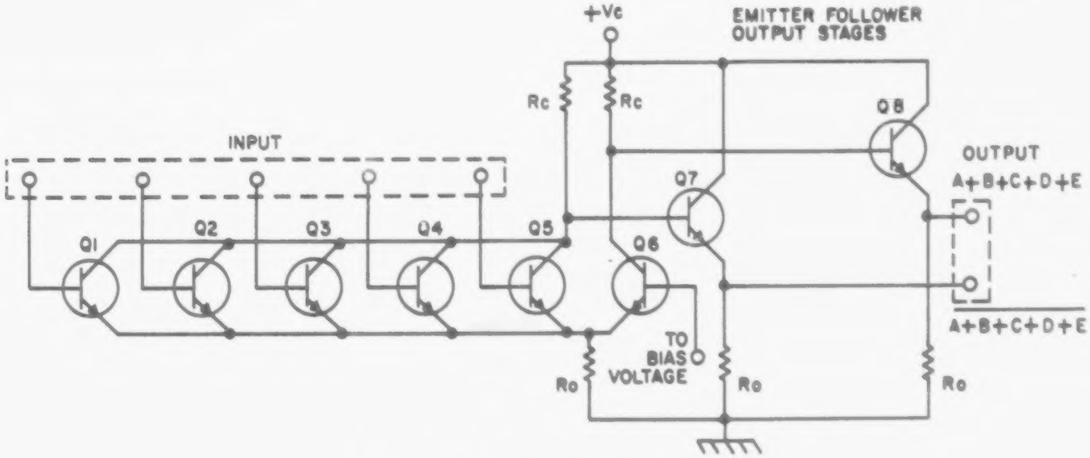


Figure 1-54. Five-input ECL logic gate.

For high-speed applications, however, the fan-out capability is considerably reduced since it is determined primarily by the capacitive loading of the succeeding stages. Though the input capacitance of an ECL gate is considerably lower than that of other types, being reduced by the large amount of negative feedback introduced by the common-emitter resistance, high-speed fan-out in general is considerably less than 100.

With a fan-out of one, for example, using a 12 pF capacitor to load down the output to simulate wiring capacitance, the measured propagation delay is approximately 3.1 ns. With a fan-out of 12, the delay increases to about 5.5 ns. Each loading stage, therefore, is seen to introduce an additional delay of approximately 0.25 ns. This corresponds to an input capacitance of about 6 pF.

ECL Advantages. In comparison with other forms of logic, the current mode operation of ECL circuits has a number of basic advantages. These circuits are extremely fast. Propagation delay is very small, since the logic decisions are performed at the low impedance level of the common-emitter node, the signal paths are essentially through emitter followers and grounded base stages, and the transistors in these circuits never become saturated. This eliminates the parameter of storage time which represents one of the primary speed-limiting factors of saturated circuit designs.

ECL current mode logic, in addition, is uniquely tolerant of component values. Absolute values of resistors are relatively unimportant so long as the proper ratios between circuit resistances are maintained. This feature is particularly important in integrated circuit technology where absolute parts values are difficult to achieve but where resistance ratios can be held to very close tolerances.

ECL current mode circuits produce unexcelled DC stability and are noncritical of transistor parameters. These features, too, are of particular importance with integrated circuits where hundreds of complete circuits are processed simultaneously on a single wafer of silicon. A high tolerance to parameter variations can make the difference between acceptance and rejection of entire lots, thus greatly affecting the yield—and, ultimately, the price—of the integrated circuit modules.

Low noise and crosstalk are additional advantages gained by the favorable impedance levels of the ECL circuits. Because input impedance is high, inductive crosstalk currents between adjacent signal lines are held to a minimum. Because output impedance is low, capacitive crosstalk in the output is minimized. Moreover, noise generated in power supply and ground lines is practically nonexistant because of the constant current property of this type of design.

Exercises (020):

1. State the basic function of the five-input ECL circuit.

2. What design feature enables the ECL to operate with an exceptionally low propagation time?

3. What is the state of Q7 with no inputs to the circuit?

4. How does the circuit function with negative logic?

5. In high-speed applications, fan-out generally is considerably less than ________ .

6. ECL current mode circuits produce unexcelled ________ stability.

021. Specify design and operating characteristics of the two-input TTL NAND integrated circuit.

Basic TTL Circuit (NAND). All transistor-transistor logic integrated circuits are derived from the simple gate schematic shown in figure 1-55. The output is *low* only if both inputs A and B are *high*. This is defined as a positive logic NAND-gate.

The circuit consists of three stages: an input stage associated with multiple emitter transistor Q1, a switching transistor Q2 (sometimes referred to as a phase splitter), and a totem pole or active pull-up output stage Q3/Q4. The NAND function is performed by Q1 and Q2, while Q3 and Q4 make up the output drive circuitry for a logic 0 and logic 1, respectively. In order to explain the operation of the TTL circuit, we will analyze it first under a logic 0 input condition and then under a logic 1 input condition.

If either or both inputs A and B are at zero volts (a logic low level) the input transistor Q1 will conduct. Q1 conducting will effectively place the base of Q2 at zero volts, which cuts Q2 off. With Q2 cut off the voltage at the collector of Q2 (base of Q4) raises to near V_{CC} (+5 volts) and turns on Q4. Under these conditions, the drop across R3 the emitter resistor of Q2 is near zero. This puts an effective zero volts on the base of Q3, which cuts

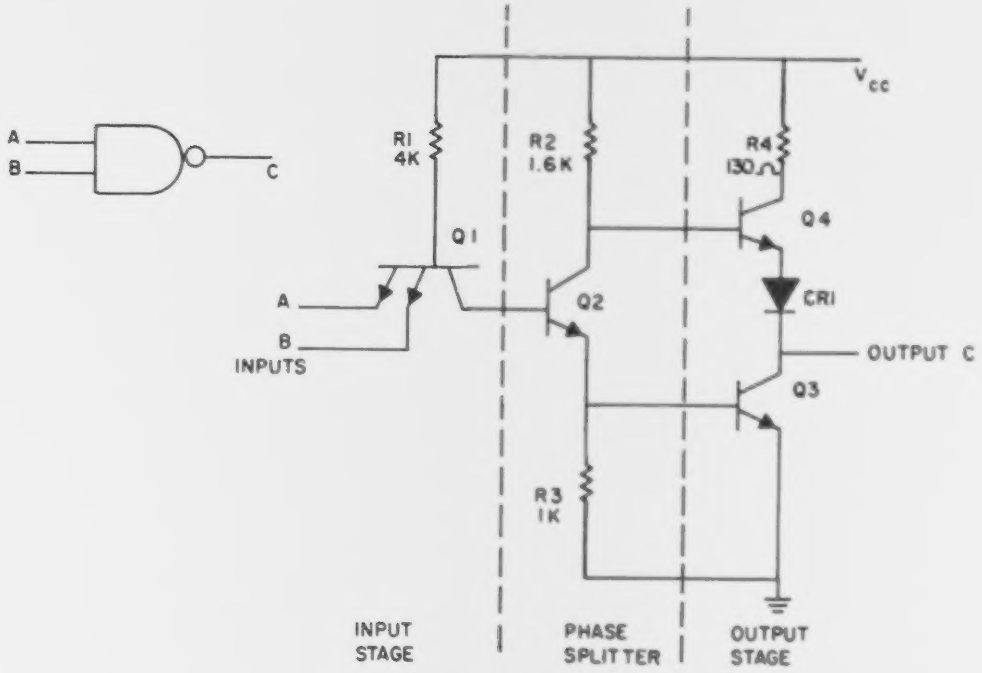


Figure 1-55. Basic TTL circuit (NAND).

it off. The high voltage at the output C will be near +5 volts a logic high level. With TTL logic this will be approximately +3.5 volts.

If both inputs are raised to something greater than +2.5 volts (a logic high level) input transistor Q1 cuts off. The voltage on the base of Q2 will raised accordingly and Q2 begins to conduct. As Q2 turns on it supplies base current to Q3, causing it to conduct also. The collector voltage of Q2 will drop, causing Q4 to cut off. When Q3 is fully turned on (saturated), it sinks current from any load connected to the output terminal and keeps the output terminal at a logic low. Thus, with a zero volts (logic low) on either or both inputs, between 3.5 and 5 bolts will appear on the output (logic high); and conversely, if the inputs are both high 2.5 to 5 volts the output will be zero volts or low. The TTL circuit diagrammed in figure 1-55 has one output and two inputs. To get additional inputs, additional emitters could be put on Q1. Whie a transistor with several emitters may look unusual, be assured that it operates like any transistor; that is, if B-E current flows, the collector will be pulled down toward the emitter. Having multiple emitters on Q1 allows the device to be made smaller; and therefore cheaper, than an IC with separate transistors. So the real contribution of TTL is the input circuitry, although the totem pole is also a good feature.

Exercises (021):

1. List the sections of the basic TTL gate (NAND).

2. Which transistors constitute the NAND-circuit?

3. Which transistor keeps the output at a logical low?

4. What is determined by R1?

5. When is Q4 turned on?

5. When is Q4 turned on?

1-3. Boolean Algebra

Boolean algebra provides an economical, straightforward way of describing the circuitry used in computers. It also enables the logic designer to simplify the circuitry used. When applied to digital computers, the simplest form of the Boolean expression is the one that will be programmed. This reduces costly steps and saves time in computer operation.

022. Define Boolean algebra symbols.

Symbols of Boolean Algebra. The father of Boolean algebra is George Boole, an English logician and mathematician, who in the spring of 1847 presented a pamphlet on symbolic logic. He later (1854) presented a much expanded text on which are founded the mathematical theories presently used for the analysis of logical processes. A close analogy exists between the symbolic language used by Boole to express logical forms and relationships and the symbology used in algebra to express mathematical forms and relationships, hence the term "Boolean algebra." In fact, an examination of the table of Boolean connectives and variables, table 1-1, will show that the symbols and connectives used are the same; however, their meanings and usage may have been modified to fit a particular application.

Exercises (022):

1. Either the dot or a small ________ may be used to show the ________ operation.
2. The vinculum indicates that the terms overlined are to be ________ .
3. The plus sign denotes that the terms are to be ________ .

023. State the uses, rules, and characteristics of Boolean algebra; derive Boolean equations and truth tables from logic diagrams; construct logic diagrams from Boolean equations.

Basic Boolean Logic Functions. All logic diagrams and Boolean equations in the Boolean system consist of three basic functions: OR, AND, and NOT logic. Let's review these briefly before we consider more complex equations and diagrams.

OR-gate. The OR-gate performs the OR function. The OR-gate has a high output with any input (or when all of its inputs are high). Understand that the term "input" in logic means a high or a low signal applied to the input terminals. There is either a *high* input or a *low* input. The same is true with regard to the output; there is either a *high* output or a *low* output. Figure 1-56 shows the logic symbol for a two-input OR-gate.

TABLE 1-1

TABLE OF BOOLEAN CONNECTIVES AND VARIABLES

=	The equal sign, just as in conventional mathematics, represents a relationship of equivalence between the expressions so connected.
· or x	The dot or small x indicates the logical product, or conjunction of the terms so connected. The operation is also frequently indicated with no symbol used, i.e., A·B = A x B = AB. Most generally referred to as the AND operation, the terms so related are said to be "ANDed."
+	The plus sign indicates the logical sum operation, a disjunction of the terms so connected. Usually called the OR operation and the terms so connected are said to be ORed.
——	The vinculum serves a dual purpose. It is at the same time a symbol of grouping and of operation. As a sign of operation it indicates that the term(s) so overlined are to be complemented. As a symbol of grouping it collects all terms to be complemented together. Terms so overlined are often said to be NEGATED, the process of taking the complement is then called NEGATION.
( ) [ ]	These familiar signs of grouping are used in the customary fashion to indicate that all terms so contained are to be treated as a unit.
A,B, etc.	Various letters are used to represent the variables under consideration, generally starting with A. Since the variables are capable of being in only one of two states, the numerals 0 and 1 are the only numbers used in a Boolean expression.

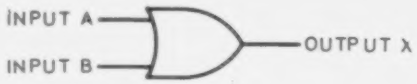


Figure 1-56. Two-input OR-gate.

The basic rules for the two-input OR-gate are shown in figure 1-57. Rule 1 states that A is low and B is low, so output X is low. This follows the definition of the OR-gate given earlier, which states: "With low inputs present, there will be a low output from the OR-gate." Rule 2 states X is high since A is high. Rule 3 states X is high because B is high. Rule 4 states X is

	A	B	X	
1.	0	0	0	READ AS: NOT A, NOT B = NOT X
2.	1	0	1	READ AS: A, NOT B = X
3.	0	1	1	READ AS: NOT A, B = X
4.	1	1	1	READ AS: A + B = X

REP4-2083

Figure 1-57. Rules for two-input OR-gate.

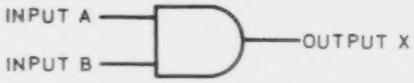


Figure 1-58. Two-input AND-gate.

high since A or B is high. Both inputs need not be high to produce X, since the definition for the OR-gate states the OR-gate will have a high output when any of its inputs are high. Thus, the OR-gate is an "any or all" gate.

AND-GATE The AND-gate (fig. 1-58) performs the AND function. This gate will have an output only when all of its inputs are high. When any of the inputs are low, the output will be low. Thus, the AND-gate is an "all or nothing" gate.

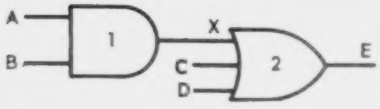
	A	B	X	
5.	0	0	0	READ AS: NOT A, NOT B = NOT X
6.	0	1	0	READ AS: NOT A, B = NOT X
7.	1	0	0	READ AS: A, NOT B = NOT X
8.	1	1	1	READ AS: A·B = X

REP4–2085

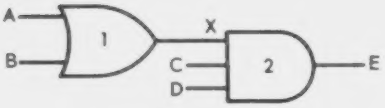
Figure 1-59. Rules for two-input OR-gate.

The basic rules for the two input AND-gate are given in figure 1-59. Rule 5 states that A is low, B is low, and therefore X is low. Rule 6 shows that A is low and B is high and X is low. Rule 7, indicates that A is high, B is low, and X remains low. Rule 8 states that both A and B are high and this results in X also being high.

Equations From Logical Diagrams. For the OR-circuit of figure 1-56, the Boolean equation is written as A + B = X. Translating verbally, this becomes: "If inputs A or B, or both, are high there will be a high output X." Further, this output will be high as long as any of the inputs are high.



A. **OR Matrix**



B. **AND Matrix**

Figure 1-60. Matrices.

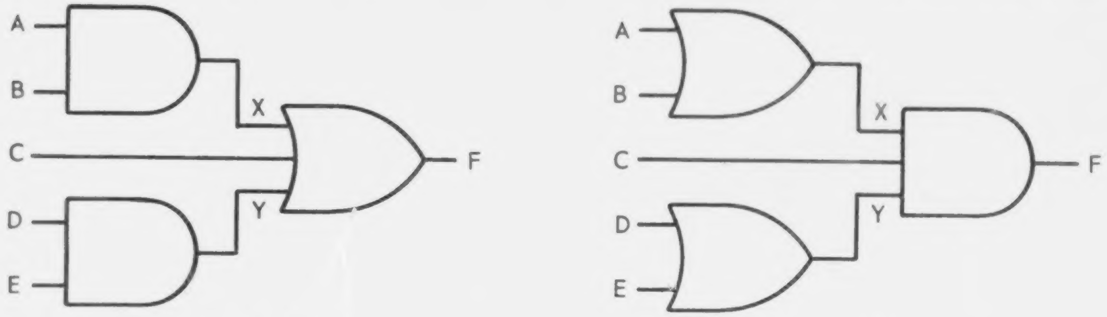
A Boolean equation for figure 1-58 is written as A · B = X, or AB = X. If the equation is translated verbally, it becomes: "If, and only if, inputs A and B are high at the same time, there will be a high output X." Further, this output will be high only for the duration of time that both inputs are high.

When writing equations for logic diagrams which have an AND-circuit feeding an OR-circuit, or vice-versa, a problem of grouping within the equation arises. A system which will allow systematic expansion of the functions within an expression is required.

Figure 1-60,A, is an AND-gate feeding an OR-gate. This logic diagram is called an OR matrix. Only four primary inputs are involved; writing the equation for this diagram, however, is more complex.

Designating the output of the AND-gate (1) in figure 1-60,A, as X simplifies the problem. The equation for the OR-gate (2) is X + C + D = E. The equation for the AND-gate is AB = X. Therefore, the equation for the output E is AB + C + D = E; this equation describes the structure of the logic diagram.

Figure 1-60,B, shows an OR-gate feeding an AND-gate. This logic diagram is called an AND matrix. Similarly, there are still only four primary inputs



(A)
OR MATRIX

(B)
AND MATRIX

Figure 1-61. Three-gate matrices.

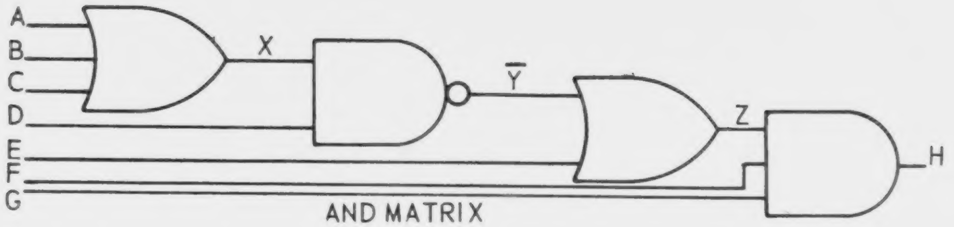


Figure 1-62. Building a Boolean equation.

involved. Again, we can simplify the problem by designating the output of the OR-gate (1) as X. The simplified equation for the AND-gate (2) becomes XCD = E. X taken by itself is stated as A + B = X. Combining the equation A + B with CD, directly would result in A + BCD, which gives a false impression of the overall structure. To insure that logic diagrams are not misunderstood, signs of groupings must be used for the separation of terms. Thus the term "A + B" is placed within parentheses (A + B) to indicate that A and B are to be combined in an OR-gate before the complete quantity is combined in the AND-gate with signals C and D to make up the output signal E. The correct equation becomes (A + B) CD = E. Other signs of grouping will be discussed as they are required.

Figure 1-61,A, illustrates two AND-gates feeding an OR-gate. This is an OR matrix because the final gate is an OR-gate. Therefore, in the same manner as before, the AND-gate outputs may be designated as "X and Y" to simplify writing the equation.

The equation for the OR-gate becomes X + C + Y = F. Working with the AND-gates, AB = X and DE = Y. Substitute the quantities of X and Y in the overall equation. Thus, AB + C + DE = F. Note that the original structure is retained, and each AND function is treated as a single quantity.

Figure 1-61,B, illustrates an AND matrix. A simplified equation for the AND-gate may be written as XCY = F, A + B = X, and D + E = Y. At this time, substitute the quantities for X and Y in the overall equation. Remember, anytime an OR-gate feeds an AND-gate, signs of grouping must be used to indicate the OR-quantity. Thus, the final equation becomes (A + B)C(D + E) = F. Again, we retain the original diagram structure.

The diagram in figure 1-62 represents an AND matrix having three inputs. Letters X, Y, and Z are considered to be secondary inputs. Working in the same manner as before, the simplified equation becomes ZFG = H. In a step-by-step process, the final equation is developed as follows:

(1) ZFG = H.
(2) $\overline{Y}$ + E = Z, substitute for Z.
(3) ($\overline{Y}$ + E)FG = H.
(4) XD = $\overline{Y}$, substitute for $\overline{Y}$.
(5) ($\overline{XD}$ + E)FG = H.
(6) A + B + C = H, substitute for X.
(7) $[\overline{(A + B + C)D} + E]FG = H$. This is the complete equation for figure 1-62.

In step 5, we placed the OR function in parentheses to retain the given quantity: (XD + E). Within this quantity exists another quantity A + B + C, represented by X. To maintain identity and correct separation, the quantity of A + B + C requires grouping signs. The algebraic rule is to inclose the inner group in parentheses and then place the total expression in brackets, as in step 7.

We can find the output expression for a logic diagram, begin at the left and find the output of each logic symbol (see fig. 1-63).

(1) To find the output expression for a logic diagram, begin at the left and find the output of each logic symbol (see fig. 1-63).

(2) If a logic symbol is at the extreme left of the diagram, its inputs are single letters (see fig. 1-63).

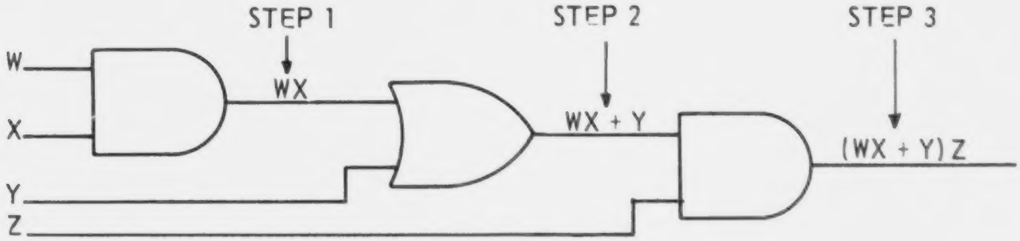


Figure 1-63. Grouping terms.

(3) An input signal to any symbol NOT at the extreme left may be represented by two or more letters. These letters should remain grouped in the output expression (see fig. 1-64).

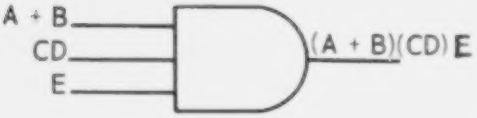


Figure 1-64. Using parentheses.

(4) Parentheses are used to indicate grouping, except for an ANDed input to an OR or NOT logic symbol (see fig. 1-65).

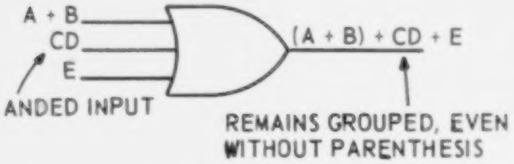


Figure 1-65. Parentheses not required for ANDed inputs.

(5) If additional grouping signs are necessary for an expression that already contains parentheses, use brackets (see fig. 1-66).

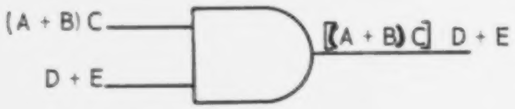


Figure 1-66. Using brackets.

(6) The vinculum is used to group the portion or portions of the output expression that have been inverted (see fig. 1-67).

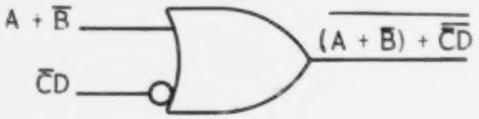


Figure 1-67. Using the vinculum.

Logical Diagrams From Equations. Simple equations, such as $ABCD = E$ or $A + B + C + D = E$, offer no particular problem in drawing the correct logic diagram. Also, the equation $(A + B)(C + D) = E$ should offer no problem, because it is an overall AND matrix with two inputs, each of which is an OR-gate having two inputs. Following through in the manner previously explained, designate one OR quantity as X and the other as Y. The diagram becomes an AND-gate with X and Y inputs. Then expand X and Y to show the complete structure. The diagram is shown in figure 1-68.

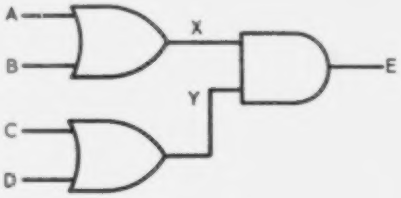


Figure 1-68. Overall AND matrix.

For the purpose of explanation, let's diagram the following equation step-by-step. Equation: $[(A + B + C)(D + E) + F + G(H + I)] J = K$.

(1) Identify the overall equation as a two-input, AND matrix J AND Z, where Z represents the quantity within the brackets.

(2) Draw a logic symbol of an AND-gate with J and Z inputs (fig. 1-69).

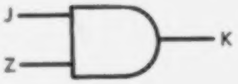


Figure 1-69. Example equation - step 2.

(3) Identify Z as a three-input OR-gate: $(A + B + C)(D + E) + F + G (H + I) = Z$ (Observe that three quantities are connected by two plus signs.)

(4) Draw an OR-gate with the three inputs, W, F, and Y, where W represents $(A + B + C)(D + E)$ and Y represents $G (H + I)$ (fig. 1-70).

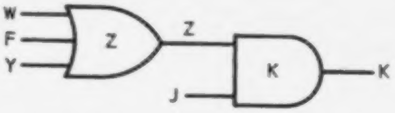


Figure 1-70. Example equation - step 4.

(5) Draw two AND-gates, one for W and one for Y (fig. 1-71).

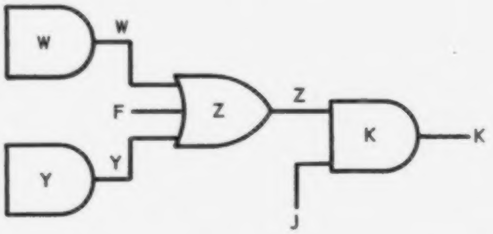


Figure 1-71. Example equation - step 5.

(6) Identify the two inputs to AND-gate Y as G and V, where V represents (H + I).

(7) Develop input V by drawing a two-input OR-gate and labeling the inputs H and I (fig. 1-72).

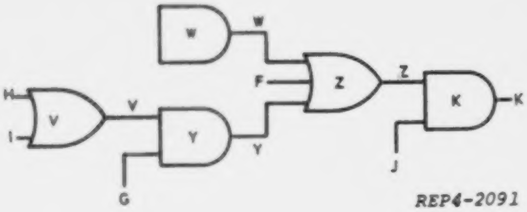

W
W
F
Z
Z
K
K
H
I
V
V
Y
Y
G
J
REP4-2091

Figure 1-72. Example equation - step 7.

(8) Identify the two inputs to AND-gate W as U and T, where U represents A + B + C and T represents D + E. (Follow this step and the last two steps by use of fig. 1-73.).

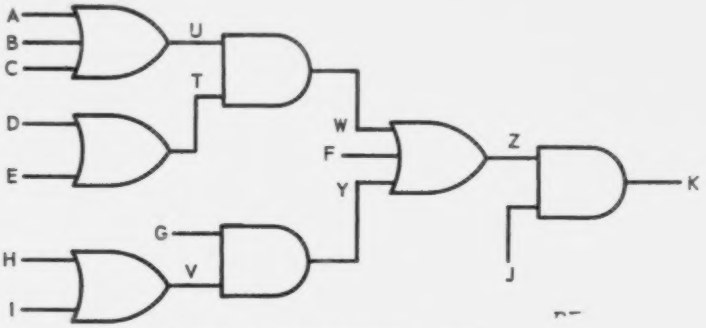

A
B
C
U
T
D
E
W
F
Y
Z
K
G
H
V
I
J

Figure 1-73. Example equation - step 8.

(9) Draw the OR-gate for U and label the inputs A, B, and C.

(10) Draw the OR-gate for T and label the inputs D and E.

The diagram is now complete as shown in figure 1-73. Check the completed drawing for errors by writing the Boolean equation from the diagram.

We can summarize how to construct a logic diagram from an output expression by means of the following five-step procedure:

(1) Begin drawing at the right and work left until all inputs are single letters.

(2) Never separate letters within a group until that group has been separated from the rest of the expression, as illustrated in figure 1-74.

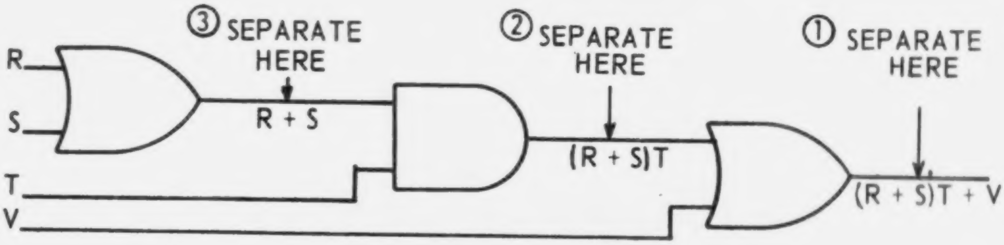

③ SEPARATE HERE
R + S
② SEPARATE HERE
(R + S)T
① SEPARATE HERE
(R + S)T + V
R
S
T
V

Figure 1-74. Constructing a logic expression.

(3) When an expression contains a vinculum, do not remove the vinculum until you have isolated this part of the expression from the rest of the expression, and do not separate the letters under the vinculum until you have removed the vinculum (see fig. 1-75).

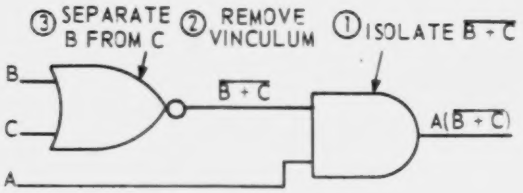
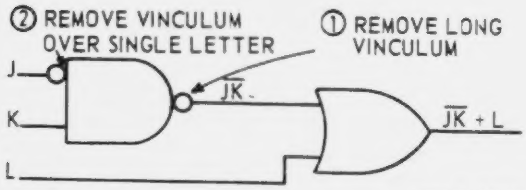

③ SEPARATE B FROM C
② REMOVE VINCULUM
① ISOLATE $\overline{B+C}$
B
C
A
$\overline{B+C}$
$A(\overline{B+C})$

Figure 1-75. Removing vinculum.

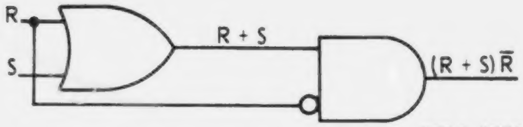
(4) If a vinculum extends over more than one letter, use a NOR or NAND symbol to remove it. If a single letter is inverted, use a NOT symbol on the input as shown in figure 1-76.


② REMOVE VINCULUM OVER SINGLE LETTER
① REMOVE LONG VINCULUM
J
K
L
$\overline{\overline{J}K}$
$\overline{\overline{J}K} + L$

REP4-1577

Figure 1-76. Vinculum vs "NOT."

(5) If a single letter is an input to more than one logic symbol, connect input lines with a dot as illustrated in figure 1-77.


R
S
R + S
$(R + S)\overline{R}$

REP4-1578

Figure 1-77. Same input to more than one gate.

Exercises (023):

1. What is one of the main or practical uses of Boolean algebra?

2. In Boolean algebra, the • (dot) sign means ______ and the + (plus) sign means ______ .

3. Parentheses and brackets are used for ______ .

4. A line over a letter or group of letters is called a ______ .

5. The vinculum indicates the ______ or ______ function.

6. The ______ ______ is used in diagramming an expression with a vinculum.

7. In diagramming an equation, the gate on the ______ is drawn first.

8. The vinculum cannot be used as a grouping sign. (True/False)

9. Each grouping in the expression can be represented by a single gate. (True/False)

10. The three logical functions are ______ , ______ , and ______ .

11. Draw the logic diagram for each of the following equations:
    a. $[(\overline{AB+C}) \bullet D] + E \backslash q\ X$
    b. $A \cdot B + C + \overline{D} \cdot \overline{E} = Z$

12. Write the Boolean equation for each of the following logic diagrams:
    a. Diagram of Boolean expression shown in figure 1-78.

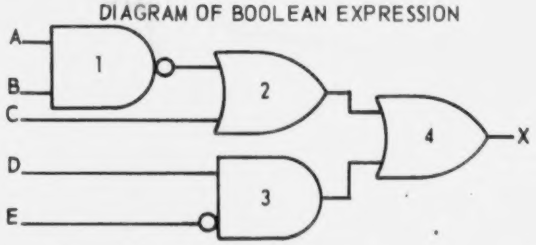


DIAGRAM OF BOOLEAN EXPRESSION
A
B
C
D
E
1
2
3
4
X

Figure 1-78. Figure for objective 023, exercise 12a.

b. Diagram of Boolean expression shown in figure 1-79.

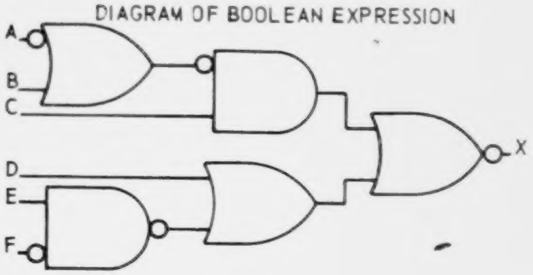
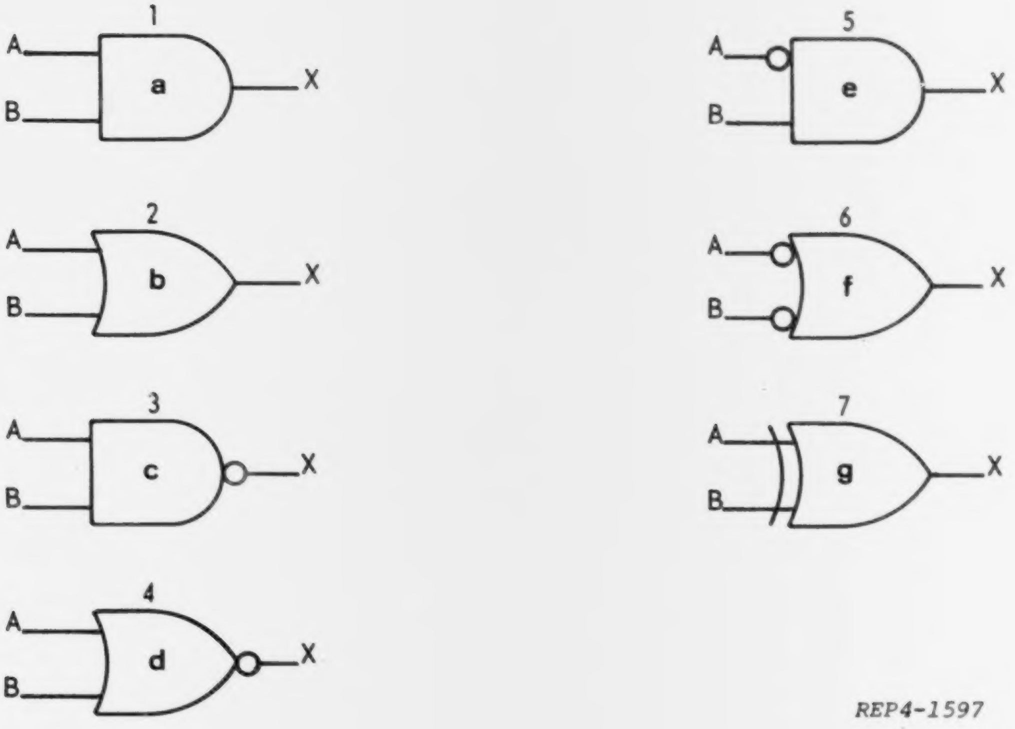


DIAGRAM OF BOOLEAN EXPRESSION
A
B
C
D
E
F
X

Figure 1-79. Figure for objective 023, exercise 12b.

13. Identify the logic symbols and complete the truth table shown in figure 1-80.

A	B	X1	X2	X3	X4	X5	X6	X7
L	L							
L	H							
H	L							
H	H							


1
A
B
a
X
2
A
B
b
X
3
A
B
c
X
4
A
B
d
X
5
A
B
e
X
6
A
B
f
X
7
A
B
g
X

REP4-1597

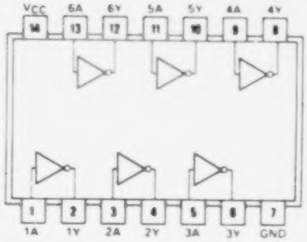
Figure 1-80. Figure for objective 023, exercise 13.

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

06

**HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS**

positive logic:
Y = $\overline{A}$

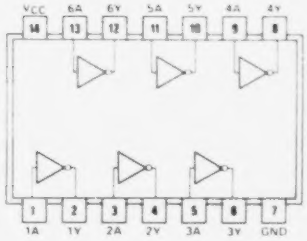

VCC
6A
6Y
5A
5Y
4A
4Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1Y
2A
2Y
3A
3Y
GND

SN5406/SN7406(J, N, W)

16

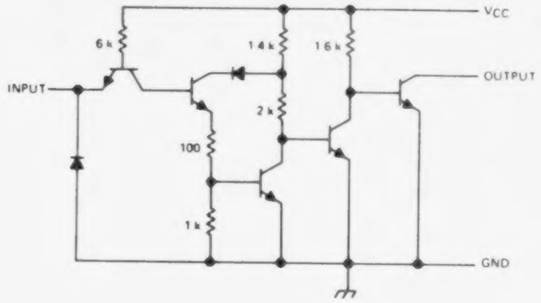
**HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS**

positive logic:
Y = $\overline{A}$


VCC
6A
6Y
5A
5Y
4A
4Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1Y
2A
2Y
3A
3Y
GND

SN5416/SN7416(J, N, W)

schematics (each gate)


VCC
6 k
1.4 k
1.6 k
INPUT
OUTPUT
2 k
100
1 k
GND

'06, '16 CIRCUITS

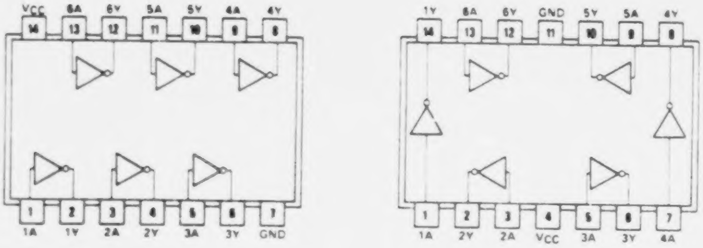
Figure 1-81. Hex inverter buffers/drivers with open-collector high-voltage outputs.

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

04

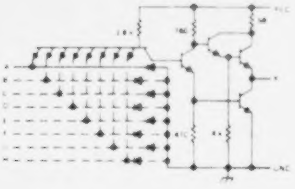
HEX INVERTERS

positive logic:
Y = $\overline{A}$



SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)

SN5404/SN7404(W)
SN54H04/SN74H04(W)
SN54L04/SN74L04(T)



'H00, 'H04, 'H10, 'H20, 'H30 CIRCUITS

Resistor values shown are nominal and in ohms.

Figure 1-82. Circuit types SN54H04, SN74H04 hex inverters.

14. Draw the logic diagrams for the following Boolean equations:
    a. $(\overline{AB} + C)(\overline{D}\,E) = X$

    b. $[(\overline{AB} + CD)(\overline{E} + \overline{F})] + G + H = X$

1-4. Digital Integrated Circuits (DICs)

So far in our discussion of logic circuits, we have explained the discrete forms of logic circuits using individual components and described some of the basics concerning integrated circuits. In this section we will concentrate on the most widely used form of integrated digital logic circuits known as TTL or transitor-transitor logic. TTL is best represented by the SN54/74 series of DICs. Texas Instruments Corporation originally developed this series of logic ICs, but a number of manufacturers make them and use the same numbering system.

024. Identify the diagrams of TTL ICs, and specify the characteristics of the TTL logic family.

The TTL Logic Family. The SN54 (SN stands for Semiconductor Network) series is more expensive and designed for a greater temperature range than the SN74 series. The SN54 devices will operate over a range of temperature from -55 to 125° Centigrade, whereas the SN74 devices operate over a range from 0 to 70° Centigrade.

TTL ICs operate on a power supply voltage of 5 volts and require a well-regulated 5-volt power source. The most common IC packages available in TTL are the 14 or 16 pin dual in-line package. Larger packages such as the 20, 24, and 28 pin Dips usually consist of medium or large scale integrated circuits. The listing below identifies the different versions of TTL available, the power requirements per gate, and operating speed:

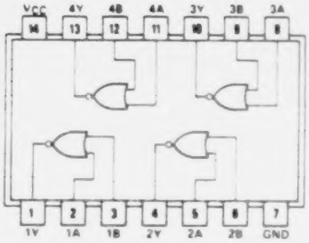
Version		*Power/Gate Speed*
		10mW35MHz
SN54/74	Standard	22mW50MHz
SN54H/74H	High Speed	1mW 3MHz
SN54L/74L	Low Power	19mW125MHz
SN54S/74S	Non-saturating/Schottky	
SN54LS/74LS	Low-power Schottky	2mW45MHz

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

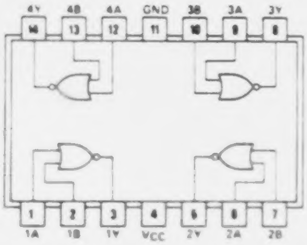
02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B}$

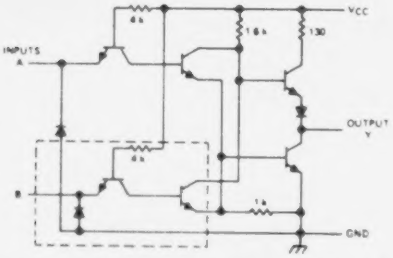


SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)



SN5402/SN7402(W)
SN54L02/SN74L02(T)

schematics (each gate)



The portion of the schematic within the dashed lines is repeated for the C input of the '27.

'02, '27 CIRCUITS

Figure 1-83. SN7402 quadruple two-input positive NOR-gates.

Analyzing the power and speed characteristics shows that if you want low power in a TTL IC, you will have to sacrifice speed, and vice-versa.

Schottky TTL uses a Schottky barrier diode between base and collector of internal transistors to prevent saturation. The Schottky diode switches very fast and requires only 0.1 to 0.3 volts of forward bias, depending on temperature. When this diode is added, speed is increased because the time required to get a transistor out of saturation is not a factor. The diode will conduct before the transistor is allowed to saturate. Any kind of non saturating logic is inherently faster than saturating logic.

The logical output for a TTL gate at binary 1, in positive logic, is approximately 3 volts. For a binary 0, the output voltage of a gate is usually 0.8 volt or less. TTL logic should never be subjected to voltages greater than 5.25 volts nor any negative voltage. Any noise voltage in TTL logic should be less than 1.0 volt in order to prevent erratic operation. A well regulated power supply for TTL logic is a necessity to prevent damage to the logic and erratic operation of the logic circuits.

The different versions of TTL may be mixed in a logic circuit depending on design requirements. This proves beneficial because some of the logic circuits must operate faster than others so that circuit outputs arrive at their destinations at the proper time.

The following DICs are representative of the types available in TTL form. The ones included here are similar to the discrete gates that have already been discussed. Logic diagrams will show the individual symbols for gates or inverters and will indicate that the gate is part of a particular IC package. The TO or manufacturer's literature will describe how the logic diagram for that particular piece of equipment is read and interpreted.

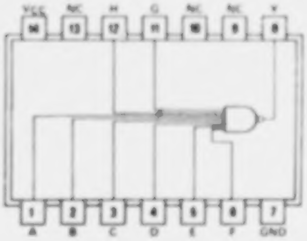
The digital integrated circuits that are presented in this section are from either "The TTL Data Book for Design Engineers" or "Supplement to the TTL Data Book for Design Engineers," CC-411 and CC-416, published by the Texas Instruments Corporation, Dallas, Texas. Because of the unusually well organized manner of presentation of the material covered, we will not deviate from their format. Both of the books are excellent references when the individual

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

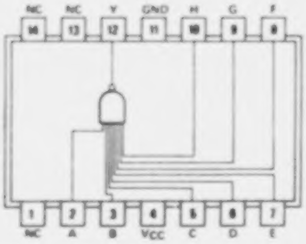
30

8-INPUT POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCDEFGH}$



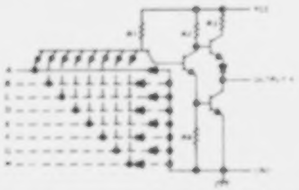
SN5430/SN7430(J, N)
SN54H30/SN74H30(J, N)
SN54L30/SN74L30(J, N)
SN54LS30/SN74LS30(J, N, W)
SN54S30/SN74S30(J, N, W)



SN5430/SN7430(W)
SN54H30/SN74H30(W)
SN54L30/SN74L30(T)

NC—No internal connection

schematics (each gate)



CIRCUIT	R1	R2	R3	R4
'00, '04, '10, '20, '30	4 k	1.6 k	130	1 k
'L00, 'L04, 'L10, 'L20, 'L30	40 k	20 k	500	12 k

'00, '04, '10, '20, '30
'L00, 'L04, 'L10, 'L20, 'L30, CIRCUITS

Input clamp diodes not on
SN54L'/SN74L' circuits.

Figure 1-84. SN54H30, SN74H30 eight-input positive NAND-gates.

technician might have a question on a device but might not be able to locate the information in the appropriate technical manual.

Hex Inverter Buffers/Drivers. Types SN5406, SN5416, SN7406, and SN7416 are shown in figure 1-81. These are typical monolithic integrated circuits which feature high-voltage, open-collector outputs for interfacing with high-level circuits (such as MOS) or for driving high-current loads (such as lamps or relays). They also can be used for driving TTL inputs when used as inverter buffers. Additional functions of this circuit are shown in figure 1-81.

Hex Inverters. Types SN54H04 and SN74H04, shown in figure 1-82, are high-speed TTL devices. The circuit performs a simple inversion of the input logic level. The explanatory Boolean expression $Y = \overline{A}$ portrays the operation.

Quadruple Two-Input Positive NOR-Gates. The type SN7402, shown in figure 1-83, is the standard IC NOR-gate configuration. The operation of this circuit is expressed by the Boolean equation, $Y = \overline{A + B}$. Both of the types of IC packages are shown. The S-flat package configuration differs from the J or N DIPs not only in physical appearance but also in pin assignment numbers. The J package is made of ceramic, whereas the N package is plastic. Many of the common integrated circuits are produced in more than one physical package type.

Eight-Input Positive NAND-Gates. Refer to figure 1-84. Circuit types SN54H30 and SN74H30 are shown. The pin connections for the two package types are shown also. The Boolean expression is $Y = \overline{ABCDEFGH}$.

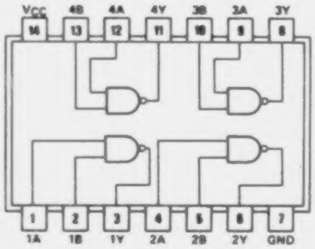
Quadruple Two-Input High-Voltage Interface NAND-Gates. Types SN5426 and SN7426 are shown in figure 1-85. They operate, logically, just like standard NAND-gates. The Boolean equation is $Y = \overline{AB}$. These are open collector NAND-gates which feature high-output voltage ratings for interfacing with low threshold voltage MOS logic circuits or other 12-volt systems. Open collector outputs permit tying a number of gate outputs to one pull-up resistor and implementing the wired OR function. These features differentiate these particular NAND-gates from standard NAND-gate functions.

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

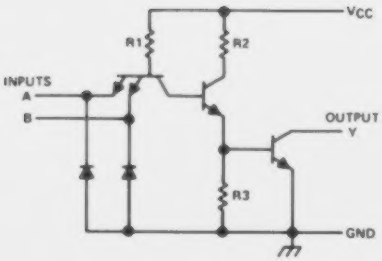
26

**QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES**

positive logic:
$Y = \overline{AB}$



SN5426/SN7426(J, N)



CIRCUITS	R1	R2	R3
'26	4 kΩ	1.6 kΩ	1 kΩ
'38	4 kΩ	600 Ω	400 Ω

'26, '38 CIRCUITS

Figure 1-85. SN5426, SN7426 quadruple two-input high-voltage interface NAND-gates.

Quadruple Two-Input Positive NAND Buffer. Types SN5437 and SN5438, are shown in figure 1-86. Logically, their output is low only when all inputs are high. These devices will drive three times as many loads as the same NAND-gates of the SN7400 series. The SN5438/SN7438 are also NAND-gates but have open-collectors similar to SN7403. See the figure for more details.

Quadruple Two-Input Exclusive OR-Gates. Types SN5486 and SN7486 are shown in figure 1-87. The Boolean equations for these gates is $Y = \overline{A}\,B + A\overline{B}$.When the input states are complementary, the output goes to a logic 1. Additional information is given in figure 1-87.

Exercises (024):

1. If you need a TTL IC to operate at a clock frequency of 100 MHz, what version of the SN54/74 series would you use?

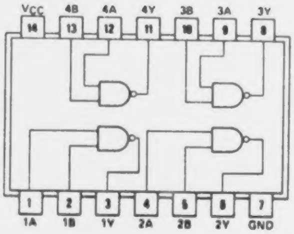
2. What series of TTL would you use in an extreme temperature environment?

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

37

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

positive logic:
Y = $\overline{AB}$



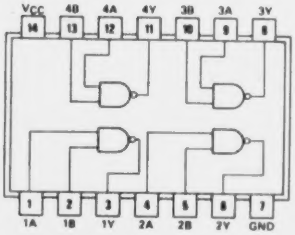
VCC
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND

SN5437/SN7437(J, N, W)
SN54LS37/SN74LS37(J, N, W)

38

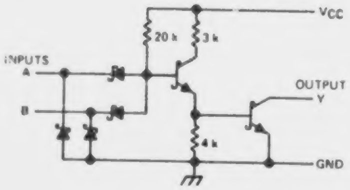
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
Y = $\overline{AB}$



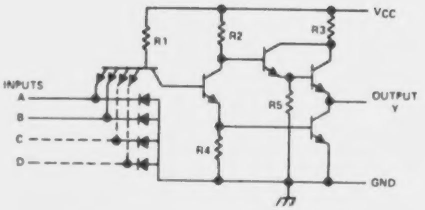
VCC
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND

SN5438/SN7438(J, N, W)
SN54LS38/SN74LS38(J, N, W)



VCC
20 k
3 k
INPUTS
A
B
OUTPUT
Y
4 k
GND

'LS38 CIRCUITS



VCC
R1
R2
R3
INPUTS
A
B
C
D
R5
R4
OUTPUT
Y
GND

'37, '40, 'H40 CIRCUITS

	'37	'40	'H40
R1	4 k	4 k	1.4 k
R2	600	600	390
R3	100	100	45
R4	400	400	250
R5	4 k	4 k	2 k

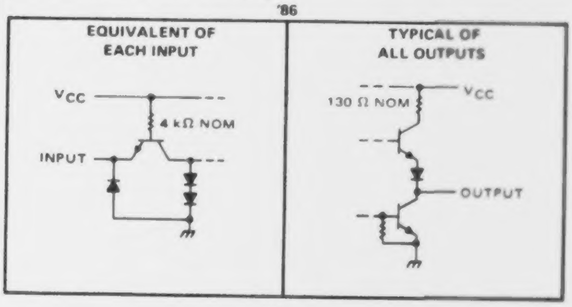
Figure 1-86. Quadruple two-input positive NAND buffer.

TYPES SN5486, SN54L86, SN54LS86, SN54S86, SN7486, SN74L86, SN74LS86, SN74S86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

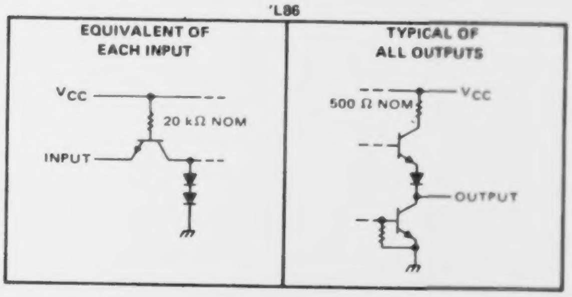
BULLETIN NO. DL-S 7211825, DECEMBER 1972

schematics of inputs and outputs

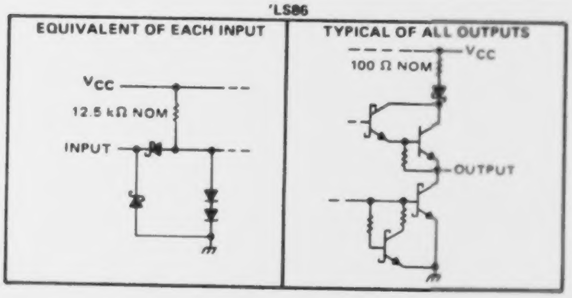
'86


EQUIVALENT OF EACH INPUT
TYPICAL OF ALL OUTPUTS
V_{CC}
4 kΩ NOM
INPUT
130 Ω NOM
V_{CC}
OUTPUT

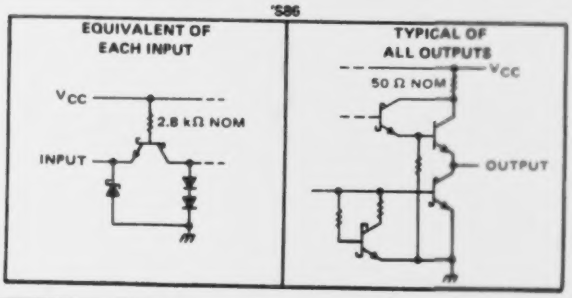
'L86


EQUIVALENT OF EACH INPUT
TYPICAL OF ALL OUTPUTS
V_{CC}
20 kΩ NOM
INPUT
500 Ω NOM
V_{CC}
OUTPUT

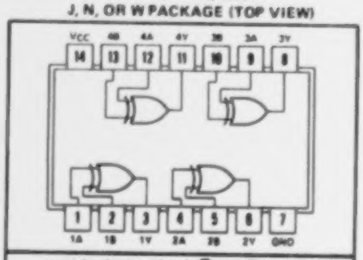
'LS86


EQUIVALENT OF EACH INPUT
TYPICAL OF ALL OUTPUTS
V_{CC}
12.5 kΩ NOM
INPUT
100 Ω NOM
V_{CC}
OUTPUT

'S86

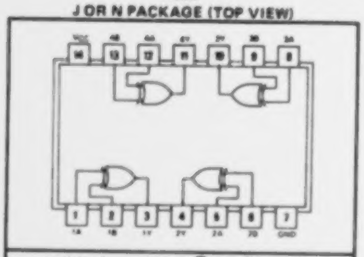

EQUIVALENT OF EACH INPUT
TYPICAL OF ALL OUTPUTS
V_{CC}
2.8 kΩ NOM
INPUT
50 Ω NOM
V_{CC}
OUTPUT

'86, 'LS86, 'S86
J, N, OR W PACKAGE (TOP VIEW)


VCC
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND

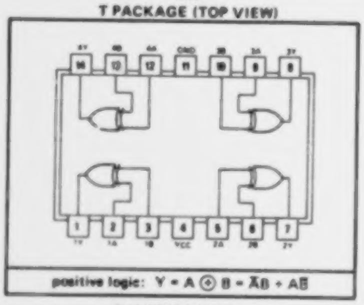
positive logic: Y = A ⊕ B = $\bar{A}B + A\bar{B}$

'L86
J OR N PACKAGE (TOP VIEW)


VCC
4B
4A
4Y
3Y
3B
3A
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2Y
2A
2B
GND

positive logic: Y = A ⊕ B = $\bar{A}B + A\bar{B}$

'L86
T PACKAGE (TOP VIEW)


4Y
4B
4A
GND
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1Y
1A
1B
VCC
2A
2B
2Y

positive logic: Y = A ⊕ B = $\bar{A}B + A\bar{B}$

FUNCTION TABLE

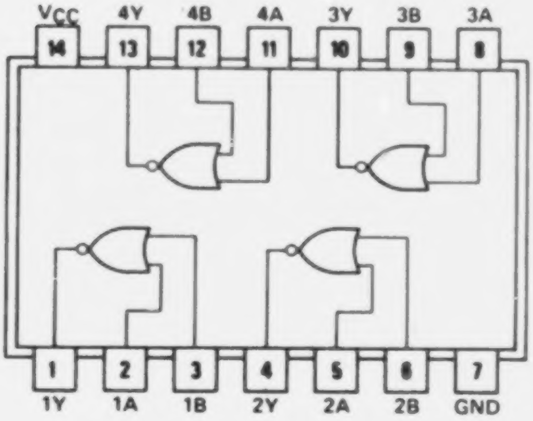
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'L86	55 ns	15 mW
'LS86	10 ns	30.5 mW
'S86	7 ns	250 mW

Figure 1-87. SN5486, SN7486 quadruple two-input EXCLUSIVE OR-gates.

3. The circuit shown in figure 1-88 is what type of IC?


VCC
4Y
4B
4A
3Y
3B
3A
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1Y
1A
1B
2Y
2A
2B
GND

positive logic:

$Y = \overline{A+B}$

Figure 1-88. S-flat package/J or N dual-in-line package (top views) (objective 024, exercise 3).

4. The SN74LS04J has what kind of logic circuit in it and uses what version of the TTL family?

5. Using a SN54H30N TTL device, what package material is used and what kind of logic does the device provide?

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Garrett, Lane S. "Integrated-Circuit Digital Logic Families," IEEE Spectrum, Vol. 7, No. 10, October 1970, pp. 46-58; Vol. 7, No. 11, November 1970, pp. 63-72; Vol. 7, No. 12, December 1970, pp. 30-42.

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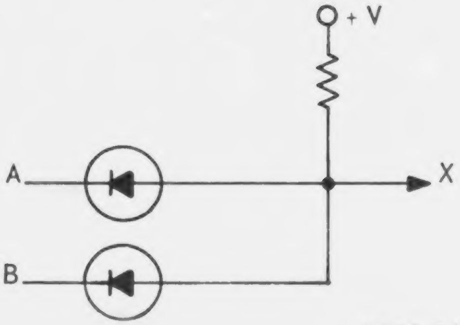
Answers for Exercises

CHAPTER 1

Reference:

001 - 1. Low.
001 - 2. High.
001 - 3.



REP4-1388

Figure 1. Answer for objective 001, exercise 3.

001 - 4. False.
001 - 5.

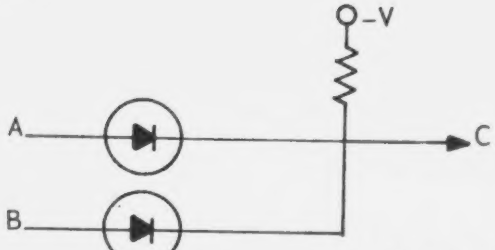
A	B	X
H	H	H
H	L	L
L	H	L
L	L	L

REP4-1389

Figure 2. Answer for objective 001, exercise 5.

001 - 6. High.
001 - 7. High.
001 - 8. High.

001 - 9.



REP4-1603

Figure 3. Answer for objective 001, exercise 9.

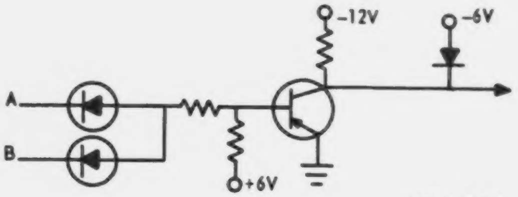
001 - 10. True.
001 - 11.

A	B	X
H	H	H
H	L	H
L	H	H
L	L	L

REP4-1604

Figure 4. Answer for objective 001, exercise 11.

002 - 1. Inversion.
002 - 2. Input.
002 - 3. C.
002 - 4. Low.
002 - 5.



REP4-1395

Figure 5. Answer for objective 002, exercise 5.

002 - 6.

A	B	X
H	H	L
H	L	H
L	H	H
L	L	H

REP4-1396

Figure 6. Answer for objective 002, exercise 6.

002 - 7. Low.
002 - 8. High.
002 - 9.

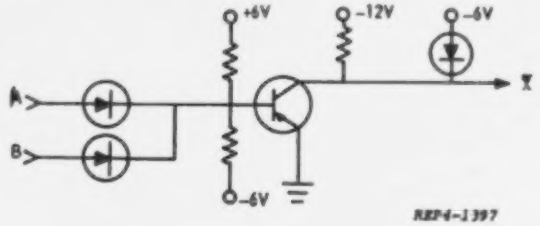


Figure A-7. Answer for objective 002, exercise 9.

002 - 10.

A	B	$\overline{X}$
H	H	L
H	L	L
L	H	L
L	L	H

REP4-1398

Figure 8. Answer for objective 002, exercise 10.

003 - 1. Electrical inversion, increased speed, voltage or current gain, and high input and output impedance.
003 - 2. The RTL has improved operation in terms of operating speed and power gain.

004 - 1. The collector voltage is equal to V_{CC} and thus is reverse-biased.
004 - 2. −6 volts.
004 - 3. No effect.
004 - 4. They should be of a high enough value to provide isolation between the inputs.

005 - 1. Forward-bias.
005 - 2. Both are turned off due to reverse-bias on the emitter-base junction.

006 - 1. The production of a signal that is identical to, but of opposite polarity from, the input signal.
006 - 2. It always provides a signal inversion.

007 - 1. The transistor will be turned on, causing a large current flow through R4, resulting in a drop of the V_{CC} (−6V).
007 - 2. It provides reverse-bias for Q1.

008 - 1. The circuit in figure 1-42 is reverse-biased by the positive V_{BB}, preventing the transistor from conducting without an input. In the circuit represented by figure 1-43 the V_{BB} is negative, causing the transistor to conduct heavily without inputs.
008 - 2. Saturation.
008 - 3. A signal at both inputs, causing an IR drop across R3 sufficient to overcome the forward-bias.

009 - 1. By using diode clamps to limit signal excursion in the output.
009 - 2. Cl further increases switching speed by increasing the slope of the input signal.
009 - 3. Inversion; amplification; impedance matching.
009 - 4. For emitter stabilization.

010 - 1. To provide power gain and impedance matching.
010 - 2. Forward; diodes; transistor-emitter junction.

011 - 1. CR1, CR2, R1, and V_{BB}.
011 - 2. 0 volt.

012 - 1. Common-emitter.
012 - 2. Decreases.

013 - 1. Increases; forward-bias.
013 - 2. Amplified; inverted.

014 - 1. 1 on A and 0 on B.
014 - 2. Quarter Subtractor.
014 - 3. 0 at A, 0 at B; 0 at A, 1 at B; and 1 at A, 1 at B.

015 - 1. Q1 and Q2 are cascade-coupled with the amplified signal of Q1, which is directly coupled to the base of Q2.
015 - 2. There is little or no charge, since the positive signal increases the reverse bias.
015 - 3. Signal voltage amplitudes are on the order of millivolts and fewer components are required, thus increasing circuit efficiency.

016 - 1. In series between the load and ground.
016 - 2. Positive.
016 - 3. Both high.

017 - 1. Parallel; load; ground.
017 - 2. When both inputs are at zero potential.

018 - 1. Two inhibitors; OR.
018 - 2. Forward-biased; reverse-biased.
018 - 3. Zero.

019 - 1. LSI.
019 - 2. TTL.
019 - 3. ECL.
019 - 4. TTL.
019 - 5. CMOS.
019 - 6. CMOS.
019 - 7. TTL.

020 - 1. It functions essentially as a current mode switch and two emitter followers.
020 - 2. The transistors never become saturated.
020 - 3. Conducting.
020 - 4. As an AND/NAND-gate.
020 - 5. 100.
020 - 6. DC.

021 - 1. Input stage, phase splitter, totem pole output.
021 - 2. Q1, Q2.
021 - 3. Q3.
021 - 4. The input low current, and the input high-leakage current.
021 - 5. When Q2 is off.

022 - 1. x, AND.
022 - 2. Complemented.
022 - 3. ORed.

023 - 1. To simplify detailed schematics in the design, use, and maintenance of digital electronics equipment.
023 - 2. AND; OR.
023 - 3. Grouping.
023 - 4. Vinculum.
023 - 5. NOT; inverse.
023 - 6. State indicator.
023 - 7. Right.
023 - 8. False. It is used as a grouping sign.
023 - 9. True.
023 - 10. AND; OR; inverse (OR NOT).
023 - 11.

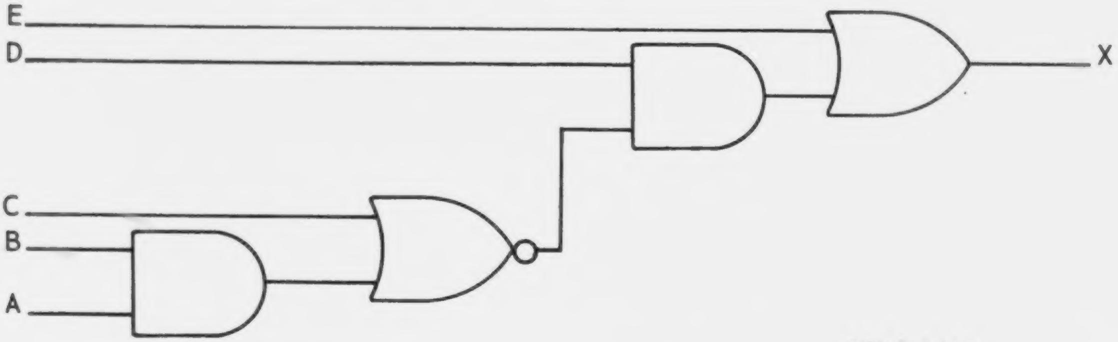


Figure 9. Answer for objective 023, exercise 11a.

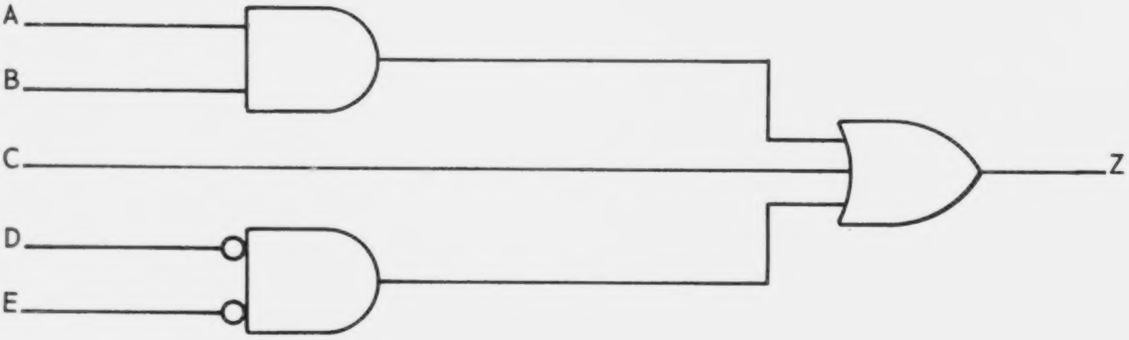


Figure 10. Answer for objective 023, exercise 11b.

023 - 12. a. $(\overline{AB} + C) + D\bar{E} = X$

b. $\overline{(\overline{\bar{A} + B})C + (D + \overline{E\bar{F}})} = \bar{X}$

A	B	X1	X2	X3	X4	X5	X6	X7
L	L	L	L	H	H	L	H	L
L	H	L	H	H	L	H	H	H
H	L	L	H	H	L	L	H	H
H	H	H	H	L	L	L	L	L

REP4-1600

Figure 11. Answer for objective 023, exercise 13.

023 - 13.
a. Two input AND-gate.
b. Two input OR-gate.
c. Two input AND-gate with state indicator in the output or two input NAND.
d. Two input OR-gate with state indicator in the output or two input NOR.
e. Two input AND-gate with state indicator on one input.
f. Two input OR-gate with state indicators on both inputs.
g. Exclusive OR-gate.

023 - 14.

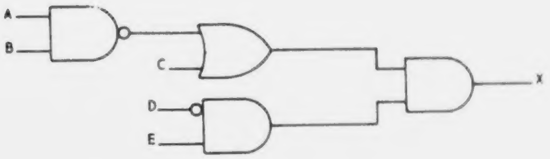


Figure 12. Answer for objective 023, exercise 14a.

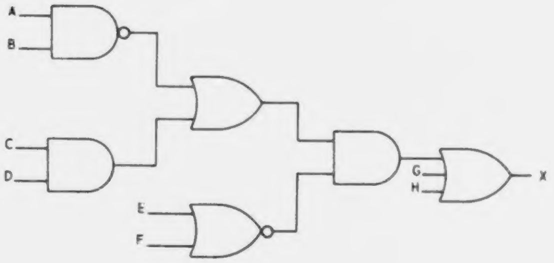


Figure 13. Answer for objective 023, exercise 14b.

024 - 1. SN54S/74S, the nonsaturating or Schottky version of TTL.

024 - 2. The SN54 series.

024 - 3. Quadruple two-input positive NOR-gates.

024 - 4. Hex inverters using low-power Schottky TTL.

024 - 5. Plastic; eight-input positive NAND-gates.

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MODULE 10005

DIGITAL TECHNIQUES

Unit 3

Clock/Pulse Generators

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Preface

THIS UNIT to Module 10005, *Digital Techniques,* presents the devices and circuits critical to the proper timing of digital electronics functions. Waveshaping circuits are discussed first since they are primarily responsible for conditioning signals used within various timing circuits. Oscillators and multivibrators provide the basic timing signals needed to activate data processing circuits. The various timing circuits in Chapter 4 serve to generate, convert, and/or process timing signals so that a number of functions can be performed—all at the correct time.

Code numbers appearing on figures are for preparing agency identification only and should be of no concern to the student.

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Material in this unit is technically accurate, adequate, and current as of March 1980.

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Answers for Exercises . . . 50

NOTE: In this unit the subject matter is developed by a series of student-centered objectives. Each of these carries a three-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see whether your answers match those in the back of this unit. If your response to an exercise is incorrect, review the objective and its text.

Waveshaping Circuits

THE FUNCTION OF many electronic circuits is waveshaping for timing and control. Waveshaping circuits such as integrators, differentiators, limiters, clampers, and Schmitt triggers produce a variety of waveforms. The duration and/or amplitude of these waveforms are controlled with respect to time by these circuits. Proper operation of a waveshaping circuit will depend on the circuit's response to the transient voltage or current applied.

A transient voltage is an instantaneous surge of voltage which occurs as the result of a change from one steady-state condition to another. Transients can be good if they are intended as a trigger for a logic circuit, or they can be harmful if they occur when not desired. Many an integrated circuit or solid-state device has died from undesired transients.

1-1. Differentiation and Integrators

A circuit's response to a transient waveform will determine what form the signal will have at the output of that circuit. Waveshaping circuits must insure that timing and data signals adhere to the waveform and voltage specified for the circuits that follow. Differentiation and integration are two processes which provide specific waveforms for a desired circuit operation.

001. Specify the characteristics of differentiation and integration circuits.

Differentiators. Differentiating circuits produce an output voltage that is proportional to the rate of change of the input. Note that in the RC differentiator illustrated in figure 1-1, an output voltage occurs only when the square wave rises or falls. An RC differentiator requires a short-time constant (1/10 the input frequency) with the output taken across the resistor. Remember that the time constant (TC) in an RC circuit is equal to the product of R and C. At TO, the input changes rapidly from one steady state to another; that is, the rate of change is minimum and the output voltage is maximum. From T0 to T1, there is zero rate of change and the output drops to zero at T1. How fast the output drops to zero depends on the RC time constant for the circuit which determines the charge rate of the capacitor. At T1, there is another sudden change of direction with a maximum rate of change, and the output voltage is again maximum but in the opposite direction. The sharpness of the output spike depends on the shortness of the RC time constant. Differentiators, such as described here, are used as part of the input circuitry of flip-flops where a sharp spike is needed to trigger the circuit.

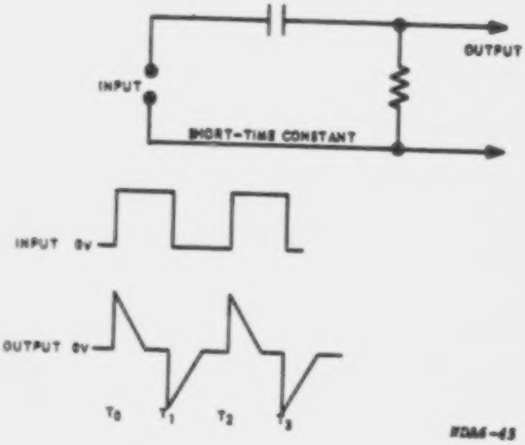


Figure 1-1. RC differentiator.

Integrators. Recall that integration is the process of summing up an infinite number of minute quantities. An integrating circuit produces an output voltage that is essentially the time integral of its input waveform. In

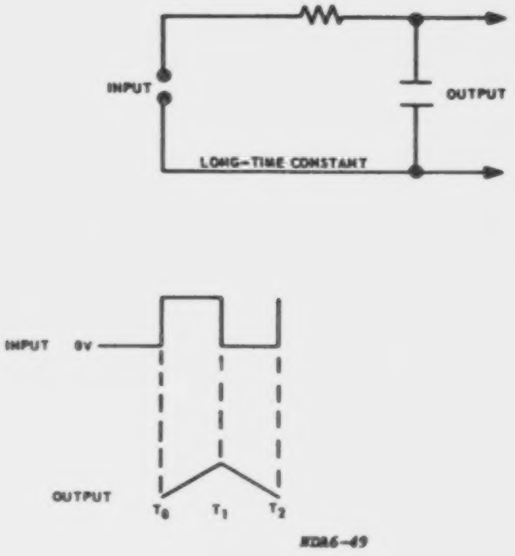

INPUT
OUTPUT
LONG-TIME CONSTANT
INPUT 0V
OUTPUT
T_0
T_1
T_2
NDA6-49

Figure 1-2. RC integrator.

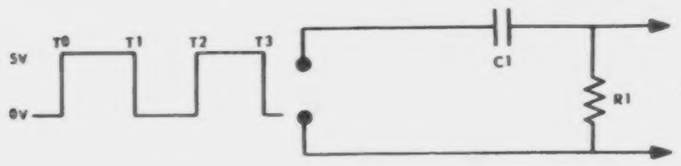
an RC integrator circuit, a long-time constant (10 times the input frequency) is used, and the output voltage is taken across the capacitor. Refer to figure 1-2 for this discussion of an integrator circuit. At time T0, the area under the square-wave input is zero. As time progresses from T0 to T1, the same amount of area is added with each increment of time. The output increases in a linear fashion, and it reaches a maximum at time T1. The input voltage during the time integral from T1 to T2 is negative, and the output decreases linearly toward zero volts.

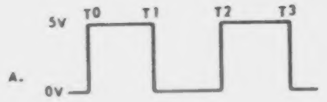
An integrating circuit can be used as an input to a Schmitt trigger circuit where a predetermined threshold voltage must be reached before the circuit fires or conducts. This threshold voltage could be a function of an integrator circuit that is receiving valid radar returns or tape drive sync-pulse inputs.

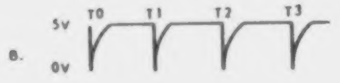
We should note here that RC coupling circuits are similar to integrator circuits, and this fact could cause confusion. RC coupling circuits are used primarily to transfer waveforms from one circuit to another so that the output closely resembles the input. Like the RC integrator, RC coupling circuits use a long-time constant (10 times the input frequency), but the output is taken across a resistor.

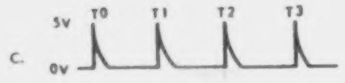
Exercises (001):

1. In the following circuit, C1 is shorted (fig. 1-3). Select the output of the circuit.


T0
T1
T2
T3
5V
0V
C1
R1
OUTPUT


A.
5V
0V
T0
T1
T2
T3


B.
5V
0V
T0
T1
T2
T3


C.
5V
0V
T0
T1
T2
T3

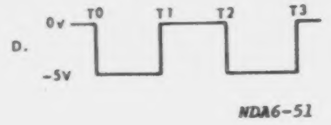

D.
0V
-5V
T0
T1
T2
T3
NDA6-51

Figure 1-3. For objective 001, exercise 1.

2. Why are differentiators used as part of the input circuitry of flip-flops?

3. List one use for an integrator.

4. Which circuit technique described in this section could also be called a summing circuit?

1-2. Limiters, Clippers, and Clampers

These circuits use active devices, such as diodes, tubes, or transistors, to perform the function of controlling signal amplitudes and voltage levels. The use of limiting, clipping, and clamping circuits in electronic equipment insures reliable operation. Limiters and clippers act to control the amplitude of a signal, and clampers act to establish a relationship between a signal and some desired voltage level.

002. Specify the characteristics of limiters/clippers and clamping circuits.

Limiters. A limiter is defined as a device which prevents some characteristics of a waveform from exceeding a predetermined value. Limiting is used for waveshaping or for circuit protection by preventing a voltage from becoming too large. The two types of limiters discussed here are the series and shunt (parallel).

Series limiter. A limiter can be designed using a diode and a resistor. When the output is in series with the diode, the circuit is called a series limiter. Parts A and B of figure 1-4 are diagrams of a positive and a negative series limiter. Note that the diode allows conduction in only one direction and blocks or limits the signal in the opposite direction. In part A of the figure, the diode is reverse-biased by the positive alternation of the input; this prevents the positive alternation from being developed at the output. The diode is forward-biased by the negative alternation of the input, and this alternation is developed at the output. In part B, the diode is forward-biased by the positive and reverse-biased by the negative alternation. Therefore, the negative alternation is blocked or limited.

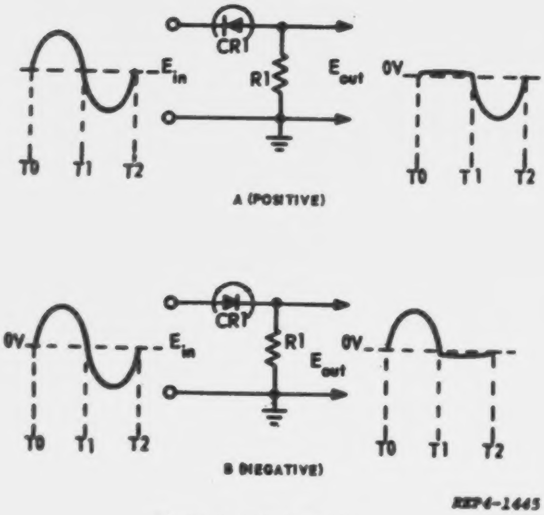


Figure 1-4. Series limiter.

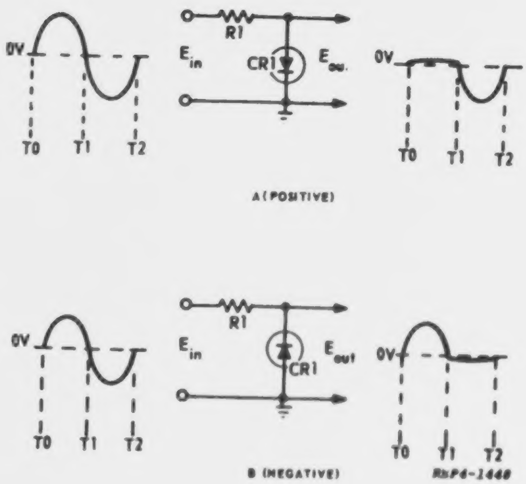
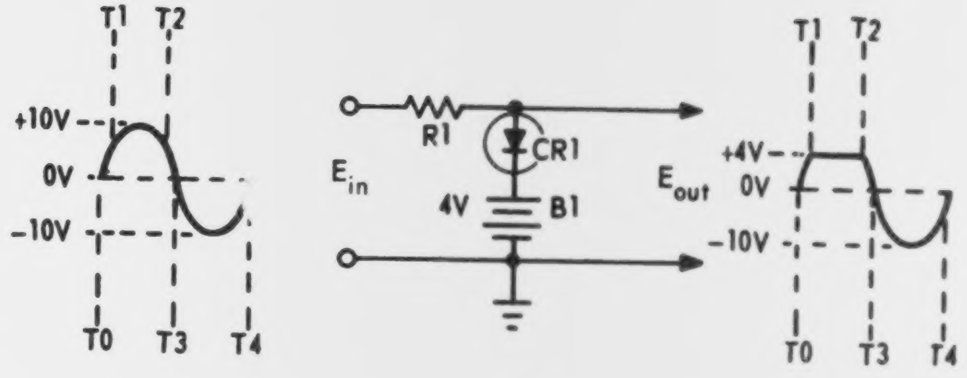


Figure 1-5. Shunt limiter.

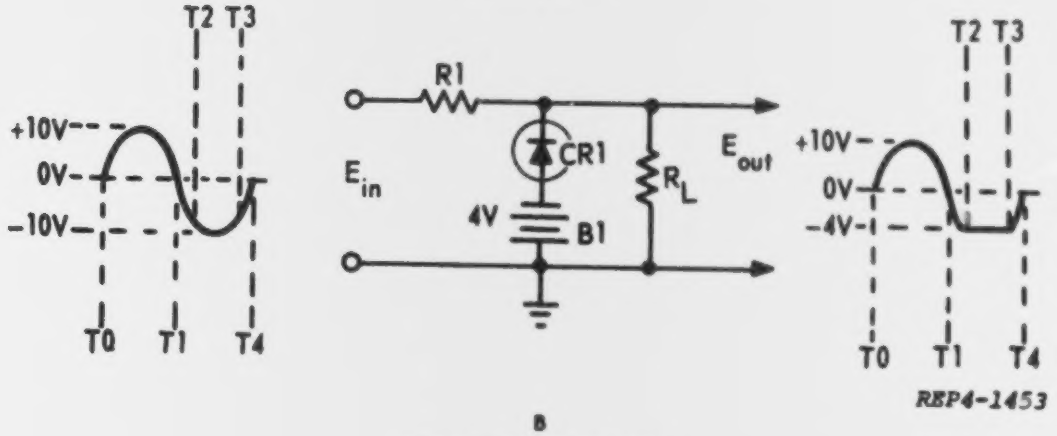
Shunt limiter. When the output is in shunt (parallel) with the limiting device, a shunt limiter is formed. Shunt positive and negative limiters are illustrated in figure 1-5, A and B. The function of the shunt limiter is the same as the series limiter; that is, limit a portion of the input signal. However, note that, in the shunt limiter, limiting occurs during the conduction of the limiting device.

In the shunt limiters just discussed, limiting occurred near a zero-reference level. This reference level could be controlled by providing a bias voltage for the limiting device. Depending on the value of this bias voltage, limiting may remove only a portion of one alternation of an input sine wave. Figure 1-6, A, illustrates a positive shunt limiter with positive bias. Note that in this particular circuit, the battery causes the diode to be reverse-biased until the input goes more positive than a +4 volts. Therefore, limiting does not occur until the input reaches this positive bias voltage level from T_1 to T_2. Note that this is the only time that the diode conducts. Now look at the shunt negative limiter with negative bias, illustrated in figure 1-6, B. In this circuit, the battery causes the diode to be reverse-biased until the input goes more negative than -4 volts. Once the input reaches this level, the diode



A

POSITIVE LIMITER WITH POSITIVE BIAS



B

NEGATIVE LIMITER WITH NEGATIVE BIAS

Figure 1-6. Shunt limiter, with Bias Voltage.

conducts—causing limiting to occur from T_2 to T_3. In some texts, limiters are also called clippers. They perform the same limiting (clipping) function discussed here. It is possible, by combining the circuits of figure 1-6, A and B, to provide clipping of both the positive and negative peaks of the waveform. Another method would be to use two Zener diodes, rated at 4 volts each, connected back-to-back to limit our waveform to ±4-volt excursions. Whenever we limit a waveform with a limiter, we also reduce the average power available from the signal. This reduction of power may be desired in some applications.

Clampers. There are certain circuit applications within digital electronics which require the upper or lower extremity of a waveform to be fixed at a specific DC level or ground. Clampers are the circuits which perform this function.

Positive clamper. Figure 1-7, A, illustrates a positive clamper. The identifying feature to note here is that the diode's cathode is connected to the capacitor. At T0, the +25-volt input causes CR1 to conduct and C charges to 25 volts. At T_1, the 25 volts across C and the +25-volt input are series-aiding. Thus, +50 volts appears across R and CR1. At this time, CR1 is reverse-biased. From T_1 to T_2, C discharges to approximately 23 volts (determined by the value of R and C), and the output (part B of the figure) drops from 50 to 48 volts. At T_2, the input is −25 volts, CR1 conducts, and the output goes to approximately −2 volts. From T_2 to T_3, C charges quickly through CR1, from 23 to 25 volts and the output goes from −2 to 0 volt. Note that the peak-to-peak value of the output is the same as the input (50 volts), but its lower extremity is clamped to zero volts or ground. Whenever we clamp a waveform to zero reference or ground, the circuit becomes what is known as a *DC restorer.*

Negative clamper. The identifying feature of this type of clamper is that the diode's anode is connected to the capacitor. If the clamper in figure 1-7 were a

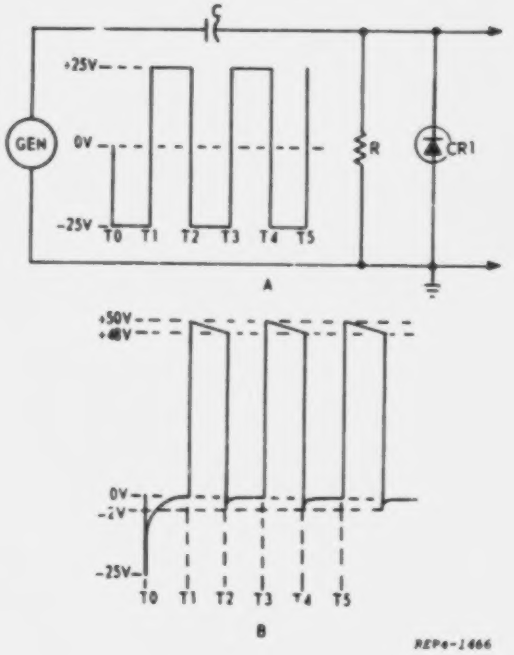


Figure 1-7. Positive clamper circuit and waveforms.

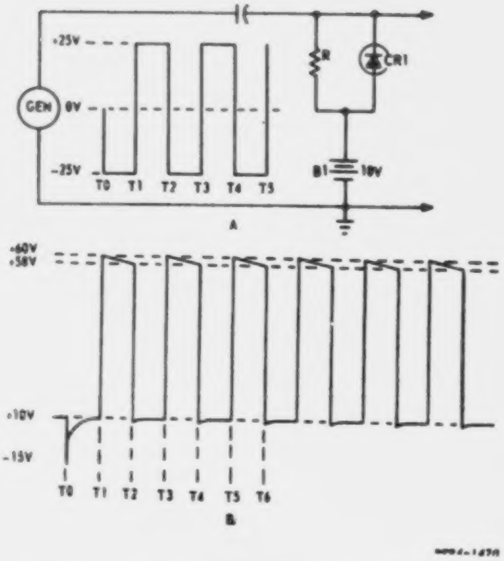


Figure 1-8. Positive clamper with positive bias (10V).

negative clamper, the diode would be turned around (anode connected to capacitor) and the output would vary between 0 and −50 volts.

Establishing the clamping reference. Some circuit applications require a signal clamped to a voltage other than ground. If we add a +10-volt bias battery between the signal-return line and the resistor and diode, as shown in figure 1-8, we would change the clamping reference from 0 to +10 volts. In the positive clamper shown, the minimum value of the signal is clamped to the +10-volt bias. In a negative clamper, the maximum value of the signal would be clamped to this bias.

Determining the output of a clamper. In troubleshooting a clamper circuit, you must know how to determine its output for a given input; otherwise, you will not know whether the output is correct. The following three steps are a guide for determining a clamper's output:

(1) Determine whether it is a positive or negative clamper from the position of the diode in the circuit.

(2) Draw the clamping reference level which is ground or a bias voltage.

(3) Draw the input waveshape exactly as it is with respect to shape and peak-to-peak amplitude; however, the lower extremity should be drawn on the clamping reference level for a positive clamper or the upper extremity drawn on the clamping reference level for a negative clamper.

Figure 1-9 illustrates the use of these three steps for a square wave and a sawtooth. Note in part A of the figure that the peak-to-peak amplitude of these waveshapes is 250 volts (−50 to +200 volts). B and C of the figure illustrate positive clamping, because the lower extremity is clamped to the reference level. D and E illustrate negative clamping, because the upper extremity is clamped. This figure also shows that clamping does not change the amplitude of the signal to any great extent.

Exercises (002):

1. In the following circuit (fig. 1-10), the output is

   incorrect. What is the most probable cause for the incorrect output?

2. Which is the correct output for the following circuit (fig. 1-11)?

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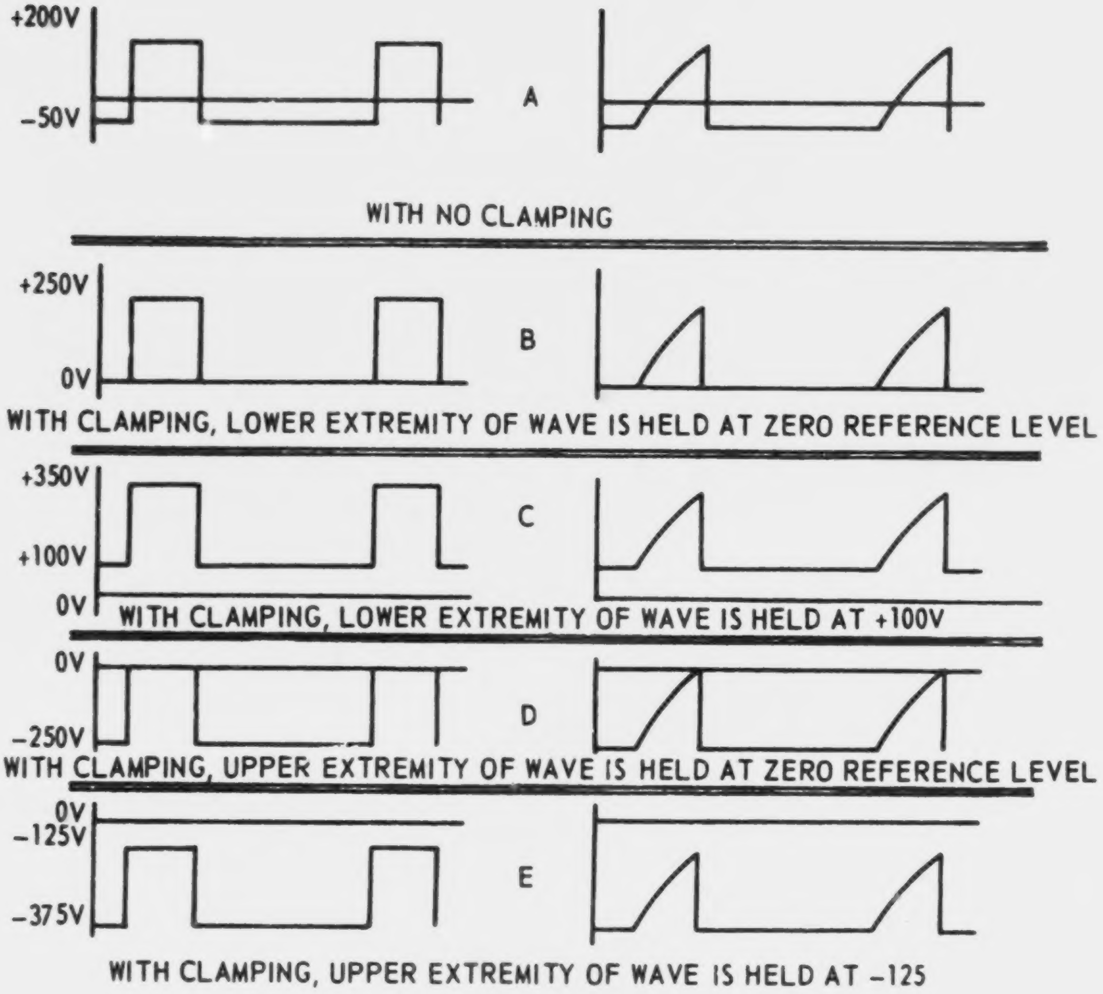
+200V
-50V
A
WITH NO CLAMPING
+250V
0V
B
WITH CLAMPING, LOWER EXTREMITY OF WAVE IS HELD AT ZERO REFERENCE LEVEL
+350V
+100V
0V
C
WITH CLAMPING, LOWER EXTREMITY OF WAVE IS HELD AT +100V
0V
-250V
D
WITH CLAMPING, UPPER EXTREMITY OF WAVE IS HELD AT ZERO REFERENCE LEVEL
0V
-125V
-375V
E
WITH CLAMPING, UPPER EXTREMITY OF WAVE IS HELD AT -125

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Figure 1-9. Clamping waveforms.

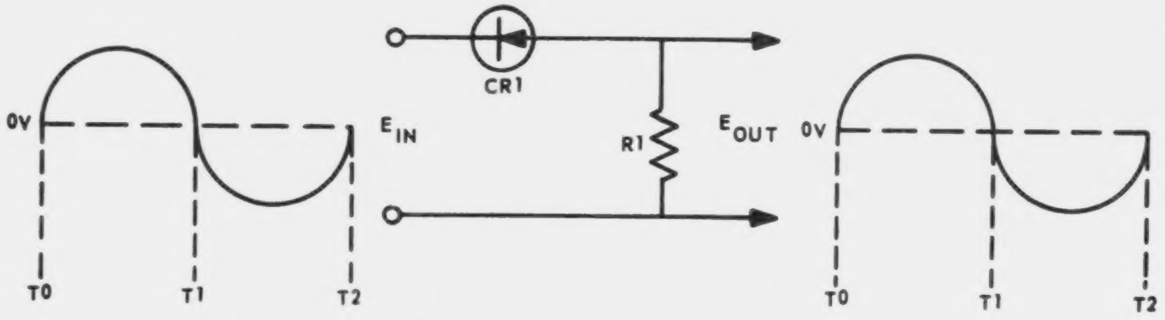
0V
T0
T1
T2
CR1
E_{IN}
R1
E_{OUT}
0V
T0
T1
T2

Figure 1-10. For objective 002, exercise 1.

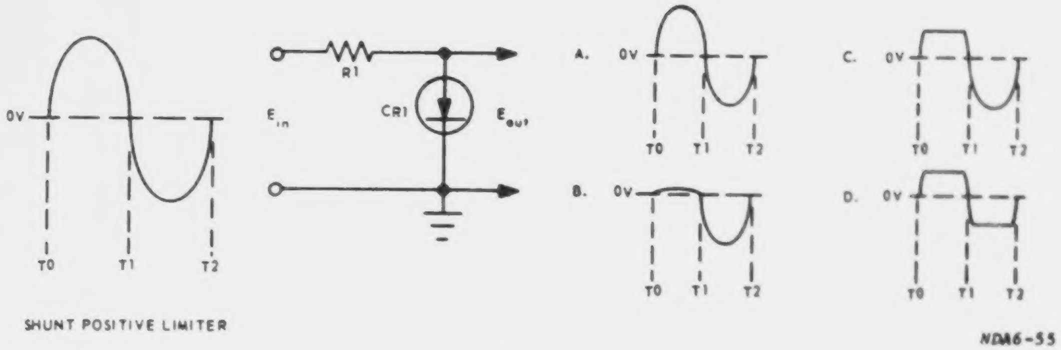
0V
T0
T1
T2
SHUNT POSITIVE LIMITER
R1
E in
CR1
E out
A.
B.
C.
D.
0V
T0
T1
T2
NDA6-55

Figure 1-11. For objective 002, exercise 2.

3. What is the identifying feature of a negative clamper?

4. What is the clamping circuit used to reference a waveform to a 0 volts or ground?

1-3. The Schmitt Trigger

Digital pulse signals will deteriorate over time, especially when transmitted over long signal lines. The pulses lose their rectangular shape and pick up noise signals. It is then necessary to condition the pulses to restore their original waveshape. The Schmitt trigger circuit of figure 1-12 is designed to perform this function.

003. Specify two purposes for the Schmitt trigger circuit and state how it operates.

In its quiescent state, the input to the Schmitt trigger at R1 is at 0 volts and Q1 is cut off. The voltage divider—composed of R3, R4, and R5—divides the source voltages of − 12 volts and + 12 volts so that the base of Q2 is forward biased. Q2 will be saturated. The current through Q2 develops a voltage drop across R7 which reverse biases Q1 and keeps it cut off. In this

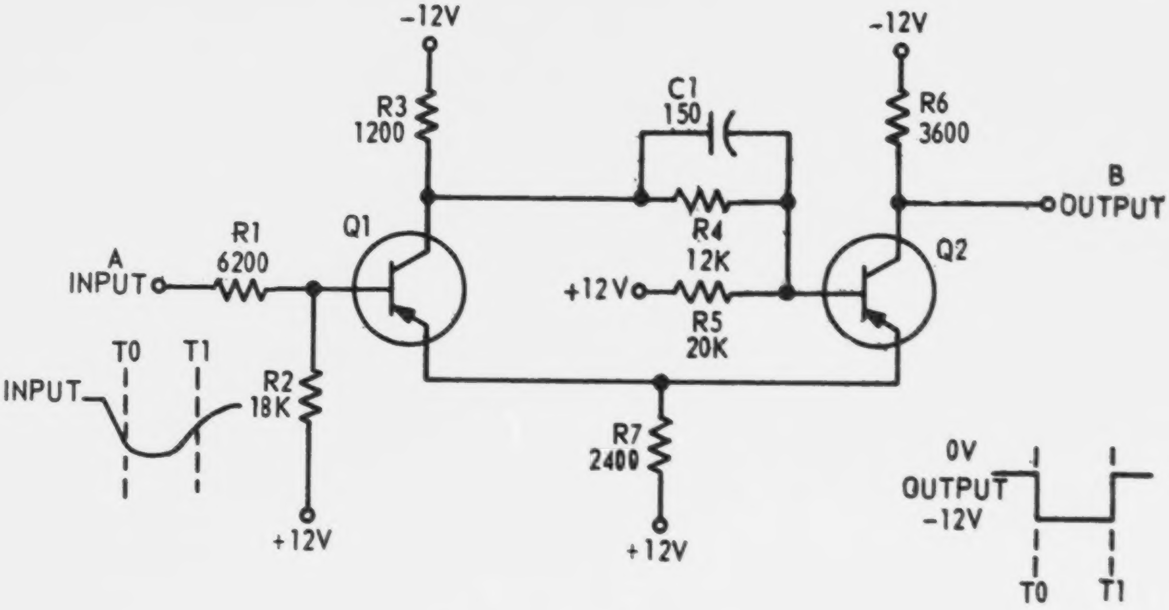
-12V
R3
1200
C1
150
-12V
R6
3600
B
OUTPUT
R1
6200
Q1
A
INPUT
R4
12K
+12V
R5
20K
Q2
T0
T1
INPUT
R2
18K
+12V
R7
2400
+12V
0V
OUTPUT
-12V
T0
T1

Figure 1-12. Schmitt trigger diagram.

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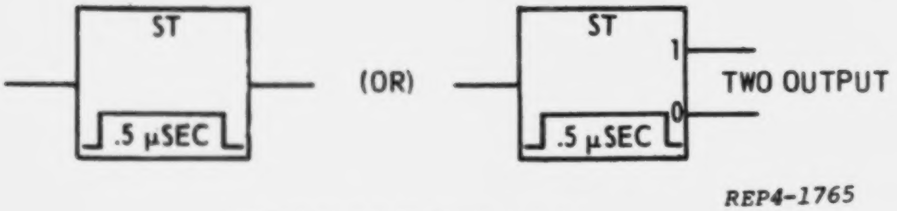


Figure 1-13. Schmitt trigger logic symbols.

condition, the output taken from the collector of Q2 is nearly 0 volts.

At time T_0, the negative signal applied at A input has sufficient amplitude to bias Q1 on, and its collector goes toward 0 volts. This change is coupled to the base of Q2 and causes Q2 to cut off. The decrease in current through R7 reduces the reverse bias on Q1, causing it to saturate. The collector voltage of Q2 is now − 12 volts.

The circuit remains in this state until T_1, when the input voltage becomes less negative, decreasing to a value that causes Q1 to start conducting less. The collector potential of Q1 starts in the negative direction. This change is coupled to the base of Q2 and turns it on. The increase in current through Q2 and R7 puts a reverse bias on Q1 which cuts it off. As a result, Q2 conducts near saturation, and the collector voltage is near 0 volt.

Notice how the rounded input wave is converted to a square-wave output between T_0 and T_1. The sharp rise and fall at the output is due to the feedback between Q2 and Q1. Any slight change ~~in~~ the conduction of Q1 is applied to the ~~base of~~ Q2 which, in turn, changes Q1 emitter voltage. Capacitor C1 speeds the transition from one state to the other.

Schmitt trigger circuits find applications as squaring and voltage-level sensing circuits. Voltage-sensing circuits are useful in warning or control circuits. If the input voltage rises above or falls below a specified level, the Schmitt trigger produces an output which then actuates warning or correction circuitry.

The Schmitt trigger (ST) function symbols are shown in figure 1-13. The ST is actuated when the input signal crosses a certain THRESHOLD voltage. Output signal amplitude and polarity are determined by the circuit characteristics of the ST and not by the input signal. Waveforms may be shown inside or outside the symbol, indicating amplitude, polarity, and threshold voltage. The unactuated state of an ST is either zero or one. When actuated, it changes to the opposite state and remains in the opposite state as long as the input exceeds the threshold value.

The Schmitt trigger circuit may be used in its discrete form, as discussed here, but it is also available as an integrated circuit. The SN54/74 series of ICs has the SN5413/7413, which is a dual 4-input positive NAND Schmitt trigger IC. The SN5414/7414 has six Schmitt trigger inverters in one package. The IC version of the Schmitt trigger circuit works functionally the same as the circuit discussed here.

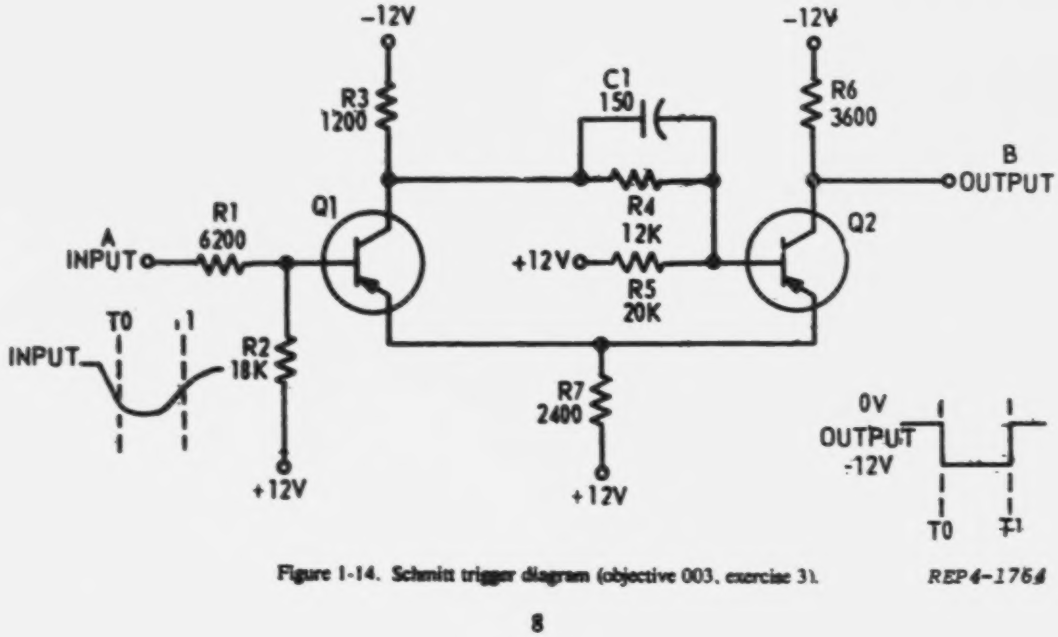


Figure 1-14. Schmitt trigger diagram (objective 003, exercise 3). REP4-1764

Exercises (003):

1. What are the two purposes of the Schmitt trigger?

2. Explain what happens when a negative pulse arrives at the input of the Schmitt trigger circuit in figure 1-12.

3. How long will transistor Q1 in figure 1-14 continue to conduct?

CHAPTER 2

Oscillators

SINUSOIDAL, OR SINE-WAVE oscillators, are electronic circuits which generate a frequency determined by circuit constants. Oscillators are a basic component in a great variety of electronic equipment. Electronic computer and switching systems require oscillators to produce the various timing signals needed to process analog and digital data. The oscillators presented in this chapter are the basic sinusoidal types common to many electronics systems. The nonsinusoidal or multivibrator-type oscillators will be discussed in the next chapter.

2-1. Theory and Operation of Oscillators

You probably have been present at a gathering where the public address system developed a shrill whistle. This objectionable noise results from "acoustic feedback" caused by the microphone being in the path of the sound from the loudspeaker. Any slight noise present at the microphone is amplified as it comes from the loudspeaker. When some of this sound reaches the microphone, it reinforces the original noise. The noise contains a large number of frequencies and their harmonics.

The frequency at which feedback is most effective is determined by the length of the path from the loudspeaker to microphone, together with the stiffness of the loudspeaker and microphone diaphragms. Such a device can well be called an audio oscillator.

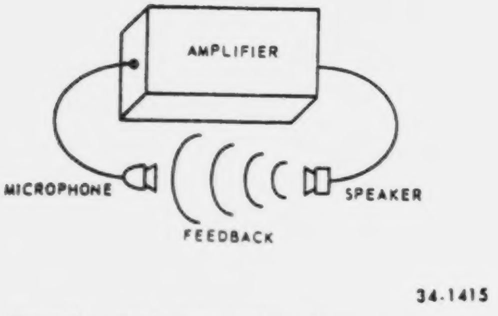


Figure 2-1. Feedback in a public address system.

004. Cite operating characteristics of the basic oscillator.

Basic Oscillator. As an electronic technician, you will probably spend some time troubleshooting, repairing, and adjusting timing circuits. Oscillators are used to generate timing signals or frequencies used to process information within communication and computer systems. They are also used in CRT monitors, radars, television, and test equipment. The oscillator must generate a signal that is stable with respect to time, temperature, and frequency.

The whistle you heard from the public address system occurs when the system becomes an oscillator. To understand how this whistle occurs, we will analyze a public address system. The system contains an amplifier, a microphone, and a loudspeaker, as shown in figure 2-1.

The whistle starts wih a small noise picked up by the microphone. The noise is amplified by the amplifier and then sent to the speaker. With the microphone in the path of the speaker, the noise is fed back to the microphone, which starts the process again. This continues until the amplifier is overdriven and amplitude of the noise reaches a steady value. You hear this as a loud whistle. If you remove the microphone from the path of the speaker (break the feedback path), the oscillations will cease. Another method used to stop the oscillations is to decrease the gain of the amplifier. This will decrease the feedback amplitude to the point that oscillations cease.

The basic requirements for sustained oscillations are: (1) amplification, (2) a frequency-determining device, and (3) regenerative feedback.

An amplifier and its associated circuitry require a power source for its operation. (Refer to fig. 2-2.) The amplifier provides the necessary gain, and the feedback network provides regenerative feedback. The frequency-determining device sets the output frequency.

Amplifier. The amplifier must provide enough gain for the output load and for regeneration in order to maintain constant amplitude and frequency. The amplifier can be a common-emitter, common-

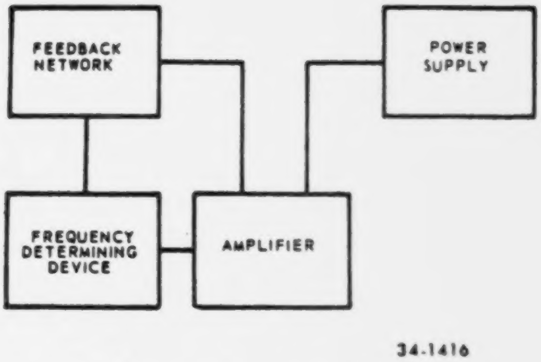


Figure 2-2. Block diagram of an oscillator.

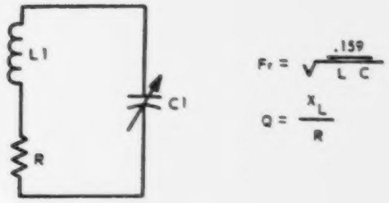
collector, or common-base configuration. The circuit is often a common-emitter configuration because of its power gain characteristics and because the input and output impedance can be matched easily.

Frequency-determining device. The frequency-determining device (FDD)—as the name implies—determines the frequency of operation of the oscillator. Devices used include RC networks, LC tank circuits, and crystals.

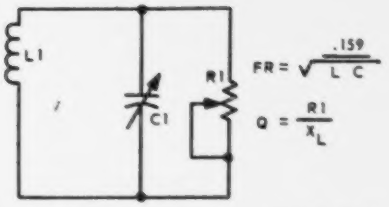
A common FDD uses LC components in either series or parallel-resonant circuits. The resonant frequency of a tank circuit is determined by the size of L and C, using the formula:

$$F_o = \frac{.159}{\sqrt{LC}}$$

Changing tank capacitance or inductance will tune the tank. Decreasing C or L causes the resonant frequency of the tank to increase. Conversely, if either C or L is made larger, the resonant frequency of the tank circuit will decrease. By properly adjusting the capacitor or coil, the desired resonant frequency can be obtained.



A. RESONANT CIRCUIT



B. RESONANT CIRCUIT WITH EXTERNAL LOADING

Figure 2-3. Tank circuit loading.

Refer to figure 2-3, A. Resistor R represents the total internal resistance of the tank. Remember that R is one of the factors used to determine the Q of the tank, where the formula for Q is:

$$Q = \frac{X_L}{R} \text{ or } \frac{X_C}{R} \text{ when } X_L = X_C$$

This formula shows that Q and internal resistance are inversely related. Assume that, at resonance, the ratio of reactance to resistance is greater than 20; the Q of the tank will be greater than 20.

Refer to figure 2-3, B, and notice the external resistor R1. Resistor R1 can be used to control the Q of the tank. Q for this arrangement is $Q = \frac{R1}{X_L}$ (R in shunt). When R1 is made smaller (less resistance), the tank circuit is shunted with a low resistance, which causes more losses in the circuit and, therefore, lowers the Q. This is a common method of changing the Q of a tank circuit. A limitation is the fact that the Q cannot be made any higher than it was before the resistor was added. All R1 can do is lower the Q.

When the FDD is a tank circuit, the L and C determine the frequency, but the Q of the tank determines the feedback requirement. A low Q requires more feedback than a high Q. The greater the feedback requirement, the greater the load on the complete oscillator circuit.

Regenerative feedback. Feedback is the process of transferring energy from a high-level point in a system to a low-level point in a system. This usually means transferring energy from the output of an amplifier back to its input. If the feedback opposes the input signal, the feedback is degenerative. However, if the feedback aids the input signal, the feedback is regenerative.

Regenerative feedback is required in an oscillator. It furnishes the input signal to the amplifier. The amplified feedback signal compensates for damping in

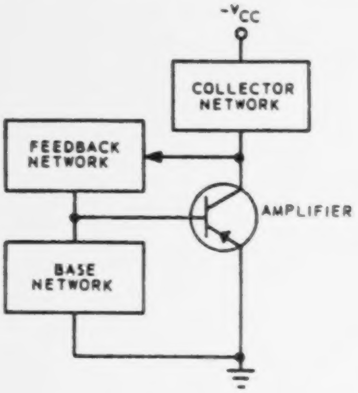


Figure 2-4. Oscillator block diagram.

the FDD circuit. Since all circuits have some losses, the regenerative feedback must be equal to the losses and provide a circuit gain of unity. Unity gain means that circuit losses are being exactly compensated for.

Figure 2-4 shows a feedback network connected between the collector and base of a transistor amplifier. Since a common-emitter configuration shifts the signal 180°, the feedback network must shift the collector voltage an additional 180° for it to be regenerative feedback. Transformers, resistance-capacitance networks, interelement capacitance, and inductance networks provide this 180° shift. With a common-base or common-collector amplifier configuration, no phase shift is required.

Buffer amplifier. Sometimes the output circuit of an oscillator acts as a load placed on the frequency-determining device. This type loading affects oscillator amplitude and frequency. A "buffer" amplifier decreases this loading effect on the oscillator by reducing interaction between the load and the oscillator.

Figure 2-5 is the schematic of a buffer amplifier. This circuit is a common-collector amplifier. A common collector has a high-input impedance and a low-output impedance. Since the output of the oscillator is connected to the high-input impedance of the common collector, the buffer has little effect on the operation of the oscillator. The output of the common collector is then connected to an external load, with the result that changes in the output load cannot reflect back to the oscillator circuit. Thus, the buffer amplifier reduces interaction between the load and oscillator. This is "one-way" coupling since the oscillator signal is coupled forward but load changes are not coupled back to the oscillator.

Exercises (004):

1. The basic requirements for sustained oscillations are ______ , a ______ ______ ______ , and ______ ______ .
2. The ______ provides the necessary gain, the ______ ______ provides regenerative feedback, and the frequency-determining device sets the ______ ______ .
3. A ______ ______ configuration is used most often as an amplifier because of its power gain characteristics and because the ______ and ______ impedance can be matched easily.
4. ______ ______ , ______ ______ ______ , and ______ are used as frequency-determining devices.
5. ______ feedback is required in an oscillator.
6. A buffer amplifier ______ the loading effect on the oscillator by ______ interaction between the load and the ______ .

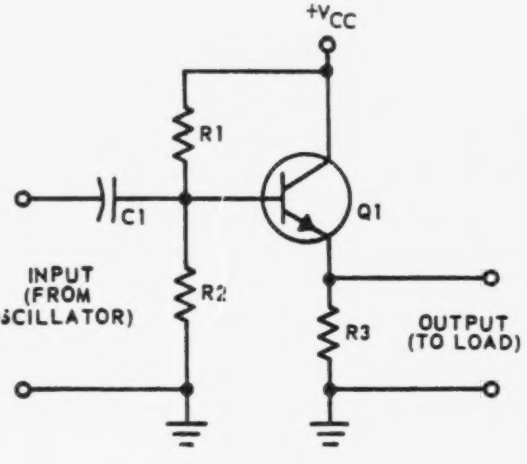


Figure 2-5. Buffer amplifier.

2-2. Types of Oscillators

There are numerous types of oscillators used to generate frequencies from audio to microwave. Discussed in this section are the most common oscillator circuits used as accurate and stable frequency sources.

005. State how an Armstrong oscillator operates.

Armstrong Oscillator (Tuned Base NPN). We have discussed the requirements of oscillators. Let's put them together in a complete oscillator circuit.

Figure 2-6, A, shows a conventional amplifier. R2 provides the forward bias for Q1; C2 is a coupling capacitor; and L1 and R1 form the collector-load impedance. This is a common-emitter configuration which gives a 180° shift between the base and collector. Figure 2-6, B, shows a frequency-determining device composed of inductance L2 and capacitance C1. C1 is the tuning device used to adjust the resonant frequency to the desired value. Figure 2-6, C, is the feedback network which uses collector lead L1 as the primary and L2 as the secondary windings of a coupling transformer to provide 180° phase shift. Variable resistor R1 controls the amount of current through L1. With R2 adjusted for maximum resistance, most of the current flows through L1. The transformer now couples maximum signal into the tank circuit. This represents a large feedback amplitude. If R1 is adjusted for a smaller resistance, less current flows through L1, and less energy is coupled to the tank circuit; therefore, feedback amplitude decreases. R1 is adjusted so that the L1 current is adequate to sustain tank oscillation.

Figure 2-6, D, shows the complete oscillator circuit. By connecting the feedback network through coupling capacitor C2 to the base of Q1, we have a "closed loop" for feedback (shown by the solid arrows). Let's verify that the feedback is regenerative:

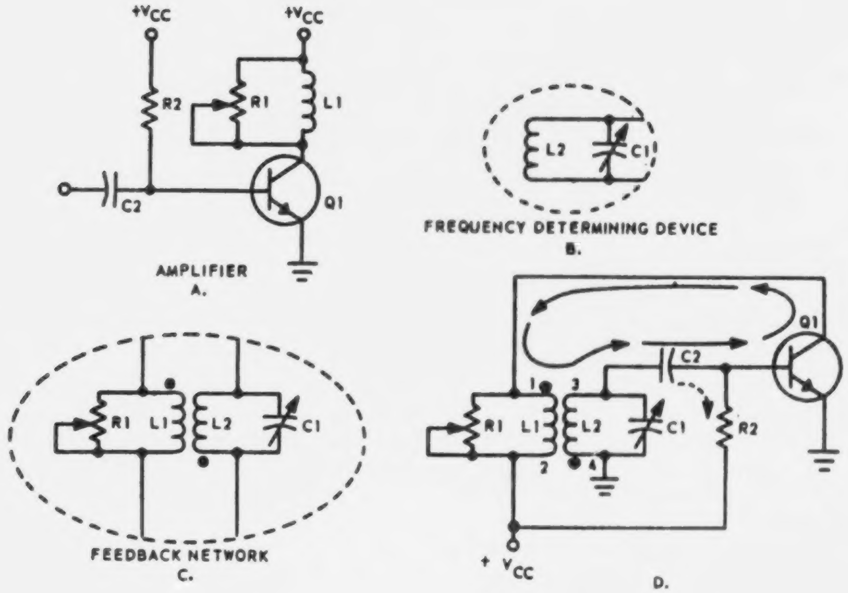


Figure 2-6. Oscillator circuit. 34-1419

assume a positive signal on the base of Q1. The transistor amplifies this signal and inverts it 180°. The negative collector signal is applied to primary L1 of the transformer, which is connected so that there is a 180° phase shift between leads 1 and 3. The negative signal applied to lead 1 appears at lead 3 as a positive signal. The positive signal is now coupled through C2 to the base of Q1. Notice that we assumed a positive signal on the base and that the voltage fed back is of the same polarity. If we assume a negative signal voltage on the base, the feedback signal will be negative. In either case, the regenerative feedback compensates for damping in the FDD, and it has sufficient amplitude to provide a circuit gain of unity.

Figure 2-6, D, fulfills the requirements for an oscillator: amplification, a frequency-determining device, and regenerative feedback. The schematic shows a "tuned base" oscillator because the FDD is in the base circuit. (If the FDD were in the collector circuit with C1 in parallel with L1, it would be a "tuned collector" oscillator.) This particular circuit is an Armstrong oscillator. A transformer is used, and the inductive feedback adjusted by R1 is just enough to "tickle" the circuit to sustain oscillation. With this operation, L1 is called a *tickler* coil.

Refer to figure 2-6, D, as we discuss the circuit operation. When V_{cc} is applied to the circuit, a small amount of base current flows through R2, which sets forward bias on Q1. This forward bias causes collector current to flow from ground through Q1 and through L1 to $+V_{cc}$. The current through L1 develops a magnetic field which induces a voltage into the tank circuit. The voltage is positive at the top of L2 and C1. At this time, two actions occur. First, resonant tank capacitor C1 charges to this voltage; the tank circuit now has stored energy. Second, coupling capacitor C2 couples the positive signal on its base; Q1 will conduct harder. With Q1 conducting harder, more current flows through L1, a larger voltage is induced into L2, and a larger positive signal is coupled back to the base of Q1. This is the regenerative feedback action of the circuit. While this is storing more energy, C1 charges to the voltage induced into L2.

The transistor will continue to increase in conduction until it reaches saturation. At saturation, collector current of Q1 is at a maximum value and cannot increase any further. With a steady current through L1, the magnetic fields are not moving, and no voltage is induced into the secondary.

With no external voltage applied, C1 now acts as a voltage source and discharges. As it does, it transfers its energy into the magnetic field of L2, and the voltage across C1 decreases.

Now let's look at C2. The coupling capacitor has charged to approximately the same voltage as C1. As C1 discharges, C2 will discharge. The prime discharge path for C2 is through R2 (shown by the dashed arrow).

As C2 discharges, the voltage drop across R2 reduces the forward bias on Q1, and collector current begins to decrease.

A decrease in collector current allows the magnetic field of L1 to collapse. The collapsing field of L1 now induces a negative voltage into the secondary which is coupled through C2 and makes the base of Q1 more negative. This, again, is regenerative action, and it continues until Q1 is driven into cutoff.

When Q1 is cut off, the tank circuit continues to flywheel or oscillate. The flywheel effect not only produces a sine-wave signal but also aids in keeping Q1 cut off. Without feedback, the oscillations of L2 and C1 would dampen out after several cycles. To insure that the amplitude of the signal remains constant, regenerative feedback is supplied to the tank once each cycle as follows: As the voltage across C1 reaches a maximum negative, C1 begins discharging toward 0 volts. Q1 is still below cutoff. C2 continues to discharge through 0 and becomes charged positively. The tank circuit voltage is coupled to the base of Q1, so the base voltage becomes positive and allows collector current to flow. The collector current causes a magnetic field in L1 which is coupled into the tank. The action replaces any lost energy in the tank circuit. This feedback also drives Q1 into saturation. After saturation is reached, the transistor is again driven into cutoff.

The operation of the tuned base oscillator is basically this: power applied to the transistor allows energy to be applied to the tank circuit. When the transistor cuts off, the tank circuit oscillates. Once every cycle, the transistor conducts for a short period of time (class C operation) and returns enough energy to the tank to insure a constant amplitude signal.

Class C operation has high-efficiency and low-loading characteristics. The longer Q1 is cut off, the less the loading on the frequency determining device. For class A operation, the feedback amplitude must be reduced, and C2 is usually larger. The reduced feedback amplitude prevents the amplifier from going all the way into saturation and cutoff, and the larger capacitor makes a longer time constant, so C2 cannot charge or discharge any appreciable amount.

Figure 2-7 shows the tuned-base RF oscillator as you will probably see it. R3 has been added to improve temperature stability; C3 prevents degeneration, C4 is a coupling capacitor, and T2 provides a method of coupling the output signal. T2 is usually a loose-coupled RF transformer, which reduces undesired reflected impedance from the load back to the oscillator.

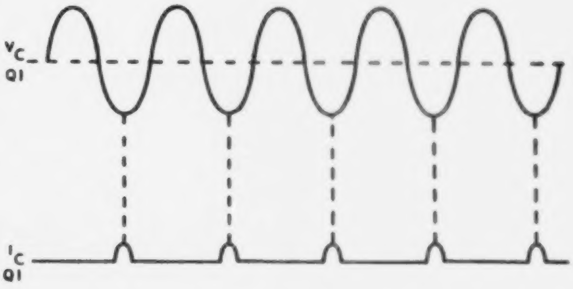


Figure 2-8. Collector current and voltage of Class C oscillator.

The tuned-base RF oscillator is an example of how a class C amplifier can produce a sine-wave output that is not distorted. Although class C operation is nonlinear and many harmonic frequencies are generated, only one frequency receives enough gain to cause the circuit to oscillate. This is the frequency of the resonant tank circuit. Thus, we can have high efficiency and an undistorted output signal.

The waveforms in figure 2-8 illustrate the relationship between the collector voltage and collector current. Notice that collector current I_C flows for only a short time during each cycle. While the tank circuit is oscillating, L2 acts as the primary of a transformer and L1 acts as the secondary. The signal from the tank is therefore coupled through T1 to a coupling capacitor C4, and the output collector voltage is a sine wave.

Armstrong Oscillator (Tuned Base PNP). The tuned-base PNP oscillator circuit is almost the same as the NPN version, with the exception of the negative V_{cc} and the PNP transistor, as shown in figure 2-9. The regenerative feedback path is still from the collector to L1, to L2, and through C2 to the base of Q1. R1 controls the amplitude of feedback; L2 and C1

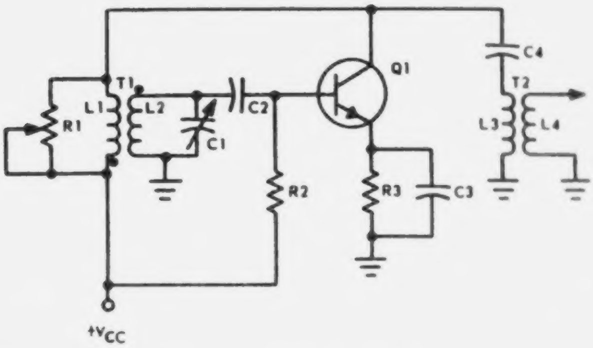


Figure 2-7. Armstrong oscillator.

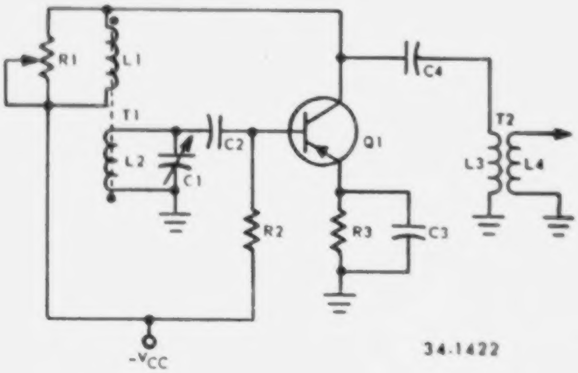


Figure 2-9. Armstrong oscillator PNP tuned base.

form the frequency-determining device, and R2 provides the forward bias to start circuit operation. C4 and T2 make up the output coupling circuit.

Exercises (005):

1. Refer to figure 2-6, B. ______ and ______ are the frequency-determining device.
2. Refer to figure 2-6, C. ______ is adjusted so that the ______ through L1 is adequate to sustain tank oscillations.
3. Refer to figure 2-6, D. The negative collector signal is applied to ______ of the transformer, which is connected so that there is a ______ phase shift between leads 1 and ______.
4. Refer to figure 2-6, D. With Q1 conducting harder, more current flows through ______, a larger voltage is induced into ______, and a larger ______ signal is coupled back to the base of Q1.
5. Class C operation has ______ efficiency and ______ loading characteristics.
6. Refer to figure 2-7. R3 has been added to improve ______ ______.
7. The difference between a tuned-base PNP oscillator circuit and a tuned-base NPN oscillator circuit is the ______ ______ and the ______.

006. Identify types of Hartley oscillators.

Hartley Oscillator, Series Fed. One of the most common oscillator circuits is the Hartley: series fed and shunt fed. We will first discuss the series-fed Hartley oscillator. Refer to figure 2-10 for the components.

R1 and R2	Voltage divider network for forward bias.
R3	Swamping resistor for thermal stability.
C1	Bypass capacitor for R3 to prevent degeneration.
C2	Feedback coupling capacitor.
C3, L1, and L2	Frequency-determining device.
L3	Coupling for the output circuit.

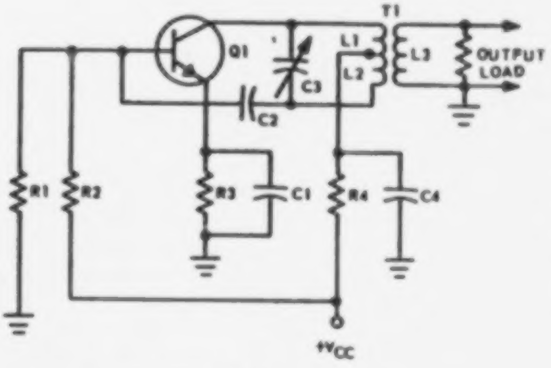


Figure 2-10. Series-Fed hartley oscillator.

R4 and C4	Low-pass filter network (decoupling network).

The identifying feature of a Hartley oscillator is the tapped coil. The oscillator is series fed because DC flows through the tank. Observe that DC flows from ground, through R3, Q1, L1, and R4 to + V_{cc}. When a part of the tank circuit is in series with the power supply so that DC flows through it, the circuit is said to be "series fed." Regenerative feedback from the collector to the base of Q1 is through autotransformer action between L1 and L2.

To understand the circuit operation, assume that the circuit is oscillating and that the signal on the base (from the FDD) is going in a positive direction. The positive signal will cause the collector current to increase, and the voltage across L1 will be negative at the top with respect to the tap. The voltage induced into L2 will be positive at the bottom with respect to the tap. This positive signal will be coupled through C2 to the base of Q1. The signal coupled back is in phase with the original signal, and it is regenerative. The negative alternation of the signal on the base causes collector current to decrease. This decrease in current will cause the voltage across L1 to go positive at the top with respect to the tap. The voltage induced into L2 will be negative at the bottom with respect to the tap. This negative signal is coupled through C2 to the Q1 base. Once again, the signal fed back is in phase with the original signal and, therefore, is regenerative.

The regenerative feedback path, then, is from the collector through L1 to L2, through C2 to the base. The amplitude of the feedback is controlled by the position of the tap. When the tap is moved up, the feedback amplitude increases. The tap is positioned to send the correct amplitude of regenerative feedback to the base of the transistor as indicated by the shape of the output waveform. Observe that, regardless of the tap position, the frequency determining network does not change, so the output frequency does not change.

The low-pass filter network (R4-C4) is used for two purposes. First, the resistor drops V_{cc} to the desired value for the transistor. Second, the oscillator signal is isolated from the power supply by the large filter capacitor C4, connected between R4 and the tank circuit. The high frequencies will be shunted around the power supply, and the low frequencies (DC in this case) will pass on to the power supply.

Hartley Oscillator, Shunt Fed. The second Hartley oscillator is the shunt-fed type. Figure 2-11 shows the schematic. Again, we find a tapped coil—the identifying feature of a Hartley oscillator. The frequency-determining device (C4, L1, and L2) is now in shunt with the DC path through the amplifier (ground, R2, Q1, and R4 to V_{cc}).

The following list shows the purpose of the components:

R1 and R3	Voltage divider network for forward bias.

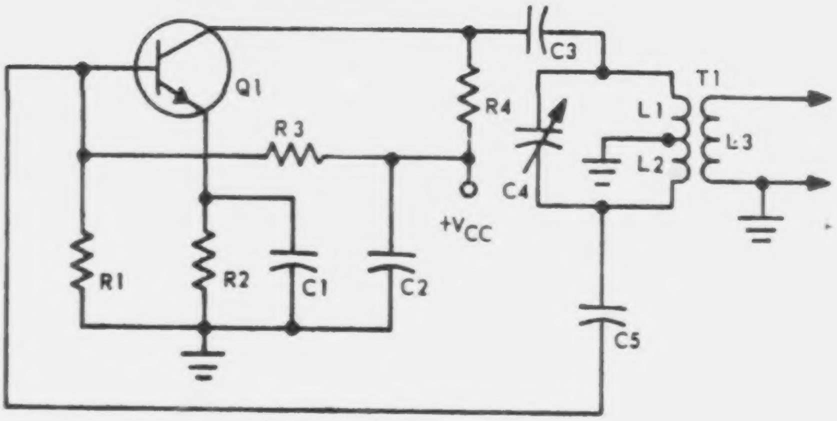


Figure 2-11. Shunt-Fed hartley oscillator.

R2	Swamping resistor for thermal stability.
C1	Bypass capacitor to prevent degeneration.
C2	Filter capacitor for the power source.
R4	Collector-load resistor.
C3	Coupling capacitor.
C5	Feedback coupling capacitor.
C4, L1, and L2	Frequency-determining device.
L3	Coupling for the output circuit.

Coupling capacitors C3 and C5 block DC from the tank circuit; thus, the oscillator is "shunt fed." Regenerative feedback from the collector to the base of Q1 is through C3 as a result of autotransformer action between L1 and L2 and through capacitor C5.

To understand the circuit operation, assume that the circuit is operating and that the signal on the base is going positive. The positive signal will cause collector current to increase and collector voltage to decrease (go in a negative direction). This negative-going signal couples through C3, and the voltage across L1 will be negative at the top with respect to the tap. The voltage induced into L2, then, will be positive at the bottom with respect to the tap. This positive-going signal is then coupled through C5 to the base. Since the signal coupled back is in phase with the original signal, it is regenerative.

The negative alternation of the signal on the base causes the collector current to decrease and the collector voltage to increase (go in a positive direction). This positive-going signal is coupled through C3, and the voltage across L1 will be positive at the top with respect to the tap. The voltage induced into L2, then, will be negative at the bottom with respect to the tap. This negative-going signal is then coupled through C5 to the base. Once again, the signal fed back is in phase with the original signal and is, therefore, regenerative.

The regenerative feedback path, then, is from the collector, through C3 to L1, to L2, and through C5 to the base. Once again, the position of the tap determines the amount of feedback in the circuit. Use figure 2-11 to troubleshoot the shunt-fed Hartley oscillator. Assume class A operation. *Symptom:* No output and V_c is 0 volts; the possible troubles include R4 open, C2 shorted, or C3 shorted. *Symptom:* No output and V_c is normal; the possible trouble could be C5 open, C3 open, L1 open, or L2 open. *Symptom:* No output and V_c is approximately equal to V_{cc}; the trouble now could be R2 open, R3 open, R1 shorted, C5 shorted, or R4 shorted.

Exercises (006):

1. The identifying feature of a Hartley oscillator is the ________ ________ .
2. Refer to figure 2-10. The purpose of R3 is to act as a ________ ________ for thermal ________ .
3. Refer to figure 2-10. Regenerative feedback from the collector to the base of ________ is through ________ action between L1 and L2.
4. Refer to figure 2-10. The signal on the base is going in a positive direction; the signal coupled back is ________ ________ with the original; and it is ________ .
5. Refer to figure 2-11. In a shunt-fed Hartley oscillator, the frequency-determining device is in ________ with the DC path through the ________ .
6. Refer to figure 2-11. The purpose of L3 is the ________ for the ________ ________ .

007. Cite operating characteristics of the Colpitts oscillator.

Colpitts Oscillator. Another typical oscillator is the Colpitts. Figure 2-12 shows the schematic. The identifying feature of this oscillator is split capacitors. The following list gives the purpose of the components:

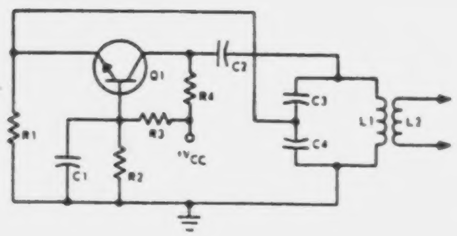


Figure 2-12. Colpitts oscillator.

R1	Emitter resistor to develop the feedback signal.
R2 and R3	Voltage divider network for forward bias.
C1	Base bypass capacitor that keeps the base at AC ground.
R4	Collector-load resistor.
C2	Coupling capacitor between the collector and the tank.
C3, C4, and L1	Frequency-determining device.
L2	Output coupling device.

The two capacitors (C3 and C4) in the frequency-determining device provide the Colpitts oscillator with capacitive feedback. As the Hartley oscillators use a tapped coil for inductive feedback, Colpitts oscillators use split capacitors for capacitive feedback. Before discussing the operation of the two capacitors, let's trace the regenerative feedback path.

Starting at the collector of Q1, the feedback goes through C2, to the tank circuit, and from the connection between the two capacitors to the emitter of Q1. Q1 is connected in a common-base configuration and does not phase shift the signal. Neither does the tank circuit. So, the feedback is regenerative.

To illustrate the purpose of the two capacitors, C3 and C4, refer to figure 2-13, a rearrangement of components from figure 2-12. This shows only the emitter to base circuit with respect to the tank circuit. Notice the interelement capacitance between the emitter and base.

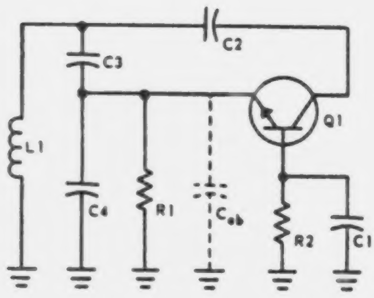


Figure 2-13. Colpitts oscillator; emitter circuit redrawn.

When a tank circuit is connected across a junction of a transistor, the transistor interelement capacitance becomes part of the tank capacitance. If this interelement capacitance changes, the frequency of the tank circuit will change. Among other things, heat and the amount of bias affect the capacitance between the transistor elements; therefore, C_{eb} is subject to change. In the Colpitts oscillator, one of the two capacitors in the tank circuit, C4, is connected across the emitter-base junction. This connection places C_{eb} parallel with C4. To decrease the effects of a change in C_{eb}. For example, if C_{eb} is 10 picofarads, then select 1,000 picofarads for C4. The total parallel capacitance of C_{eb} and C4 would be 1,010 picofarads. The size of C3 is selected to make the circuit resonant with L1 at the desired frequency. Let's arbitrarily say that C3 is 100 picofarads. The total tank capacitance is about 90.9 picofarads.

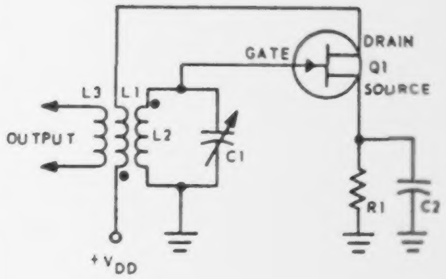
To illustrate our example, let's assume that the interelement capacitance increases 100 percent to 20 picofarads. How much does the total tank capacitance change? We find that the total tank capacitance is now about 9.1 picofarads. This represents a change in total tank capacitance of about 0.2 percent. So, with a 100 percent change in interelement capacitance, the resonant frequency changes less than 0.2 percent. By a more diligent selection of component sizes, an even smaller degree of change can be achieved.

By now, you may have guessed why the sizes of the two capacitors in the Colpitts oscillator are different. The capacitors reduce the undesirable effect of transistor interelement capacitance changes on the frequency-determining device. This allows the Colpitts oscillator to have good frequency stability characteristics. The two capacitors also act as a voltage divider to insure the correct amplitude of feedback.

The Colpitts oscillator may be tuned by varying the inductance or capacitance. However, when capacitance tuning is used, both capacitors must be tuned at the same time. Since C3 and C4 (fig. 2-13) form a voltage divider network for the regenerative feedback, if one capacitor is varied, the ratio of C3 and C4 changes and the amount of feedback changes. To maintain the ratio and thus reduce the possibility of distortion or loss of oscillations, capacitors connected on the same shaft (ganged capacitors) are used with capacitive tuning.

Exercises (007):

1. The identifying feature of the Colpitts oscillator is ________ ________.
2. Refer to figure 2-12. The purpose of R2 and R3 is to act as a ________ ________ ________ for ________ ________.
3. The transistor ________ ________ becomes part of the tank capacitance when a tank circuit is connected ________ a junction of a transistor.



34-1429

Figure 2-14. N-type JFET oscillator (tuned gate).

4. The Colpitts oscillator has two capacitors that are of different sizes. This allows for good _______ _______ _______. They also act as a voltage divider to insure the _____ _____ of _______.
5. The Colpitts oscillator may be tuned by varying the _______ or _______.

008. Name the frequency-determining device and the desirable features of the tuned-gate oscillator.

Tuned-Gate Oscillator. The junction field effect transistor (JFET) has characteristics that make it well suited for oscillator circuits. Figure 2-14 shows the schematic of an N-type JFET RF oscillator.

This is called a tuned-gate oscillator because the frequency-determining device is in the gate circuit. Observe that the requirements for an oscillator are present: Amplification with Q1, frequency-determining device L2 and C1, and regenerative feedback L2 to L2. The feedback path is from the drain, through the transformer primary L1, to the frequency-determining device L2 and C1, to the gate. L3 is a loose-coupled third winding of the transformer used to couple the signal to the load. R1 is the bias resistor, and C2 prevents degeneration.

One of the desirable features of this circuit is the high Q that can be obtained in the frequency-determining device (L2-C1). The input impedance to the gate is 1 to 10 megohms, and the frequency-determining device is in parallel with this high impedance. Recall the formula for Q using resistance parallel to the tank circuit:

$$Q = \frac{R}{X_L}$$

The high impedance of Q1 does not load the tank circuit, so the Q of the tank remains high and oscillates at a constant frequency, free of undesired variations.

Exercises (008):

1. What is the frequency-determining device in a tuned-gate oscillator?
2. What are the desirable features of the tuned-gate oscillator?

009. Identify characteristics of crystals.

Characteristics of Crystals. Crystal oscillators are the standard means of maintaining the frequency of radio transmitting stations at the desired value. They are also used extensively in receiver systems which involve specified frequencies. A natural quartz crystal has a hexagonal cross section, pointed ends, and three axes (fig. 2-15). The axis joining in the points at the ends of the crystal is the optical, or Z, axis. The three diagonals passing through the corners of the hexagonal cross section are the electrical, or X, axes. The three lines which are perpendicular to the faces of the crystal are called the mechanical, or Y, axes.

Sections cut from such a crystal exhibit the property of piezoelectricity. Figure 2-16 shows three types of cuts. The X-cut is cut with the face of the crystal perpendicular to the Y-axis. The AT-cut is a special cut with the face of the crystal at a 35° angle to the Z-axis. The purpose of the special cut is to increase the stability of the crystal by reducing its temperature drift. Temperature drift is the name given to changes in the crystal resonant frequency resulting from changes in temperature. The temperature coefficient expresses the relationship between the frequency change and the temperature change, and it is determined by the type of cut. If the frequency increases with a temperature rise, the crystal has a positive temperature coefficient (Y-cut); if the frequency decreases with a temperature rise, the crystal has a negative temperature coefficient (X-cut); if variations in temperature have little or no effect on frequency, the crystal has a zero temperature coefficient (AT-cut).

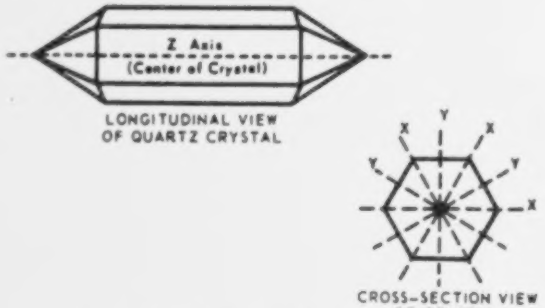

Z Axis
(Center of Crystal)
LONGITUDINAL VIEW OF QUARTZ CRYSTAL
Y
X
X
Y
Y
X
CROSS-SECTION VIEW OF CRYSTAL

Figure 2-15. Quartz crystal.

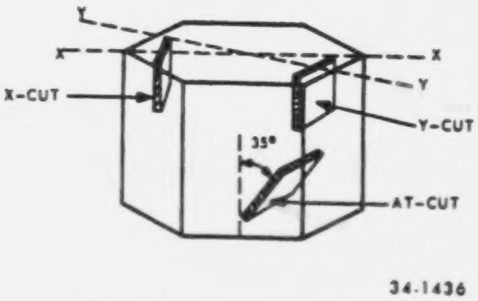


Figure 2-16. Types of cuts of crystal.

In addition to a special cut (such as the AT-cut), circuits which require a very high degree of frequency stability use temperature controlled ovens to prevent variations in crystal temperature. These ovens are thermostatically controlled containers in which the crystals are placed.

At the series resonant frequency, determined by the mechanical vibrating characteristics of the crystal, the impedance of the crystal is low. At a frequency slightly above series resonance, the inductive reactance is greater than the capacitive reactance, and the net inductance combines with the capacitance between the electrodes to form a parallel resonant circuit. At parallel resonance, the resonant frequency is determined by the crystal and the externally connected circuit elements, and the impedance is high. Table 2-1 will give you an idea of the size and electrical characteristics of a typical crystal.

The high-frequency limit of a crystal is restricted by the dimensions to which the crystal can be ground and still be rugged enough to be useful. For this reason, circuits have been developed in which a crystal will vibrate at frequencies greater than the fundamental frequency. These frequencies are called overtones and represent additional resonant frequencies. Crystal overtones differ from harmonics in that they are not exact multiples of the fundamental frequency. When the crystal is manufactured for overtone operation, it vibrates in several sctions. For example, if it vibrates in three sections, it is a third overtone crystal.

TABLE 2-1

ELECTRICAL CHARACTERISTICS OF A TYPICAL CRYSTAL

Inductance	3.3 henrys
Capacitance	.042 picofarads
Capacitance of Holder	5.8 picofarads
Q	23,000
Thickness	0.25 inches
Width	1.3 inches
Length	1.08 inches
Resonant Frequency	430 kilohertz

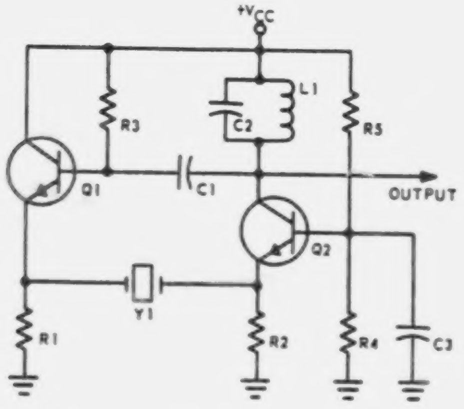


Figure 2-17. Crystal oscillator (butler type).

Exercises (009:

1. A natural quartz crystal has a ________ cross section, ________ ends, and ________ axes.
2. The temperature coefficient expresses the relationship between the ________ change and the ________ change, and is determined by the ________ of cut.
3. A Y-cut crystal has a ________ temperature coefficient.
4. At ________ resonance, the resonant frequency is determined by the crystal and the ________ ________ ________ ________.

010. Name the two primary features of the Butler oscillator and state the functions of given components in a schematic of a Butler oscillator.

Butler Oscillator. The Butler oscillator, shown in figure 2-17, has two primary identifying features: two transistors are used, and a crystal is connected between the emitters. The purpose of the components is listed below:

R1	Emitter resistor of Q1, develops the emitter output of Q1.
R2	Emitter resistor of Q2, develops the input signal to Q2.
Y1	Frequency-determining device.
R4 and R5	Forward-bias voltage divider for Q2.
C3	Base bypass capacitor for Q2.
L1 and C2	Resonant tank-load impedance for collector of Q2.
C1	Coupling capacitor.
R3	Forward-bias resistor for Q1.

Q1 is a common-collector configuration, and Q2 is a common-base configuration. The regenerative feedback path is as follows: from the collector of Q2, through C1 to the base of Q1, to the emitter of Q1, through the crystal Y1, and back to the emitter of Q2. The regenerative feedback must pass through the crystal. The crystal is operated in its series-resonant mode. At its resonant frequency, the crystal has a very low impedance and will pass the feedback signal to the emitter of Q2. All other frequencies will be blocked because of the high impedance of the crystal.

The output signal from the circuit can be obtained directly from the collector of Q2. The tank circuit, L1 and C2, will flywheel and produce a signal on the collector. At the same time, the crystal is vibrating to produce a signal on the emitter of Q2. With both transistors operated class C, Q2 will be cut off for a majority of the time. This condition provides buffer action between the collector circuit of Q2 and the crystal. When the output is taken from the collector, the external load will have very little effect on the crystal operation. This eliminates the need for another circuit to provide buffer action. Remember that the frequency determining device is the crystal and not L1 and C2. The L1 and C2 resonant frequency should be near that of the crystal. When both transistors are operated class A, L1 and C2 can be replaced by a resistor.

Exercises (010):

1. What are the two primary features of the Butler oscillator?

2. Refer to figure 2-17. What is the purpose of R3?

3. What is meant by series-resonant mode of a crystal?

4. Refer to figure 2-17. Where is the output taken from?

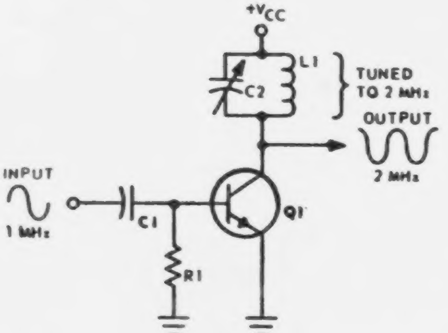


Figure 2-18. Frequency multiplier.

011. Cite characteristics of frequency multipliers.

Frequency Multipliers. To obtain higher frequencies than the resonant frequency of an oscillator, the oscillator output can be fed to a frequency multiplier. As the name implies, a frequency multiplier circuit is one whose output frequency is some multiple of the input frequency. For example, a frequency doubler will double the input frequency, a tripler will triple the frequency, and a quadrupler will multiply the input frequency by four.

To multiply a frequency, a circuit must generate harmonic frequencies in the output. This requires class B or class C amplifier operation. Figure 2-18 is the schematic of a frequency multiplier, a doubler in this example. Assume that Q1 operates class C. Q1 is cut off with no input signal because it has no forward bias. During the positive alternation of the input signal, Q1 is forward-biased by the signal and coupling capacitor C1 charges rapidly. Once the capacitor is charged and the input signal starts in the negative direction, the transistor is cut off. The only discharge path for C1 is through R1. This is a long-time constant, so C1 cannot discharge very fast. The average voltage on C1 becomes the reverse bias for the base-emitter junction and allows class C operation for the transistor. Of necessity, the input signal must be larger than that normally applied to an amplifier circuit.

With class C operation, the transistor will generate many harmonics of the input signal. The output signal is the harmonic to which the collector-tank circuit is tuned. In figure 2-18, the tank circuit is tuned to the second harmonic of the input signal. With 1 megahertz input, the output signal will be a sine-wave signal of 2 megahertz.

If the collector tank were tuned to 3 megahertz—the third harmonic of the input signal—the output would be 3 megahertz. The same is true with the fourth harmonic. The fourth harmonic, or frequency quadrupler, is normally as high in multiplication as practical, because, as you tune to higher harmonics, the output signal becomes weaker. Two doublers are often more desirable than one quadrupler. Although each will produce the same frequency multiplication, two doublers provide more power in the output signal.

If the input frequency and the component values of the tank circuit are known, you can determine whether the stage is a doubler or tripler. For example, if the input signal is 10 MHz, would a .026 millihenry inductor and a 4-picofarad capacitor form a frequency doubler or tripler? Using the formula:

$$f_r = \frac{.159}{\sqrt{LC}}$$

we find the tank circuit's resonant frequency

$$f_r = \frac{.159}{\sqrt{.016} \times 10^{-3} \times 4 \times 10^{-12}}$$

$$= \frac{.159}{\sqrt{.064} \times 10^{-15}} = \frac{.159}{\sqrt{64 \times 10^{-18}}}$$

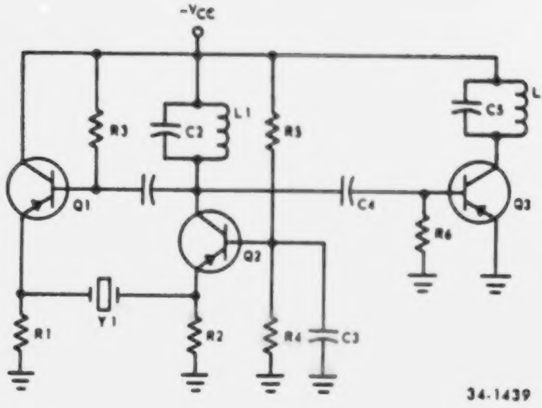


Figure 2-19. Butler oscillator and frequency multiplier.

$$= \frac{.159}{8 \times 10^{-9}} = 19.9 \text{ or } 20 \text{ MHz}$$

So these tank component values make a frequency doubler. In a problem of this type, rounding off .159 to .16 will simplify the calculations.

Another feature of frequency multipliers is that they provide the characteristics of a buffer amplifier. Since the transistor is operated class C, the load of the multiplier does not reflect impedance back to the base circuit. And, because of class C operation, the input impedance to the base is relatively high (the base-emitter junction is reverse-biased most of the time). Figure 2-19 shows the schematic of a Butler oscillator connected to a frequency multiplier. Q3 and its circuitry are the frequency multiplier, which also serves as a buffer amplifier for the oscillator.

Exercises (011):

1. A frequency multiplier circuit is one whose ________ frequency is some ________ of the input frequency.
2. In order for a circuit to multiply a frequency, it must generate ________ ________ in the output.
3. Refer to figure 2-18. The ________ voltage on C1 becomes the reverse bias for the ________ ________ ________ and allows class ________ operation for the transistor.
4. A frequency ________ is normally as high in multiplication as practical, because, as you tune to higher harmonics, the output signal ________ ________.
5. The advantage of using two doublers instead of one quadrupler is that two doublers provide ________ ________ in the ________ ________.
6. Other features of frequency multipliers are that they provide the characteristics of a ________ ________ and there is usually no need for ________ or ________ of the circuit.

012. State how blocking oscillators operate.

Blocking Oscillator. The blocking oscillator is a special type of wave generator used to produce a narrow pulse, sometimes called a trigger. Blocking oscillators have many uses, most of which are concerned with the timing of some other circuit. They can be used as frequency dividers or counter circuits, and for switching other circuits on and off at specific times. This objective discusses a basic blocking oscillator circuit and its output waveforms.

Before going into the blocking oscillator circuit, several general considerations which apply to all blocking oscillators need to be discussed. First, the timing pulses of electronic circuits have strict requirements. The times involved vary from a few hundredths of a microsecond to several thousand microseconds.

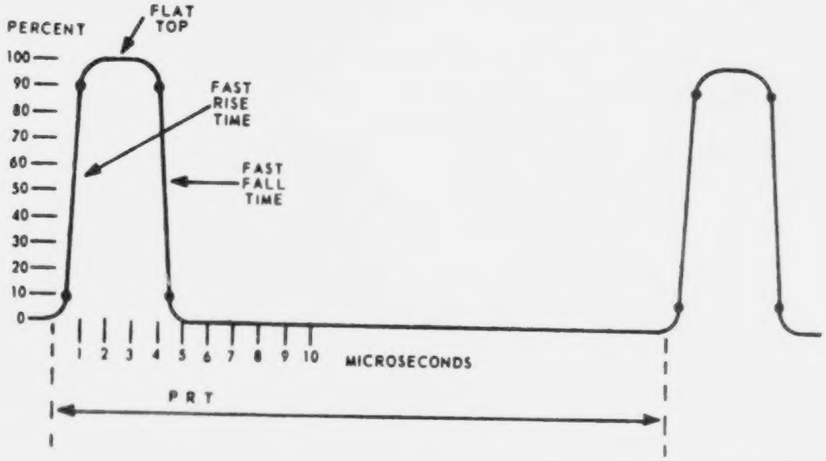
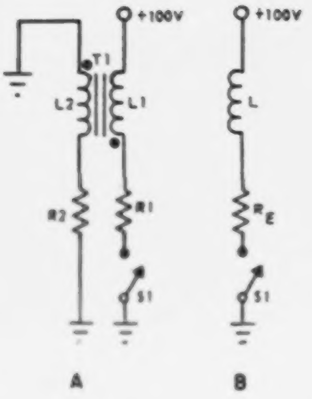


Figure 2-20. Timing pulses.



34-1441

Figure 2-21. RL circuits.

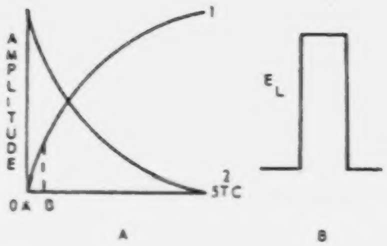
Figure 2-20 shows two timing pulses. The basic requirements are:

(1) Fast rise time.
(2) Flat top.
(3) Flat fall time.
(4) Specific and accurately controllable frequency. The leading edge of the pulse should be as steep as possible; that is, the rise time should be short. The top of the pulse should be as flat as possible, especially when the duration is long. The trailing edge of the pulse should also be as steep as possible; that is, the fall time should be short. The pulse recurrence time (PRT) should be stable and accurately controllable because it determines the pulse recurrence frequency (PRF). In a free-running blocking oscillator, the pulse width (PW), PRT, and PRF are all controlled by the size of certain resistors and capacitors and by the operating characteristics of the transformer. The transformer primarily determines the duration and shape of the output. Because of its importance in the circuit, let's briefly discuss transformer action and review series RL circuits.

Figure 2-21, A, shows a transformer with resistance in both the primary and secondary circuits. If S1 is closed, current will flow through R1 and L1. As the current rises, it induces a voltage into L2. With induced voltage in L2, a current flows through R2. The voltage across L2 depends on the turns ratio between L1 and L2.

The secondary load impedance, R2, will affect the primary impedance through reflection from secondary to primary. If we increase the load on the secondary (decrease R2), we also increase the load on the primary. Similarly, if we decrease R1, primary and secondary currents increase.

Since T1 has an effective inductance, and since any change in R1 or R2 will change the current, we can show T1 as an inductor and R1-R2 as a combined or equivalent series resistance. The equivalent circuit is shown in figure 2-21, B. It acts as a simple series RL circuit, and we can discuss it in those terms.



34-1442

Figure 2-22. Voltage across a coil.

In the simple series RL circuit, when S1 is closed, L acts as an open at the first instant, and the source voltage appears across it. As current begins to flow, E_L decreases, and E_R and I increase, all at exponential rates. Figure 2-22, A, shows these curves. In a time equal to 5 time constants

$$(5 \times \frac{L}{R_E})$$

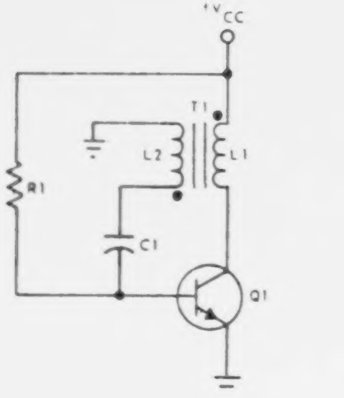
voltage and circuit current will be maximum, and E_L will be 0.

If we close S1 in figure 2-21, B, the current will follow curve 1 of figure 2-22, A. The time required for the current to reach maximum depends on the size of L and R_E. If R_E is small, then we have a long time constant RL circuit. If we use only a small portion of curve 1 (A to B), then the current rise would have maximum change in a given time period. Further, the smaller the time increment, the more nearly linear is the current rise. A constant current rise through the coil is a key factor in a blocking oscillator.

A basic principle of inductance is that, if the rise of current through a coil is linear—that is, if the rate of current rise is constant with respect to time—then the induced voltage will be constant. This is true in both the primary and secondary of a transformer. Figure 2-22, B, shows the voltage across the coil when the current through it rises at a constant rate. Notice that this is similar in shape to the trigger pulse in figure 2-20.

Now we are ready to discuss a blocking-oscillator circuit. By definition, a blocking oscillator is a special type of oscillator which uses inductive regenerative feedback, with output duration and frequency determined by the characteristics of a transformer and its relationship to the circuit. Figure 2-23 shows the schematic of a blocking oscillator. This is a simplified form used to discuss circuit operation.

When power is applied to the circuit in figure 2-23, R1 provides forward bias and transistor Q1 conducts. Current flow through Q1 and the primary of T1



34-1443

Figure 2-23. Blocking oscillator.

induces a voltage of L2. The phasing dots on the transformer indicate that there is a 180°-phase shift. So, as the bottom side of L1 is going negative, the bottom side of L2 is coupled to the base of the transistor through C1, and Q1 conducts harder. This provides more collector current and more current through L1. This action is regenerative feedback. Very rapidly a voltage is applied to the base of the transistor that is sufficient to saturate the base. Once the base becomes saturated, it loses control over collector current. This circuit now can be compared to a small resistor (Q1) in series with a relatively large inductor (L1), or a series RL circuit.

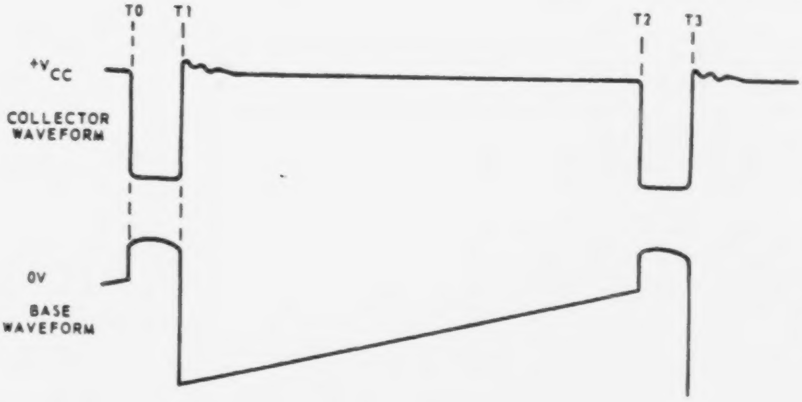
The operation of the circuit to this point has generated a very steep leading edge of the output pulse. Figure 2-24 shows the idealized collector and base waveforms. Once the base of Q1 becomes saturated, the current rise in L1 is determined by the time constant of L1 and the total series resistance. From T0 to T1 in figure 2-24, the current rise will be approximately linear. The voltage across L1 will be a constant value as long as the current rise through L1 is linear.

At time T1, L1 saturates. At this time, there is no change in magnetic flux and thus no coupling from L1 to L2. C1, which has charged during time T0 to T1, will now discharge through R1 (fig. 2-23). This discharge of C1 will place a negative voltage on the base of Q1 and cut Q1 off. This will cause collector current to stop, and the voltage across L1 will return to 0.

The length of time between T0 and T1 is the pulse width, which depends mainly on the characteristics of the transformer and on the point that the transformer saturates. A transformer is chosen that will saturate about 10 percent of the total circuit current. This insures that the current rise is nearly linear. The transformer controls the pulse width because it controls the slope of collector current rise between points T0 and T1. Since TC = L/R, the greater the L, the longer the TC. The longer the time constant, the slower the rate of current rise. When the rate of current rise is slower, the voltage across L1 is constant for a longer time. This primarily determines the pulse width.

From T1 to T2 (fig. 2-24), transistor Q1 is held at cutoff by C1 discharging through R2 (fig. 2-23). The transistor is now said to be "blocked." As C1 gradually loses its charge, the voltage on the base of Q1 gradually returns to a forward-bias condition. At T2, the voltage on the base has become sufficiently positive to forward bias Q1, and the cycle repeats.

The collector waveform may have an inductive overshoot of "parasitic oscillations" at the end of the pulse. When Q1 cuts off, current through L1 ceases, and the magnetic field collapses, inducing a positive voltage at the collector of Q1. These oscillations are not desirable, so some means has to be employed to



34-1444

Figure 2-24. Idealized waveforms.

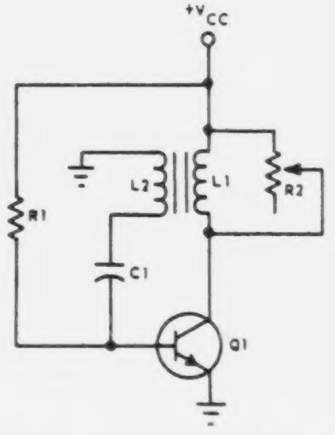

+VCC
L2
L1
R2
R1
C1
Q1
34-1445

Figure 2-25. Circuit damping.

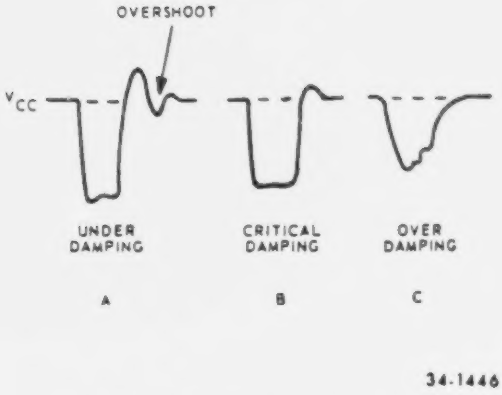

OVERSHOOT
VCC
UNDER DAMPING
CRITICAL DAMPING
OVER DAMPING
A
B
C
34-1446

Figure 2-26. Waveform damping.

reduce them. The transformer primary may have a high DC resistance and, thus, a low Q; this will decrease the amplitude of these oscillations. It may be necessary, however, to have more damping than a low Q coil alone can achieve. If so, a swamping or damping resistor can be placed in parallel with L1, as shown in figure 2-25.

When an external resistance is placed across a tank, the formula for Q of the tank circuit is $Q = X_L$ where R is the equivalent total circuit resistance, in parallel with L. You can see from the equation that the Q in figure 2-25 is directly proportional to the damping

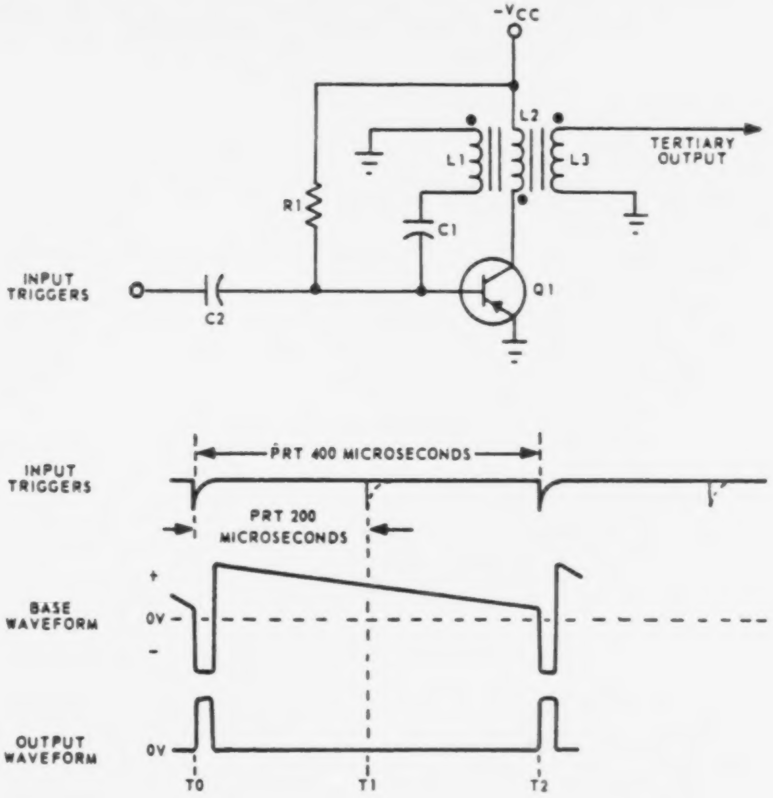

-VCC
L2
L1
L3
TERTIARY OUTPUT
R1
C1
Q1
INPUT TRIGGERS
C2
PRT 400 MICROSECONDS
INPUT TRIGGERS
PRT 200 MICROSECONDS
+
BASE WAVEFORM
0V
-
OUTPUT WAVEFORM
0V
T0
T1
T2
34-1447

Figure 2-27. Synchronized blocking oscillator.

resistance. Damping resistor R2 is used to adjust the Q and thus reduce the amplitude of overshoot or parasitic oscillations. As R2 is varied from infinity toward zero, the decreasing resistance will load the transformer to the point that pulse amplitude, pulse width, and PRF are affected. If reduced enough, the oscillator will cease to function. By varying R2, different degrees of damping can be achieved, three of which are shown in figure 2-26. Critical damping gives the most rapid transient response with maximum overshoot. Figure 2-26, B, shows that oscillations are damped out. Underdamping gives rapid transient response with overshoot. Figure 2-26, A, shows underdamping. Overdamping gives a slower transient response and may reduce the pulse amplitude, as shown in figure 2-26, C.

The blocking oscillator we have been discussing is a free-running circuit. For a fixed PRF, we need some means of stabilizing the frequency. One method is to apply external synchronization triggers. (Refer to fig. 2-27.) Coupling capacitor C2 feeds input synchronization (sync) triggers to the base of Q1.

If we make the trigger frequency slightly higher than the free-running frequency, the blocking oscillator will "lock in" at the higher frequency. For instance, assume the free-running frequency of this blocking oscillator is 2 kHz, with a PRT of 500 microseconds. If sync pulses with a PRT of 400 microseconds or 2.5 kHz are applied to the base, the blocking oscillator will "lock in" and run at 2.5 kHz. If the sync PRF is too high, however, frequency division will occur. This simply means that if the synchronization (sync) PRT is too short, some of the triggers occur when the base is far below cutoff. The blocking oscillator may then synchronize with every second or third sync pulse. For example, in figure 2-27, if trigger pulses are every 200 microseconds (5 kHz), the trigger that appears at T1 is not of sufficient amplitude to overcome the cutoff bias and turn Q1 on. At T2 capacitor C1 has nearly discharged and the trigger does cause Q1 to conduct. Note that with 200 microsecond triggers, the output PRT is 400 microseconds. The output frequency is thus one-half the input trigger pulse frequency, and this blocking oscillator becomes a frequency divider.

Exercises (012):

1. Blocking oscillators can be used as frequency ________ or counter ________, and for switching other circuits ________ and ________ at specific times.
2. The basic requirements for a timing pulse are a fast ________ ________, ________ ________, ________ ________ ________, and specific and ________ ________ frequency.
3. The PRT determines the ________.
4. Refer to figure 2-21. If the load on the secondary is increased, the load on the primary will ________.
5. A ________ ________ ________ through the coil is a key factor in a blocking oscillator.
6. A blocking oscillator uses ________ regenerative feedback.
7. Refer to figure 2-23. When the base becomes saturated, the circuit can be compared to a small ________ in series with a relatively large ________.
8. Refer to figure 2-23. As C1 discharges, it will place a ________ voltage on the base of Q1 and ________ ________ ________.
9. When an external resistance is placed across a tank, the formula for Q of the tank circuit is ________.
10. ________ damping gives the most rapid transient response with minimum overshoot.

CHAPTER 3

Multivibrators

THE MULTIVIBRATOR is a form of relaxation oscillator. It is widely used in electronic equipment, such as computers, radar sets, television sets, electronic switches, stroboscopes, and oscilloscopes. A multivibrator is a two-stage amplifier with the output of the second stage fed back regeneratively to the input of the first stage. Some are free-running, and others require that a trigger be introduced into the circuit to control the frequency of operation.

3-1. Theory and Operation of Multivibrators

Many electronic circuits are not in an on condition all of the time. In computers, for example, waveforms must be turned on and off at specific times and for specific lengths of time. The time intervals vary from tenths of microseconds to several thousand microseconds. Square or rectangular waveforms provide the switching action.

This chapter discusses methods of generating square and rectangular waves, using multivibrators. There are several terms and characteristics of square and rectangular waves that must be discussed prior to the circuitry itself. Let's first review terms you already know; then we will discuss new terms.

013. Define terms associated with waveforms.

Waveforms. A waveform that undergoes a pattern of changes, returns to its original value, and repeats the same pattern of changes is called a periodic waveform. Each completed pattern is called a cycle, and the time for each cycle is called the period of the waveform. The frequency of the waveform is the number of cycles or periods completed in 1 second.

Figure 3-1 shows a square-wave pattern. A square wave is identified by two alternations, equal in time. The amplitude is measured vertically, and the time of a completed cycle is measured between corresponding points on the wave (T0 to T2, or T1 to T3).

One alternation is often called a pulse. In this case, the time for one complete cycle is called the pulse recurrence time (PRT). The pulse recurrence frequency (PRF) represents how many times a second the cycle repeats itself. In figure 3-1, if each alternation were 200 microseconds, the PRT would be 400 microseconds, and the PRF is 2,500 Hertz.

$$\mathrm{PRF} = \frac{1}{\mathrm{PRT}} \text{ and } \mathrm{PRT} = \frac{1}{\mathrm{PRF}}$$

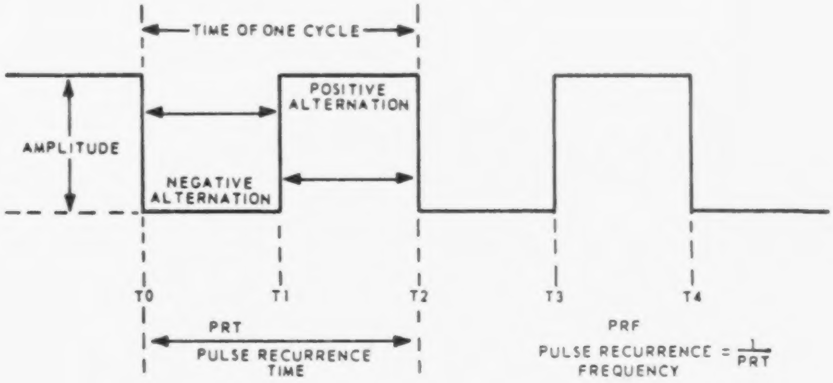
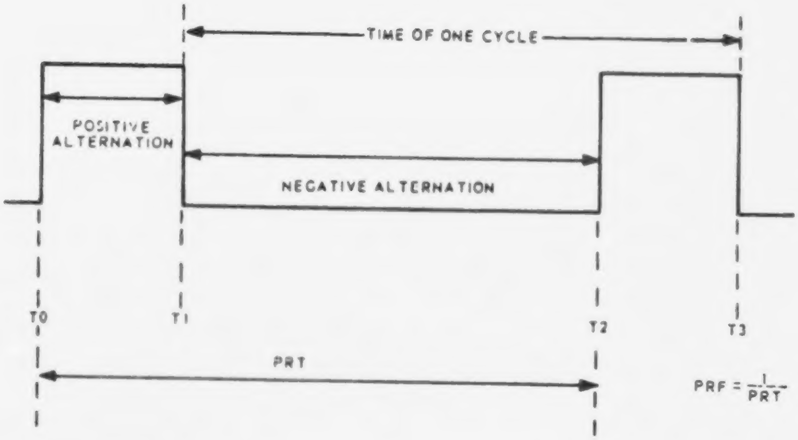


Figure 3-1. Square waves. 34-1452


TIME OF ONE CYCLE
POSITIVE ALTERNATION
NEGATIVE ALTERNATION
T0
T1
T2
T3
PRT
PRF = 1/PRT

34-1453

Figure 3-2. Rectangular waves.

Figure 3-2 shows a typical rectangular wave. A rectangular wave has two alternations, unequal in time. (Fig. 3-2 shows the negative alternation longer than the positive, although this could be the other way around.) If the negative alternation is 300 microseconds and the positive alternation is 100 microseconds, the PRT is 400 microseconds, and the PRF is 2,500 Hertz.

Another important part of square and rectangular waves is the transient interval, shown in figure 3-3. It takes time for a voltage or current to change in amplitude. The transient interval is the total time required to go from 0 percent to 100 percent of the applied voltage or from 100 percent to 0 percent. Transient intervals occur on the leading edge of the pulse and on the trailing edge of the pulse.

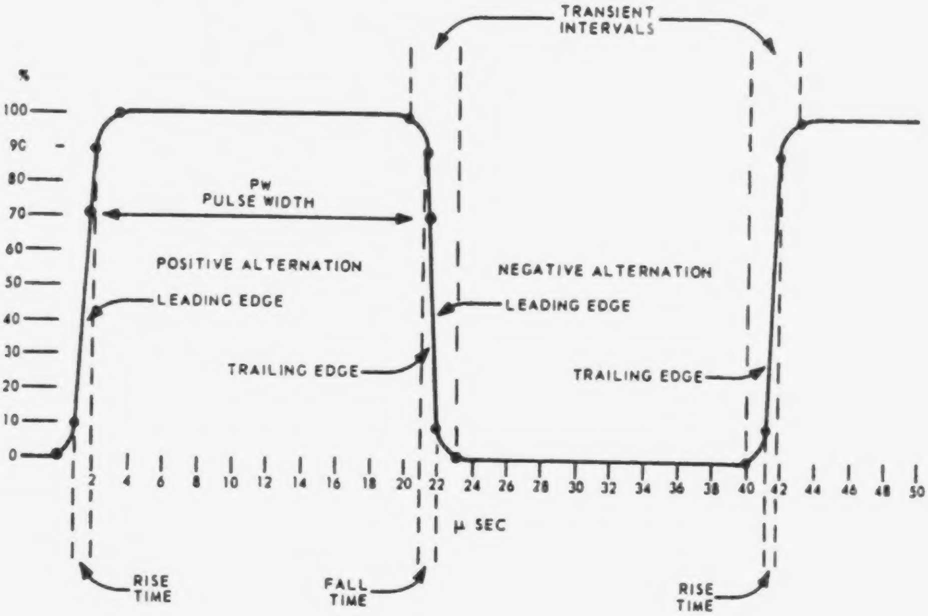
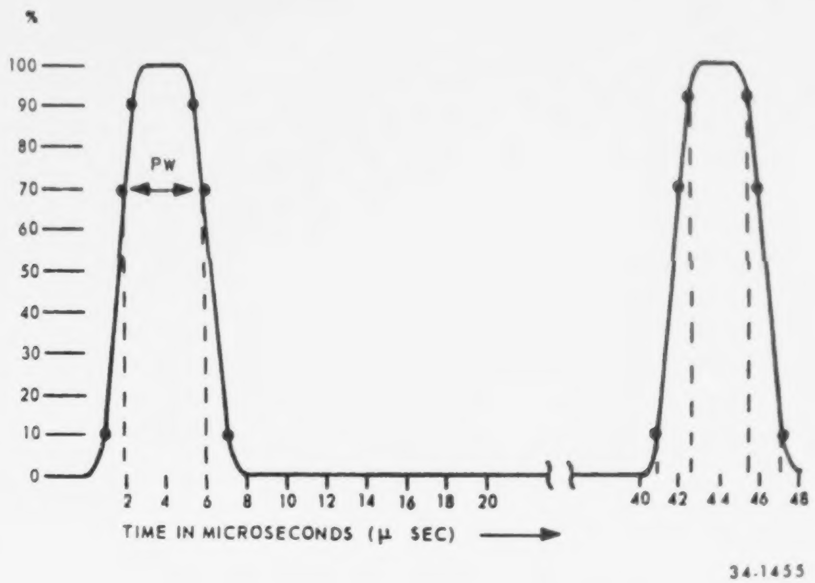

TRANSIENT INTERVALS
%
100
90
80
70
60
50
40
30
20
10
0
PW
PULSE WIDTH
POSITIVE ALTERNATION
NEGATIVE ALTERNATION
LEADING EDGE
LEADING EDGE
TRAILING EDGE
TRAILING EDGE
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
32
34
36
38
40
42
44
46
48
50
μ SEC
RISE TIME
FALL TIME
RISE TIME

Figure 3-3. Square waves with transient intervals.

34-1454



34-1455

Figure 3-4. Rectangular waves with transient intervals.

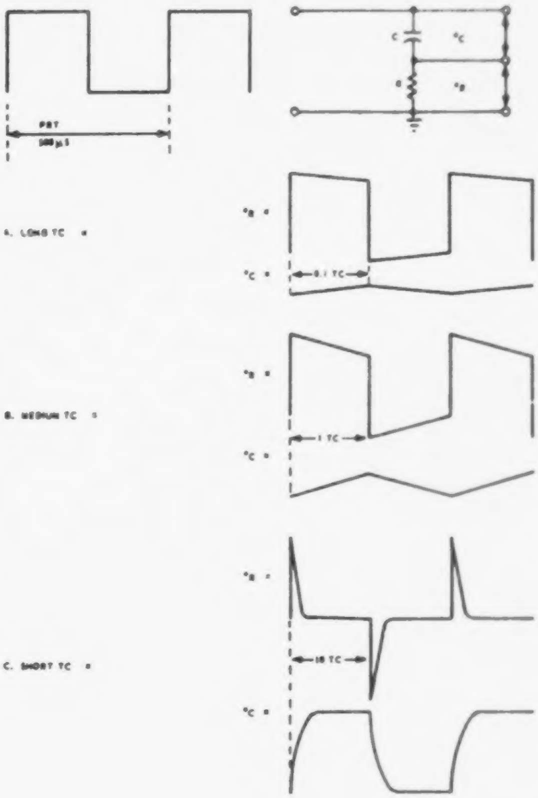
Other names used with transient intervals are rise time and fall time. Rise time is defined as the time required for the voltage to build up from the 10-percent to the 90-percent amplitude point. Fall time is the time required for the voltage drop from the 90-percent point to the 10-percent point. Figure 3-3 shows a transient interval of 3 microseconds and a rise time of 1 microsecond. The rise and fall times of a wave are not necessarily equal.

Another term used is pulse width (PW). This indicates the length of the pulse measured in time, and it is often expressed as the time between the half-power points (.707 times the peak pulse amplitude). Figure 3-3 shows the pulse width, measured at the 70-percent points, as approximately 19.4 microseconds. In computers, pulse width is the time between the two 90-percent points.

You may ask, "Why worry about transient interval?" This is a logical question; to answer it, look at figure 3-4. Notice that the PW is 4 microseconds and that the rise time and fall time make up a large percentage of the pulse. To have a rectangular pulse, the transient interval must be as small as a fraction of a microsecond. Waveforms like these should have very short rise and fall times. This waveform is often called a trigger. A trigger is normally used to turn other circuits ON or OFF.

Many times a circuit must pass square or rectangular waves; in these cases, the coupling circuits must pass the waveform without distortion. Other times the wave is deliberately distorted. Whether the signal is coupled with or without distortion depends on the coupling circuit.

Figure 3-5 shows a square wave applied to a series RC circuit. The waveforms for long, medium, and



34-1456

Figure 3-5. Square wave applied to RC circuit.

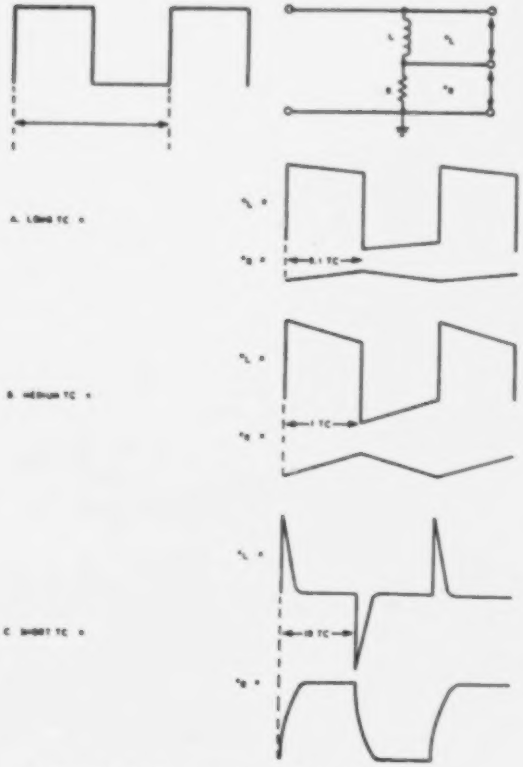


Figure 3-6. Square wave applied to RL circuit.

short time constants give a good picture of whether the signal is distorted or not. Let's analyze these waveforms in closer detail. With an input square wave that has a PRT of 500 microseconds, each alternation will be 250 microseconds. The time constant of R × C (TC = RC) must be greater than 2,500 microseconds to be a long TC. (Recall that a long TC exists when the RC product is 10 or more times the time for an alternation.) For the long TC shown in figure 3-5, A, notice that e_C is very small in amplitude and that e_R is approximately the same shape and amplitude as the input signal. An output taken across R, then, has little distortion.

A medium TC is an RC product that is .1 to 10 times the time for one alternation—in this case, 25 to 2,500 microseconds. Figure 3-5, B, shows that e_C is larger in amplitude and that e_R is no longer square. An output taken across either component is distorted with respect to the input signal.

For a short TC, the RC product is .1 (or less) of time for one alternation. The waveshapes of figure 3-5, C, show how e_C resembles the input, but will have rounded corners. The voltage across R is greatly distorted when compared to the input. The e_R now resembles a trigger, and it can be used for this purpose. So, by proper selection of components, a square wave can be coupled to another circuit without distortion, or it can be changed into triggers, whichever is required.

A series RL circuit can do a similar job. Figure 3-6 shows the circuit with the same square-wave input. Figure 3-6, A, shows a long-time constant. Recall TC =L/R, and when the time or L/R is 10 or more times one alternation of the wave, we have a long TC. The undistorted signal is e_L, and e_R has only a small voltage across it. The medium TC of figure 3-6, B, has the time of the applied square-wave alternation equal to L/R. Both e_L and e_R are distorted with respect to the input. For a short TC, L/R is one-tenth (or less) of the time for one alternation. Figure 3-6, C, shows that the short TC produces a reasonably good square wave across the resistor and a trigger across the coil.

Exercise (013):
Place the letter corresponding to the correct choice from column B in front of the appropriate term in column A.

Column A

____ (1) Short time constant.
____ (2) Pulse width.
____ (3) Rise time.
____ (4) Pulse recurrence frequency.
____ (5) Frequency of waveform.
____ (6) Medium time constant.
____ (7) Fall time.
____ (8) Transient interval.
____ (9) Pulse recurrence time.
____ (10) Periodic waveform.

Column B

a. L/R is one-tenth or less of the time for one alternation.
b. The time for one complete cycle.
c. The time required for the voltage to drop from the 90-percent to the 10-percent amplitude point.
d. The number of times a second the cycle repeats itself.
e. Undergoes a pattern of changes, returns to its original value, and repeats the same pattern of changes.
f. The total time required to go from 0 percent to 100 percent of the applied voltage or from 100 percent to 0 percent.
g. The RC product that is .1 to 10 times the time of one alternation.
h. Indicates the length of the pulse measured in time, and is often expressed as the time between the half-power point (.707 times the peak pulse amplitude).
i. The time required for the voltage to build up from the 10 percent to 90 percent amplitude point.
j. The number of cycles or periods completed in 1 second.

014. Identify types of multivibrators with their operating characteristics.

Types of Multivibrators. The type of circuit most often used to generate square or rectangular waves is a multivibrator. A multivibrator is basically two amplifier circuits arranged with regenerative feedback. Usually, one of the amplifiers is conducting while the other is cut off.

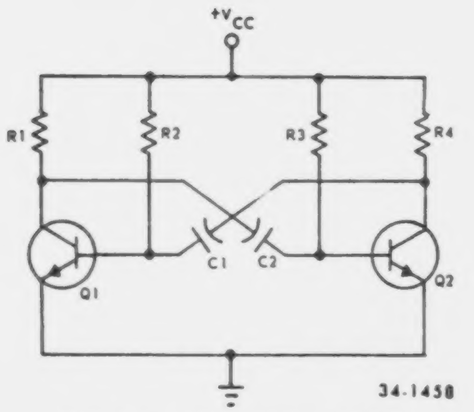


Figure 3-7. Astable multivibrator (NPN).

When an input signal is large enough, the transistor can be driven into cutoff, and its collector voltage will be approaching V_{cc}. When the transistor is driven into saturation, its collector voltage will be about 0 volts. By designing the circuit to make transistors go quickly from cutoff to saturation, a square or rectangular wave can be produced. This principle is used in multivibrators.

In general, there are three types of multivibrators, according to the number of steady (stable) states of the circuit. (A steady state exists when circuit operation is essentially constant; one transistor remains in conduction, and the other remains cut off until an external signal is applied.) The three types of multivibrators are:

(1) Astable—the circuit has no stable state. With no external signal applied, the transistors alternately switch from cutoff to saturation, at a frequency determined by the RC time constants of the coupling circuits.

(2) Monostable—as the name implies, this circuit has one stable state with one transistor conducting and the other cut off. A signal must be applied to change this condition. After a period of time, determined by the internal RC components, the circuit will return to its original condition, where it will remain until the next signal arrives.

(3) Bistable—this multivibrator has two stable states. It remains in one of the stable states until a trigger is applied; then it goes to the other stable condition to remain there until another trigger is applied to change it back to its first stable state.

Astable multivibrator. Figure 3-7 shows a collector-coupled astable multivibrator using NPN transistors, connected in a common-emitter configuration. The collector voltage of each transistor is coupled back to the base circuit of the other transistor. This provides regenerative feedback. R1 and R4 are the collector-load resistors; R2 and R3 provide the forward bias for the transistors; and C1 and C2 are the coupling capacitors. Assume that Q1 = Q2, R1 = R4, R2 = R3, and C1 = C2.

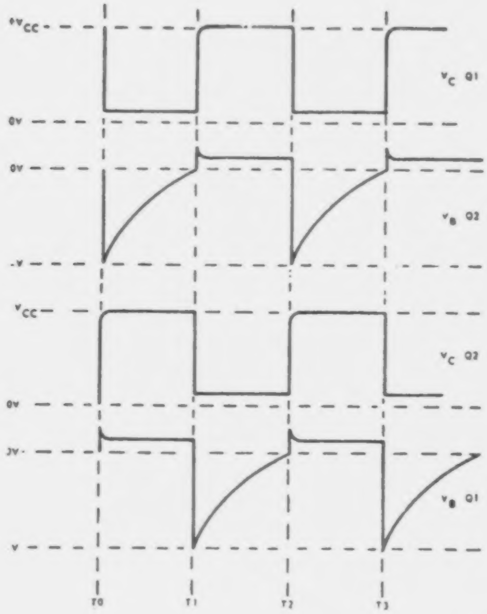


Figure 3-8. Astable multivibrator waveshapes.

When V_{cc} is applied, both transistors will conduct. Current will flow through the load resistors, R1 and R4, and the collector voltage on each transistor will drop to some value below V_{cc}. Since no two circuits can be exactly balanced, assume that Q1 conducts harder than Q2, causing the collector voltage of Q1 to decrease. C2, as it discharges through R3, couples this negative-going signal to the base of Q2. This negative voltage will cause Q2 to cut off, and the collector voltage of Q2 will increase to V_{cc}. C1 charges to V_{cc} through the forward-biased junction of Q1. Q1 is now saturated, and Q2 is cut off. This condition continues until C2 discharges enough to permit the emitter-base junction of Q2 to become forward-biased. When Q2 starts to conduct, its collector voltage decreases, causing C1 to discharge through R2. Discharging C1 couples a negative-going signal to the base of Q1, causing it to cut off. As Q1 cuts off, its collector voltage increases toward V_{cc}, and C2 charges to this value. Now, Q1 is cut off, and Q2 is conducting at saturation. The circuit remains in this state until C1 discharges enough to permit Q1 to conduct, and the cycle repeats.

Figure 3-8 shows the waveshapes for figure 3-7. Note that when the collector voltage of Q1 is near 0 volts, the collector voltage of Q2 is at V_{cc}. These waveshapes indicate that Q1 is saturated (on condition) and Q2 is cut off (*off* condition) from T0 to T1. The opposite conditions are shown between T1 and T2 (Q1 off and Q2 on). Refer once again to time T0-T1; note that, while Q2 is cut off (collector voltage at V_{cc}), the base waveshape for Q2 (V_{BQ2}) indicates a negative signal, going toward 0 volts. This waveshape

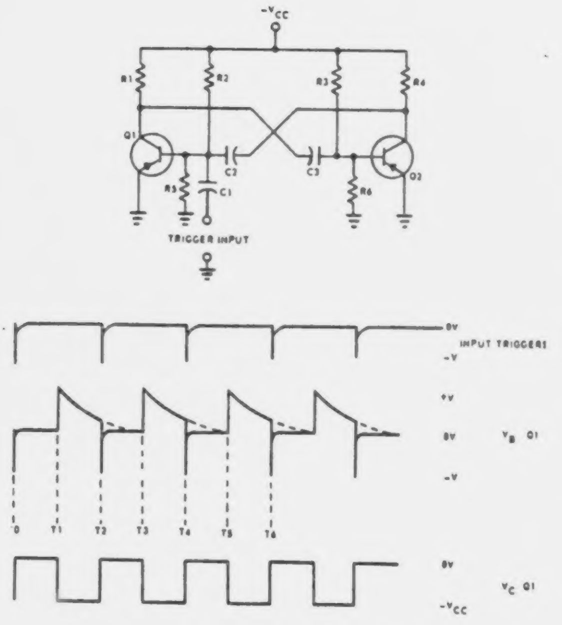


Figure 3-9. Triggered astable multivibrator.

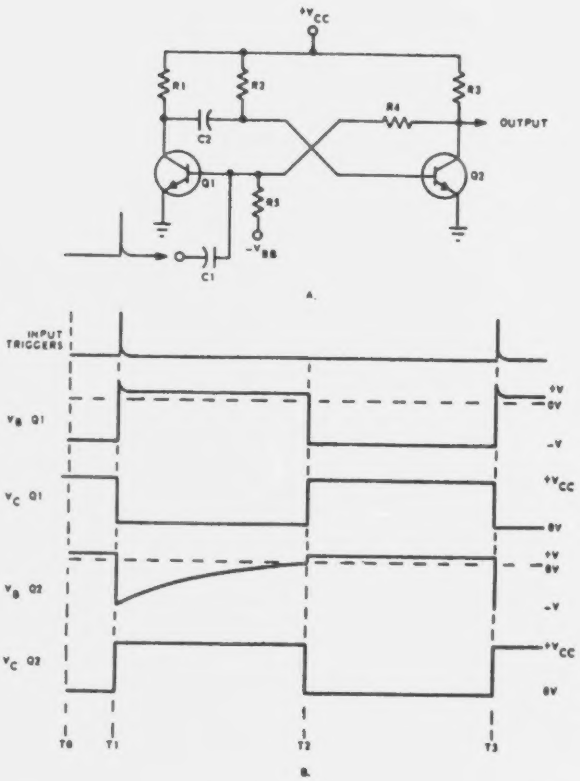


Figure 3-10. Monostable multivibrator with output waveshapes.

is a result of C2's discharging through R3, placing a negative signal on the base of Q2. Also, the base voltage of Q1 (T0-T1) indicates a positive voltage which is enough to keep it saturated. At T1, Q2 conducts, causing C1 to discharge, resulting in a negative voltage on the base of Q1 (V_{BQ1}). This action causes Q1 to cut off. From T1 to T2, Q1 is cut off, and Q2 is conducting. The circuit remains in this condition until C1 discharges enough to allow Q1 to conduct, at T2. Note that the collector voltage of Q1 does not go immediately to V_{cc} when it is cut off. The rounded portion of the waveshape is caused by C2 charging to V_{cc}. Therefore, the coupling capacitors affect the high-frequency response of the circuit.

The primary factors affecting the PRF and PRT of the circuit are the coupling components. The time each transistor is cut off depends on its time constant: C1-R2 for Q1, and C2-R3 for Q2. If C1 or R2 is increased, the cutoff time of Q1 is increased. If C2 or R3 is decreased, the cutoff time of Q2 is decreased.

Some astable multivibrators must have a high degree of frequency stability. A method of obtaining a greater degree of frequency stability is to apply triggers. Figure 3-9 shows the schematic of a triggered astable multivibrator using PNP transistors. At time T0, the negative input trigger to the base of Q1 causes Q1 to go into saturation, which drives Q2 to cutoff. The circuit will remain in this condition as long as the base voltage of Q2 is positive, determined by C3, R3, and R6. Observe the parallel paths for C3 to discharge.

At time T1, Q2 comes out of cutoff and goes into saturation. Also, Q1 comes out of saturation and is cut off. The base voltage waveform of Q1 (fig. 3-9) shows a positive potential that is holding Q1 cut off. This voltage would normally hold Q1 cut off until a point between T2 and T3. However, at time T2, another trigger is applied to the base of Q1, causing it to begin conducting. Q1 goes into saturation, and Q2 is cut off. This action repeats each time a trigger is applied (T2, T4, T6).

The PRT of the input triggers must be shorter than the natural free-running PRT of the astable multivibrator, or the trigger PRF must be slightly higher than the free-running PRF of the circuit. This is to make certain the triggers control the PRT of the output.

Monostable multivibrator. The monostable multivibrator (also called the one-shot multivibrator) is used in digital circuits for pulse stretching, pulse shaping, gate operation, and for providing adjustable delayed gates. This multivibrator is capable of producing several different types of outputs.

The integrated circuit (IC) one-shots available require the addition of a resistor and capacitor to set the timing for the IC. A second type of IC one-shot is the retriggerable one-shot. As long as a constant pulse frequency of some value is maintained at the input of the device, a constant output is present. This characteristic of the retriggerable one-shot makes it useful as a missing pulse detector.

The monostable multivibrator is a square or rectangular wave generator with one stable condition.

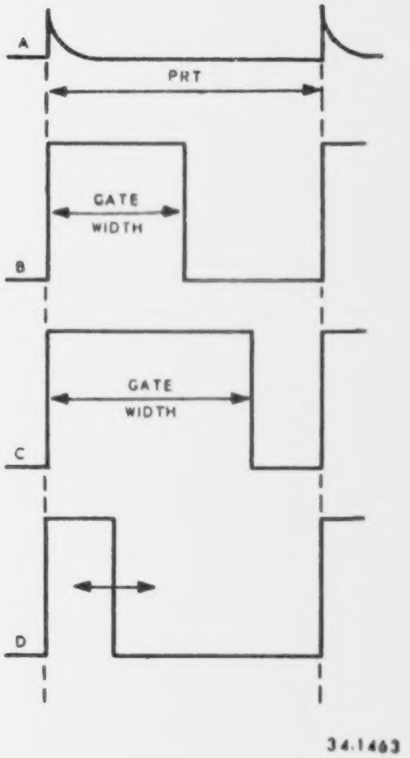


Figure 3-11. Monostable waveforms with variable gate widths.

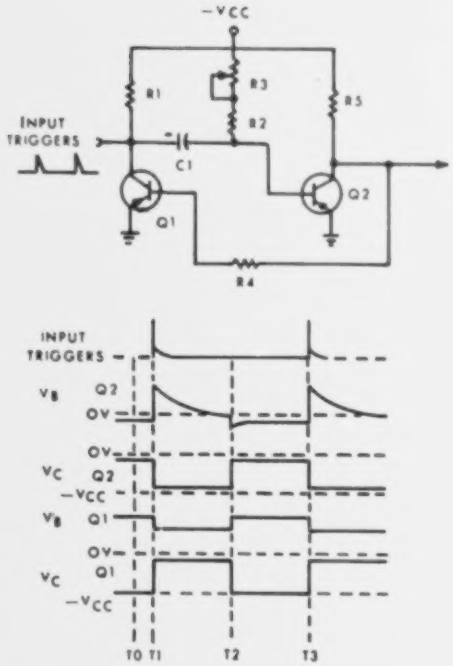


Figure 3-12. Monostable multivibrator with waveshapes.

With no input signal (quiescent condition), one amplifier conducts and the other is cut off. When an external trigger is applied, the multivibrator will change state for a period of time determined by an RC circuit, and then it will return to its stable state, where it will remain until triggered again. One trigger input causes a full-cycle output.

The monostable multivibrator is used when it is necessary to maintain a constant frequency (PRF), yet have a variable gate output (variable on and off times). This circuit is frequently used as a variable-gate generator.

Figure 3-10 shows a monostable multivibrator discrete circuit with its output waveshape. When power is applied to the circuit, Q2 will conduct, and Q1 will be cut off. Confirm this by checking the forward-bias arrangement for the transistors: The Q2 forward bias is conventional, using R2; the Q2 bias uses voltage divider network R3-R4-R5, connected between $+V_{cc}$ and $-V_{BB}$. Since the circuit uses a negative V_{BB}, it is possible for the voltage on the base of Q1 to be positive or negative with respect to the emitter (ground). When Q2 conducts, its collector voltage is near 0 volts; this causes a negative voltage on the base of Q1, holding it at cutoff. The stable condition of the circuit is Q1 cut off and Q2 conducting (T0, fig. 3-10, B).

The positive input trigger applied to the base of Q1 causes Q1 to conduct. The collector voltage of Q1 decreases to almost 0 volts, and this negative-going signal is coupled by C2 (discharging through R2) to the base of Q2, which cuts Q2 off. The collector voltage of Q2 now increases toward $+V_{cc}$. Now voltage divider R3-R4-R5 conduction results in the base of Q1 being positive with respect to its emitter. This voltage keeps Q1 conducting until C2 discharges enough to allow Q2 to conduct once again (T2, fig. 3-10, B). When Q2 conducts, its collector voltage decreases, and the base of Q1 becomes negative, resulting in Q1 being cut off. The circuit is again in its quiescent condition, and it will remain there until another trigger is applied (T3, fig. 3-10, B).

The output frequency is controlled by the input trigger frequency. Internally, the point at which the circuit returns to the stable state determines the gate width; this is controlled by the RC time constant of C2 and R2. Figure 3-11 shows the relationship between the trigger and output signal. Part A shows the input triggers; parts B and C illustrate different gate widths. Notice that, while the duration of the gate is different, the duration of the complete cycle is the same as the trigger PRT. Part D of figure 3-11 indicates that the trailing edge of the positive alternation is variable.

Another version of the monostable multivibrator is shown in figure 3-12. In its stable condition (at T0), Q1 is cut off, and Q2 is conducting. The input trigger (positive pulse at T1), applied to the collector of Q1 and coupled by C1 to the base of Q2, cuts Q2 off, and the collector voltage of Q2 will go toward $-V_{cc}$. The more negative voltage at the collector of Q2 will forward bias Q1, and collector voltage of Q1 will go to

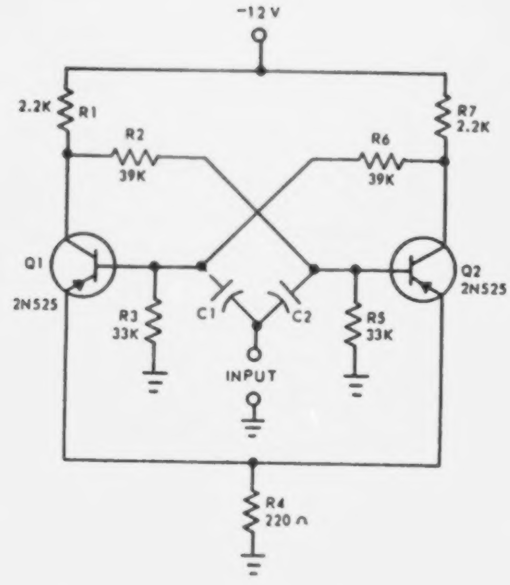


Figure 3-13. Bistable multivibrator with circuit values indicated.

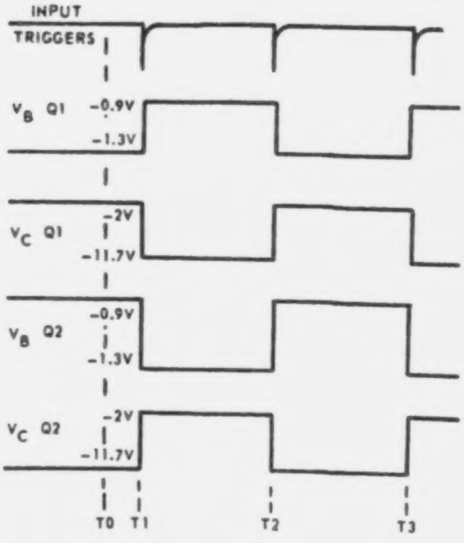


Figure 3-14. Waveshapes for figure 3-13.

about 0 volts. C1 will now discharge and keep Q2 cut off. Q2 remains cut off until C1 discharges enough to allow Q2 to conduct again (T2). When Q2 conducts again, its collector voltage will go toward 0 volts, and Q1 will be cut off. Thus, the circuit returns to its quiescent state and has completed a cycle. The circuit will remain in this stable state until the next trigger arrives (T3).

Note that R3 is variable to allow adjustment of the gate width. Increasing R3 increases the discharge time for C1. This increase increases the cutoff time for Q2. Making R3 large, therefore, widens the gate. To decrease the gate width, decrease R3.

Bistable multivibrator. The bistable circuit, as the name implies, has two stable states. If a trigger of the correct polarity and amplitude is applied, the circuit will change state and remain there until triggered again. The trigger need not have fixed PRF; in fact, triggers from different sources, occurring at different times, can be used to switch this circuit.

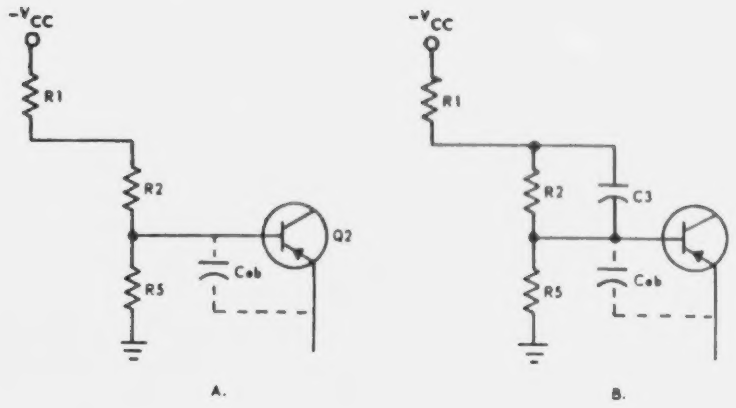
The bistable multivibrator circuit is shown in figure 3-13. In this circuit, R1 and R7 are the collector-load resistors. Voltage dividers R1-R2-R5 and R7-R6-R3 provide forward bias for Q2 and Q1; they also couple the collector signal from one transistor to the base of the collector signal from one transistor to the base of the other. Observe that this is direct coupling of the feedback. This type coupling is required because the circuit depends on input triggers for operation and not RC time constants inside the circuit. Both transistors use common-emitter resistor R4, which provides emitter coupling. C1 and C2 couple the input triggers to the transistor bases.

Notice that the circuit is nearly symmetrical, since each transistor amplifier has the same component values. When power is first applied, the voltage divider networks place a negative voltage at the bases of Q1 and Q2. Both transistors have forward bias, and both conduct.

Due to the slight difference between the two circuits, one transistor will conduct harder than the other. Assume that Q1 conducts harder than Q2. The increased conduction of Q1 causes the collector voltage of Q1 to be less negative (more voltage drop across R1). This decreases the forward bias of Q2 and decreases the conduction of Q2. When Q2 conducts less, its collector voltage goes more negative. The negative-going change at the collector of Q2 is coupled to the base of Q1 and causes Q1 to conduct still harder. This regenerative action continues until Q2 is cut off and Q1 is saturated. The circuit is then in a stable state and will remain there until a trigger is applied.

At T0, figure 3-14, current through Q1 causes a 1-volt drop across R4, which places a − 1-volt potential on the Q2 emitter. The collector of Q1 is at −2 volts, which is dropped across R2 and R5, so the base of Q2 is −0.9 volt. With its base at −0.9 volt and emitter at − 1 volt, Q2 is reverse-biased (cut off). Note that the Q2 collector is at 11.7 volts (0.3-volt drop across R7) and that the Q1 base potential is − 1.3 volts, making a 10.4-volt drop across R6 due to Q1 base-to-emitter current.

At T1, a negative trigger is applied to both bases through C1 and C2. The trigger does not affect Q1 since it is already conducting. The trigger overcomes



34-1467

Figure 3-15. High-Frequency compensation network.

cutoff bias on Q2 and causes it to conduct. As Q2 goes into conduction, its collector rises to −2 volts. The positive-going change at the Q2 collector causes reverse bias on Q1, and its collector voltage drops to −11.7 volts. The switching action causes a very rapid change of state, with Q2 now conducting and Q1 now cut off.

At T2, a negative trigger is again applied to both bases. This time, Q1 is brought into conduction, and the regenerative switching action cuts Q2 off. The bistable multivibrator will continue to change states as long as triggers are applied. Notice that two input triggers are required to produce one gate; one to turn it on, and the other to turn it off. The input trigger frequency is twice the output frequency.

The transient interval (the time it takes the transistor to go from cut off to saturation or vice-versa) is limited by the interelement capacitance between the base and emitter (C_{eb}). The switching action can be no faster than the time required to charge the interelement capacitance. This leads to rounded corners of the waveforms. It also represents loss of the high-frequency components of the square or rectangular waves.

In figure 3-15, the base circuit of Q2 (fig. 3-13) is redrawn. The base voltage on Q2 can change only at the rate that C_{eb} charges. To charge C_{eb}, current must flow through R1 and R2. This sets up an RC time constant. The load resistor is relatively small (2.2K), and C_{eb} is relatively small (a few picofarads). But R2 is large (39K, fig. 3-13), which makes the time constant long enough to cause rounding of the corners. This is referred to as "high-frequency loss."

To allow the interelement capacitance to change faster, the opposition in its charge path must be reduced. A method commonly used is to bypass R2 with a capacitor. Figure 3-15, B, shows C3 connected across R2. C3 is a low impedance to the high-frequency component of the square wave. C3 effectively removes R2 from the circuit during a fast change, and it allows C_{eb} to charge faster, reducing the rounded corners of the output waveshop.

Exercises (014):

1. Place the letter corresponding to the correct choice in column B in front of the appropriate term in column A. Items in column B may be used more than once.

Column A

___ (1) Bistable multivibrator.
___ (2) Astable multivibrator.
___ (3) Monostable multivibrator.
___ (4) Steady state.

Column B

a. Exists when circuit operation is essentially constant.
b. Has no stable state.
c. Has one stable state with one transistor conducting and the other cut off.
d. Has two stable states. It remains in one of the stable states until a trigger is applied; then it goes to the other stable condition to remain there until another trigger is applied to change it back to its first stable state.
e. Also known as free-running multivibrator.
f. Primary factors affecting PRF and PRT of the circuit are the coupling components.
g. Output frequency is controlled by the input trigger frequency.
h. Will continue to change states as long as triggers are applied.
i. Circuit is frequently used as a variable gate generator.
j Requires two input triggers to produce one cycle in the output.

3-2. Troubleshooting Multivibrator Circuits

Like previous systems studied, a multivibrator system will produce specific symptoms that will lead the technician to a faulty component. The following is a discussion of some common failures of transistor multivibrators.

015. Analyze schematics of a multivibrator with hypothetical malfunctions to determine the possible causes of the malfunctions.

Troubleshooting a multivibrator is relatively simple as long as you remember the operation of each one of the different types of multivibrators. Here is a brief review of each type.

The astable multivibrator is a free-running square or rectangular-wave generator that has no stable condition. It consists of two RC-coupled amplifiers with 100-percent regenerative feedback. The PRF, PRT, and gate width are controlled internally by RC networks.

The monostable multivibrator or one-shot, is a square- or rectangular-wave generator with one stable condition. The PRF and PRT are controlled by input triggers, and the gate width is controlled internally by an RC network. One input trigger initiates an output cycle so that trigger frequency equals output frequency.

The bistable multivibrator is a square or rectangular-wave generator with two stable conditions. The PRF, PRT, and gate width are controlled by the input triggers. Two triggers are required to produce one cycle in the output.

Exercises (015):

1. Refer to figure 3-9. Assume that normal operation is free-running, with a square-wave output obtained from the collector of Q2. *Symptom:* The negative alternation of the output is longer than normal. What could cause this particular condition?

2. Refer to figure 3-9. Assume normal operation is free-running with a square-wave output obtained from the collector of Q2. *Symptom:* V_{cc} on Q2 is high, and V_{cc} on Q1 is very low. This indicates Q1 is saturated. What could cause this particular condition?

3. Refer to figure 3-13. *Symptom:* Positive triggers at the collector of Q1, and negative triggers at the frequency of the input triggers at the collector of Q2. What could cause this particular condition?

4. Refer to figure 3-13. *Symptom:* Q1 collector to ground measures 0 volts. Positive-going triggers at the collector of Q2. What could cause this particular condition?

CHAPTER 4

Timing Circuits

IN ADDITION TO THE OSCILLATORS AND MULTIVIBRATORS used to develop basic timing frequencies for electronic equipment, other timing circuits are needed. These circuits convert the source frequency to the timing signals needed to accomplish all functions within a unit. By using an accurate, stable source frequency to generate additional timing signals, synchronization of circuit functions is accomplished.

4-1. The Regenerative Frequency Divider

The circuits that develop the basic timing frequency for electronic computer and switching systems have been discussed. As you know, our equipment needs many timing frequencies to accomplish its functions. All of these timing signals must be synchronized one with the other.

016. State the general operating principles of the regenerative frequency divider.

Rather than develop separate timing signals that must be synchronized together, computer and switching equipment develop a master timing signal and feed it to other circuits that will develop multiples or sub-multiples of it. The regenerative frequency divider is one such circuit. Figure 4-1 is an example of this type of circuit. The heart of this circuit consists of a mixer stage (Q2) and a frequency multiplier (Q3). The tank circuit in the mixer collector is tuned to frequency f/x (where x = any whole number, in this case a 4) and begins to oscillate at this frequency upon the application of the input f. It does not continue to oscillate, since the input does not support it. The output f/x is, therefore, fed to a frequency multiplier that is tuned to f (x − 1). We can convert this formula to 3f for our use.

Before going any further with this type of analysis, let us put some practical figures to work. A timing frequency of 2,400 Hz (f) is available but an 1,800-Hz signal is also needed. 1,800 is equal to 3/4 of 2,400.

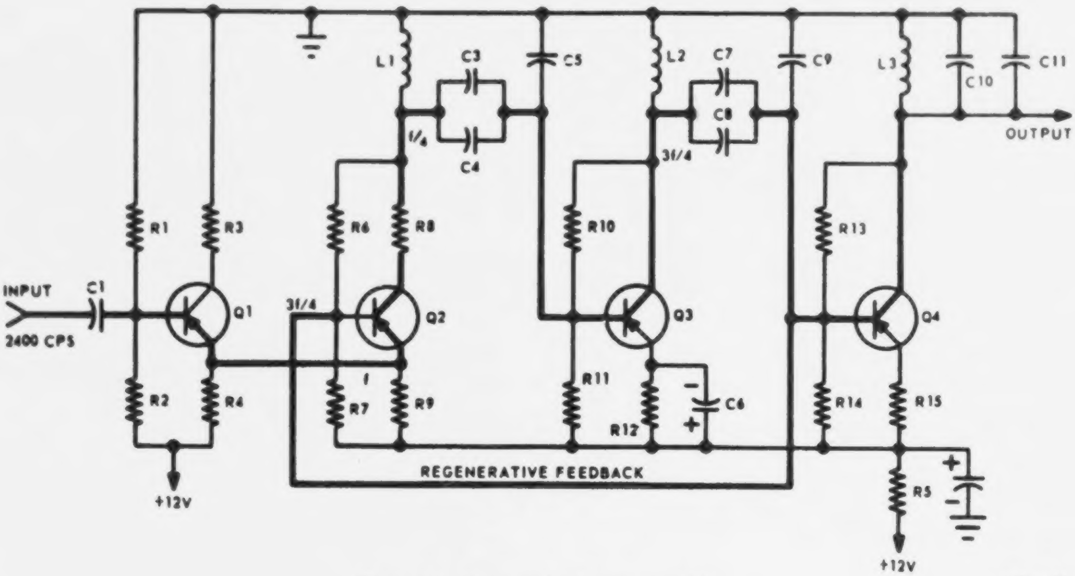


Figure 4-1. Regenerative frequency divider.

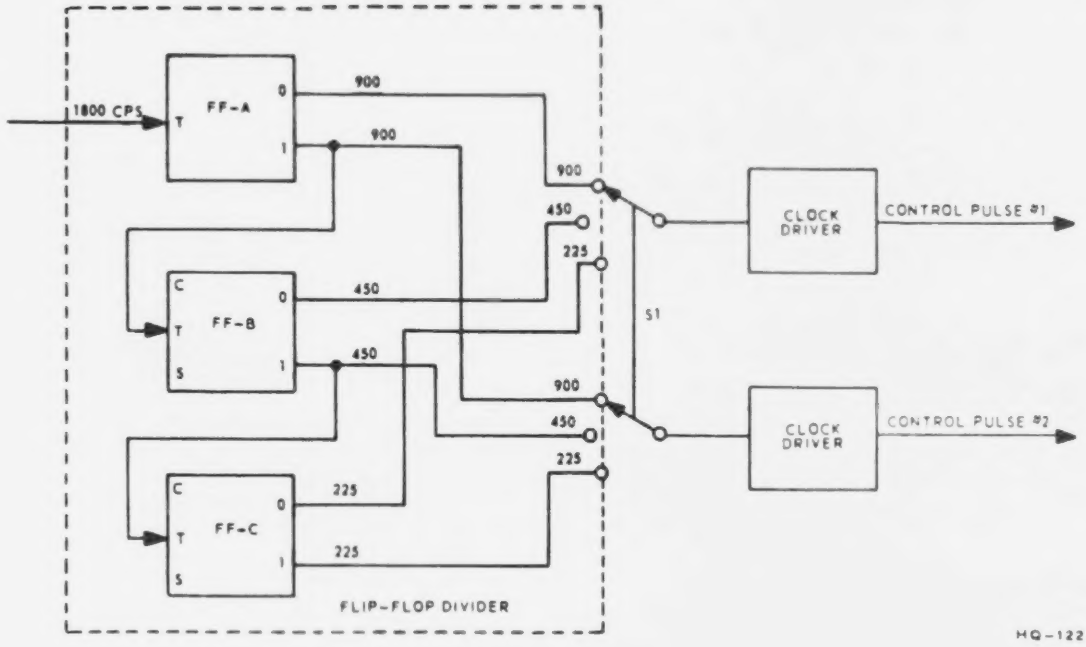


Figure 4-2. Clock-Pulse circuit.

To develop 1,800, first you must divide 2,400 by 4 then multiply the result by 3:

$$\frac{2,400}{4} \times 3 = 1,800 = \frac{f(x-1)}{x}$$

Now apply this 2,400-Hz signal to the mixer and tune its collector to 600 (2,400 ÷ 4). The 600 is then fed to multiplier Q3, which is tuned to 1,800 (600 × 3). This results in the desired frequency but, without some way of maintaining the 600-Hz mixer output, it would only last momentarily. The 1,800 Hz is, therefore, fed back to the mixer as a second input. The mixer is already tuned to the difference (2,400 − 1,800 = 600) and a stable 600 Hz is maintained. Q4 in the circuit amplifies and distributes the output. Q1 matches the input impedance to the impedance of the mixer.

Exercises (016):

1. What is the purpose of the regenerative frequency divider?

2. With an input frequency of 3,000 Hz and x = 5, what is the output of the divider?

3. What does Q2, the mixer stage, actually mix?

4-2. Flip-Flop Dividers

A very common method of developing different timing pulses from a basic clock pulse is the use of the bistable multivibrator or flip-flop. A flip-flop designed for frequency division will divide its input by 2. By using a series of flip-flops an input frequency can be divided into any number of output frequencies.

Integrated circuit dividers are also available which can be wired to divide an input into a number of different frequencies. For example, the SN7490 decade divider can be set to divide by 2, 5, or 10.

017. Cite the operating characteristics of two types of flip-flop dividers.

The flip-flop is a device that can be readily adapted for use as a frequency divider. It is usually limited to division in the lower range of frequencies due to the time lag occuring through a series of flip-flops. The conventional flip-flop can be designed to be triggered on either the positive-going (upclock) or negative-going (downclock) portion of an input signal. If a sine wave, a square wave, or a pulsed input is applied, the flip-flop changes state each time the input signal goes in the required direction. It must change state twice to produce one cycle of output and, thus, to provide a division factor of two. A series of flip-flops arranged like a counter provides division in multiples of two.

The clock-pulse circuit of figure 4-2 is an example of a circuit using a flip-flop divider. Flip-flop A provides for a division by two; flip-flop A and flip-flop B combined provide for division by four; and flip-flops A, B, and C provide for division by eight. Using

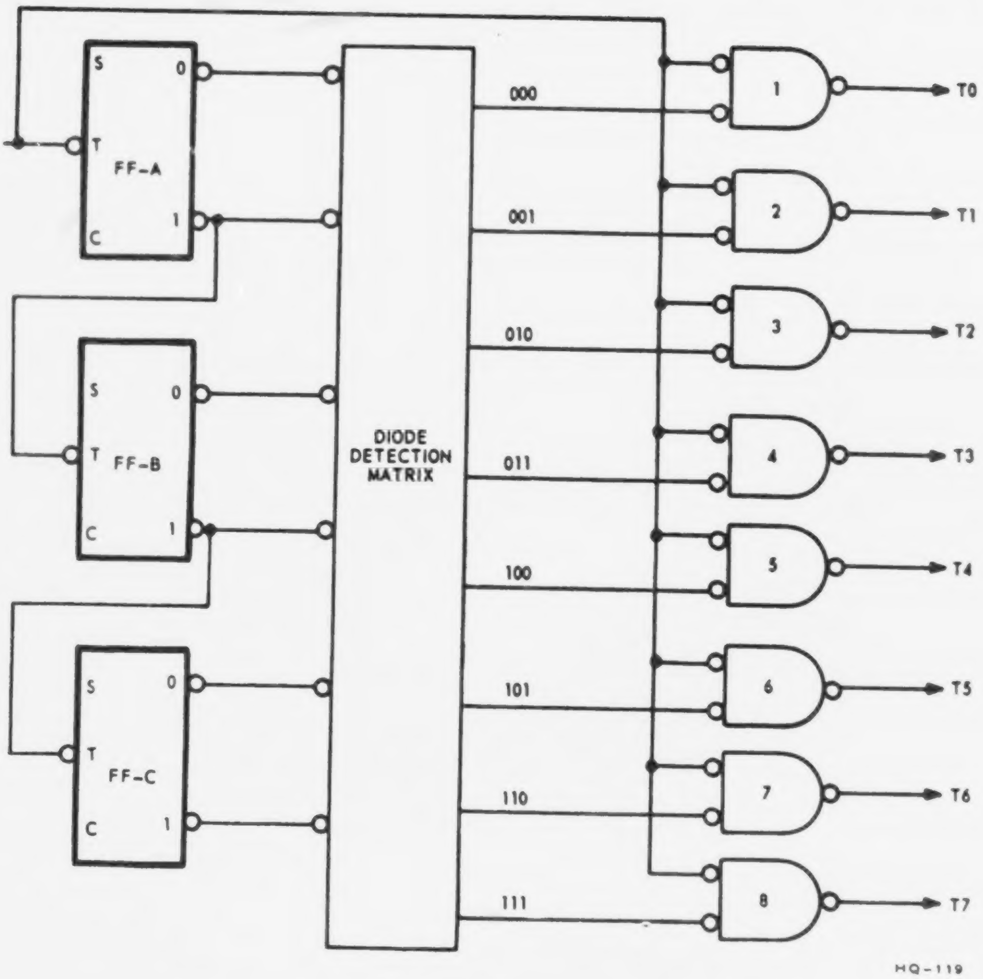


Figure 4-3. Time-Pulse generator.

selector switch S1, any one of the three frequencies can be individually selected or all can be used, if desired, to control separate circuits. Notice that selection switch S1 is a three-positioned switch and can be set to only one frequency at a time.

If successive operations require groups of timing pulses, the flip-flop divider may also be used. One such case is a system that requires successive groups of eight timing pulses that are to be used in the assembly of a digital message. In this system, the basic timing pulses are fed as the input to a three-stage binary counter. The ONE and ZERO outputs of the counter are then fed to a diode count detection matrix. This particular arrangement is shown in figure 4-3. As the counter progresses through its counting from 000 to 111, each particular count is detected and fed to a control gate as a conditioning level. The original input timing pulses are also fed to the control gates. When a count of 000 is detected, AND-gate 1 is conditioned and passes the negative half of the timing pulse to input as TO pulse. AND-gate 2 passes the timing pulse when the count 001 is detected, and this pulse becomes T1. This process continues until the T7 pulse is generated as the count of 111. The next input resets the counter and another series of pulses is begun.

Exercises (017):

1. In figure 4-2, how many output frequencies may be used at one time?

2. What is the total division factor for a three-stage flip-flop divider?

3. In figure 4-3, if all flip-flops are reset, how many trigger inputs to each of the three flip-flops are necessary to form T5?

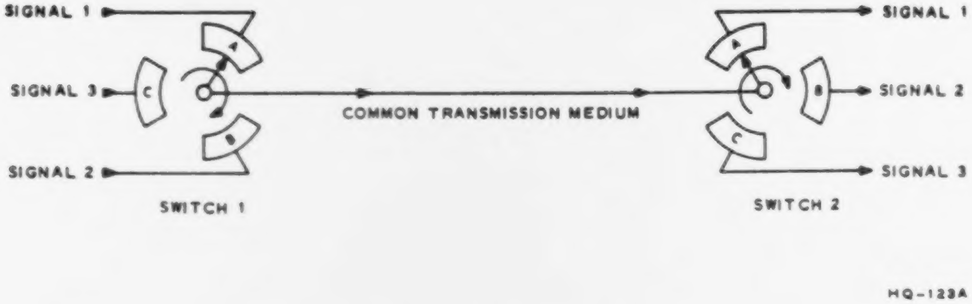


Figure 4-4. Signal switching.

4-3. Time-Division Multiplexing (TDM)

How many telephone conversations can be transmitted at the same time over one line? Depending on the system design, many conversations could be taking place through the use of time-division multiplexing.

018. State how a time-division multiplexing system works and specify the technique of signal sampling.

TDM Theory. A time-division multiplexing system combines the signals for transmission over the common transmission medium by alternately connecting each voice-band signal source to the transmission medium for a short period of time.

Figure 4-4 shows each end of the transmission medium connected to a rotary switch. As switch 1 passes contact A, signal 1 can pass to switch 2. Switch 2 operates in synchronization with switch 1 and passes the signal through the A contact to the signal reproducing equipment. When switches 1 and 2 advance to the B position, the B circuit is completed and the A circuit is broken. The switch then advances through the C position and returns to the A position. In this manner, each circuit has exclusive use of the transmission medium for a small period of time (time division). Each time the switch contacts are closed, only a portion or sample of the signal is allowed to pass. All signals share the same transmission medium, with each signal being transmitted for a portion of the total time required for the switches to complete a full revolution.

As you can see, any system using time-division multiplexing transmits only a portion of the original signal information. The human ear, like the human eye, does not require the continuous presence of information because of the illusion of continuity. When these samples or bits of information arrive often enough, the sound can be made to appear as if the

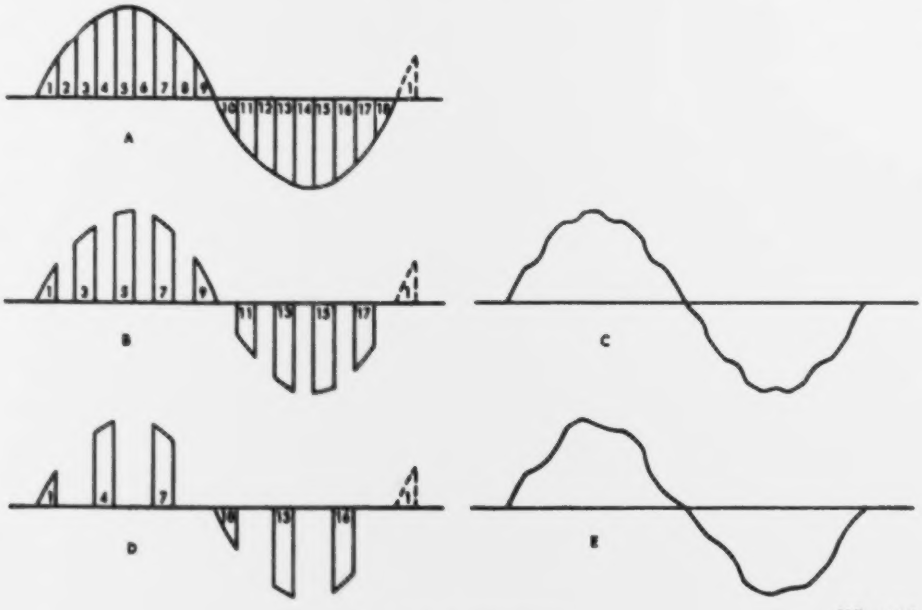


Figure 4-5. Signal samples.

transmission path is unbroken. As shown in figure 4-5, A, one cycle of a voice-band signal can be divided into a series of pulses or samples. If we remove all of the even-numbered pulses, as in figure 4-5, B, the remaining pulses still retain the basic shape of the original sine wave. If these remaining off-numbered pulses are then passed through an LC circuit, the inductance and capacitance action of such a circuit reconstructs a waveform like that in figure 4-5, C. This waveform is very nearly the same as the original waveform in figure 4-5, A. When every third pulse is being transmitted, as in figure 4-5, D, and the pulses pass through an LC circuit, the resultant is as shown in figure 4-5, E. Again, this waveform is almost the same as the original waveform.

Figure 4-5 could be expanded further to indicate all of the possible waveforms that would occur due to the selection of different samples of the sine wave. The extent to which we can carry this limiting of transmitted information is determined by two factors. First, the signal transmitted must have a frequency (or repetition rate) accurately reproduced if satisfactory reception is to occur. Second, the amplitude ratio within the signal must be retained if the received signal is to have quality. If a system could be designed that would guarantee that sample 5 and sample 14 would always be transmitted, such a system would insure that the proper frequency would be reconstructed at the receiving station. An arrangement such as this could be obtained from a system that would be transmitting and receiving single tones of definite frequencies. The received samples could be applied to high-Q tuned filters, which would accurately reproduce the original signal. If a voice-band signal is to be transmitted and received via the time-division multiplexing system, the problem becomes infinitely more difficult due to the complex waveform. Experiments with time-division multiplexing have shown that the highest frequency in a voice-band signal must be sampled at least three times each cycle if quality reproduction is to occur in the receiver.

Sine Wave Amplitude Sampling. A sine wave also has amplitude which must be reproduced by the receiver. Amplitude itself is an easy characteristic to reproduce because it can be obtained from any conventional amplifier stage. Amplitude ratio within a signal (an important factor to be considered when limiting information) is maintained by using a sample rate that is at least three times the highest frequency. This sampling rate insures that consecutive samples or bits of information are not taken from the same portion of each successive cycle. A proper sampling rate is illustrated in figure 4-6.

In figure 4-6, cycles 1, 2, and 3, although drawn above each other, can be considered as occurring in sequence. Note how the position of the samples change. If this figure were continued for several additional cycles, a complete waveform would eventually be transmitted, as shown by the cumulative effect waveform. Transmission of the entire waveform is not necessary, due to the LC effect previously mentioned. This shifting of the position of the sample insures that the reconstructed wave has an average amplitude characteristic that is similar to that in the original waveform.

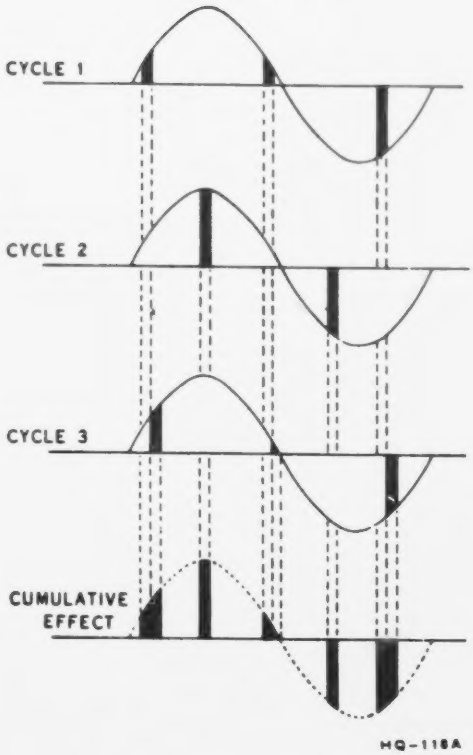


Figure 4-6. Samples, adding effect.

Distortion in the amplitude of the reproduced signal, such as that shown in figure 4-5, E, is amplified in any audio amplifier. Thus, you would think that the signal reproduced in the telephone would be distorted in amplitude. Such distortion would not normally be heard, however, if the original signal were sampled at a rate three times that of the highest frequency within the signal, due to the design characteristics of the telephone reproduction apparatus. Such distortions in amplitude are smoothed over in the telephone receiver by the movement of the diaphragm which, due to mechanical limitation, cannot follow or reproduce all of the small changes in amplitude. Consequently, the problem of distortion from amplitude changes due to multiplexing action is very small.

The discussion thus far has been concerned with the sampling of a theoretical sine wave and the reconstruction of this sine wave in the receiver. Each cycle must be sampled at least three times if it is to be accurately reconstructed at the receiver. The rate of sampling must then be equal to the highest frequency sampled multiplied by the sampling rate per cycle. If you multiply 4000 Hz (the highest frequency in the voice-band signal) by 3, you find that the minimum

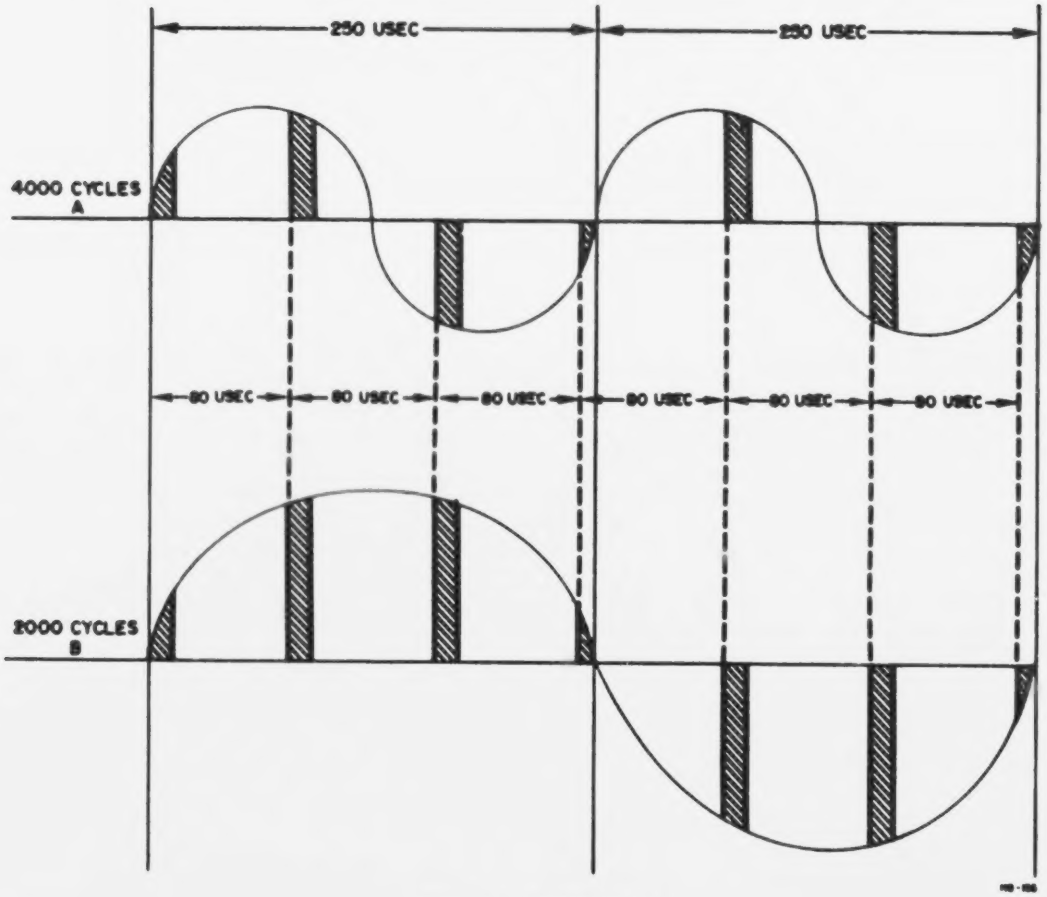


Figure 4-7. Samples, 80 μs.

sampling rate is equal to 12,000 (12 kHz) times per second. Since the clock frequency in the AN/TTC-30, Telephone Switching Center, is 250 kHz, the nearest to the 12 kHz that this frequency (250 kHz) could be divided easily was 12.5 kHz (20 to 1 ratio). The 12.5 kHz is used throughout the AN/TTC-30. If a specific voice-band channel is to be sampled 12,500 times per second, adjacent samples within this channel occur each 80 μsec because 1 second divided by 12,500 equals 80 μs. Figure 4-7, B, shows one cycle of a 2,000-Hz voice-band signal, which is also sampled each 80 μs. The leading edge (left edge) of the adjacent pulse in either A or B is separated by 80 μs. In this example, note that the 2,000-Hz wave has twice as many samples per cycle as the 4000-Hz wave. The separation between adjacent pulses in either waveform is 80 μs. The additional pulses in the lower frequency wave insure that this wave is accurately reconstructed in the receiver.

A definite sampling rate for a specific frequency has been established. Therefore, if the leading edges of the adjacent samples in any voice-band channel are separated by 80 μs, we have a period of time when no intelligence is being transmitted. This unused period of time may be used to transmit samples from other voice-band channels. You now need to determine the number of pulses or signals that can be transmitted during this 80 μs period before the first signal must be sampled again.

Exercises (018):

1. Briefly, explain how a time-division multiplexing system works.

2. What factor determines the minimum sampling rate for a voice-band signal?

3. What is the minimum sampling rate of a voice-band signal?

4. How are distortions in pulse amplitude smoothed over in the telephone receiver?

5. What is the minimum sampling rate for the highest frequency in the voice-band signal?

019. State the purpose of considering certain areas when pulse sampling.

Reference Level. Each of the pulse samples shown in figures 4-5, 4-6, and 4-7 are pictured as having a definite width. This pulse width limits the number of pulses that may be placed within the 80 μs sampling period. Theoretically, any sample of the waveform amplitude could be a point or a dot, as in figure 4-8, A. To sample the relative amplitude of the waveform at any given point, you must first establish a known reference level. This reference level can be a DC level, as in figure 4-8, B. Figure 4-8, C, shows the sine wave superimposed on the DC reference level. All of the samples now have a common reference level and always rise in the same direction (positive) instead of rising in both positive and negative directions, as shown in figures 4-5, 4-6, and 4-7. This use of a common reference level eliminates the need of the receiver to determine whether a specific pulse sample occurred during the positive or during a negative portion of the sine wave. The use of a specific reference level produces pulses that are all of the same polarity. The amplitude of these pulses is such that the pulses trace out the relative amplitude of the original sine wave, as shown in figure 4-8.

Noise-Pulse Factor. Before you can definitely determine the number of pulses that can be placed within a specific time interval, you must consider the noise/pulse width ratio. Figure 4-9 shows two pulses that are amplitude samples of a specific wave. Pulse A is 0.5 μs wide, and pulse B is 2.0 μs wide. Superimposed on each pulse is a 0.1-μs pulse of noise. This noise distorts B only 5 percent of its time due to the increased pulse width. Pulses that convey intelligence by changes in amplitude are subject to noise interference. The effects of amplitude distortion increase as the pulse width is decreased.

Guard Band. Pulses cannot be placed adjacent to each other without a guard band because they merge, and the result is one pulse which has an amplitude that is the average value of both pulses. Without a guard band, the pulses lose their identity; and the receiver is unable to distinguish between pulses originating in different channels. Such a guard band is usually equal to the width of the pulse; yet, if exceptionally high engineering standards are maintained, this guard band may be decreased to a time equal to one-fifth of the total pulse width.

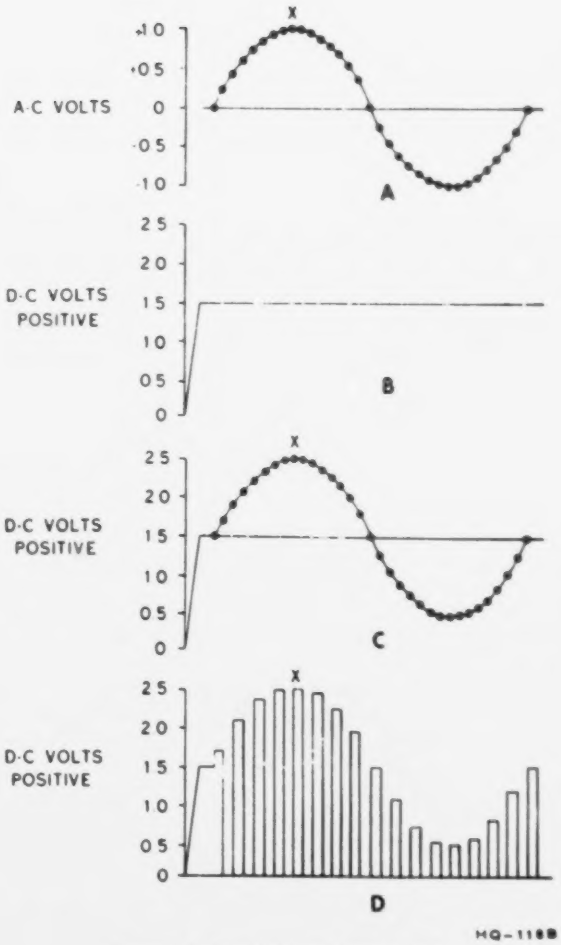


Figure 4-8. Establishing reference level.

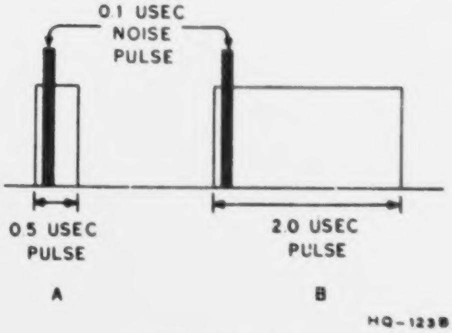


Figure 4-9. Noise/Time.

Exercises (019):

1. Why is it necessary to establish a DC reference level for an AC signal?

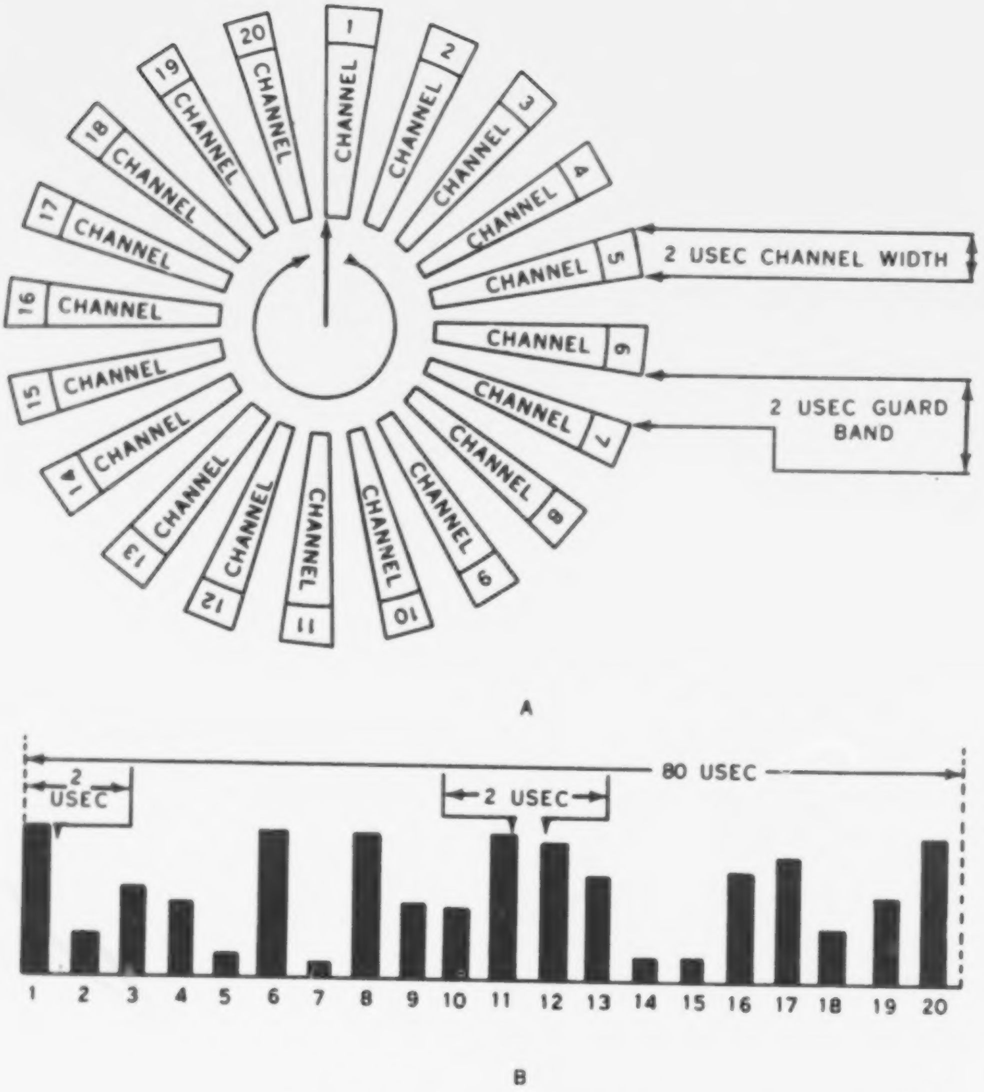

CHANNEL 1
CHANNEL 2
CHANNEL 3
CHANNEL 4
CHANNEL 5
CHANNEL 6
CHANNEL 7
CHANNEL 8
CHANNEL 9
CHANNEL 10
CHANNEL 11
CHANNEL 12
CHANNEL 13
CHANNEL 14
CHANNEL 15
CHANNEL 16
CHANNEL 17
CHANNEL 18
CHANNEL 19
CHANNEL 20
2 USEC CHANNEL WIDTH
2 USEC GUARD BAND
A
80 USEC
2 USEC
2 USEC
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
B
HQ-121

Figure 4-10. Pulse amplitude modulation.

2. What must be considered when determining how many pulses may be placed within a specific time interval?

3. Why must a guard band be used?

020. State techniques used in transmitting pulse samples.

Pulse Amplitude Modulation (PAM). Thus far, the primary concern has been with the techniques of sampling and the basic factors affecting pulse width. The technique that is used to transmit the amplitude variations in the pulse samples also determines, to a certain degree, the number of channels that may be transmitted during a definite time period. Six such techniques for the transmission of pulsed information have been developed. The four most commonly used techniques are pulse amplitude modulation (PAM), pulse-duration modulation (PDM), pulse-position modulation (PPM), and pulse-code modulation (PCM). The other two techniques, delta modulation and random pulses, are not in general use. Of the four sampling techniques mentioned, the primary concern at this time is PAM. In this system, the signal is periodically sampled; and a pulse is obtained whose height (amplitude) is proportional to the amplitude of

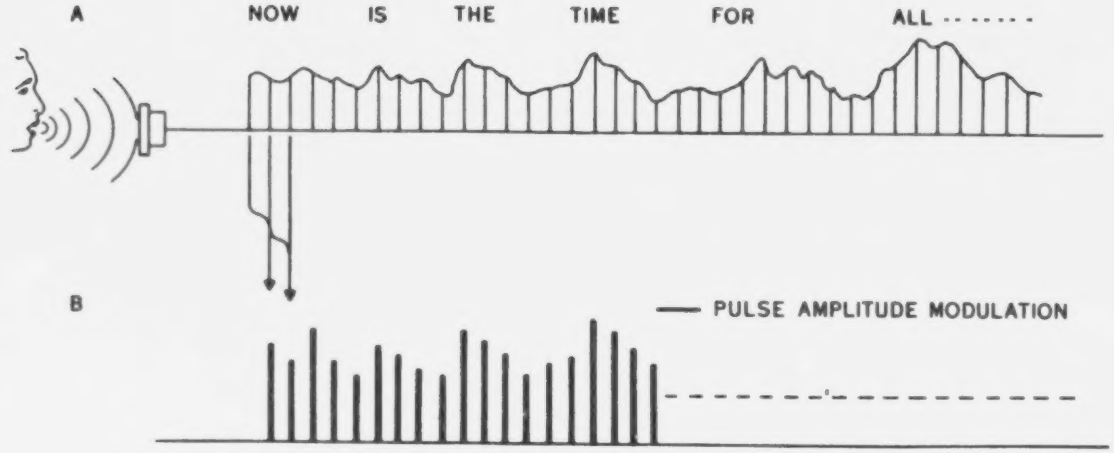


Figure 4-11. Principles of PAM.

the signal at the instant of sampling, as previously discussed. The requirement of pulse polarity identification is eliminated by superimposing the signal to be sampled on DC reference voltage, as shown in figure 4-8. When such a signal is sampled, all samples are of the same polarity, although the amplitude of any individual sample is determined by the instantaneous amplitude of the sine wave.

Using 2 μs as the base width of the intelligence pulses, you can divide 80 μs (minimum sample repetition rate) by 2 and obtain what appears to be 40 units of time for pulse transmission. However, a guard band of time is provided between each pulse; and with the guard band being equal to the time of one pulse, there will be 20 units of 2 μs of intelligence and 20 units of guard band time.

The channeling and multiplexing action of a typical 20-channel PAM time-division multiplexing system is shown in figure 4-10. The channels, each of which provides a 2-μs pulse of information, have been arranged in a circle to illustrate the repetition factor. As the arm of the rotary switch passes a contact, a 2-μs information pulse is obtained. The arm then passes through a 2-μs time of no contact time, which provides a 2-μs guard band between adjacent pulses. The arm returns to channel 1 every 80 μs and the sampling sequence is repeated. A typical group of 20 pulses is shown in figure 4-10.

In addition to all of the sampling and the modulation techniques necessary for PAM, one other consideration is pulse identification in the receiver. Not only must the message be properly reconstructed by the receiver, but it must also be correctly routed. In order to identify the pulses (to identify which is channel 1, 2, 3, etc.), some form of coding or synchronization must be included to send each pulse to its proper destination. This synchronization may be accomplished by modulating channel 1 with a special pulse to the composite group as a marking pulse to identify the start of each pulse group.

Figure 4-10 indicates the use of a rotary switch to obtain a sample of the information available in a channel when the switch is in any specific position. Such a switch would have to rotate at a speed of 750,000 revolutions per minute because it must connect to a specific channel 12,500 times per second. This is a fantastic speed for any mechanical rotary device. Consequently, you find such switching action is done electronically instead of mechanically. To further explain PAM, the following paragraphs describe its use as applied to the AN/TTC-30 ESC.

As the contact memory of the AN/TTC-30 ESC is scanned, stored information is sent to sensing circuits which are guided in turning on or off equipment unit connections so that each line calling or being called sends or receives information at 12.5-kHz rate. Thus, each line sends or receives a 2-μs burst of signal energy during a 4-μs portion of every 80-μs scanning period, or 12,500 bursts per second. Although the sampling of information transmitted takes place at the 12.5-kHz rate, the duration of each pulse sample is so short that the power applied, for example to a telephone receiver, is too small to cause audible reproduction. Since all samples are not taken at points of peak signal amplitude, the average amplitude of the samples is less than that of the complete transmission signal. Therefore, a lowering of the amplitude of the received signal is another reason for the lack of audible reproductions.

The power (energy) in a speech signal is affected by both the amplitude and the duration of the signal, as shown in figure 4-11. Since a 4-μs pulse is only a fraction of the entire 80 μs signal duration, the maximum power of the pulse is only a fraction of the entire signal power. Because of this, when such pulses are applied directly to a telephone receiver, they are not heard. To remedy this, each line circuit includes a low-pass filter to smooth out each pulse, thus filling in the gaps between pulses. This filter is a type that releases energy slowly so that one pulse runs into the

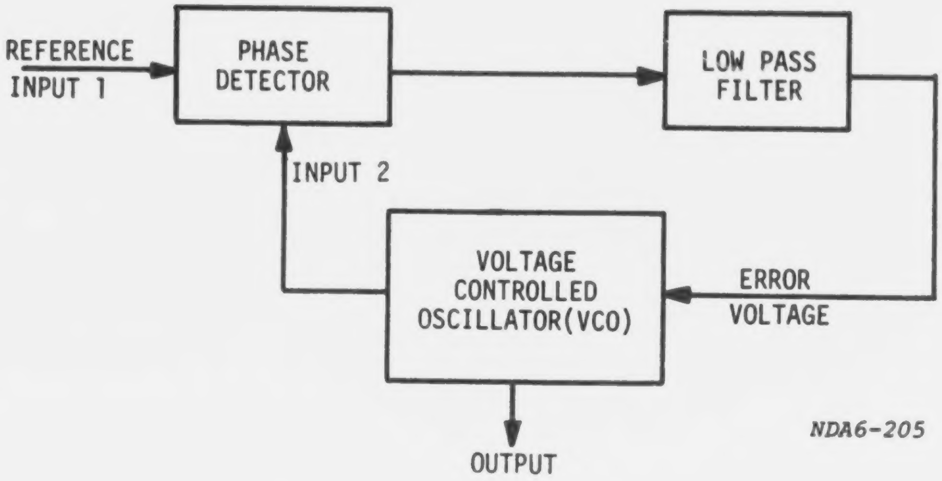


Figure 4-12. Block diagram of basic PLL circuit.

next, resulting in a waveform resembling that of the original, except that its amplitude is somewhat less. The low-pass filter also tends to block any interference.

During the first portion of each of the 4-μs pulse periods, the entire highway (the term now used for transmission medium) is grounded to insure that one conversation time slot does not actually overlap into another. Thus, any conversation or part of a pulse that is still on a highway drains off to ground. As a result, each pulse position starts at a zero energy level. This grounding of a highway "between" pulses is called highway clamping (guard band or highway discharge).

An efficient transfer of energy is possible while using pulse amplitude modulation by directing the speech signal into a capacitor during the interval between samples and then discharging the capacitor through a resonant circuit. Assuming that the components forming the resonant circuit are perfect and the circuit contains no resistance, the transfer of energy takes place without loss.

Exercises (020):

1. What is the technique called which is used to transmit amplitude variations?

2. How is the requirement of pulse polarity identification eliminated in a PAM system?

3. Using a 20-channel voice-band, how many times will each channel be sampled in 80 μs?

4. What is meant by highway clamping?

5. What is the purpose of the low-pass filter?

6. What type of circuit is used to connect a highway to provide an efficient transfer of energy?

4-4. The Phase-Lock Loop (PLL)

The phase-lock loop principle and the technology have been availabe for over 40 years. The inherent cost in implementing the technique limited its use until recently. The original PLL circuit required a multitude of components, and adjustment was very critical. Integrated circuit technology came to the rescue of the PLL by providing a cheap, easy way of using the PLL circuit.

The PLL has many uses in both analog and digital circuits. The digital technician will see this technique used in double-density magnetic disk units and digital data circuits. In examining this invaluable circuit technique, we need to know what a PLL is, the basic parts of the circuit, its origin, and how the PLL is put to use.

021: State the basic function of the phase-lock loop circuit.

PLL Origin. H. de Bellescize first described the PLL principle in 1932. The PLL circuit was used in conjunction with a synchronous radio receiver being developed at that time. The receiver used a mixer with an incoming radio signal as one input and a second input, equal in frequency, from an oscillator. The modulation from the radio signal was the only output from the mixer IF the inputs to the mixer were equal in frequency. The difficulty was in keeping the oscillator from changing frequency due to time, temperature, and vibration. The PLL circuit was designed to correct for errors in frequency and phase produced by the oscillator. This was done by using a phase detector to detect phase/frequency differences between the two inputs. When the two inputs were not the same, the phase detector produced an error/feedback voltage which was used to put the oscillator back on frequency.

One of the first major uses of the PLL principle was in synchronizing the vertical and horizontal oscillators in television sets in order to produce a stable display. As the circuit has evolved in recent years to microelectronic form, the ability to use a PLL has increased dramatically for a great many applications.

The PLL Defined. The phase lock loop is an electronic servo or automatic control system. It's a closed loop requiring the use of feedback to chase and control an input signal. The PLL automatically corrects for timing errors by using electronic feedback. The loop consists of a phase detector which is used to compare two *related* inputs and produce an error voltage. Secondly, a low-pass filter (LPF) is used to smooth the error voltage and produce the DC correction voltage for the oscillator. Last, but not least, is the voltage controlled oscillator (VCO). As its name implies, the VCO's frequency is controlled by the error voltage. The output from the PLL can be taken from the detector or the VCO, depending on the application. A block diagram of the basic PLL circuit is shown in Figure 4-12.

Exercises (021):

1. What is the purpose of the PLL circuit?

2. Name the basic part of a PLL.

3. What is an important characteristic of the two input signals to the phase detector?

022. Name the three basic parts of the PLL circuit and state the function of each.

Basic PLL Components. The three main parts of a PLL circuit, as mentioned briefly earlier, are the phase detector, the low-pass filter, and voltage-controlled oscillator. The original design used many components in order to make up these parts. The complexity of the circuit and the cost of parts were two of the PLL's drawbacks to begin with. With the advent of the integrated circuit these problems were reduced. Therefore, most PLLs you see in circuits today are in IC form.

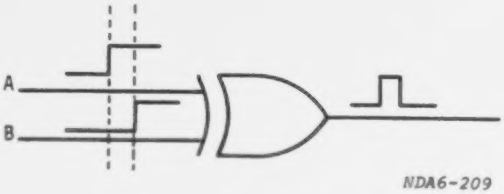


Figure 4-13. Exclusive-OR phase detector.

The phase detector (PD). Phase detectors are simple to build using an IC chip or discrete components. Various types of logic circuits can be used as phase detectors. Two of the more common circuits used are the exclusive OR gate and the D flip-flop.

An example of the exclusive OR phase detector is shown in figure 4-13 with its associated waveforms. Suppose that here we want to check and see if two waveforms are equal in phase. Due to the characteristics of an exclusive OR, we have an output only when the inputs are different. With inputs A and B out of phase, we develop an output from the phase detector which we will use to produce an error signal. One of our original inputs (A or B) was taken from the VCO, so now we'll use the error voltage developed to correct the VCO output to obtain "phase-lock." Next, we need to process the output of the detector in such a way as to provide us with a DC voltage for oscillator correction.

The low-pass filter (LPF). This part of the PLL performs the filtering or smoothing function for the detector output. The LPF is illustrated simply in figure 4-14. The capacitor eliminates the high frequency component from the detector waveform and provides a DC level of voltage. The error voltage produced is usually in the range of 2-5 volts DC. Some DC voltage level will always be present at the output of the LPF in order to maintain a control over the VCO. Depending on the amount of phase lead or lag at the detector, the error voltage will vary about the reference or quiescent level. A change in error voltage above or below the reference will shift the VCO up or down in frequency to maintain phase-lock.

The Voltage-controlled oscillator (VCO). The VCO is the third major component of the basic PLL circuit. The VCO can be implemented in the PLL using individual components for the discrete circuit or with ICs dedicated to the VCO function. The IC forms available usually require the addition of an external capacitor to set the frequency for the VCO. External adjustment by means of a potentiometer is also possible. The combination of resistance, capacitance, and DC voltage level present at the VCO determines the final frequency of operation. VCOs in discrete

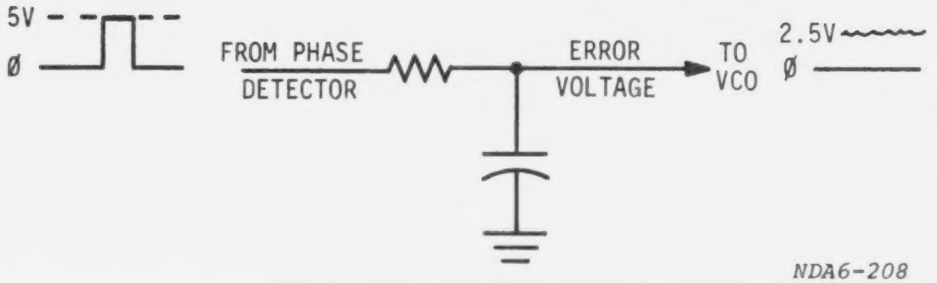


Figure 4-14. Low-pass filter circuit.

form are used extensively in analog circuits and may use a quartz crystal for more stable operation.

Voltage control of the oscillator may be accomplished by applying the LPF error voltage to a pin of the IC, or it may be necessary to use a varactor diode as the frequency determining element. The varactor diode is used as a varying capacitance to set or change the frequency of the VCO. Its capacitance can be varied as its reverse bias is changed; therefore, we can use the error voltage from the LPF as the varactor's reverse bias supply. All components of the PLL must work together to accomplish its primary function, that of precise control.

The phase comparator, low-pass filter, and voltage-controlled oscillator comprise the major components of the PLL. Understanding the function of each is necessary to see the relationship between them in the loop. If any part of the loop fails to function, we no longer have PLL operation. Because of this, troubleshooting a PLL can be difficult. Therefore, being able to logically analyze each part of the loop for correct operation is necessary.

PLL Characteristics. There are two basic characteristics of the loop which need to be mentioned briefly. These are the *capture range* and the *lock range* capabilities. When the inputs to the phase detector are not related or close in phase/frequency relationship, phase-lock will not occur. As soon as the input signals are close enough in phase, the loop will *start* to lockup—we have now entered the capture range. Once the loop has phase-locked, it will go into the lock range. If we lose lock because of no signals, then the capture process must start again. The lock range is always greater than the capture range, but the loop must be phase-locked first before it will stay within the lock range. The PLL inputs must have a phase/frequency relationship in the desired application.

Exercises (022):

1. What are the component parts of a PLL circuit?

2. What circuit in a PLL provides the smoothing function for the error voltage?

3. Besides the exclusive OR gate, what other logic circuit can be used as a phase detector?

4. What is one method, using reverse bias, of controlling the VCO's frequency?

5. Which is greater, the lock range or capture range of a PLL?

023. Specify two important uses for the PLL circuit in digital applications.

PLL Applications. Applications of the PLL touch most of us in one way or another. If you have an AM-FM stereo tuner, a PLL may be in use to provide precise FM frequency control. The forty channel citizens' band radio (CB) you have in your car probably uses a PLL as a frequency synthesizer to provide each channel frequency for reception and transmission. Using a PLL frequency synthesizer in a CB requires only one crystal for the reference input instead of a crystal for each channel, without the PLL. The PLL is also used for decoding stereo FM reception, detecting AM signals and for motor speed control.

Magnetic disk storage units frequently use a PLL as a data synchronizer. Inherent data shift occurs whenever data are read or written to magnetic media. This results in a frequency difference between data clocking rates on and off the media. PLLs are used to synchronize the data back to its original clock rate, thereby insuring data integrity. The PLL technique is also used with digital data communications links to perform a similar purpose.

Another important use of the PLL is that of the frequency synthesizer. By inserting a programmable divider between the VCO and phase detector, we allow the VCO to operate at a frequency other than that of the reference. This we do by tuning the VCO for our frequency of interest, then programming the divider to provide the proper division ratio. In this manner a

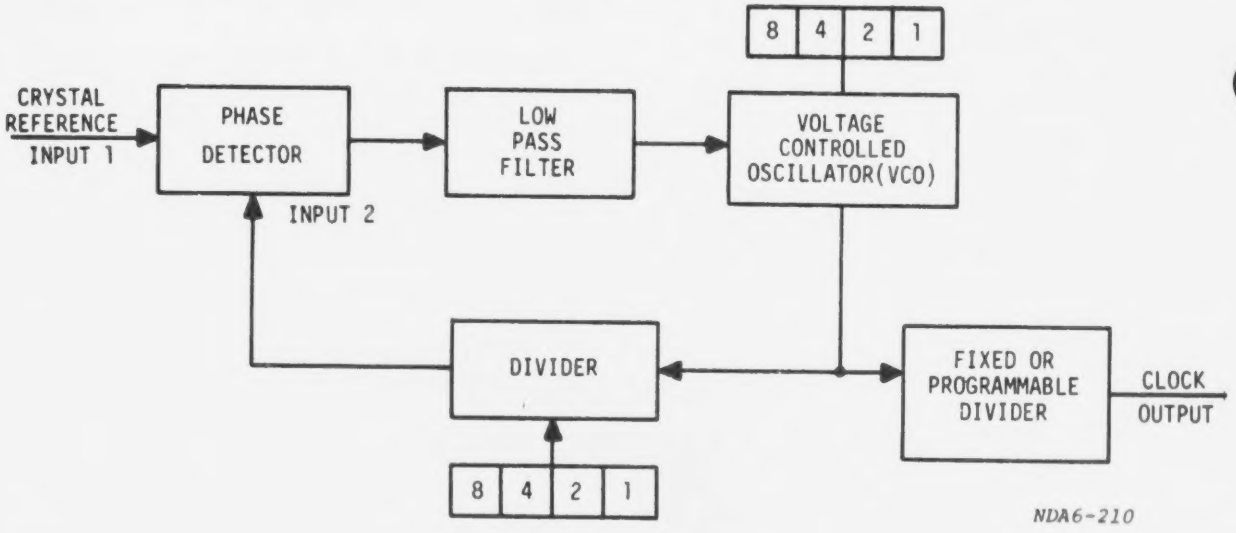

8
4
2
1
CRYSTAL REFERENCE
INPUT 1
PHASE DETECTOR
INPUT 2
LOW PASS FILTER
VOLTAGE CONTROLLED OSCILLATOR(VCO)
DIVIDER
FIXED OR PROGRAMMABLE DIVIDER
CLOCK
OUTPUT
8
4
2
1
NDA6-210

Figure 4-15. A PLL frequency synthesizer.

signal equal to the reference will allow phase-lock to occur. Using transistor-transistor logic (TTL) ICs, the PLL will be able to operate over a range of approximately 30-100 mhz. By piacing a programmable or fixed divider after the VCO as an output, we can develop any number of accurate, precisely controlled clocks for a system's use (fig. 4-15).

The applications described here demonstrate the versatility of the PLL technique. You, as an electronics technician, are apt to see a PLL in equipment presently used in the Air Force. If you see a phase detector and a voltage controlled oscillator in a circuit diagram—you can be sure a low pass filter is in there somewhere too! A divider may be used, and if so, it could be fixed or programmable. Crystals are frequently used as a stable reference input, or a system clock may be used. An understanding of the PLL and its component parts, and recognizing it when you see it, will enable you to break the PLL apart and logically troubleshoot it.

Exercises (023):

1. In what peripheral device does inherent data shift require the use of a PLL circuit?

2. Which application of the PLL can provide a number of precisely controlled clock outputs?

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Answers for Exercises

CHAPTER 1

Reference:

001 - 1. The correct choice is A.
001 - 2. To produce a sharp spike.
001 - 3. Used as an input to a Schmitt trigger.
001 - 4. An integrator circuit.

002 - 1. CR1 is shorted, allowing the positive portion of the input signal to be developed across R1.
002 - 2. Choice B is the correct output.
002 - 3. The diodes anode is connected to the capacitor.
002 - 4. A DC restorer.

003 - 1. Squaring off a rounded wave and voltage-level sensing.
003 - 2. Q1 will conduct.
003 - 3. As long as the input pulse exceeds the threshold voltage.

CHAPTER 2

004 - 1. Amplification; frequency-determining device; regenerative feedback.
004 - 2. Amplifier; feedback network; output frequency.
004 - 3. Common-emitter, input; output.
004 - 4. RC networks; LC tank circuits; crystals.
004 - 5. Regenerative.
004 - 6. Decreases; reducing; oscillator.

005 - 1. L2; C1.
005 - 2. R1; current.
005 - 3. Primary L1; 180°, 3.
005 - 4. L1; L2; positive.
005 - 5. High; low.
005 - 6. Temperature stability.
005 - 7. V_{cc} polarity; transistor.

006 - 1. Tapped coil.
006 - 2. Swamping resistor; stability.
006 - 3. Q1; autotransformer.
006 - 4. In phase; regenerative.
006 - 5. Shunt; amplifier.
006 - 6. Coupling; output circuit.

007 - 1. Split capacitors.
007 - 2. Voltage-divider network; forward bias.
007 - 3. Interelement capacitance; across.
007 - 4. Frequency stability characteristics; correct amplitude, feedback.
007 - 5. Inductance; capacitance.

008 - 1. The gate current.
008 - 2. High Q; it oscillates at a constant frequency free of undesired variations.

009 - 1. Hexagonal; pointed; three.
009 - 2. Frequency; temperature; type.
009 - 3. Positive.
009 - 4. Parallel; externally connected circuit elements.

010 - 1. Two transistors are used, and a crystal is connected between the emitters.
010 - 2. Forward-bias resistor for Q1.
010 - 3. At its resonant frequency, the crystal has a very low impedance and will pass the feedback signal to the emitter.
010 - 4. Directly from the collector of Q2.

011 - 1. Output; multiple.
011 - 2. Harmonic frequencies.
011 - 3. Average; base-emitter junction; C.
011 - 4. Quadrupler; becomes weaker.
011 - 5. More power; output signal.
011 - 6. Buffer amplifier; unilateralization; neutralization.

012 - 1. Dividers; circuits; on; off.
012 - 2. Rise time; flat top; fast fall times; accurately controllable.
012 - 3. PRF.
012 - 4. Increase.
012 - 5. Constant current rise.
012 - 6. Inductive.
012 - 7. Resistor; inductor.
012 - 8. Negative; cut Q1 off.
012 - 9. $\frac{R}{X_L}$.
012 - 10. Critical.

CHAPTER 3

013 - 1. (1) a.
(2) h.
(3) i.
(4) d.
(5) j.
(6) g.
(7) c.
(8) f.
(9) b.
(10) e.

014 - 1. (1) d, h, j.
(2) b, e, f.
(3) c, g, i.
(4) a.

015 - 1. R3 or C3 has increased in size.
015 - 2. R3 or Q2 open.

015 - 3. R6 open. Q1 will be cut off, and Q2 will be conducting. Negative triggers are amplified and inverted by Q1 and cause Q2 to cut off for the duration of the triggers. No gate is produced due to the absence of feedback.

015 - 4. B1 open. With R1 open, Q1 has no direct path for current flow. The base of Q2 is at ground potential through R5. Negative input triggers cause Q2 to conduct, but no feedback occurs.

CHAPTER 4

016 - 1. To provide multiple or submultiples of the basic tuning pulse.
016 - 2. 2,400 Hz.
016 - 3. The input frequency and the output frequency.

017 - 1. One.
017 - 2. Eight.
017 - 3. 5 pulses to FF-A, 2 pulses to FF-B, and 1 pulse to FF-C.

018 - 1. A time-division multiplexing system combines the signals for transmission over the common transmission medium by alternately connecting each voice-band signal source to the transmission medium for a short period of time.
018 - 2. The minimum sampling rate is determined by the highest frequency in the voice-band signal.
018 - 3. Three times each cycle.
018 - 4. By the movement of the diaphragm which, due to mechanical limitations, cannot follow or reproduce all of the small changes in amplitude.
018 - 5. Since the highest frequency in the voice-band is 4,000 Hz and the sample rate is three times per cycle, then the minimum sample rate is equal to 12,000 (12 kHz) times per second.

019 - 1. It eliminates the need of the receiver to determine whether a specific pulse sample occurred during the positive or negative portion of the sine wave.
019 - 2. The noise/pulse-width ration. Distortion increases as pulse width decreases.
019 - 3. When two pulses are adjacent to each other, they merge, resulting in one pulse with an amplitude equal to the average value of the two pulses.

020 - 1. PAM—pulse-amplitude modulation.
020 - 2. By superimposing the signal to be sampled on a DC reference voltage.
020 - 3. Once; 2-μsec sample and 2-μs guard time for a total of 4 μs per channel.
020 - 4. Highway clamping is the guard time. It is when the highway is grounded during the first portion of the 4-μs pulse period.
020 - 5. It smoothes out each pulse, filling in the gaps between pulses, which results in forming a signal that resembles the original signal.
020 - 6. A resonant circuit.

021 - 1. The PLL serves as an electronic servo or automatic control system by automatically correcting for phase/frequency differences between two input signals.
021 - 2. The phase detector, low-pass filter, and voltage-controlled oscillator.
021 - 3. They must be related to each other in some manner, most often by being multiples/submultiples of each other.

022 - 1. A phase detector to compare two related inputs, a low-pass filter which provides a filtered correction voltage, and the voltage-controlled oscillator to which the error voltage is applied.
022 - 2. The low-pass filter (LPF).
022 - 3. The D flip-flop.
022 - 4. By using a varactor diode for frequency control of the VCO.
022 - 5. The lock range.

023 - 1. Magnetic disk storage units.
023 - 2. Using the PLL as a frequency synthesizer circuit.

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MODULE 10005

DIGITAL TECHNIQUES

Unit 4

Sequential Logic

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Preface

IN PERFORMING its job, a data processing machine must store, retrieve, move, and manipulate large quantities of data. This unit to Module 10005, *Digital Techniques*, is a study of several circuits used to perform these tasks within a data processor or computer. Sequential logic begins by covering types and operation of flip-flop circuits. These elements are the basic building blocks for the remainder of the text which is a study of counters and registers constructed using flip-flops.

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Figure No.	*Title*
1-13	SN54H72, SN74H72 J-K master-slave flip-flops
1-14	SN7474 dual D-type edge-triggered flip-flops
1-33A&B	SN7490 decade counters
1-34A	S54160, S54161, S54162, S54163, N74160, N74161, N74162, N74163 synchronous four-bit counter
1-34B	Digital 54/74 TTL series S54/N74160, S54/N74161, S54/N74162, S54/N74163
1-34C	Data timing sequence
1-35	S54193, N74193 synchronous four-bit binary up/down counter with preset inputs
1-35B	Functional block diagrams
1-35C	Data timing sequence
1-49A&B	SN5496, SN7496 five-bit shift registers

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NOTE: In this unit, the subject matter is developed by a series of student-centered objectives. Each of these carries a three-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see whether your answers match those in the back of this unit. If your response to an exercise is incorrect, review the objective and its text.

1-1. Flip-Flops

The flip-flop is the basic logic element used in sequential logic. Certain specially configured flip-flops are the bistable elements most widely used in the construction of registers and counters. It is the bistable multivibrator which is commonly used as a flip-flop. The bistable multivibrator is used in one of three configurations for flip-flop operation. These configurations are:

(1) The set/reset flip-flop or latch.
(2) The toggle flip-flop.
(3) The J-K flip-flop.

001. Identify the circuitry and functions of components and designate input and output signals of the bistable multivibrator (flip-flop).

Set/Reset Flip-Flop. A flip-flop is a device that has two stable states. One state is called the SET state and the other state is called the CLEAR or RESET state. A flip-flop can be in only one of its stable states at a time. So, it will be either set or reset. The output levels of the flip-flop depend on its state. If the flip-flop is SET, the ONE output would be a logic high and the ZERO or RESET output would be a logic low. If the flip-flop is RESET, the ONE output is a logic low and the ZERO output is a logic high. This characteristic makes the flip-flop ideally suited for the storage of binary 1's and 0's. This storage of binary 1's and 0's by flip-flops can be either an asynchronous or synchronous operation. An asychronous operation requires that the flip-flop (FF) respond directly or immediately to changes in the inputs. Synchronous operation of a flip-flop requires a system-clock. The clock pulse will cause the flip-flop to respond when it and the input signals are applied to the flip-flop simultaneously. During your study of flip-flops, you will cover both types of operation. Let's begin the study of set/reset flip-flops with an analysis of the bistable multivibrator.

Bistable Multivibrator. The most common FF circuit used in computers is the bistable (also called an Eccles-Jordan multivibrator). The circuit of a basic bistable multivibrator and its waveforms are shown in figure 1-1. Refer to this figure for our discussion of the circuit operation. In either stable state, one transistor is conducting and the other is cut off. The states are switched by applying the proper trigger pulse. Resistors R1, R3, and R7 form the voltage divider network that develops the forward bias for Q2. R2, R4, and R5 develop the forward bias for Q1. C1 and C2 are called speedup capacitors, and they are used to couple fast changes in the collector circuits to the base circuits which increases the circuit's switching speed.

Assume that prior to time T_0, Q1 is cut off, the collector voltage (V_{C1}) is near negative V_{cc}, and the base voltage (V_{B1}) is near zero volts. Also assume that just prior to time T_0, Q2 is saturated, the collector voltage (V_{C2}) is near zero volts, and the base voltage (V_{B2}) is negative. At time T_0, a negative trigger pulse is applied to the input. This negative trigger is coupled through C3 and C4 to the base of Q1 and Q2. Q2 is already conducting, so the trigger has no effect on the conduction of Q2. Q1 is cut off and the negative trigger increases the forward bias to a point where Q1 conducts. V_{C1} then goes from near negative V_{cc} to slightly less negative than zero volts. This causes the base voltage of Q2 to change toward zero volts (cutoff). V_{C2} then changes toward the negative V_{cc}. This negative voltage is coupled to the base of Q1 and drives Q1 to saturation. Thus, a stable state of Q1 conducting and Q2 cutoff is reached. The flip-flop remains in this state until another negative trigger is applied at time T_1. At this time, the circuit is flipped back to its other stable state.

You can now see that the flip-flop has two stable states. In one state, the collector of Q1 is high and the collector of Q2 is low. The opposite is true for the other state. Thus, the output of Q1 could represent yes, true, present, 1, etc., and the output of Q2 could represent the opposite values; that is, no, false, absent, 0, etc. This two-value system is the basis for digital computer logic, and it is for this reason that the bistable multivibrator is widely used in computers. However, the basic Eccles-Jordan flip-flop we have just discussed must undergo certain circuit changes to be used as a logic FF within a computer.

Logic Flip-Flop. Just how does the basic Eccles-Jordan multivibrator differ from the logic flip-flop? Figure 1-2 illustrates a version of the computer logic FF with several circuit modifications which render it compatible for use with other logic circuits. These modifications consist of the following:

- Logical switching circuits at the inputs to insure the flip-flop triggers at the desired time.

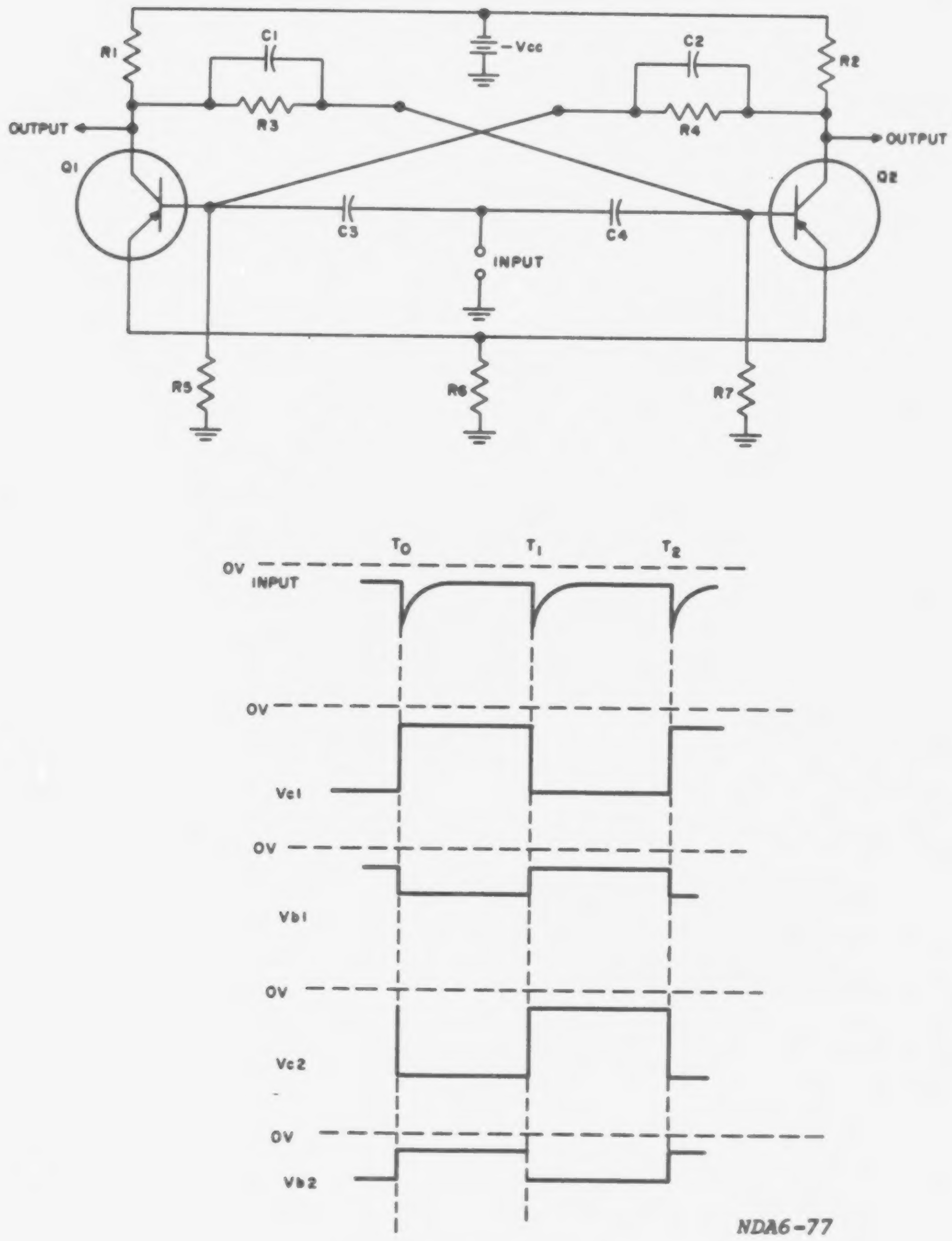
R1
C1
-Vcc
C2
R2
R3
R4
OUTPUT
OUTPUT
Q1
Q2
C3
C4
INPUT
R5
R6
R7
T0
T1
T2
OV
INPUT
OV
Vc1
OV
Vb1
OV
Vc2
OV
Vb2
NDA6-77

Figure 1-1. Bistable multivibrator.

- Circuits for presetting the flip-flop to a desired state.
- Differentiating circuits to provide sharp trigger pulses.
- Visual indicators of the flip-flop's state: ONE or ZERO.
- Limiting circuits to establish the desired logic levels.

For the following circuit analysis of this particular logic flip-flop, positive logic is assumed; that is, relatively high voltage represents the binary 1 and a low voltage represents a binary 0.

Transistors Q3 and Q4 form the basic multivibrator. Q3 is the ONE-side transistor and Q4 is the ZERO-side transistor. R1 and R2 are collector-load resistors. R2, R6, and R9 form the voltage divider network for forward-biasing Q3. R1, R5, and R10 form the voltage divider network for forward-biasing Q4. The important portion of the forward bias for operation of this circuit is

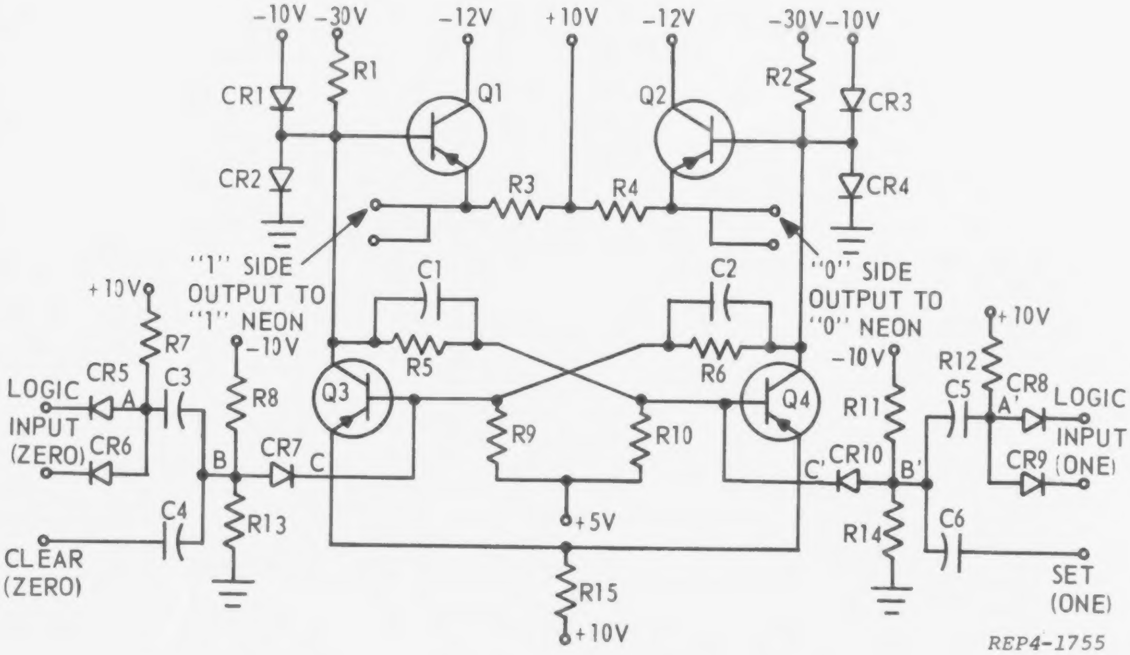

Figure 1-2. Flip-flop schematic.

developed across R9 and R10. C1 and C2 couple fast collector changes to the transistor bases in order to increase the switching speed of the flip-flop. The inputs to the flip-flop consist of SET and CLEAR circuits and logic input circuits. The logic circuits in this case are positive AND-gates. CR5, CR6, and R7 form the AND-gate that feeds the ONE-side transistor and clocks the flip-flop to the ZERO state. CR8, CR9, and R12 form the AND-gate that feeds the ZERO-side transistor and clocks the flip-flop to the ONE state. The CLEAR (ZERO) input is fed to C4 and the SET (ONE) input is fed to C6. These inputs make it possible to preset the flip-flop to a desired state.

C3, R13, C5, and R14 are networks that differentiate the outputs of the AND-gates. C4, R13, C6, and R14 form the differentiating networks for the CLEAR and SET inputs. R8, R13, R11, and R14 form voltage divider networks that place negative potentials on the anodes of CR7 and CR10. This negative potential allows them to conduct only on the positive spike of the differentiated wave and permits CR7 and CR10 to perform their functions as limiting diodes, clipping the negative spikes.

Realize that CR7 will conduct only when Q3 is conducting, because only at this time is CR7 forward biased. This is due to the negative voltage on the base of Q3 and a positive spike appearing on the anode of CR7. When Q3 is conducting, Q4 is cut off due to positive potential on the base of Q4. This reverse biases CR10 and prevents the positive spike on the anode of CR10 from reaching the base of Q4. Transistors Q1 and Q2 are emitter followers. The outputs are taken from their emitters. CR1, CR2, CR3, and CR4 are limiting diodes that maintain the logic levels at 0 volts (logic 1) and −10 volts (logic 0). The outputs are connected to neon indicators so that the state of the flip-flop can be determined by visual inspection. These indicators are not shown in the figure.

At time T_0, the flip-flop is in the ONE state. This means Q3 is conducting and Q4 is cut off. The ONE-side output is at 0 volts and the ZERO-side output is at −10 volts. At time T_1, signals are applied to CR5 and CR6, as shown in figure 1-3. The signals identified as A, B, and C in figure 1-3 are the signals at points A, B, and C in the circuit. Signal A is the output of the AND-gate. Signal B is the output of the differentiating network. Signal C is the output of the limiting diode. Since both the ONE-side and the ZERO-side input circuits and their waveshapes will be the same, it is sufficient to explain only one input circuit.

The input signals (CR5 and CR6) to the circuit are both high during the time from T_1 to T_2. This is the only time an output from the AND-gate will be present, as illustrated by signal A. Signal A is then differentiated by C3 and R13 (signal B), and the negative spike is clipped by CR7 (signal C). The positive spike of the signal at C is applied to the base of Q3 at time T_1 and will cut off Q3. The collector voltage of Q3 goes to a negative potential. This negative change is coupled by C1 to the base of Q4. This causes Q4 to conduct. The collector voltage of Q4 decreases toward zero volts. This decrease is coupled by C2 to the base of Q3 and keeps Q3 cut off. With Q3 cut off, the collector voltage is at −10 volts because of the logic level establishing diode CR1. This voltage (a low) is applied to the base of Q1, and the output of −10 volts is taken from the emitter of Q1. This is the ONE-side output.

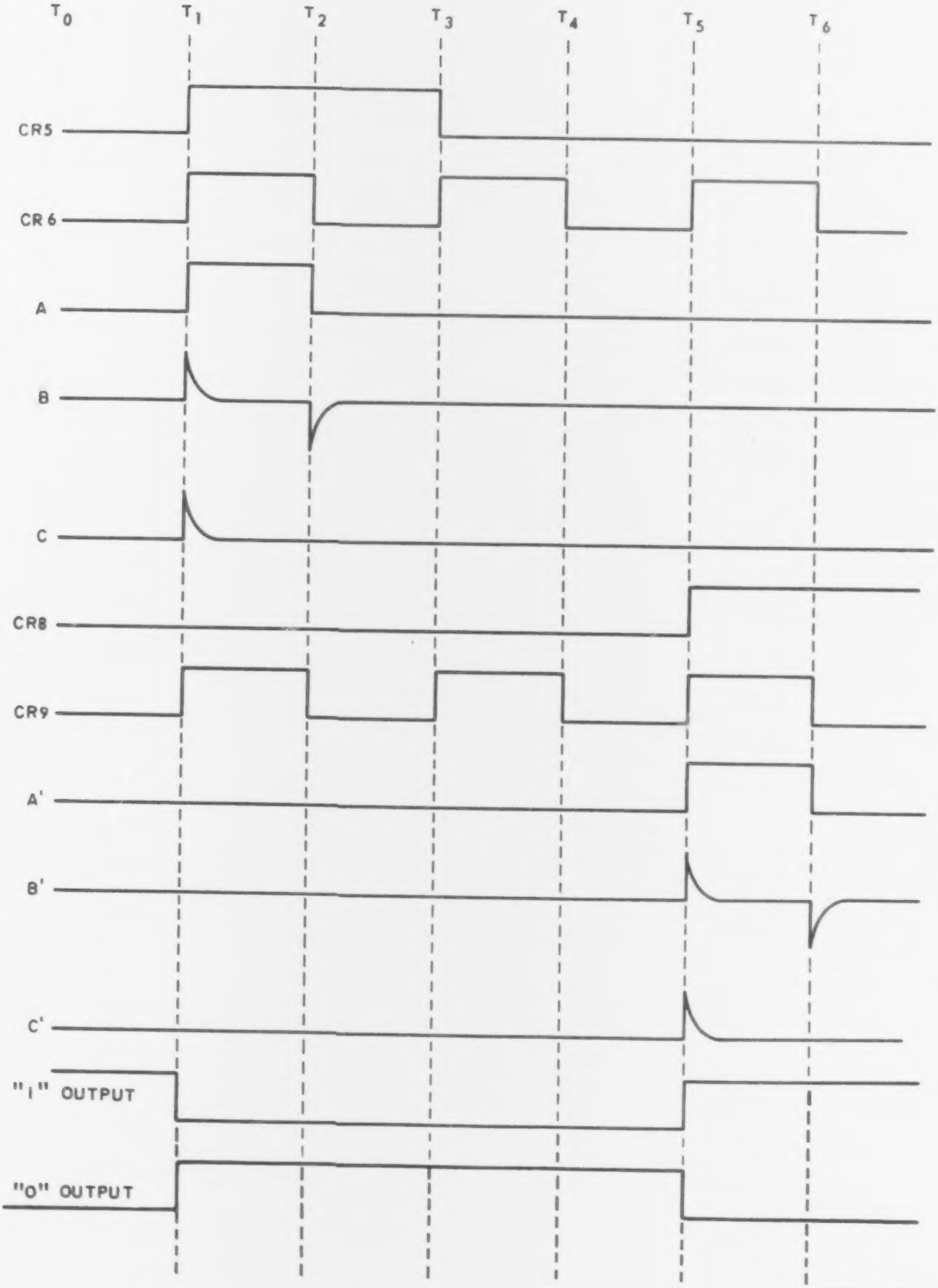
T0
T1
T2
T3
T4
T5
T6
CR5
CR6
A
B
C
CR8
CR9
A'
B'
C'
"1" OUTPUT
"0" OUTPUT
NEO13-50

Figure 1-3. Flip-flop waveforms.

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After time T_1, Q4 is saturated and the collector is at zero volts because of the clamping action of CR4. This voltage (a high) is applied to the base of Q2, and the output of zero volts is taken from the emitter of Q2. This is the ZERO-side output. The flip-flop is now in the ZERO state and remains in this stable state—the ZERO state—until time T_5. At this time, the inputs to CR8 and CR9 (as shown in fig. 1-3) activate the logic input (ONE) gate. Signals A′, B′, and C′ are generated and a positive trigger (C′) is applied to the base of Q4. This cuts off Q4 and clocks the flip-flop to the ONE state, with Q3 conducting and Q4 cut off. The multivibrator action is the same as was discussed in clocking the FF to the ZERO state.

Exercises (001):

1. What are the flip-flop outputs if they are in the CLEAR state?

2. In what state will the flip-flop be placed with a high on the C input?

3. In what state will the flip-flop be placed with a high on the S input?

4. What is the purpose of diodes CR1 through CR4 in figure 1-2?

5. What function is performed by CR5, CR6, and CR7 in figure 1-2?

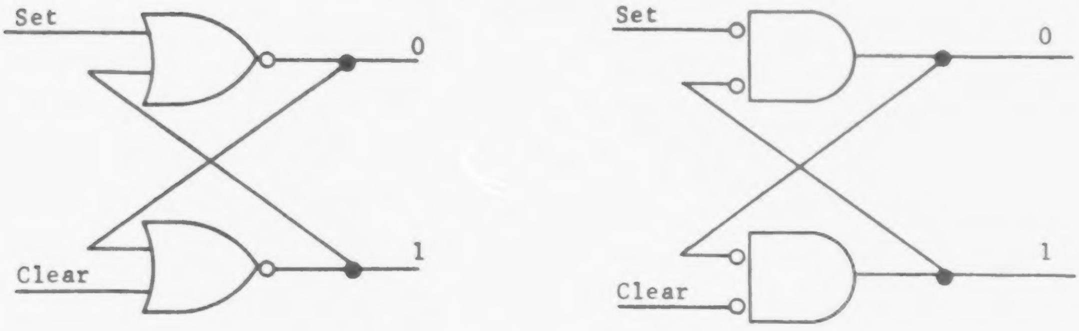
6. What transistors make up the basic multivibrator in figure 1-2?

7. Which clock of the trigger pulse changes the state of the flip-flops?

002. Identify an R-S latch flip-flop and state how the gate operates for the set and reset states.

R-S Latch Flip-Flop. The basic bistable multivibrator trigger circuits, with or without modifications, may be used to function as set/reset flip-flops in logic circuits. It is, perhaps, more practical (from the standpoint of manufacturing costs) to interconnect certain logic elements so that they will function as flip-flops. Figure 1-4 illustrates how two gates may be interconnected as an R-S latch.

NOTE: A small circle (state indicator) at the symbol output indicates that the output terminal of the activated function is relatively low (L). Conversely, the absence of the state indicator means that the active output is a relatively high (H) signal. A state indicator at the input means that a relatively low signal is required at that input to activate the logic gate. If there is no state indicator, a relative high input is required to activate the logic gate.



Set in	Clear in	"1" Output	"0" Output
L	L	no change	
L	H	L	H
H	L	H	L
H	H	L	L

Figure 1-4. R-S configuration using gates.

Assuming that the flip-flop is initially in its CLEAR state (a high at the ZERO output and a low at the ONE output), a pulse of the proper polarity and amplitude applied at the SET input will cause the flip-flop to switch to its SET state (a low at the ZERO output and a high at the ONE output). That is, a high or one applied at the set will cause the upper OR-gate to have a low or ZERO output (remember the function of the state indicator). With lows applied at both inputs, the lower OR-gate will have a high output. The high at the ONE output applied to the SET input will now hold the flip-flop in its SET state until one of two things occurs: (1) a high is applied at the CLEAR, or (2) the circuit is deenergized.

Conversely, if the flip-flop is initially in its SET state, a pulse of the proper polarity and amplitude applied to the RESET input will cause the flip-flop to switch to its CLEAR state. That is, a high applied to the CLEAR input will cause the lower OR-gate to have a low output. With lows applied at both inputs, the upper OR-gate will have a high output which is then applied to the RESET or CLEAR input. This will now hold the flip-flop in its CLEAR state until one of two things occurs: (1) a high is applied to the SET input, or (2) the circuit is deenergized. This circuit is classified as a flip-flop latch because it has outputs that are not necessarily of the opposite states. In this circuit, the application of simultaneous highs to both inputs will cause both outputs to assume the same state (in this case, a low) for the duration of the inputs.

Exercises (002):

1. Explain how the setting of the OR-latch flip-flop in figure 1-4 is accomplished.

2. Once set, how is the OR-latch flip-flop of figure 1-4 reset?

3. How is the AND-latch flip-flop of figure 1-4 held in the SET state?

4. Using the AND-gate latch of figure 1-4, how is the latch set?

003. Identify circuitry of the toggle flip-flop, and state the functions of circuit components.

Toggle Flip-Flop. A toggle flip-flop, sometimes referred to as a complementing or complemented flip-flop, is shown in figure 1-5. This flip-flop is a bistable device which will accept input pulses from a common source and changes from its existing state to the complement of that state each time it is triggered. For example, if it is in the ONE state, an input trigger will switch the flip-flop to the ZERO state, or vice versa.

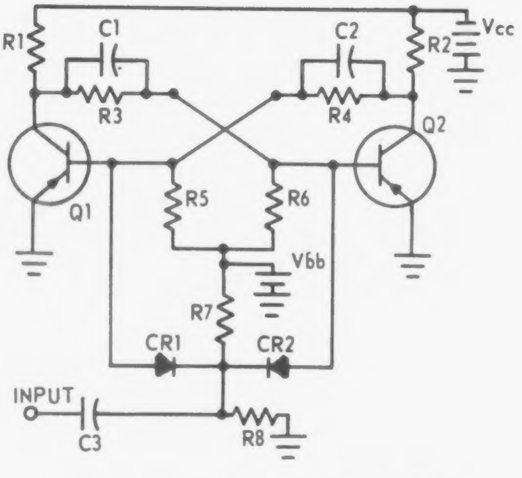


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Figure 1-5. Toggle flip-flop.

With the input pulses applied simultaneously to both transistors, switching time would be delayed, a condition which would cause the rise and fall times of the output signal to be longer. Pulse steering diodes CR1 and CR2, shown in figure 1-5, direct the input pulse to the transistor that is to be triggered into conduction. This direction prevents an increase in the rise and fall times. The circuit shown in figure 1-5 requires negative input pulses. The circuit can be modified so that positive input pulses would be required.

In figure 1-5, resistors R7 and R8 form a voltage divider from V_{bb} to ground so that the cathodes of the pulse-steering diodes are slightly positive with respect to ground. The anodes of CR1 and CR2 are at the base potentials of the transistors. The base of the conducting transistor is negative, and the base of the cutoff transistor is positive.

Let's assume that Q1 is conducting and that Q2 is cut off. In this state, CR1 has a relatively large negative potential on its anode; CR2 has a positive potential on its anode. This applies forward bias to diode CR2 and reverse bias to diode CR1. When a negative trigger is applied through coupling capacitor C3, the reverse bias on CR1 prevents the pulse from being applied to the base of conducting transistor Q1. Since diode CR2 is forward biased, the negative trigger pulse feeds through to the base of the off transistor Q2, overcomes the positive bias on the base, and turns Q2 on. When Q2 turns on, Q1 turns off. The bistable multivibrator will remain in this state until the next negative trigger pulse is applied. This pulse will feed through CR1, apply forward bias to Q1, and cause the flip-flop to switch its state again. This input pulse does not couple to the base of Q2 because of the reverse bias on CR2.

A positive trigger pulse applied to the steering circuit of figure 1-5, regardless of the state of the flip-flop, is blocked by the diodes and cannot cause the circuit to switch. For positive pulse steering, the diodes must be reversed. In this circuit, a negative potential is applied to the voltage divider R7 and R8. A positive trigger pulse, therefore, is applied through the forward biased diode to

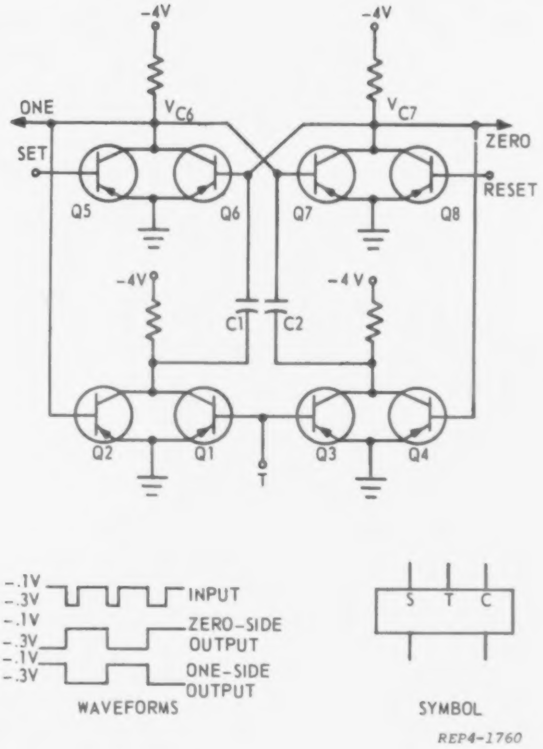


Figure 1-6. Toggle flip-flop with set and clear inputs.

the base of the on transistor, driving it to cut off. The reverse biased diode prevents the triggered pulse from being applied to the base of the off transistor. Once the circuit switches states, the bias conditions of the diodes reverse, and a second positive trigger pulse is steered to the base of the on transistor. A negative trigger pulse applied to this arrangement reverse biases the diodes and, therefore, has no effect on the circuit.

Figure 1-6 shows a complementing flip-flop circuit with set and clear capabilities. This flip-flop is reduced to its simplest form. It consists of flip-flop transistors Q6 and Q7 and two steering gates consisting of Q1-Q2 and Q3-Q4. Input to the complementing flip-flop is the leading edge of a negative pulse (downclock), and the flip-flop changes state with the downclock when all inputs are satisfied.

In the following discussion, transistors Q6 and Q7, with their associated resistors and connections, constitute the flip-flop. Transistors Q5 and Q8 serve as input switches. In figure 1-6, suppose that Q6 is off and Q7 is on. The collector voltage of Q6 is −0.3V and, applied to the base of Q7, keeps Q7 on. Collector voltage of Q7 is −0.1V and keeps Q6 off. The flip-flop is in the ZERO state. A negative pulse applied to the SET input changes the flip-flop to the ONE state.

If a −0.3V pulse is applied to the base of Q5, Q5 conducts. The collector voltage of Q5 and Q6 becomes −0.1V, which turns Q7 off. Collector voltage for Q7 then becomes −0.3V, which turns Q6 on. The flip-flop is now in the ONE state. It can be reset to the ZERO state by a −0.3V pulse applied to the CLEAR input.

A negative pulse applied to the SET input always sets the flip-flop to the ONE state (unless it is in the ONE state already). A negative pulse applied to the CLEAR input always clears the flip-flop to the ZERO state (unless it is in the ZERO state already).

With the flip-flop in the ONE state, the −0.1V on the collector of Q6 holds Q2 off while the −0.3V on Q7 holds Q4 on. With no input, Q1 and Q3 are off. With Q1 and Q2 off, their collectors are at −4V. Capacitor C1 changes to the voltage difference between the base voltage (−0.3V) of Q6 and the collector voltage (−4V) of Q1-Q2 or 3.7V. The base of Q7 and the collectors of Q3-Q4 are at −0.1V, so C2 is unchanged.

A negative pulse input (−0.2V) at terminal T turns Q1 on. This grounds the negative terminal of C1 and impresses the capacitor voltage (3.7V) across the base-emitter junction of Q6, turning Q6 off. When Q6 is cut off, the flip-flop goes to the ZERO state: C1 is unchanged, Q3 and Q4 are off, and C2 is changed to 3.7V.

To summarize the operation of the flip-flop, start with it in the ONE state. Q6 is on, Q7 is off, and Q4 on. C1 is charged and C2 is discharged. A negative pulse input at T changes the flip-flop to the ZERO state. Q1 is turned on, Q6 off, Q7 on, and Q4 off. C1 is discharged and C2 is charged. Another negative pulse input changes the flip-flop back to the ONE state.

Actually, figure 1-6 is a direct-coupled transistor logic (DCTL) circuit. DCTL circuits have two amplifier stages connected as a bistable multivibrator. One part conducts and the other is cut off until an input trigger cuts off the conducting side and the cut off side conducts. Steering circuitry allows the input to trigger one side only. The circuits of figures 1-5 and 1-6 are complementing flip-flops because one input is required to change the output from a 1 to 0 and vice-versa.

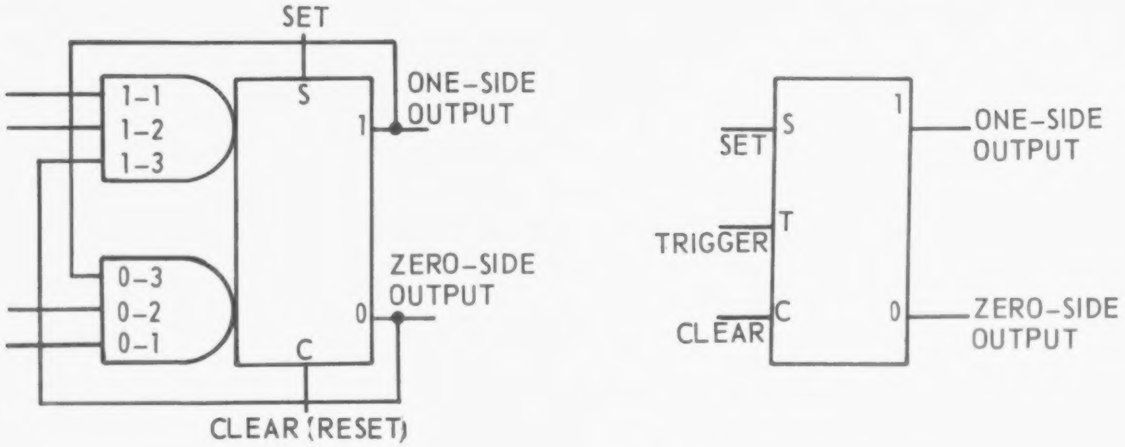
The symbols used to represent complemented and complementing logic flip-flops with SET and CLEAR provisions are shown in figure 1-7. These symbols will be used in this text. Symbol A is an internal complemented flip-flop using AND-gate inputs to the SET and CLEAR inputs. Symbol B is of the type already discussed. Notice that the complementing flip-flop requires only one input to cause a change of state to occur, whereas the complemented flip-flop with its input AND-circuitry may require any number of inputs prior to changing state.

Exercises (003):

Refer to figure 1-5 for questions 1 through 3.

1. What is the purpose of diodes CR1 and CR2?

2. How will negative polarity triggers affect the flip-flop?



A - COMPLEMENTED FLIP-FLOP

B - COMPLEMENTING FLIP-FLOP

REP4-1761

Figure 1-7. Toggle flip-flop symbols.

3. Positive polarity triggers will have what effect on the flip-flops?

Refer to figure 1-6 for questions 4 through 7.

4. What type flip-flop is the DCTL flip-flop?

5. Which transistors make up the basic multivibrator?

6. What state is the flip-flop in when C1 is charged?

7. When the flip-flop is in the ONE state, which transistors are conducting?

004. List the four types of JK flip-flops and state the function of given signals.

JK Flip-Flop. The JK flip-flop has made possible a wide variety of applications because of the flexibility of its control modes. There are several basic circuits that can be assembled using one or two JK flip-flops, and there are an unlimited number of ways several JKs can be connected. Some of the more common circuits that use JK flip-flops are binary counters, shift registers, and ring counters. The reset-set (RS), data or delay (D), and toggle-(T) type flip-flops have their own specific applications in digital equipment. Where storage is required, the RS and D-type flip-flops can be used. When toggle or complement characteristics are needed, as in counters, the T-type flip-flop can be used.

The JK flip-flop that we will study is a master-slave. There are actually two flip-flops in the total circuit; the master (which controls the slave), and the slave (which produces the outputs at Q and $\overline{Q}$). The sequence of events is:

(1) Isolate the slave from the master.

(2) Enter information (either J or K information) from the NAND-gate inputs to the master.

(3) Disable NAND-gate inputs.

(4) Transfer information from the master to the slave.

Refer to figure 1-8 as we discuss the operation. Gates 1 and 2 are the NAND-gates that receive the J, K, and clock-pulse information. To satisfy either gate 1 or 2, the J and clock pulse or the K and clock pulse must be present at the same time. This is called synchronized inputs.

The CLEAR input is normally high (logical 1), and it goes low when a CLEAR pulse is applied. Notice what happens when the CLEAR input is low. Gate 4 is disabled, setting the master flip-flop, and gate 7 is disabled, causing $\overline{Q}$ to go to the high condition. When the CLEAR pulse is gone and the CLEAR input line is again high, there is no change in the gate outputs. At this time, the master flip-flop (gates 3 and 4) is conditioned properly, Q is low to disable the K input (gate 2), and $\overline{Q}$ is high to enable the J input (gate 1).

Assume now that a high is present at J and the clock pulse goes high. This satisfies gate 1, which produces a low output. This low to gate 3 switches the master flip-flop to the opposite state. The master now has stored the input data. Notice also that the outputs of gates 5 and 6 do not change at this time. Therefore, the slave (gates 7 and 8) will not change states either.

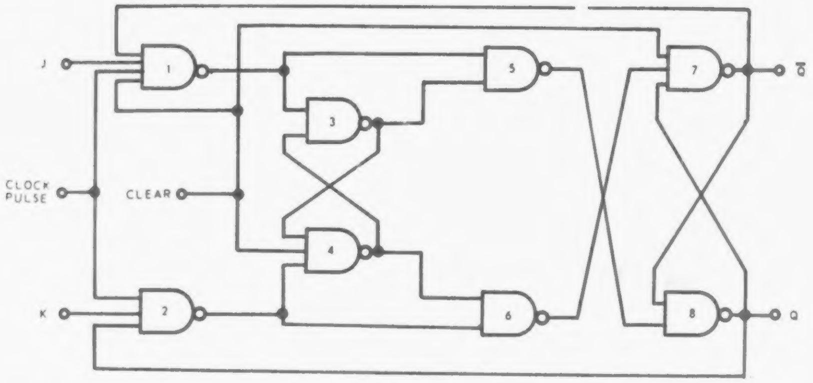
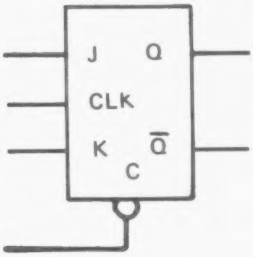


Figure 1-8. Typical master-slave J-K flip-flop.



A. SYMBOL

INTERNAL CLEAR	J	K	CLK	1	0	Q	Q̄	COMMENTS
L	X	X	X	L	H	L	H	CLEARED
H	X	X	L	PREVIOUS STATE				LOW CLK INHIBITS BOTH DATA INPUTS
H	L	L	X	PREVIOUS STATE				J & K LOW INHIBIT CLK INPUT
H	H	L	H↑	H	L	L	H	MASTER SETS TO ONE STATE
H	H	L	L↓	H	L	H	L	SLAVE SETS TO Q STATE
H	L	H	H↑	L	H	H	L	MASTER RESETS TO ZERO STATE
H	L	H	L↓	L	H	L	H	SLAVE RESETS TO ZERO STATE
H	H	H	↑↓	OPPOSITE STATE				TOGGLE OPERATION
IF ORIGINALLY IN Q STATE, THEN								
H	H	L	↑↓	H	L	H	L	NO CHANGE
IF ORIGINALLY IN Q̄ STATE, THEN								
H	L	H	↑↓	L	H	L	H	NO CHANGE

↑ UP CLOCK

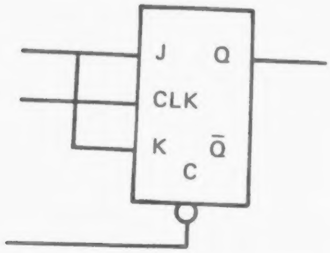
↓ DOWN CLOCK

X IRRELEVANT CONDITIONS

B. TRUTH TABLE

322-520

Figure 1-9. Expanded J-K master-slave.



A. CIRCUIT CONNECTIONS

INTERNAL CLEAR	(J-K) DATA INPUT	CLK	Q	$\overline{Q}$	COMMENTS
L	X	X	L	H	CLEARED
H	X	L	PREVIOUS STATE		CLK LOW INHIBITS DATA INPUT
H	L	↑↓	PREVIOUS STATE		LOW DATA INPUT INHIBITS CLK
H	H	↑↓	OPPOSITE STATE		TOGGLE OPERATION

↑ UP CLOCK

↓ DOWN CLOCK

X IRRELEVANT CONDITION

B. TRUTH TABLE

322-521

Figure 1-10. Synchronous toggle.

When the clock pulse goes low (downclock), gate 1 produces a high output. This high is applied to gate 3 (master flip-flop) but does not change its state. (The master was latched by the high-clock pulse with gate 3 having a high output and gate 4 having a low output.) The high from gate 1, however, does satisfy gate 5, which provides a low output to gate 8 (slave). This action causes the slave to change states (Q goes high and $\overline{Q}$ goes low). In summary, this is what happened:

(1) Gates 5 and 6 isolated the slave from the master.

(2) Information was entered at the J input at the time of the upclock, and the master stored the data.

(3) At the downclock, the J input was disabled.

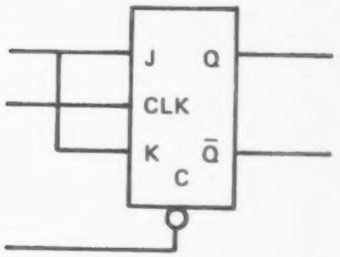
(4) Also at the downclock, the information stored in the master was transferred to the slave.

When data is entered at the K input, similar actions occur except that the input is applied to gate 4 of the master and to the isolating gate (gate 6). On the upclock, the master stores the input data, and on the downclock, the data is transferred to the slave. When K information is applied, the $\overline{Q}$ output goes high on the downclock. Another mode of operation can be accomplished by placing both J and K inputs at a high level and leaving them there. Then the slave will change states every time the downclock occurs.

Figure 1-8 shows only one of the many different versions of the JK flip-flop. Generally, other versions will operate on the same principles. Some other characteristics include clock frequencies of 30 MHz, a pulse width of 50 nanoseconds or less, and operating voltages around 5 volts. The JK flip-flop can be implemented as a JK master-slave flip-flop, synchronous or asynchronous toggle flip-flop, or a D-type flip-flop.

The general operation of the JK master-slave configuration is expanded in figure 1-9, which shows the logic symbol and associated truth table. In a synchronous toggle configuration, the JK inputs are tied together as a common data input, which must be in time coincidence with the clock pulse. Figure 1-10 illustrates the circuit connection and associated truth table. The JK flip-flop can also be implemented in an asynchronous toggle configuration. Input data is applied to the clock input and the JK inputs are tied to a permanent high. Figure 1-11 illustrates the circuit connections and associated truth table.

To use the JK flip-flop as a D or data flip-flop, the J input is inverted and applied to the K input. Since the J and K inputs are always in opposite states, the flip-flop will follow the state of whatever data is inverted and applied to the K input. Since the J and K inputs are always in opposite states, the flip-flop will follow the state of whatever data is present at the J or data input. The result of this action is to delay the data at the J input by one clock pulse. That is, the flip-flop can be considered



A. CIRCUIT CONNECTIONS

INTERNAL CLEAR	(CLK) DATA INPUT	Q	$\overline{Q}$	COMMENT
L↓	X	L	H	CLEARED
H	↓↑	OPPOSITE STATE		TOGGLE OPERATION

↑ UP CLOCK

↓ DOWN CLOCK

X IRRELEVANT

B. TRUTH TABLE

322-522

Figure 1-11. Asynchronous toggle.

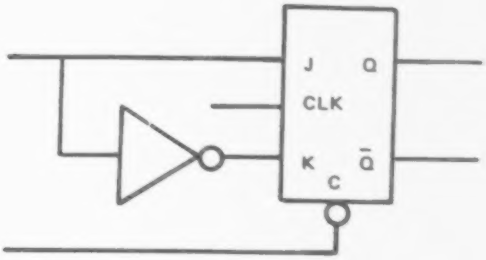
to store the data from the time of the first clock pulse until the occurence of another clock pulse. Figure 1-12 illustrates the circuit connections and associated truth table.

Exercises (004):

1. List the four types of JK flip-flops.

2. What type of circuits use JK flip-flops?

3. Explain the function of each JK flip-flop signal listed below:
   a. Clock pulse.
   b. $\overline{Q}$.
   c. Q.
   d. J.
   e. CLEAR.
   f. K.



A. CIRCUIT CONNECTION

INTERNAL CLEAR	J	K	CLK	Q	$\overline{Q}$	COMMENT
L↓	X	X	X	L	H	CLEARED
H	X	X	L	PREVIOUS CONDITION		CLK LOW INHIBITS J-K INPUTS
H	H	L	↑↓	H	L	Q STATE
H	L	H	↑↓	L	H	$\overline{Q}$ STATE

↑ UP CLOCK

↓ DOWN CLOCK

X IRRELEVANT CONDITION

B. TRUTH TABLE

322-523

Figure1-12. Synchronous operation.

005. Specify characteristics of integrated circuit (IC) flip-flops.

Integrated Circuit Flip-Flops. With the introduction and use of the digital integrated circuits, the operations remain basically the same but are accomplished at higher speeds, on a larger scale, and with less space and power requirements. The use of digital integrated circuitry to perform the same functions as solid-state logic circuitry has become more practical and therefore more frequent over the last several years.

The most widely used form of integrated digital logic circuit (DIC) is known as TTL or transistor transistor logic. TTL is best represented by the SN 54/74 series of DICs. Texas Instruments Corporation originally developed this series of logic ICs but a number of manufacturers make them and use the same numbering system.

The SN 54 (SN stands for semiconductor network) series is more expensive and designed for greater temperature range than the SN 74 series. The SN 54 devices will operate over a range of temperatures from −55° to 125° Centigrade, whereas the SN 74 devices operate over a range from 0° to 70° Centigrade.

TTL ICs operate on a power supply voltage of 5 volts and require a well-regulated 5-volt power source. The most common IC packages available in TTL are the 14-pin or 16-pin dual-in-line package (DIP). Larger packages such as the 20-, 24-, and 28-pin DIPs usually consist of medium- or large-scale integrated circuits. The listing below indicates the different versions of TTL available, the power requirements per gate, and operating speed.

Version		*Power/Gate*	*Speed*
SN 54/74	Standard	10mW	35 MHz
SN 54H/74H	High Speed	22 mW	50 MHz
SN 54L/74L	Low Power	1 mW	3 MHz
SN 54S/74S	Nonsaturating/Schottky	19 mW	125 MHz
SN 54LS/74LS	Low-power Schottky	2 mW	45 MHz

Analyzing the power and speed characteristics shows that if you want low power in a TTL IC, you will have to sacrifice speed and vice-versa.

Schottky TTL uses a Schottky barrier diode between base and collector of internal transistors to prevent saturation. The Schottky diode switches very fast and requires only 0.1 to 0.3 volts of forward bias depending on temperature. When this diode is added, speed is increased because the time required to get a transistor out of saturation is not a factor. The diode will conduct before the transistor is allowed to saturate. Any kind of nonsaturating logic is inherently faster than saturating logic.

The logical output for a TTL gate at binary 1, in positive logic, is approximately 3 volts. For a binary 0, the output voltage of a gate is usually 0.8 volt or less. TTL logic should never be subjected to voltages greater than 5.25 volts nor any negative voltage. Any noise voltage in TTL logic should be less than 1.0 volts in order to prevent erratic operation. A well-regulated power supply for TTL logic is a necessity to prevent damage to the logic and erratic operation of the logic circuits.

The different versions of TTL may be mixed in a logic circuit depending on design requirements. This proves beneficial because some parts of logic circuits must operate faster than others so that circuit outputs arrive at their destinations at the proper time.

The SN54H72, SN74H72, JK master-slave, and the SN7474, dual-D-type digital integrated flip-flops are presented with the appropriate functional explanations, diagrams, and truth tables. You will find that although there is no visible indication of an integrated circuit's similarity to the solid-state counterpart, functionally the operations accomplished are the same. These two flip-flops and their data sheets are only meant to be representative of the many available digital integrated circuits in the field. Space does not permit publication of the full line of flip-flop ICs presently in use.

JK master-slave flip-flop types SN54H72 and SN74H72 are shown in figure 1-13. These appear to be pretty much like normal flip-flops with AND-gates on the SET and RESET sides. With this type of flip-flop, the SET side is normally labeled the J side and the RESET side is labeled the K side. At the output of the flip-flop, the SET side is labeled Q and the RESET side is labeled $\overline{Q}$. The sequence of operation is the same as for other JK flip-flops. That is,

(1) Isolate the slave from the master.

(2) Enter information from AND-gate inputs to the master.

(3) Disable the AND-gate inputs.

(4) Transfer the information from the master to the slave.

In the sequence above, the slave is the flip-flop and the master is composed of the AND-gates. The flip-flop cannot retain any information that the AND-gate will not pass to it. The truth table shown in figure 1-13 will be of further assistance to you in determining the timing of information transfer.

The dual D-type edge-triggered flip-flop, SN7474, is shown in figure 1-14. These monolithic flip-flops feature direct $\overline{\text{CLEAR}}$ and PRESET inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse. The flip-flops shown in figures 1-13 and 1-14 differ only in the feature that those shown in figure 1-13 have gated inputs. Figure 1-14 shows both the truth table for these flip-flops and a functional block diagram.

Exercises (005):

1. What are the most common packages for TTL IC flip-flops?

2. What is the approximate voltage required at the J input of a SN54H72 to set the flip-flops?

3. If the flip-flop of a dual D-type flip-flop SN7474 is set, what is the voltage output at $\overline{Q}$?

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

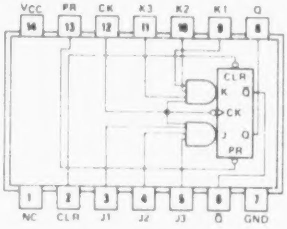
72

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

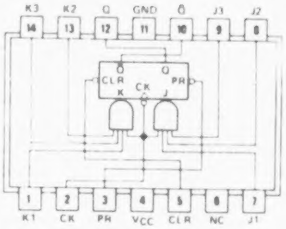
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

positive logic: J = J1·J2·J3; K = K1·K2·K3



VCC
PR
CK
K3
K2
K1
Q
14
13
12
11
10
9
8
CLR
K
$\bar{Q}$
CK
J
Q
PR
1
2
3
4
5
6
7
NC
CLR
J1
J2
J3
$\bar{Q}$
GND

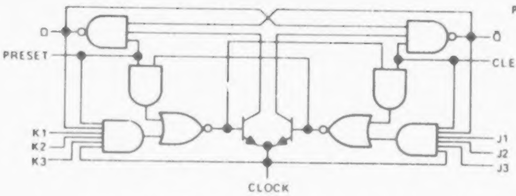
SN5472/SN7472(J, N)
SN54H72/SN74H72(J, N)
SN54L72/SN74L72(J, N)



K3
K2
Q
GND
$\bar{Q}$
J3
J2
14
13
12
11
10
9
8
$\bar{Q}$
Q
CLR
CK
PR
K
J
1
2
3
4
5
6
7
K1
CK
PR
VCC
CLR
NC
J1

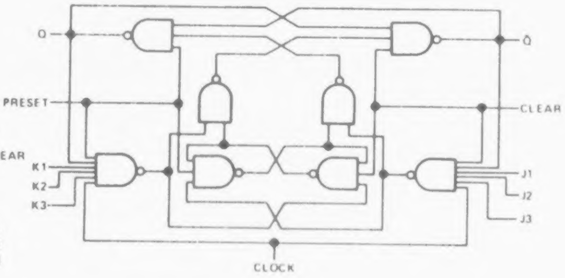
SN5472/SN7472(W)
SN54H72/SN74H72(W)
SN54L72/SN74L72(T)

NC – No internal connection



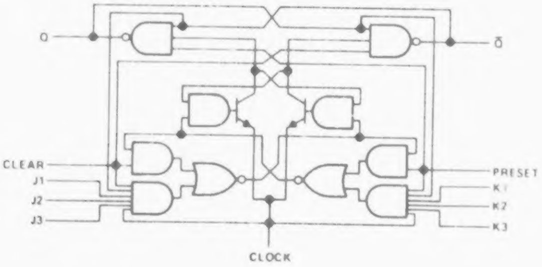
Q
$\bar{Q}$
PRESET
CLEAR
K1
K2
K3
J1
J2
J3
CLOCK

'L72–GATED J-K WITH CLEAR AND PRESET



Q
$\bar{Q}$
PRESET
CLEAR
K1
K2
K3
J1
J2
J3
CLOCK

'H72–GATED J-K WITH CLEAR AND PRESET



Q
$\bar{Q}$
CLEAR
J1
J2
J3
PRESET
K1
K2
K3
CLOCK

'72–GATED J-K WITH CLEAR AND PRESET

H = high level (steady state), L = low level (steady state), X = irrelevant

⎍ = high level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

↓ = transition from high to low level

Q_0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) state.

Figure 1-13. SN54H72, SN74H72, J-K master-slave flip-flops.

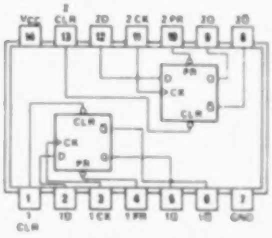
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

74

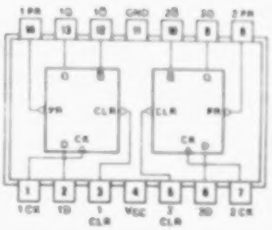
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$


VCC
2 CLR
2D
2 CK
2 PR
2Q
2Q̄
14
13
12
11
10
9
8
PR
D
CK
Q
Q̄
CLR
1
2
3
4
5
6
7
1 CLR
1D
1 CK
1 PR
1Q
1Q̄
GND

SN5474/SN7474(J, N)
SN54H74/SN74H74(J, N)
SN54L74/SN74L74(J, N)
SN54LS74/SN74LS74(J, N, W)
SN54S74/SN74S74(J, N, W)


1 PR
1Q
1Q̄
GND
2Q̄
2Q
2 PR
14
13
12
11
10
9
8
Q
Q̄
PR
CLR
D
CK
1
2
3
4
5
6
7
1 CK
1D
1 CLR
VCC
2 CLR
2D
2 CK

SN5474/SN7474(W)
SN54H74/SN74H74(W)
SN54L74/SN74L74(T)

H = high level (steady state), L = low level (steady state), X = irrelevant

⎍ = high-level pulse; data inputs should be held constant while clock is high, data is transferred to output on the falling edge of the pulse.

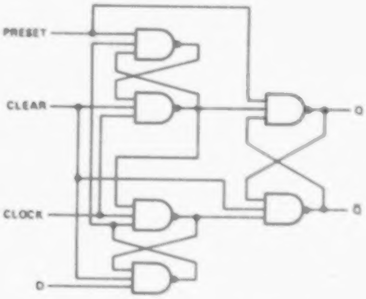
↑ = transition from low to high level, ↓ = transition from high to low level

Q_0 = the level of Q before the indicated input conditions were established.

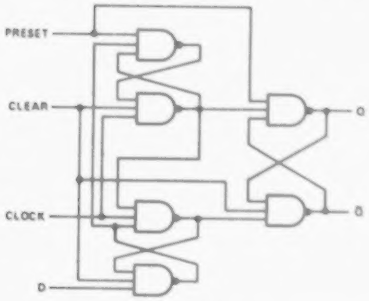
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

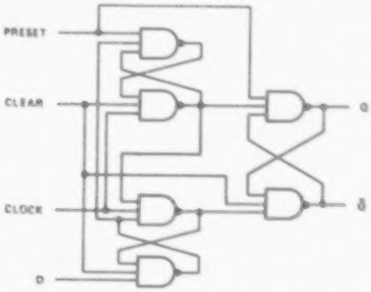
functional block diagrams


PRESET
CLEAR
CLOCK
D
Q
Q̄

'S74—DUAL D WITH CLEAR AND PRESET


PRESET
CLEAR
CLOCK
D
Q
Q̄

'L74—DUAL D WITH CLEAR AND PRESET


PRESET
CLEAR
CLOCK
D
Q
Q̄

'LS74—DUAL D WITH CLEAR AND PRESET

Figure 1-14. SN7474 dual D-type edge-triggered flip-flops.

4. What are the four sequence steps of operation for the SN74H72, JK master-slave flip-flop?

1-2. Counters

Counters are used in all computers and data processors. Some uses of counters are to count program steps, count time (seconds, minutes, etc.), and provide timing for certain computer operations. The basic circuit used in most counters is a bistable multivibrator (flip-flop). By wiring several flip-flops together in a certain way, we can make a circuit which counts in binary each time it is triggered. Figure 1-15 shows a basic three-stage counter.

006. State terms and capabilities of basic counters.

Basic Counters. When counters are classified according to circuit design, counters are referred to as either serial or parallel. When classified according to function, they are called either up-counters or down-counters. Counters can be constructed of any device having two or more stable states. Since the flip-flop has two stable states, it is a binary device. Therefore, all flip-flop counters are binary counters or modified binary counters. Straightforward binary counters are normally referred to as counters. Modified binary counters are given names such as ring counters, gray counters, modulus counters, and decimal counters. These are not all the names given to counters; however, they are the most common.

Binary counters are made up of logic flip-flops and gates connected in such a way that each flip-flop represents one place position in a binary number (2^0, 2^1, . . .2^n). A counter normally starts at 0-count and counts pulses until it resets itself to zero. This complete sequence from its starting point back to its starting point is referred to as the *cycle* of the counter. The number of pulses required to cycle the counter from 0-count to 0-count is determined by the number of stages in the counter. The number is 2^n, where N = the number of flip-flop stages. For example, a four-stage counter is able to count a total of 2^4 or 16 pulses. The number of pulses required to cycle a counter through its complete counting capacity is called the *modulus*. Thus, the four-stage binary counter has a modulus of 16.

Since each stage in the binary counter represents a different power of 2, the outputs of the stages can be sampled to determine the decimal equivalent of the binary configuration held by the counter at any time. At this time we wish to point out that although the maximum number of pulses the counter counts between resets is 2^n, the maximum decimal number the counter can represent is equal to 2^n-1. This maximum count is usually that point when all flip-flops of the counter are set. Again, using a four-stage counter as an example, the highest decimal number it can represent is 2^4-1 or 15. This is true because the first pulse applied to the counter sets the counter to 0001. Then the count progresses until the 15th pulse sets the counter to 1111, and the 16th pulse resets it to 0000. Thus, the maximum number the counter can hold is 1111, which is equal to 15.

A straightforward binary counter has a modulus (maximum count) that is a power of 2, since modulus = 2^n. By special arrangement of logic gates, counters can be made to reset after any number of pulses less than maximum. The counter can also be preset or advanced upon a given signal or command to any predetermined count within the range of the counter. Modified binary counters—counters that do not count to their maximum possible count as determined by the number of flip-flop stages—are often called modulus counters. In common terminology, the modulus is shortened to simply "mod." A mod-3 counter resets after three counts and a mod-10 counter resets after ten counts, etc. You also find the mod-10 counter called a decimal counter.

Exercises (006):

1. When counters are referred to according to circuit design, what are they called?

2. When counters are referred to according to function, what are they called?

3. What determines the number of pulses required to cycle a counter from 0-count to 0-count?

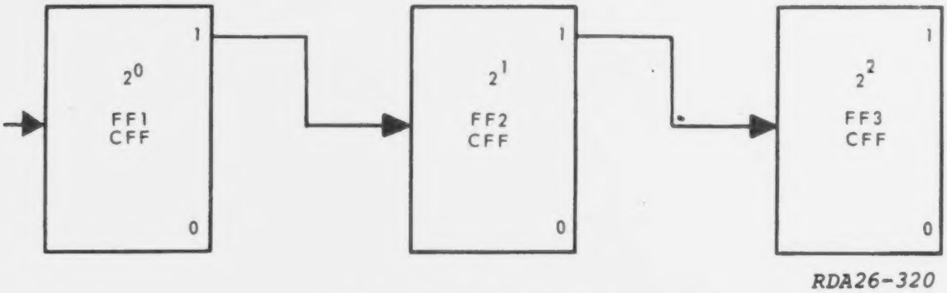


Figure 1-15. Basic three-stage counter.

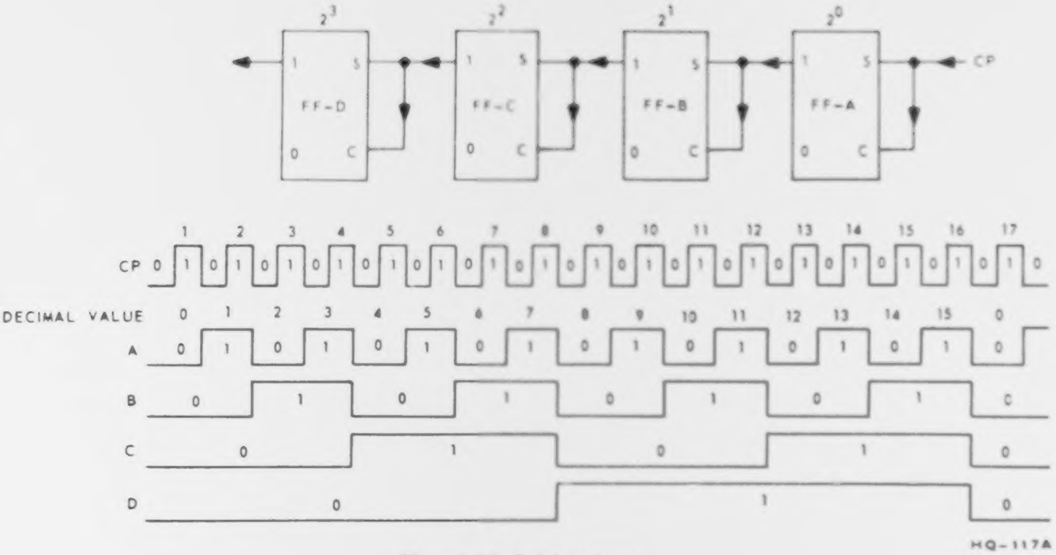


Figure 1-16. Serial-up counter.

4. What is the modulus of a four-stage binary counter?

5. What is the highest decimal number that can be represented by a four-stage counter?

6. What is the modulus of a six-stage binary counter?

007. Analyze circuit conditions of a serial-up counter and of a serial-down counter.

The Serial Counter. The serial counter is the simplest and most straightforward counter. It uses fewer circuits and its operation is the easiest to understand. It has the disadvantages, however, of being too slow for many applications.

Serial-up counter. The simplest form of a serial-up counter is shown in figure 1-16. It consists of four flip-flops labeled "A," "B," "C," and "D." Let's begin our discussion of the counter by looking at a few pertinent facts about its operation.

a. Each stage in the counter represents a place position of a binary number. In this counter, flip-flop A represents the least significant digit (LSD) and flip-flop D represents the most significant digit (MSD).

b. The flip-flops trigger on the downclock (negative-going edge) of the input pulse. The flip-flops have a differentiating and clipping circuit at each input. The downclock of the input pulse is converted to a sharp negative-going trigger.

c. A high output from the flip-flop represents a ONE; a low output represents a ZERO.

The basic four-stage serial counter shown in figure 1-16 has 16 possible combinations. Note that the input clock pulses (CPs) are fed to both the SET and CLEAR inputs of flip-flop A (FF-A), and that the ONE-side output of each flip-flop is fed to both the SET and CLEAR inputs of the succeeding flip-flop. Using figure 1-16 and its associated waveforms, let us start with the counter holding a count of 0 0 0 0 and follow through a complete counting cycle.

The first clock pulse, CP-1, is applied to both inputs of FF-A. On the downclock of this pulse, FF-2 is triggered to the ONE state. When FF-A goes to the ONE state, the output from its ONE side goes high. Since this presents an upclock to FF-B, this flip-flop remains in its present state. The counter now holds the count of 0 0 0 1. Notice that you can read this count from the waveforms by reading vertically from the bottom up to waveform A, which represents the LSD.

On the downclock of CP-2, FF-A is triggered back to the ZERO state. The ONE-side output of FF-A goes low, thus presenting a downclock to FF-B. This triggers FF-B to the ONE state. The counter now holds the count 0 0 1 0.

On the downclock of CP-3, FF-A is again triggered to the ONE state. Because the ONE-side output of FF-A presents an upclock to FF-B, FF-B does not change state. The count in the counter is now 0 0 1 1.

On the downclock of CP-4, FF-4 reverts to the ZERO state, sending a downclock to FF-B, setting it to the ZERO state. FF-B, in turn, sends a downclock to FF-C, setting it to the ONE state. The count in the counter is now 0 1 0 0.

This counting proceeds, as indicated by the waveforms of figure 1-16, until the 16th clock pulse arrives. On the downclock of this pulse, all flip-flops produce successive downclocks, thus returning the counter to 0 0 0 0. The counter has completed one counting cycle and is ready to start counting another 16 pulses.

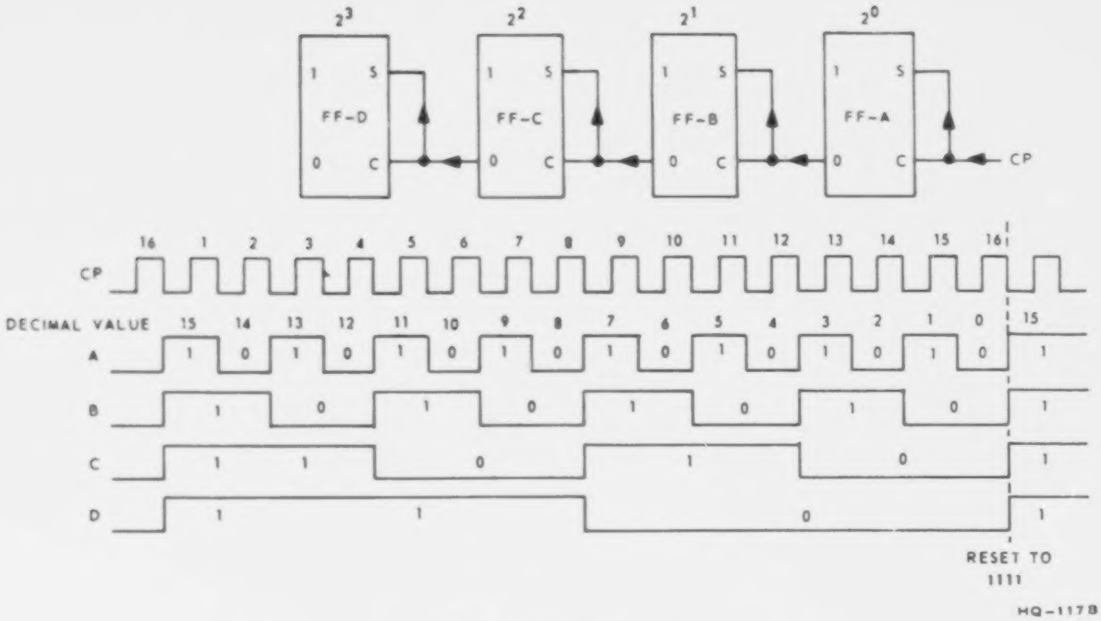


Figure 1-17. Serial-down counter.

Serial-down counter. The serial-up counter (fig. 1-16) can be easily converted to the serial-down counter (fig. 1-17). The only difference is that the up-counter stages feed the ONE-side outputs of the flip-flops to succeeding stages, whereas the down-counter feeds the ZERO-side outputs of flip-flops to succeeding stages. Compare also the decimal equivalents of the counts. The up-counter starts at 0, counts to 15, and resets to 0; the down-counter starts at 15, counts down to 0, and resets to 15.

The same facts that we established for the up-counter are true for the down-counter. With these facts in mind, refer to figure 1-17 and follow through the counting cycle. Assume that the 16th pulse from the preceding counter cycle has set all flip-flops in the counter to the ONE state; therefore, the counter holds the binary configuration 1 1 1 1, which is equal to decimal 15. Circuit action is described in the following paragraphs.

The downclock of CP-1 triggers FF-A to the ZERO state. The counter now holds a count of 1 1 1 0; in other words, one count has been removed. The downclock of CP-2 triggers FF-A to the ONE state, causing the ZERO-side output of FF-A to downclock and trigger FF-B to the ZERO state. The counter now holds the count of 1 1 0 1.

Each clock pulse reduces the count in the counter by one count. When 15 pulses have been counted, the counter holds the count of 0 0 0 0. On the downclock of CP-16, all flip-flops produce downclocks at their ZERO-side outputs. This sets all FF's to the ONE state and the counter holds the configuration 1 1 1 1. Thus, the counter has completed one counting cycle and is ready to count another 16 pulses.

Exercises (007):

1. Using figure 1-16, if flip-flops A, C, and D are in the ONE state and flip-flop B is in the ZERO state, what is the count in the counter?

2. A four-stage serial-up counter just received the 16th clock pulse. What is the state of the flip-flops?

3. When will FF-D set?

4. How can an up-counter easily be converted to a down-counter?

5. What is the sequence of counting for a down-counter?

6. Refer to figure 1-17. When will FF-B go to the ZERO state?

008. Specify the operational characteristics of parallel counters.

Parallel Counters. Instead of feeding the clock pulses to only the LSD flip-flop as in serial counters, the clock pulse can be fed to all stages of a counter at the same time.

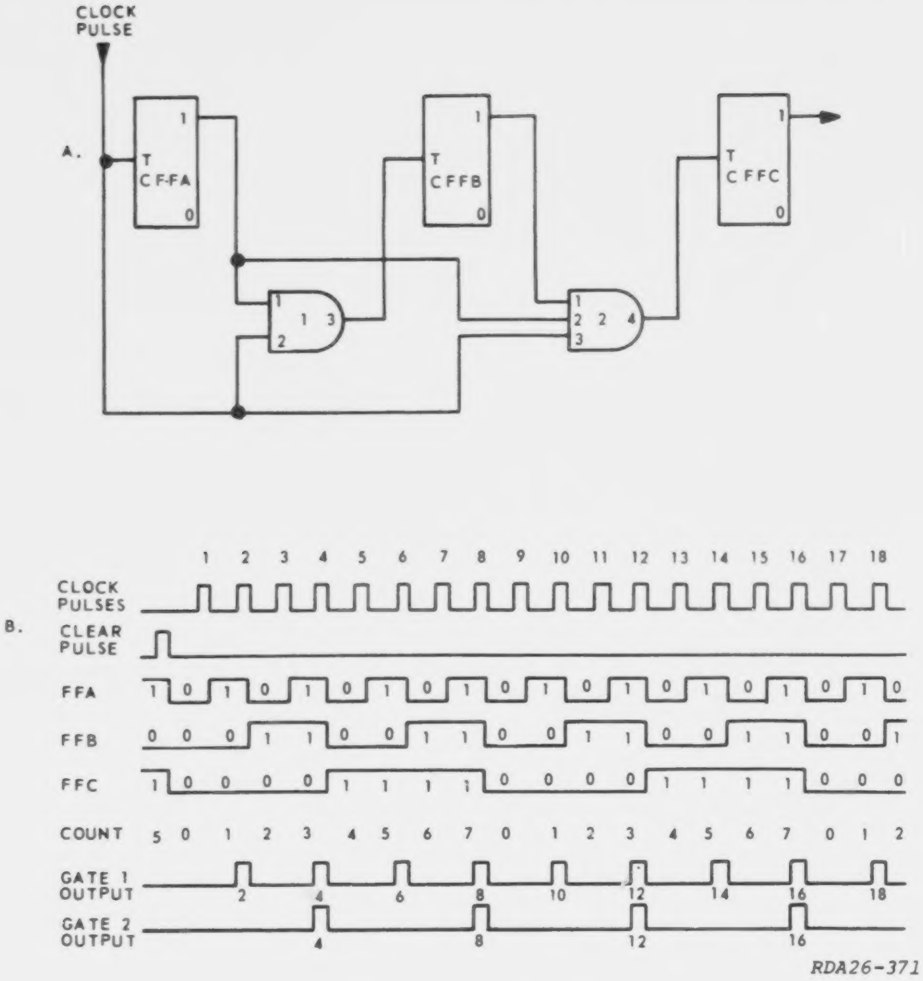

CLOCK PULSE
A.
T
C F-FA
1
0
T
C FFB
1
0
T
C FFC
1
0
1
2
1 3
1
2
3
2 4
B.
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
CLOCK PULSES
CLEAR PULSE
FFA
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
FFB
0 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1
FFC
1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0
COUNT
5 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2
GATE 1 OUTPUT
2 4 6 8 10 12 14 16 18
GATE 2 OUTPUT
4 8 12 16
RDA26-371

Figure 1-18. Parallel-up counter.

When connected in this manner, the circuit is called a parallel counter. Parallel counters may count either up or down, depending on the way the circuit is wired.

Parallel up-counter (using downclocks). The three-stage counter shown in figure 1-18 is a parallel up-counter. Observe the circuit connections very closely. Notice that the clock pulse is fed directly to the trigger input of the first stage, is gated through AND-gate 1 to the trigger input of the second stage, and is gated through AND-gate 2 to the third stage. This is the distinguishing feature of a parallel counter—the clock pulses do the actual triggering of each stage.

Let's start the explanation with the counter at a count of zero (all stages CLEAR). Both AND-gates will have a binary 0 output. Since all the flip-flops in the counter are complemented; i.e., each input pulse changes the state, FF-A will be SET by the downclock of clock pulse (CP-1). This makes FF-A the LSD flip-flop. Observe the waveshapes and note that, for the duration of CP-1, there is no output pulse from AND-gate 1 because of the binary 0 on pin 1 from the ONE-side of FF-A. This will prevent CP-1 from affecting FF-B. The count in the counter after CP-1 is $001_{(2)}$.

When CP-2 comes in, FF-A will CLEAR. Observe the waveshapes again. During CP-2, pin 1 of AND-gate 1 is activated by the binary 1 from FF-A. So when CP-2 arrives, it will be gated through AND-gate 1 and SET FF-B (note the output waveshape from gate 1). FF-C will not be affected since the clock pulse cannot get through AND-gate 2 because of the binary 0 on pin 1 from FF-B. The count in the counter is now $010_{(2)}$.

Follow the waveshapes and work the counter through CP-8. Remember that FF-A is triggered by every clock pulse, FF-B is triggered by every second clock pulse, and FF-C is triggered by every fourth clock pulse. This counter has a maximum count of $7_{(10)}$ with a modulus of 8.

Parallel down-counter (using downclocks). A four-stage positive logic parallel down-counter is shown in figure 1-19. The waveshapes are the same as those for a positive logic serial down-counter. The operation of both circuits is the same except for the fact that, in a serial counter, each

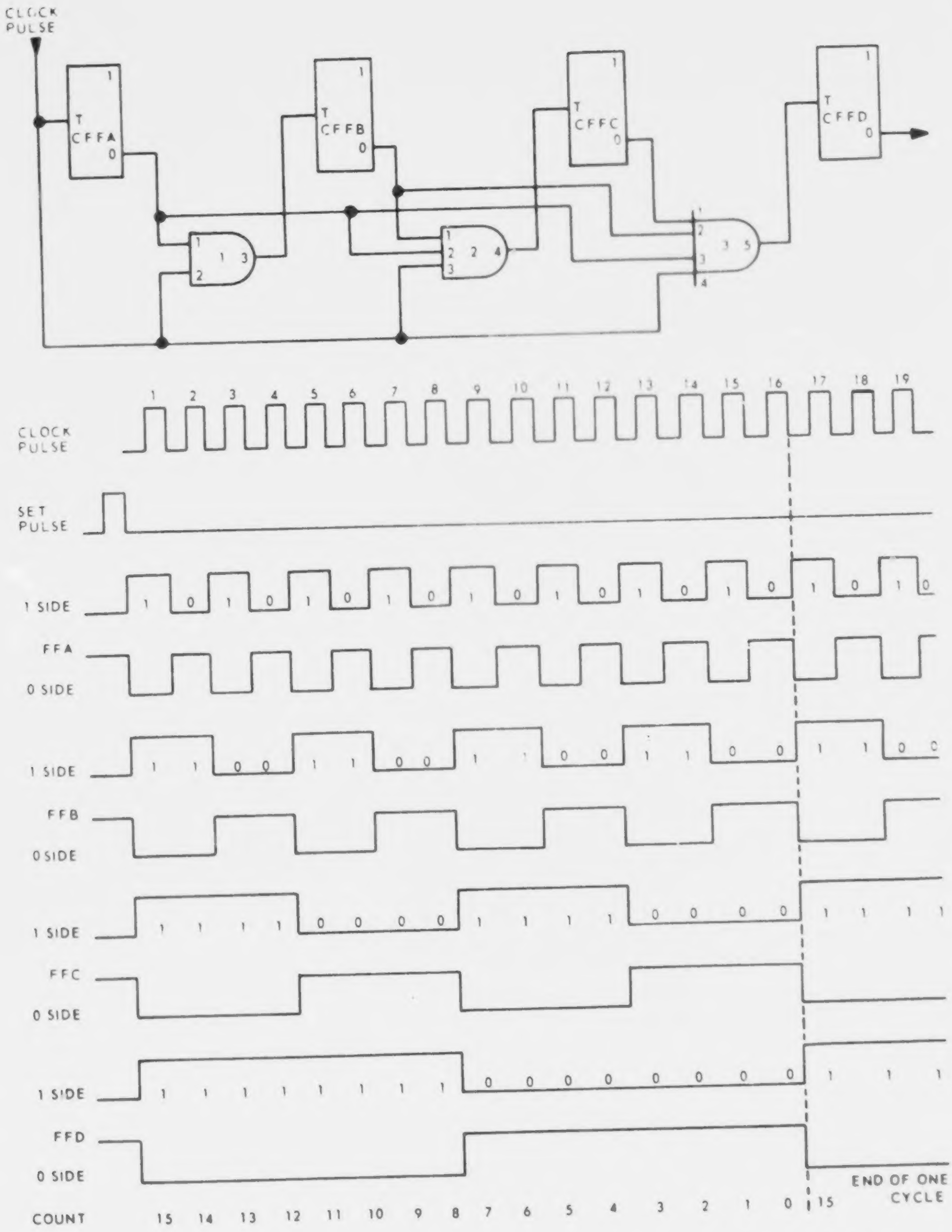

CLOCK PULSE
T
CFFA
CFFB
CFFC
CFFD
1
0
1
2
3
4
5
SET PULSE
1 SIDE
FFA
0 SIDE
FFB
FFC
FFD
COUNT
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
END OF ONE CYCLE
RDA26-369

Figure 1-19. Parallel-down counter.

flip-flop (except the LSD) is triggered by the preceding flip-flop and that, in the parallel counter, all flip-flops are triggered by the clock pulses at certain intervals. The SET pulse shown in the waveforms, although not shown on the logic diagram, is connected to the SET input of all flip-flops.

After the SET pulse is applied, the counter will contain a count of $1111_{(2)}$ or $15_{(10)}$. On the downclock of CP-1, FF-A will CLEAR. Look at the waveshapes and note that, since the flip-flops are triggered by a downclock, CP-1 cannot affect FF-B because of the binary 0 applied to pin 1 of AND-gate 1 for the duration of CP-1. So after CP-1, the count in the counter is $1110_{(2)}$ or $14_{(10)}$.

When CP-2 is applied, FF-A will be SET. FF-B will CLEAR because pin 1 of AND-gate 1 will be activated by the binary 1 from the ZERO side of FF-A and pin 2 will be activated by CP-2. The count in the counter after CP-2 is $1101_{(2)}$ or $13_{(10)}$.

Using the logic diagram and waveshapes in figure 1-19, work the counter through one complete cycle. This counter has a maximum count of $15_{(10)}$ or a modulus of 16.

Counter Characteristics. This section pertains entirely to the counters you have studied previously and will *not* apply to the modified counters you will learn later.

Observe the waveshapes in figure 1-19. Notice that the output pulse width (PW) of each stage becomes longer than the one before it. As an example, it takes two complete clock pulses to produce one cycle output from FF-A. So we can say that the pulse repetition time (PRT) of the output is twice as long as the input PRT. If we assume that the clock pulses have a PW of 1 microsecond and a PRT of 2 microseconds, the output from FF-A would have a PW of 2 microseconds, and a PRT of 4 microseconds. From this, we can say that the output PW is equal to the input PRT, or that the output PRT is twice the input PRT. Notice that this is true for each stage of the counter.

Using the same times as in the above paragraph, we can use the formula $\text{PRF} = \frac{1}{\text{PRT}}$ and determine the frequency of both the input and output waveshapes of FF-A. For the input clock pulses, the frequency would be: $\text{PRF} = \frac{1}{\text{PRT}} = \frac{1}{2}\ \mu\text{sec} = 500$ kHz. For the output, the frequency would be: $\text{PRF} = \frac{1}{\text{PRT}} = \frac{1}{4}\ \mu\text{sec} = 250$ kHz.

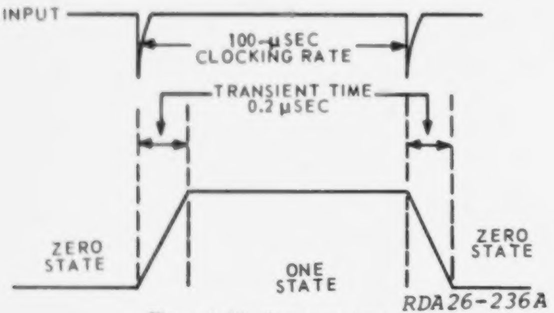


Figure 1-20. Transient time.

Thus, we can say that the output PRF is equal to one-half of the input PRF. This is also true for each of the other stages. If you continue to calculate, you will find that the output of the last stage has a PRF of 31.25 kHz with a PRT of 32 microseconds.

The time that it takes a flip-flop to switch from one state to the other (CLEAR to SET or SET to CLEAR) is called transient time. Figure 1-20 shows the output waveshape of a flip-flop with a 0.2-microsecond transient time. The time between input clock pulses is the clocking rate of the flip-flop. So the clocking rate of the flip-flop in figure 1-20 is 100 microseconds.

If the input PRT is reduced to 50 microseconds, the clocking rate of the flip-flop would also be 50 microseconds. If the input PRT is reduced to a point where the clocking rate is less (in time) than the transient time of the flip-flop, all of the input pulses could not be counted because the flip-flop could not change from one state to the other before the next clock pulse arrived. This would result in an inaccurate count. Therefore, the maximum clocking frequency is determined by the transient time of the flip-flops used in the counter.

In a parallel counter, the transient time used to make clock frequency calculations must be that of the slowest flip-flop because all flip-flops are triggered by the same clock pulse. As an example, if a four-stage parallel counter has three flip-flops with transient times of 0.1 microsecond and one flip-flop with a transient time of 0.2 microsecond, 0.2 microsecond must be used to compute the maximum clock frequency:

$$\text{PRF} = \frac{1}{\text{PRT}} = \frac{1}{0.2\ \mu\text{sec}} = 5\text{ MHz}$$

In a serial counter, only the LSD flip-flop is triggered by the clock pulse. All other flip-flops are triggered by the preceding flip-flop. Therefore, the transient times of *all* flip-flops of a serial counter must be considered when figuring the maximum clock frequency. If we use the same transient times which we used in the paragraph above, the total transient time for a serial counter would be 0.5 microsecond. The maximum clock frequency would then be:

$$\text{PRF} = \frac{1}{\text{PRT}} = \frac{1}{0.5\ \mu\text{sec}} = 2\text{ MHz}$$

From the above examples, you can see that a parallel counter is faster than a serial counter when the same flip-flops are used for both. However, you will also notice from the logic diagrams that the serial counter does not require the AND-gates that the parallel counter does. This means less circuitry is required to a serial counter.

Exercises (008):

1. In which counter can the clock pulse be fed to all stages at the same time?

2. What is an advantage of a parallel counter over a serial counter?

3. Which way will a parallel counter count, up or down?

4. Which requires more circuitry, a parallel counter or a serial counter?

5. What state must all flip-flops be in to cause any flip-flop of a parallel up-counter to change states?

6. What is the maximum value the counter in figure 1-21 can contain?

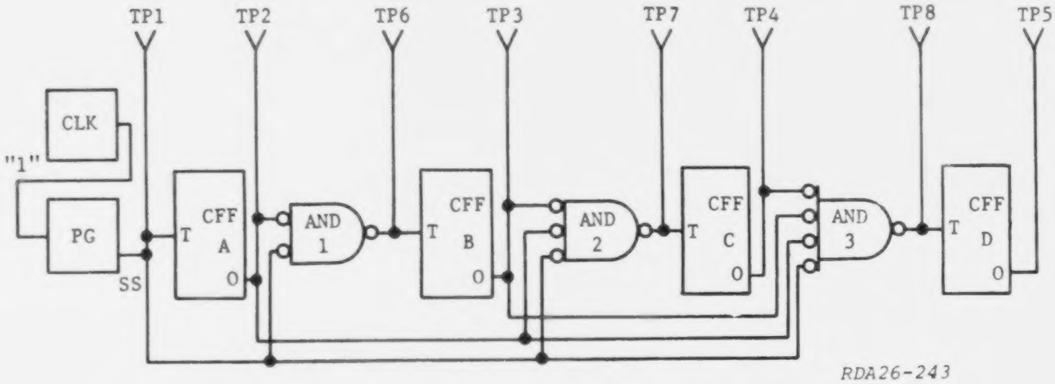


Figure 1-21. Counter (objective 008, exercises 6-9).

7. If the counter of figure 1-21 is set to a count of 12 (10), how many pulses will it take for the counter to reach a count of 0?

8. What identifies the counter of figure 1-21 as a parallel counter?

9. What identifies the counter of figure 1-21 as a down-counter?

009. Specify the operational characteristics of up-down counters.

In the preceding pages, you have studied serial and parallel counters. For the remainder of this section, you will be studying some special counters. The ones we will discuss are the up-down or reversible counter, the ring counter, and the modulus 10 and modulus 12 counters.

Up-Down Counter. The first of the special counters we will talk about is the up-down counter (sometimes referred to as a reversible counter). We will look only at the positive logic counters because, as you know, the only difference in negative logic and positive logic is the logic levels.

The up-down counter will, as the name implies, count either up or down. The way it will count depends on the state (SET or CLEAR) of the "control" flip-flop. When the control flip-flop is SET, the counter will count up. When the control flip-flop is CLEAR, the counter will count down. Figure 1-22 is the logic diagram of a serial up-down counter. We will assume that the control flip-flop is SET and that the counter contains a count of zero before the application of the first clock pulse. With the control flip-flop SET, a binary 1 is placed on one leg of AND-gates 1 and 3, activating (or satisfying) these legs. One leg of AND-gates 2 and 4 will be deactivated (not satisfied) by the binary 0 from the ZERO-side of the control flip-flop.

When the first clock pulse (CP-1) is applied, FF-A will SET. AND-gate 1 will now have a binary 1 (high output which will give a high output from OR-gate 1). Since the flip-flops are triggered on the downclock, FF-B is not SET by the binary 1 from OR-gate 1. So after CP-1, the count in the counter is $001_{(2)}$. When CP-2 is applied, FF-A will CLEAR. This will produce a downclock (transition from binary 1 to binary 0) at the output of OR-gate 1. This downclock will SET FF-B. At the end of CP-2, the count in the counter is $010_{(2)}$. As other clock pulses are applied, the counter will continue to function as a serial up-counter. Follow the waveshapes and work the counter through CP-8.

If the counter is to count down, the control flip-flop must be cleared. The binary 1 from the ZERO-side will enable one leg of AND-gates 2 and 4, and the binary 0 from the ONE-side will inhibit AND-gates 1 and 3. The counter will now function as a serial down-counter.

Up-down counters may also be connected for parallel operation, as shown in figure 1-23. This counter, like other parallel counters, is faster than the serial counter

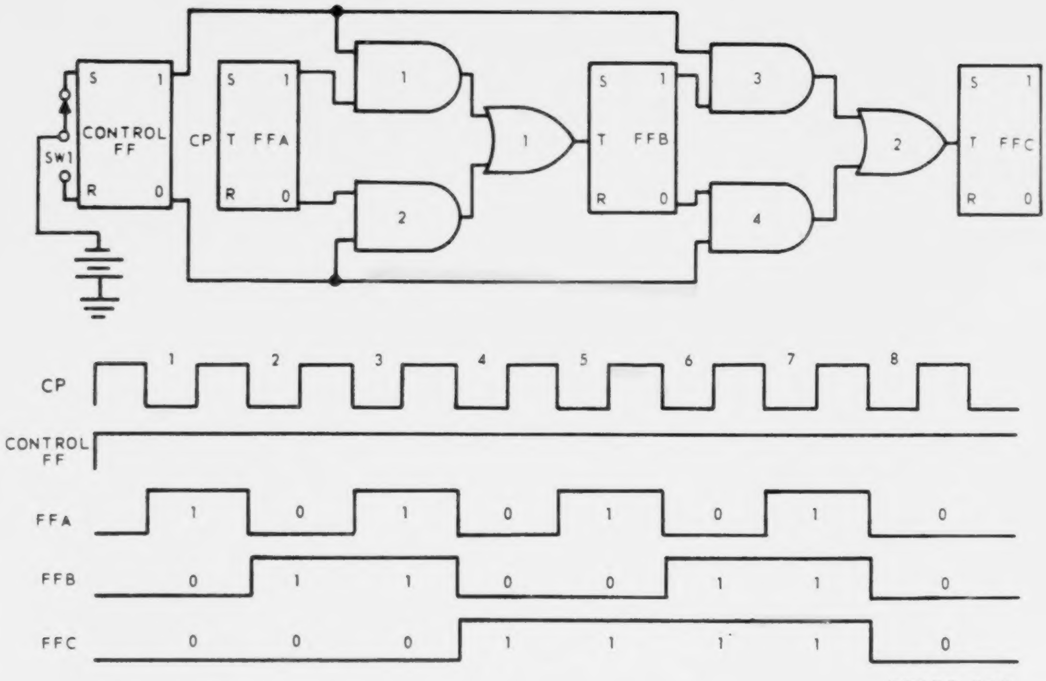

S 1
CONTROL FF
R 0
SW1
CP
S 1
T FFA
R 0
1
2
1
S 1
T FFB
R 0
3
4
2
S 1
T FFC
R 0
CP
1
2
3
4
5
6
7
8
CONTROL FF
FFA
1 0 1 0 1 0 1 0
FFB
0 1 1 0 0 1 1 0
FFC
0 0 0 1 1 1 1 0

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Figure 1-22. Serial up-down counter.

just discussed but requires more circuitry than the serial counter. It will function as a parallel up-counter or parallel down-counter, depending on the state of the control flip-flop.

Exercises (009):

1. What type of counter requires a control flip-flop and what is its function?

2. What must be done to the circuit in figure 1-24 to change the count direction?

3. Assume that the counter in figure 1-24 is cleared before the application of the first clock pulse and SW1 is in the SET position. What state will FF-A be in after the second clock pulse is applied?

010. State the basic operating characteristics of a ring counter and determine the count stored after a given number of clock pulses.

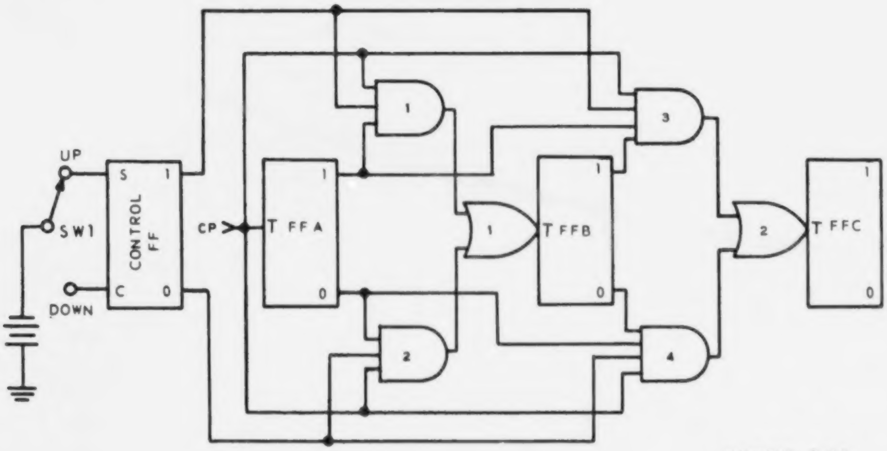
UP
SW1
DOWN
S 1
CONTROL FF
C 0
CP
T FFA
1
0
1
2
1
T FFB
1
0
3
4
2
T FFC
1
0

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Figure 1-23. Parallel up-down counter.

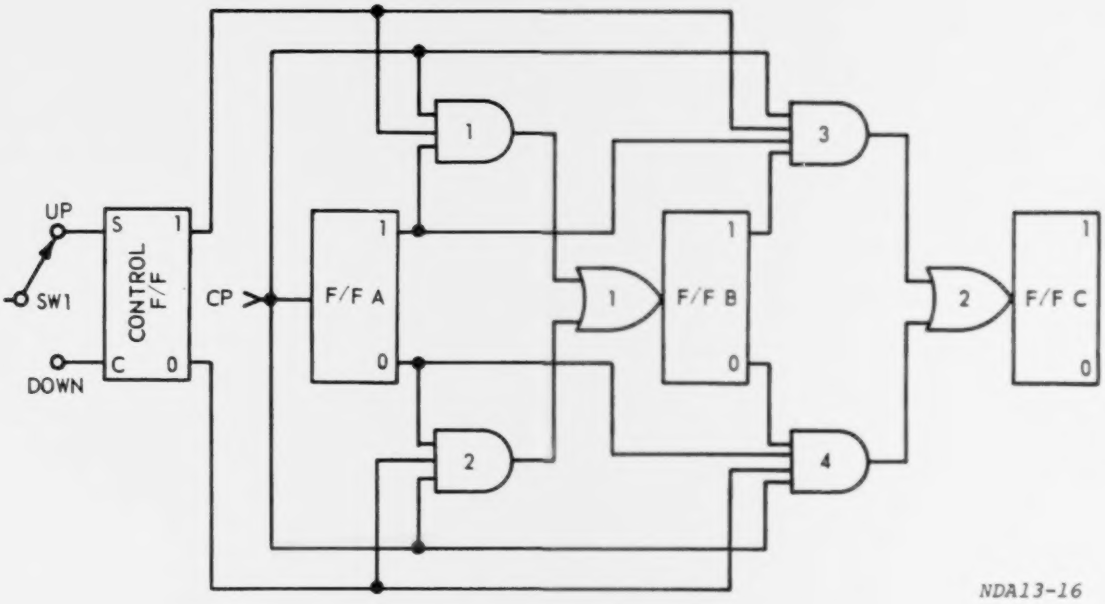


Figure 1-24. Circuit (objective 009, exercises 2 and 3).

Ring Counters. A type of counter in which only one stage of the counter is in the ONE state at any time is called a ring counter. This type of counter does not provide an output that is identifiable as a particular code, such as is provided by a binary counter or a gray counter. Instead, a ring counter provides a "one-shot" indication. That is, only one output line from the counter is energized at any one time.

Figure 1-25 shows a simple ring counter. It is designed in the form of a closed ring; that is, FF-D, the last stage, feeds back to the input stage to automatically start the count over. Not all ring counters function in this manner. Some ring counters count from a preset point and must be reset before starting over again.

Assume that FF-D is in the ONE state; thus, its output is high, indicating that four pulses have been counted. The next pulse, number 1 on the start of a new count, passes through AND-gate 4 and sets FF-A to the ONE stage and FF-D to the ZERO state. Line A is now high, indicating that the counter holds a count of one.

The next clock pulse, CP-2, passes through AND-gate 1 to set FF-A to the ZERO state and FF-B to ONE state. Line B is now high, indicating that the counter holds a count of two. The next clock pulse, CP-3, passes through AND-gate 2 to set FF-B to the ZERO state and FF-C to the ONE state. Line C is now high, indicating that the counter holds a count of three. The next clock pulse, CP-4, passes through AND-gate 3 to set FF-C to the ZERO state and FF-D to the ONE state. Line D is now high, indicating that the counter holds a count of four.

The counter has now progressed through a complete cycle. Only one stage was in the ONE state at any one time. This four-stage counter has the capability of counting only four pulses. Thus, the counter stages do not

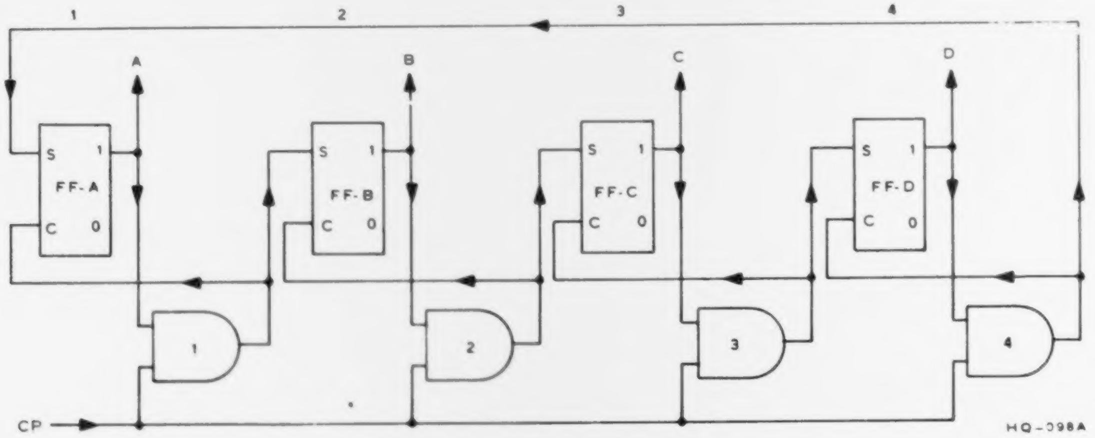


Figure 1-25. Closed ring counter.

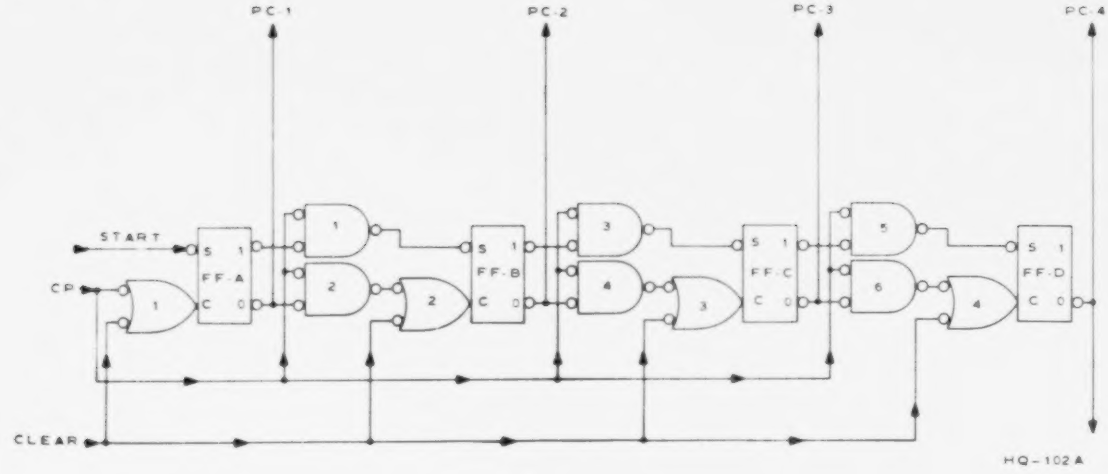


Figure 1-26. Ring counter.

represent the place position of any number system; instead, each stage represents a number.

Figure 1-26 shows another ring counter. The counter uses negative logic and the flip-flop trigger on the downclock. The control line output from each counter is taken from the ZERO side of the flip-flop; therefore, the output is high when the flip-flop is in the ONE state.

Notice that this counter is not a closed ring. It must be cleared of its count before another counting cycle can be started. The counter is cleared by a CLEAR pulse that passes through OR-gates 1 through 4 of the CLEAR sides of all flip-flops, setting them to the ZERO state.

The counter is started in its counting cycle by a start pulse that sets FF-A to the ONE state. This causes the ZERO-side output of the flip-flop to go HIGH and to indicate that the first step in the program is to take place.

The first clock pulse after the start pulse passes through AND-gate 1 to the SET input of FF-B, setting it to the ONE state. At the same time, the pulse passes through OR-gate 1, clearing FF-4 (setting it to the ZERO state). The ZERO-side of FF-B is now high, indicating that the counter holds program count 2 (PC-2). The next clock pulse passes through AND-gate 3 to SET FF-C (set it to the ONE state), and through AND-gate 1 to CLEAR FF-B (set it to the ZERO state). PC-3 is now high. The next clock pulse passes through AND-gate 5 to set FF-D and through AND-gate 4 to CLEAR FF-C. PC-4 is now high.

The next clock pulse passes through AND-gate 6 to CLEAR FF-D. The counter is now reset to ZERO, and the clear inputs are really not needed for this simplified version of the counter. However, in the 33-stage counter from which this example was obtained, the CLEAR inputs are needed. A program for this equipment may have any number of steps up to 33. When the program has less than 33 steps, one stage in the counter is left in the ONE state at the end of the program. For that reason, the counter must be cleared before another program count is started.

Exercises (010):

1. What is the name of the counter that will have only one stage in the ONE state at any one time?

2. How does a closed-ring counter work?

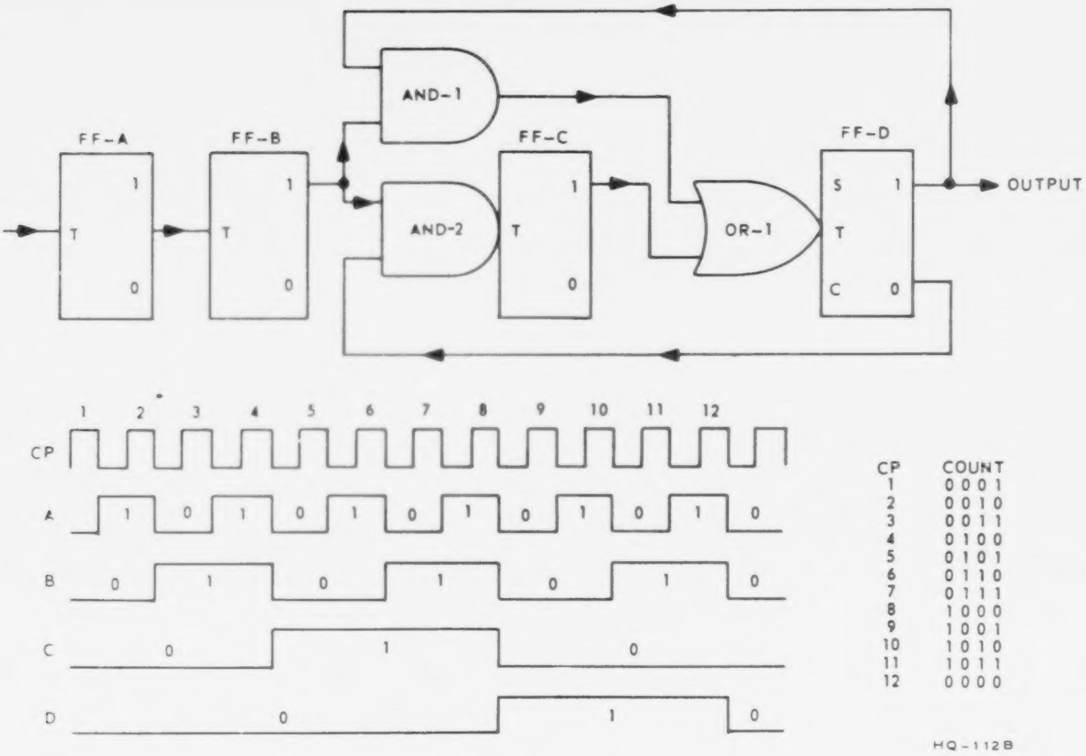
3. What count is stored in a four-stage ring counter after three clock pulses (see fig. 1-26)?

011. State how a mod-12 counter operates.

Mod-12 Counter. As pointed out earlier, binary counters that are modified to have a modulus—that is, not a power of 2—are called *modulus counters*, or are simply referred to as mod counters. Figure 1-27 shows a four-stage binary counter modified to recycle after a count of 12; hence, it is a mod-12 counter.

The counter shown in figure 1-27 is a four-stage serial-up counter. It has been modified to block FF-C from receiving counts after the count of 8. Since this flip-flop represents $2^2 = 4$, disabling it removes four counts from the maximum count capability of the counter. A four-stage binary counter has a modulus of $2^4 = 16$; thus, this modified counter has a modulus of $16 - 4 = 12$. It is, therefore, a mod-12 counter.

AND-gate 2 is the blocking gate. AND-gate 1 permits FF-C to be bypassed when it is no longer functioning as a counter stage. Until the count of 8 is counted, FF-D is in the ZERO state and its ZERO output conditions one leg of AND-gate 2; thus, all downclocks from FF-B are permitted to pass through the gate and trigger FF-C. Also, up to the count of 8, the ONE-side of FF-D is low; thus, it



CP	COUNT
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0
11	1 0 1 1
12	0 0 0 0

Figure 1-27. Mod-12 counter (count blocking).

keeps AND-gate 1 inhibited. From the waveforms and the table shown in figure 1-27, you can see that the counter functions as a normal serial-up counter up to 8. Count 8 sets FF-D to the ONE state, inhibiting AND-gate 2, and conditioning AND-gate 1. FF-C is now blocked and cannot count. FF-A and FF-B change state to provide the counts of 9, 10, and 11. Upon receipt of count 12, FF-A downclocks, triggering FF-B to the ZERO state. The downclock from FF-B passes through AND-gate 1 and triggers FF-D to the ZERO state. Thus, the counter is reset to 0 0 0 0 upon the receipt of the 12th pulse. The downclock from the ONE side of FF-D is fed to other circuits to indicate that 12 counts have been counted.

Another method of modifying a binary counter for a modulus of 12 is shown in figure 1-28. Instead of blocking four counts, this counter adds four counts. Notice that the counter counts seven pulses exactly like a serial-up counter. At the count of 7, it holds the binary configuration 0 1 1 1. When the eighth pulse arrives, the counter jumps to the 1 1 0 0 configuration, which is equal to decimal 12. Thus, only four more pulses are required to reset the counter to ZERO.

At the count of 8, the following actions take place:

a. FF-A flips to the ZERO state, sending a downclock to FF-B.

b. FF-B flips to the ZERO state, sending a downclock to FF-C.

c. FF-C flips to the ZERO state, sending a downclock to FF-D.

d. FF-D flips to the ONE state, sending a downclock from its ZERO side to the SET input of FF-C. This sets FF-C to the ONE state.

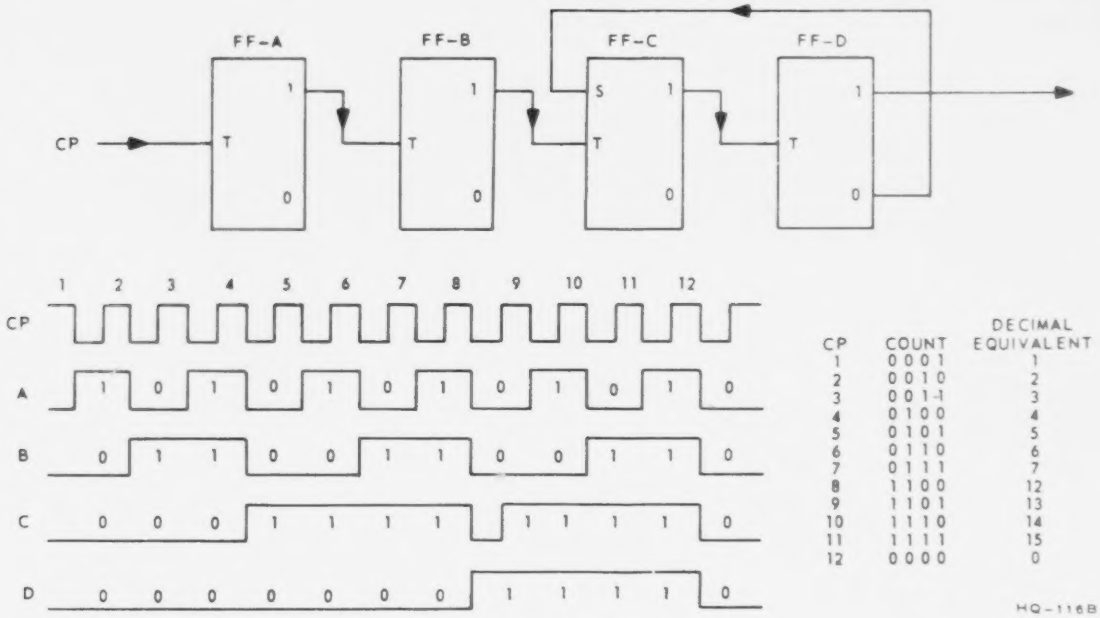
From this, you can see that the counter actually reaches the count of 8 momentarily; but before another CP can arrive, the counter is set to a count of 12. Thus, count 9 becomes 13; count 10, 14; count 11, 15; and count 12 resets the counter to ZERO. When the counter resets to ZERO, the ONE-side output of FF-D down clocks. This downclock is fed to other circuits to indicate that 12 counts have been counted.

Exercises (011):

1. How does the mod-12 counter in figure 1-27 block the count?

2. Referring to question 1, what is the result of this blocking?

3. What is meant by count adding as compared to count blocking?



CP	COUNT	DECIMAL EQUIVALENT
1	0 0 0 1	1
2	0 0 1 0	2
3	0 0 1 1	3
4	0 1 0 0	4
5	0 1 0 1	5
6	0 1 1 0	6
7	0 1 1 1	7
8	1 1 0 0	12
9	1 1 0 1	13
10	1 1 1 0	14
11	1 1 1 1	15
12	0 0 0 0	0

Figure 1-28. Mod-12 counter (count adding).

4. Describe how the count adding actually takes place.

5. On both types of mod-12 counters, what does flip-flop status 0 0 0 0 represent?

012. State how a four-stage serial-up counter can be modified to become a mod-10 counter and, given pulse counts, specify the stored count.

Mod-10 Counter. A mod-10 counter is normally called a decimal counter, since it counts to 9 and resets on the 10th count. The method of developing a mod-10 counter is the same as that described for a mod-12 counter. In the mod-10 counter, either six counts must be blocked or six counts must be added. This is true because a four-stage counter has a modulus of 16, and to modify it to have a count of 10, six counts (16 − 10) must be added or subtracted.

Figure 1-29 shows a simple mod-10 counter using the pulse-blocking method. In this counter, FF-B and FF-C are blocked from receiving counts after the count of 8 is reached. Since FF-B = 2^1 and FF-C = 2^2, the number of counts blocked is the desired six.

This counter is drawn in negative logic. Before discussing how it counts, let us establish several pertinent facts about the circuit operation.

a. The counter flip-flops trigger on the downclock of the applied pulse.

b. A low voltage represents a ONE; a high voltage represents a ZERO. Therefore, when a flip-flop switches to the ONE state, the voltage from the ONE side down clocks, and the voltage from the ZERO side up clocks. Conversely, when a flip-flop switches to the ZERO state, the voltage from the ONE side up clocks and the voltage from the ZERO side down clocks.

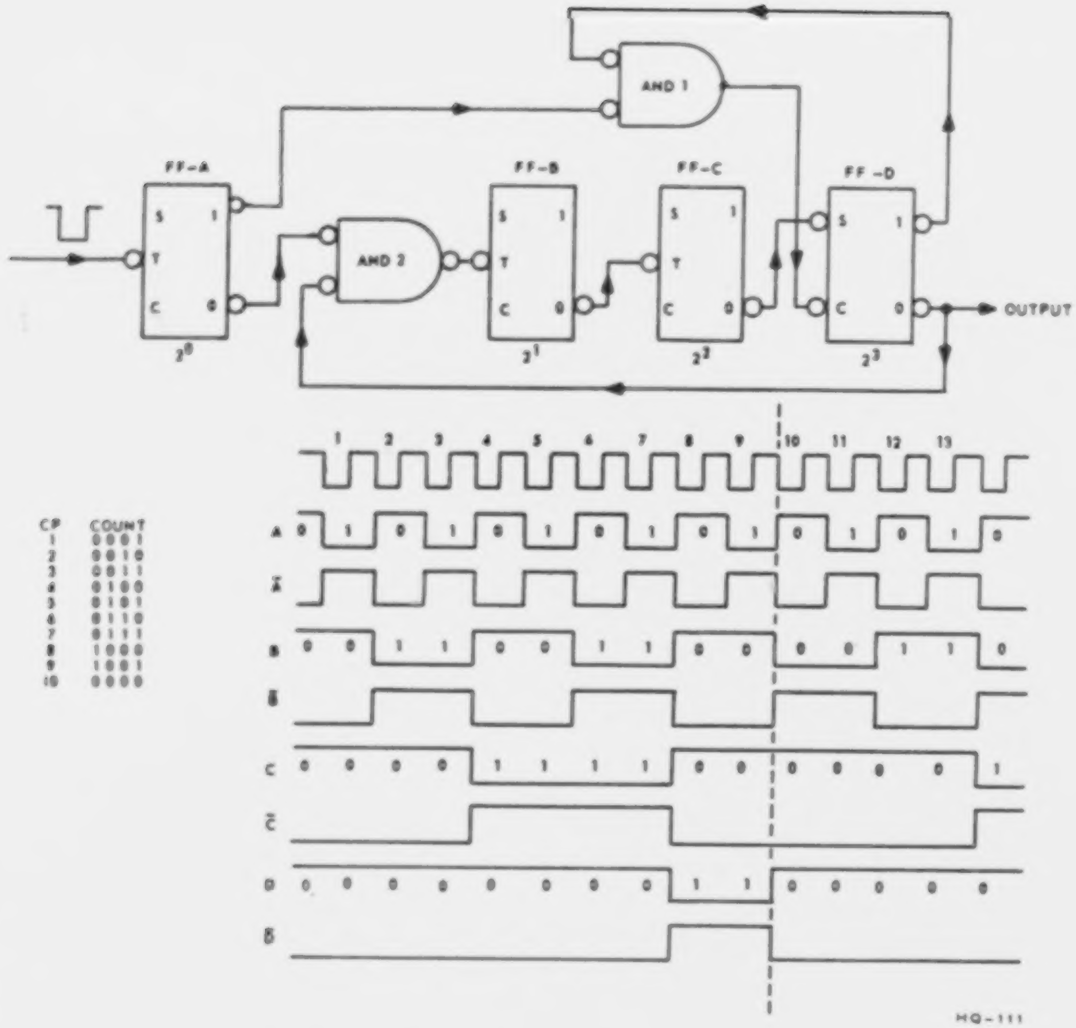
c. To make this circuit function as an up-counter, the trigger for each flip-flop is obtained from the ZERO side of the preceeding flip-flop.

To clarify these facts, the waveforms for both outputs of each stage are shown.

AND-gate 2 is the blocking gate. It passes the trigger pulses from FF-A as long as FF-D remains in the ZERO state; however, when FF-D goes to the ONE state (at the count of 8), the gate is deconditioned and both FF-B and FF-C are blocked from further counting. AND-gate 1 is a bypass gate that enables FF-B and FF-C to be bypassed when they are disabled by AND-gate 2.

The counter counts the first seven pulses as a simple serial-up counter. The eighth count sets FF-D to the ONE state, inhibiting AND-gate 2 and conditioning AND-gate 1. FF-B and FF-C are now blocked and cannot count. FF-A changes state to provide the count of 9—1 0 0 1. Upon receipt of the 10th pulse, FF-A is triggered to the ZERO state. The downclock from FF-A passes through AND-gate 1 and triggers FF-D to the ZERO state. Since FF-B and FF-C were set to the ZERO state at the count of 8 and were prevented from further counting, all counter flip-flops are now in the ZERO state. Therefore, the counter is a mod-10 counter.

Another method of modifying a binary counter for a modulus of 10 is shown in figure 1-30. Instead of blocking six counts, this counter adds six counts. Notice that the counter counts seven pulses, exactly like a serial-up counter. At the count of 7, it holds the binary



CP	COUNT
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	0 0 0 0

Figure 1-29. Mod-10 counter (count blocking).

configuration 0 1 1 1. When the eighth pulse arrives, the counter jumps to the 1 1 1 0 configuration, which is equal to decimal 14. Thus, only two more pulses are required to reset the counter to ZERO.

When the eighth pulse arrives, the following actions take place:

a. FF-A flips to the ZERO state, thus applying a downclock to FF-B.

b. FF-B flips to the ZERO state, thus applying a downclock to FF-C.

c. FF-C flips to the ZERO state, thus applying a downclock to FF-D.

d. FF-D flips to the ONE state, thus applying a downclock from its ONE side output to the SET sides of FF-B and FF-C.

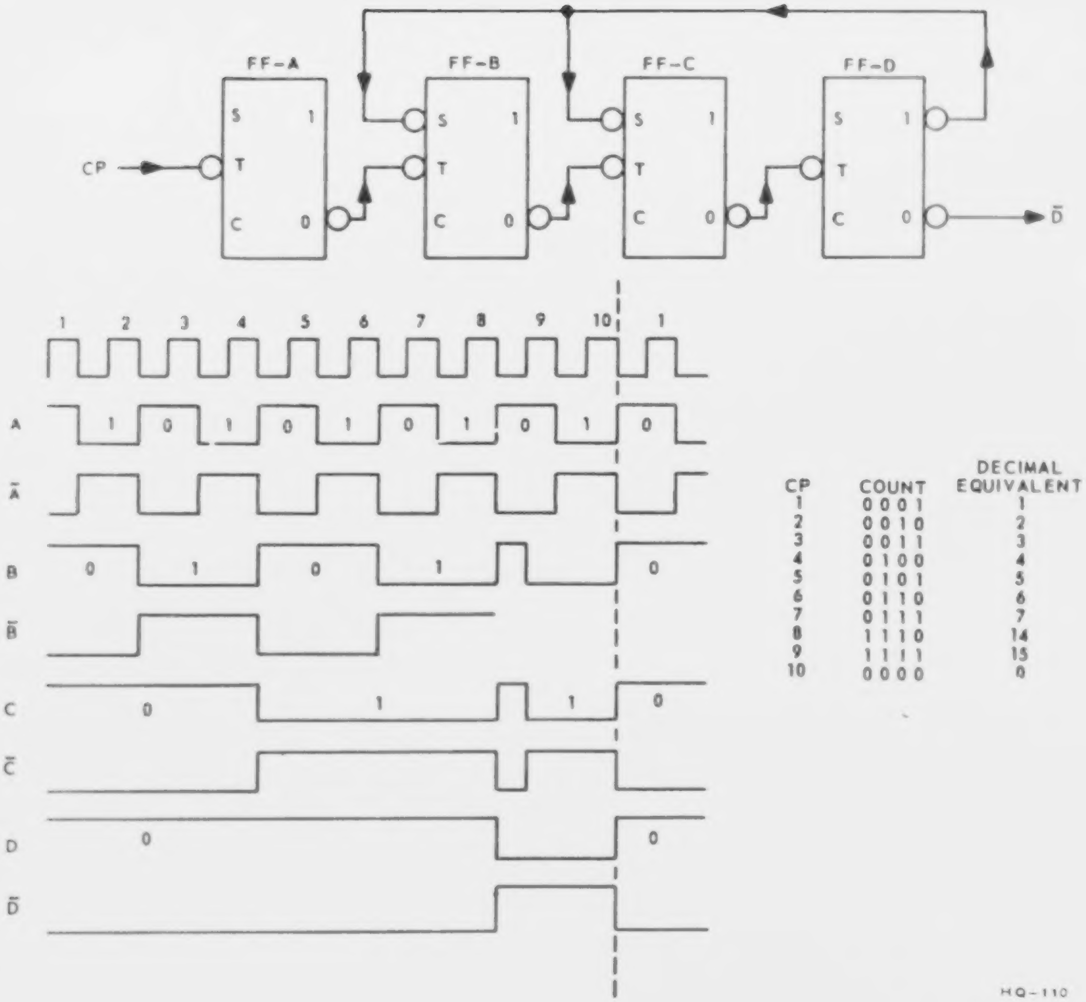
e. FF-B and FF-C flip to the ONE state. Thus, the counter holds the configuration of 1 1 1 0, which represents 14.

The ninth pulse sets FF-A to the ONE state. All stages of the counter hold ONEs. The count is 15. The 10th pulse sets all flip-flops to the ZERO state, thus ending one counting cycle.

Exercises (012):

1. Which of the modified counters is referred to as a decimal counter?

2. How can a four-stage serial-up counter be modified to become a mod-10 counter?



CP	COUNT	DECIMAL EQUIVALENT
1	0 0 0 1	1
2	0 0 1 0	2
3	0 0 1 1	3
4	0 1 0 0	4
5	0 1 0 1	5
6	0 1 1 0	6
7	0 1 1 1	7
8	1 1 1 0	14
9	1 1 1 1	15
10	0 0 0 0	0

Figure 1-30. Mod-10 counter (count adding).

3. When the ninth clock pulse is applied to a mod-10 count blocking counter, what count is stored?

4. When the eighth clock pulse is applied to a mod-10 count adding counter, what count is stored?

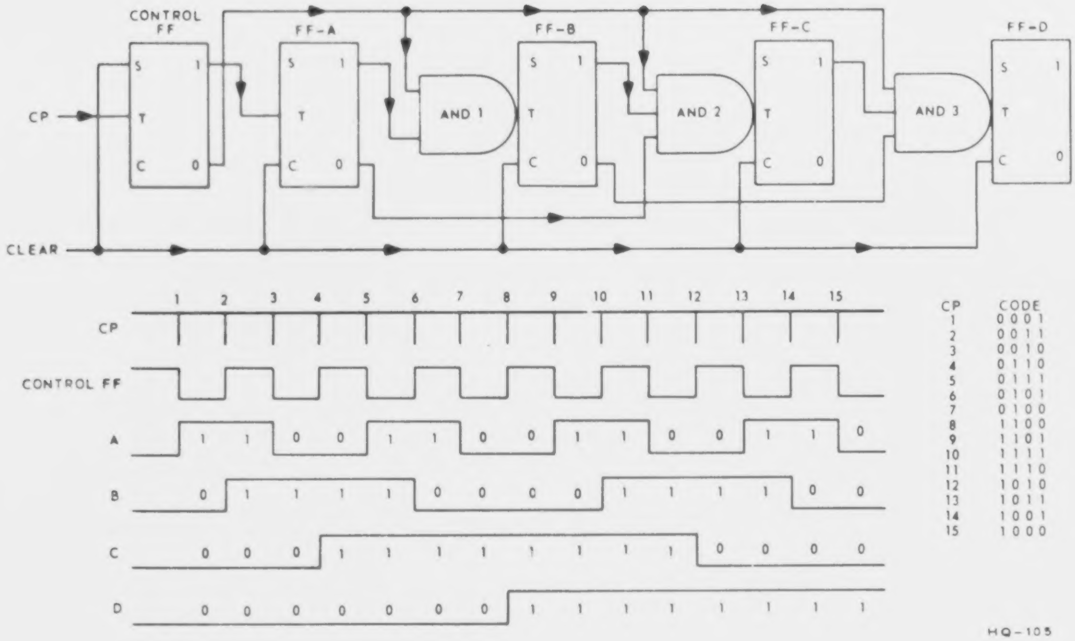
013. Specify operational characteristics of gray counters.

Gray Counters. The gray counter counts pulses and provides outputs that are coded in gray code.

Figure 1-31 shows a gray counter, its associated waveforms, and a count table. Look at the table and at each column of the code. Notice the pattern followed by each flip-flop. The right-hand column represents the pattern followed by FF-A. Notice that FF-A goes to the ONE state on the first count and stays in that state for two counts. Then it goes to the ZERO state for two counts, then to the ONE state for two counts, and continues to repeat the pattern for as many counts as the counter holds. Let us look at FF-A and see how it is designed to follow this pattern.

FF-A changes state each time a downclock is received from the control flip-flop. The control flip-flop is initially set to the ONE state by a clear pulse. Therefore, the first CP triggers it to the ZERO state, and it down clocks, triggering FF-A to the ONE state. By this means, FF-A is set to the count of 1 by the first CP.

In order to make FF-A change state every two counts, the basic clocking signal (CP) is fed to the control flip-flop, and that flip-flop develops the clocking signal for FF-A. Since a flip-flop divides by two, the control flip-flop triggers FF-A every two pulses. By this means, FF-A is forced to follow the pattern indicated by the least significant column of the code table.


CONTROL FF
FF-A
FF-B
FF-C
FF-D
S
T
C
1
0
AND 1
AND 2
AND 3
CP
CLEAR
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
CONTROL FF
A
B
C
D
HQ-105

CP	CODE
1	0 0 0 1
2	0 0 1 1
3	0 0 1 0
4	0 1 1 0
5	0 1 1 1
6	0 1 0 1
7	0 1 0 0
8	1 1 0 0
9	1 1 0 1
10	1 1 1 1
11	1 1 1 0
12	1 0 1 0
13	1 0 1 1
14	1 0 0 1
15	1 0 0 0

Figure 1-31. Basic gray counter.

Now, look at the next column to the left. It represents the pattern for FF-B. Notice that FF-B goes to the ONE state on the second count and remains in that state for four counts. Then it goes to the ZERO state for four counts, then to the ONE state for four counts, and continues to repeat this pattern. Let us see how this flip-flop is designed to follow this pattern.

FF-B cannot change state until FF-A is in the ONE state. Therefore, it cannot be set to the ONE state until the first pulse has been counted by FF-A. Since FF-B is clocked by the ZERO-side output of the control flip-flop, it cannot change state at the same time FF-A changes state. Look at the timing waveform. Notice that FF-B changes state in the center of FF-A's positive-going waveform.

Now, look at the next column to the left. This represents the pattern followed by FF-C. Notice that FF-C goes to the ONE state at the count of 4 and remains in the ONE state for eight counts. Then, it goes to the ZERO state for eight counts and continues to repeat this pattern.

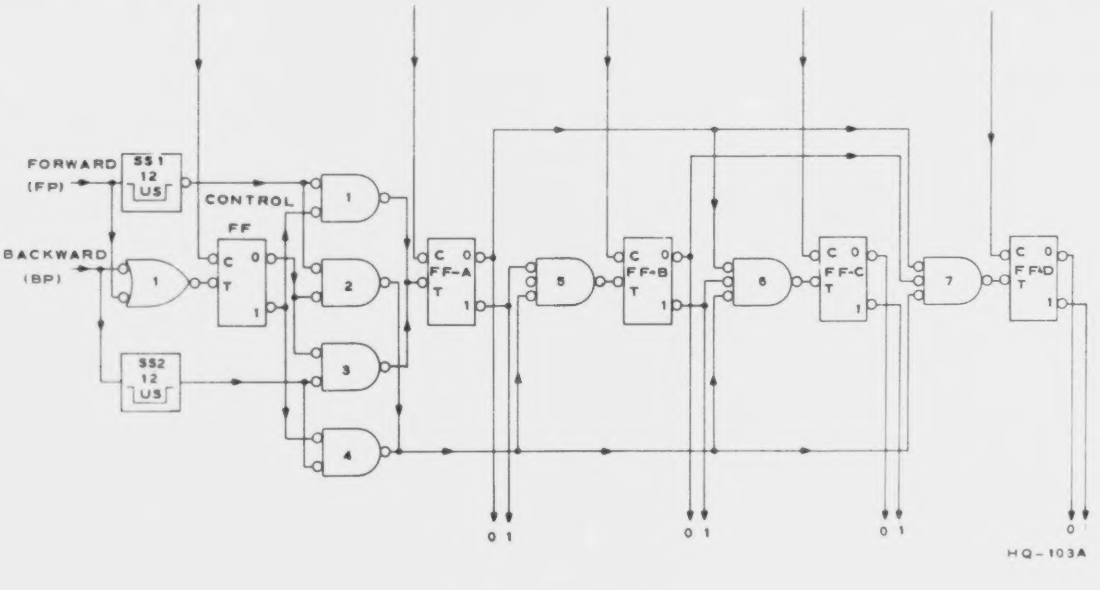

FORWARD
(FP)
SS1
12
US
BACKWARD
(BP)
CONTROL
FF
C
T
0
1
SS2
12
US
1
2
3
4
5
6
7
FF-A
FF-B
FF-C
FF-D
0 1
0 1
0 1
0 1
HQ-103A

Figure 1-32. Gray counter.

Let us see how this flip-flop is designed to follow this pattern.

FF-C cannot change state until FF-A is in the ZERO state and FF-B is in the ONE state; thus, AND-gate 2 does not permit a clock pulse (from the control flip-flop) to pass through until the count of 3. At the count of 3, the pulse from the ZERO side of the control flip-flop is upclocking. At the count of 4, the conditions to the AND-gate do not change, but the pulse from the control flip-flop is a downclock and FF-C is set to the ONE state.

The condition that satisfies AND-gate 2 occurs every eight counts; therefore, FF-C changes state every eight counts. Look at the timing waveform. FF-C changes state in the center of FF-B's positive-going waveform. FF-C cannot change state at the same time either FF-B or FF-A changes state.

You should be able to figure out FF-D's pattern and see how that pattern is accomplished by the counter. Look at the waveforms; notice that only one stage of the counter changes state from one count to the next.

Now that you understand the basic principles of a gray counter, look at the more complicated gray counter in figure 1-32. It counts in gray code and has the ability to count both forward and backward. The counter has this capability because it is used with an input keyboard to sequentially address a core memory. Each time a key is depressed on the keyboard, a character is stored in the core memory location selected by the counter, and a forward pulse (FP) is generated to step the counter ahead one count to the next memory address. If the operator depresses the wrong key, the error can be corrected by backspacing. The operator depresses the backspace key, thus generating a backward pulse. The backward pulse steps the counter back one count to reselect the memory location where the erroneous character was stored. By depressing the correct key, the operator destroys the data at that memory location and inserts the correct data. Before proceeding to the operation of this counter, note the following facts:

a. The counter is in negative logic. Thus, a low at the ONE side of a flip-flop indicates that the state holds a ONE.

b. Both the forward pulse (FP) and backward pulse (BP) are 1 millisecond wide and are negative-going.

c. All flip-flops trigger on the downclock.

d. Both single shots trigger on the upclock but produce negative-going pulses.

With these facts in mind, we apply four forward pulses and one backward pulse to the counter to see how it operates. At the start of the operations, the reset pulse clears all the flip-flops. When the operator depresses the key to send the first character of a message, a 1-millisecond negative-going forward pulse is applied to the counter. The downclock of this pulse passes through OR-gate 1, setting the controlling flip-flop to the ONE state. At this time, the character is loaded into the core memory location 0 0 0 0. One millisecond later, the upclock of the forward pulse triggers single-shot 1, causing it to produce a 12-μsec negative-going pulse. This pulse is fed to AND-gates 1 and 2. Since the control flip-flop is in the ONE state, AND-gate 1 is enabled. The pulse passes through AND-gate 1 to set FF-A to the ONE state.

When the second key is depressed, the second forward pulse is applied to the counter. The downclock of the pulse clears the control flip-flop; and after 1 millisecond, the upclock triggers single-shot 1. Since the control flip-flop is in the ZERO state, AND-gate 2 is enabled; and the downclock from the single-shot passes through it and is fed to AND-gates 5, 6, and 7. Since only FF-A is in the ONE state, only AND-gate 5 is enabled. The pulse passes through AND-gate 5 to set FF-B to the ONE state. During the 1-millisecond interval between the arrival of the forward pulse and the setting of the counter to the next count, the character generated by the key is stored in memory location 0 0 0 1, and the counter is now stepped to the next location—0 0 1 1.

The third forward pulse sets the control flip-flop to the ONE state, and the pulse from single-shot 1 passes through AND-gate 1 to clear FF-A. The counter now holds the configuration 0 0 1 0.

The fourth forward pulse clears the control flip-flop, and the pulse from single-shot 1 passes through AND-gate 2. Since AND-gate 6 is enabled (FF-A = ZERO; FF-B = ONE), the pulse sets FF-C to the ONE state. Now the count of 4 is contained in the counter, and it holds the configuration 0 1 1 0.

Assume that the operator punched the fourth key on the keyboard, and hit the wrong key. This character was inserted into memory before the counter stepped to count 4. To correct the character, the counter must be stepped back to count 3. The operator does this by depressing a backspace key which generates a backward pulse.

The backward pulse has the same duration and polarity as the forward pulse. Its downclock switches the control flip-flop to the ONE state. Then the pulse from single-shot 2 arrives at AND-gates 3 and 4; it passes through AND-gate 4 and through AND-gate 6 to set FF-C to the ZERO state. The counter now holds the configuration 0 0 1 0, which in gray code is a 3; thus, the count in the counter has been reduced from 4 to 3.

Exercises (013):

1. With the CP triggering the control FF, how does FF-A change to the ONE state on the first clock pulse?

2. What is required to trigger FF-B?

3. How many clock pulse times will FF-C remain in the ONE state?

4. What is required to trigger FF-D?

5. On figure 1-32, what determines whether a forward pulse triggers FF-A or FF-B, FF-C, and FF-D as required?

6. On figure 1-32, what is required to enable AND-gate 3?

014. Specify operational characteristics of TTL integrated circuit counters.

TTL IC Counter Circuits. Just as flip-flops are found as integrated circuits, you will find complete counters on a single IC chip. As equipment becomes more digital and integrated circuitry is used more extensively, these are the type counters you will encounter. Remember, the operation of digital integrated circuits is basically the same as that of their solid-state counterparts.

The digital integrated counter circuits which are presented in this section are from either the *The TTL Data Book for Design Engineers* (CC-411) or *Supplement to The Data Book for Design Engineers*, (CC-416), published by the Texas Instruments Corporation, Dallas, Texas. Because of the unusually well organized manner of presentation of the material covered, we will not deviate from their format. Both of the books are excellent references when the individual technician might have a question on some new device but is unable to locate the information in the appropriate technical manual.

The following digital integrated counter circuits are only meant to be representative of the available ICs in the field. Space does not permit publication of the full line presently in use.

MSI TTL high-speed decade counter. The type SN7490 counter IC is shown in figures 1-33A and B, along with the applicable truth tables. These decade counters find use in digital computer systems, data-handling systems, and in control systems. They consist of four dual-rank, master-slave flip-flops internally connected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to logical zero or to a binary coded decimal (BCD) count of 9. See figures 1-33A and B for specific count modes of operation.

Synchronous four-bit counter. The types SN54160/SN74160, SN54161/SN74161, SN54162/SN74162, and SN54163/SN74163 counters are shown in figure 1-34A. These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The SN54160, SN54162, SN74160, and SN74162 are decade counters, and the SN54161, SN54163, SN74161, and SN74163 are four-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous counters. By using the timing sequences shown in figure 1-34C, while looking at the logic diagram in figure 1-34B, operation of the internal elements may be logically analyzed.

Synchronous four-bit binary up/down counter with preset inputs. Counter types SN54193 and SN74193 are shown in figures 1-35A, B, and C, along with the operational timing sequence and functional block diagram. Synchronous operation of the counters is provided by having all flip-flops simultaneously clocked so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are associated with asynchronous counters. All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulus-N dividers by simply modifying the count length with the preset inputs.

Exercises (014):

1. What type of counter is the SN7490?

2. How is synchronous operation provided by the SN74163?

3. What is meant by the SN74193 being fully programmable?

4. What characteristic is eliminated by synchronous operation of the four-bit counter?

5. What circuits are contained within a SN7490 TTL IC?

1-3. Registers

Data is processed within a data processing machine in a specific sequence. Although there are variations from machine to machine, the sequence is basically:

a. Bring the raw data in.
b. Store it temporarily.
c. Shift and rearrange it.
d. Perform any mathematical function.
e. Shift and rearrange it again.
f. Send the processed data out.

During this process, the data will be checked one or more times to make sure that it has not gained or lost bits

TTL
MSI

TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93, SN7490A, SN7492A, SN7493A, SN74L90, SN74L93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

BULLETIN NO. DL-S 7211807, DECEMBER 1972

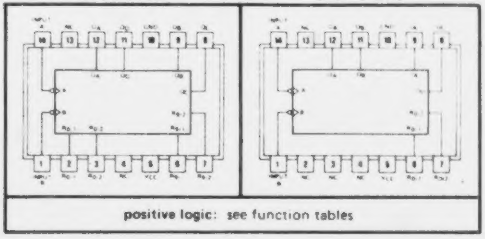
'90A, 'L90 . . . DECADE COUNTERS

'92A . . . DIVIDE-BY-TWELVE COUNTER

'93A, 'L93 . . . 4-BIT BINARY COUNTERS

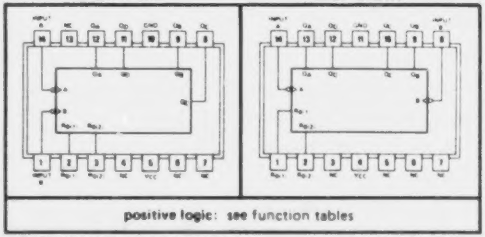
'90A . . . J, N, OR W PACKAGE
'L90 . . . J, N, OR T PACKAGE
(TOP VIEW)

'92A . . . J, N, OR W PACKAGE
(TOP VIEW)


positive logic: see function tables

'93A . . . J, N, OR W PACKAGE
(TOP VIEW)

'L93 . . . J, N, OR T PACKAGE
(TOP VIEW)


positive logic: see function tables

NC—No internal connection

description

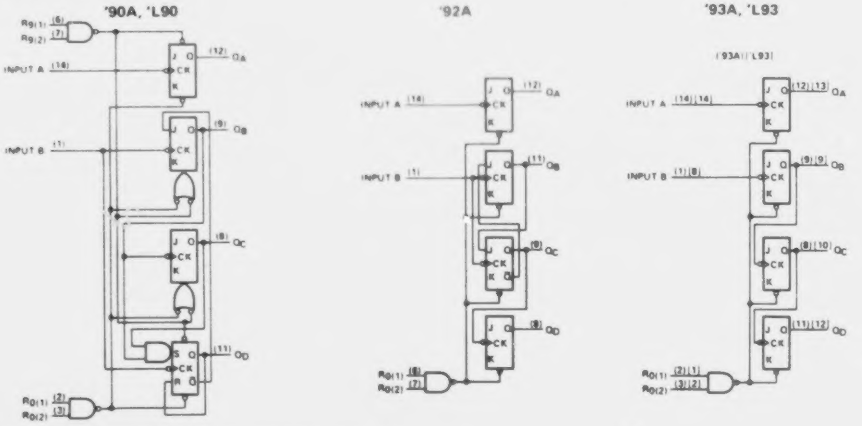
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'L90, divide-by-six for the '92A, and divide-by-eight for the '93A and 'L93.

All of these counters have a gated zero reset and the '90A and 'L90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'L90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'92A, '93A	130 mW
'L93	16 mW

functional block diagrams


'90A, 'L90

'92A

'93A, 'L93

—◇— . . . dynamic input activated by transition from a high level to a low level.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

Figure 1-33A. SN7490 decade counters.

'90A, 'L90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93A, 'L93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

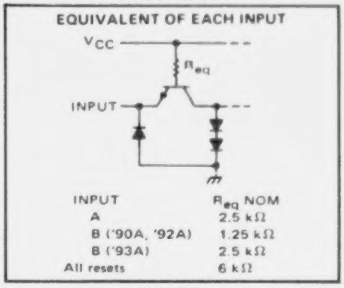
'92A, '93A, 'L93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

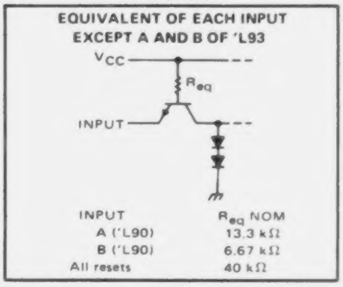
schematics of inputs and outputs

'90A, '92A, '93A


EQUIVALENT OF EACH INPUT
V_{CC}
R_{eq}
INPUT

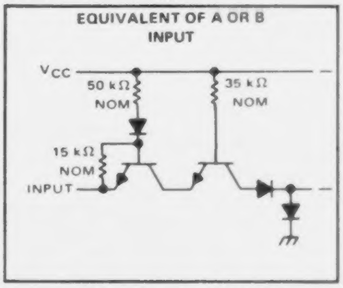
INPUT	R_{eq} NOM
A	2.5 kΩ
B ('90A, '92A)	1.25 kΩ
B ('93A)	2.5 kΩ
All resets	6 kΩ

'L90, 'L93


EQUIVALENT OF EACH INPUT
EXCEPT A AND B OF 'L93
V_{CC}
R_{eq}
INPUT

INPUT	R_{eq} NOM
A ('L90)	13.3 kΩ
B ('L90)	6.67 kΩ
All resets	40 kΩ

'L93


EQUIVALENT OF A OR B
INPUT
V_{CC}
50 kΩ
NOM
35 kΩ
NOM
15 kΩ
NOM
INPUT

'90A, '92A, '93A, 'L90, 'L93

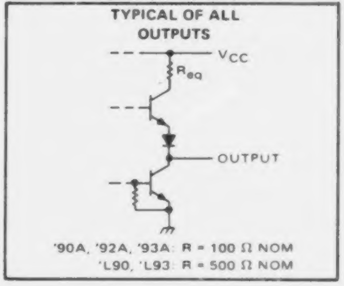

TYPICAL OF ALL
OUTPUTS
V_{CC}
R_{eq}
OUTPUT
'90A, '92A, '93A: R = 100 Ω NOM
'L90, 'L93: R = 500 Ω NOM

Figure 1-33B. SN7490 decade counters (contd).

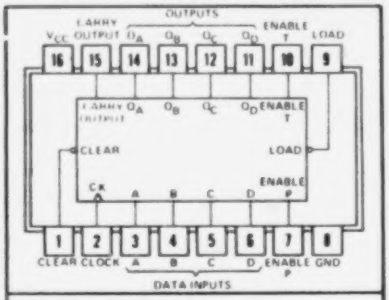
TYPES SN54160 THRU SN54163, SN74160 THRU SN74163
SYNCHRONOUS 4-BIT COUNTERS

BULLETIN NO. DL-S 7211385, OCTOBER 1970 - REVISED DECEMBER 1972

SN54160, SN54161, SN74160, SN74161 . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
SN54162, SN54163, SN74162, SN74163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting Schemes
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs
- Typical Maximum Input Clock Frequency . . . 32 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see description

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The '160 and '162 are decade counters and the '161 and '163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs. The clear function for the '162 and '163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Input clock frequency is typically 32 megahertz and power dissipation is typically 325 milliwatts.

Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 circuits are characterized for operation from 0°C to 70°C.

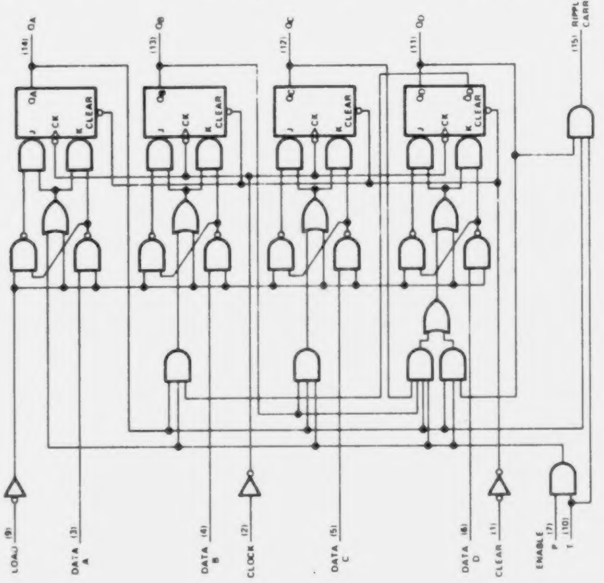
Figure 1-34A. S54160, S54161, S54162, S54163, N74160, N74161, N74162, N74163 synchronous four-bit counter.

TYPES SN54160 THRU SN54163, SN74160 THRU SN74163
SYNCHRONOUS 4-BIT COUNTERS

functional block diagrams

SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

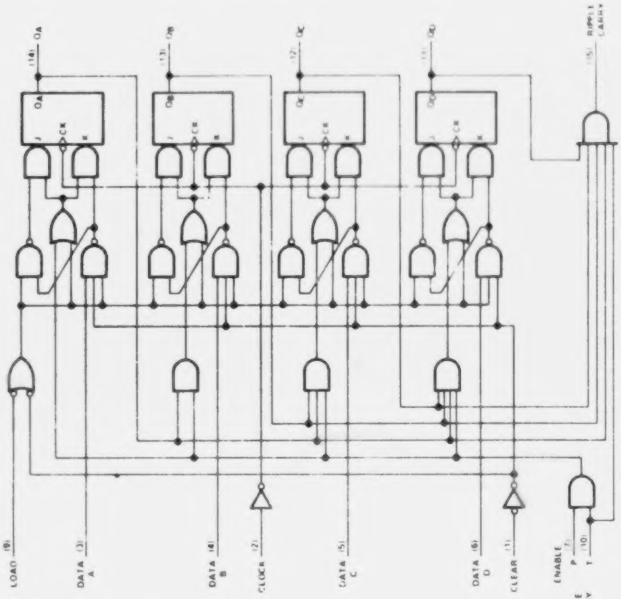
SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.



LOAD (9)
DATA A (3)
DATA B (4)
CLOCK (2)
DATA C (5)
DATA D (6)
CLEAR (1)
ENABLE P (7)
T (10)
(14) QA
(13) QB
(12) QC
(11) QD
(15) RIPPLE CARRY
J
CK
K
CLEAR

SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



LOAD (9)
DATA A (3)
DATA B (4)
CLOCK (2)
DATA C (5)
DATA D (6)
CLEAR (1)
ENABLE P (7)
T (10)
(14) QA
(13) QB
(12) QC
(11) QD
(15) RIPPLE CARRY
J
CK
K

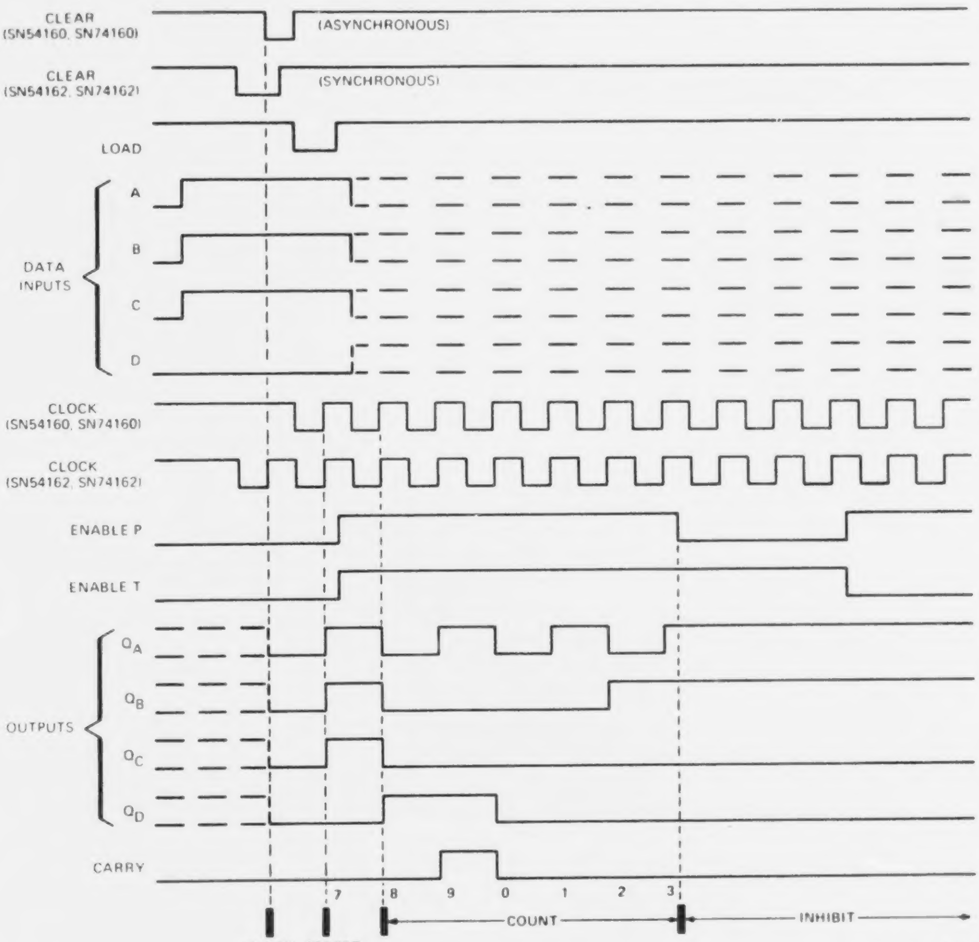
Figure 1-34B. Digital 54/74 TTL series S54/N74160, S54/N74161, S54/N74162, S54/N74163.

SN54160, SN54162, SN74160, SN74162 SYNCHRONOUS DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit


CLEAR (SN54160, SN74160)
(ASYNCHRONOUS)
CLEAR (SN54162, SN74162)
(SYNCHRONOUS)
LOAD
DATA INPUTS
A
B
C
D
CLOCK (SN54160, SN74160)
CLOCK (SN54162, SN74162)
ENABLE P
ENABLE T
OUTPUTS
Q_A
Q_B
Q_C
Q_D
CARRY
7
8
9
0
1
2
3
COUNT
INHIBIT
CLEAR
PRESET

NEO20-158

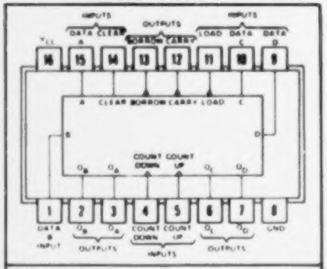
Figure 1-34C. Data timing sequence.

TYPES SN54192, SN54193, SN54L192, SN54L193, SN54LS192, SN54LS193 SN74192, SN74193, SN74L192, SN74L193, SN74LS192, SN74LS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

BULLETIN NO. DL-S 7211828, DECEMBER 1972

- **Cascading Circuitry Provided Internally**
- **Synchronous Operation**
- **Individual Preset to Each Flip-Flop**
- **Fully Independent Clear Input**

'192, '193 . . . J, N, OR W PACKAGE
'L192, 'L193 . . . J OR N PACKAGE
'LS192, 'LS193 . . . J, N, OR W PACKAGE
(TOP VIEW)



logic: Low input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'L192, 'L193	7 MHz	43 mW
'LS192, 'LS193	32 MHz	85 mW

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192, 'L192, and 'LS192 circuits are BCD counters and the '193, 'L193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

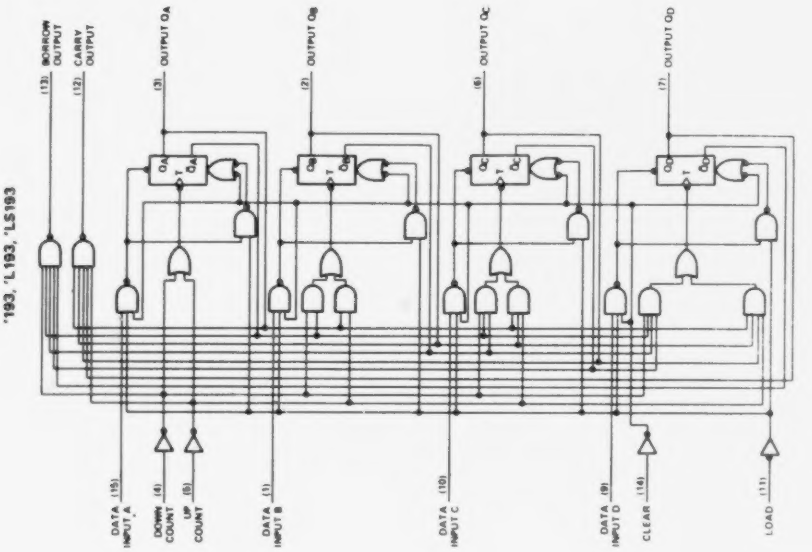
	SN54'	SN54L'	SN54LS'	SN74'	SN74L'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	8	7	7	8	7	V
Input voltage	5.5	5.5	7	5.5	5.5	7	V
Operating free-air temperature range	–55 to 125			0 to 70			°C
Storage temperature range	–65 to 150			–65 to 150			°C

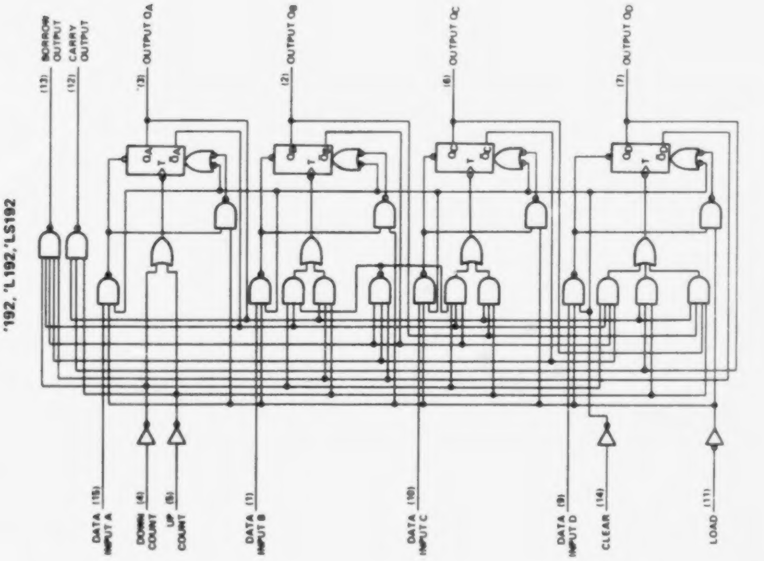
NOTE 1: Voltage values are with respect to network ground terminal.

NEO20-160

Figure 1-35A. S54193, N74193 synchronous four-bit binary up/down counter with preset inputs.

functional block diagrams


'193, 'L193, 'LS193
(13) BORROW OUTPUT
(12) CARRY OUTPUT
(3) OUTPUT QA
(2) OUTPUT QB
(6) OUTPUT QC
(7) OUTPUT QD
QA T QA
QB T QB
QC T QC
QD T QD
DATA INPUT A (15)
DOWN COUNT (4)
UP COUNT (5)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
CLEAR (14)
LOAD (11)


'192, 'L192, 'LS192
(13) BORROW OUTPUT
(12) CARRY OUTPUT
(3) OUTPUT QA
(2) OUTPUT QB
(6) OUTPUT QC
(7) OUTPUT QD
QA T QA
QB T QB
QC T QC
QD T QD
DATA INPUT A (15)
DOWN COUNT (4)
UP COUNT (5)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
CLEAR (14)
LOAD (11)

. . . . Dynamic input activated by a transition from a high level to a low level

NEO20-161

Figure 1-35B. Functional block diagrams.

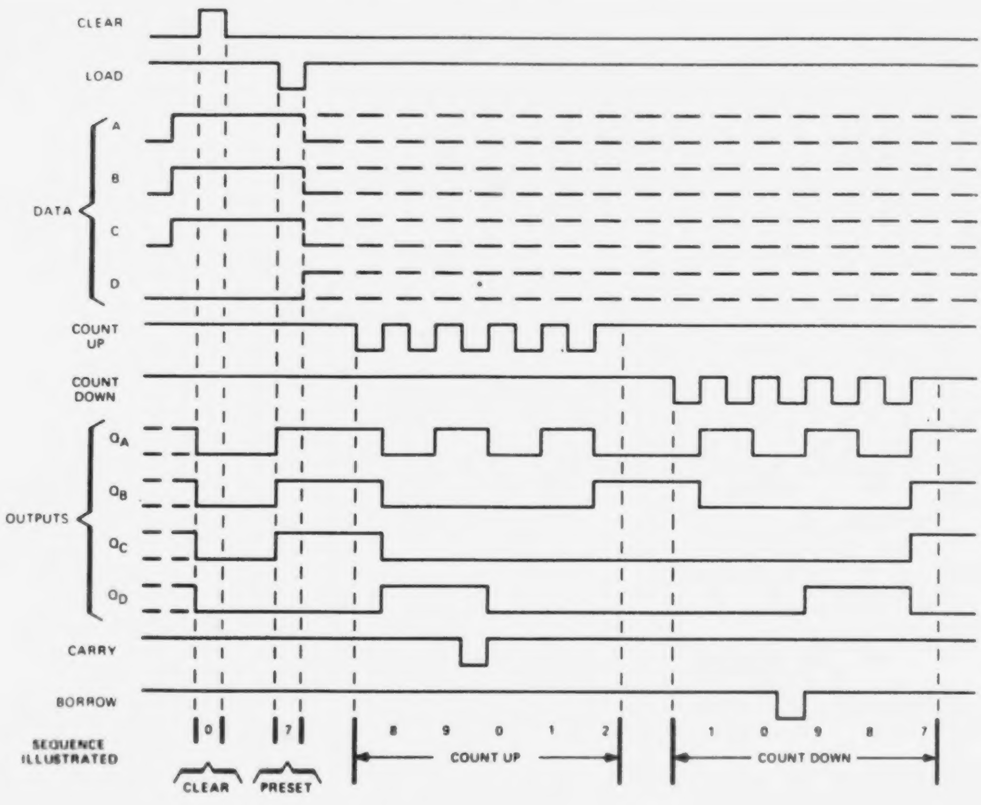
TYPES SN54192, SN54L192, SN54LS192, SN74192, SN74L192, SN74LS192
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

'192,'L192, 'LS192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



CLEAR
LOAD
DATA
A
B
C
D
COUNT UP
COUNT DOWN
OUTPUTS
Q_A
Q_B
Q_C
Q_D
CARRY
BORROW
SEQUENCE ILLUSTRATED
0
7
8
9
0
1
2
1
0
9
8
7
CLEAR
PRESET
COUNT UP
COUNT DOWN

NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

NEO20-162

Figure 1-35C. Data timing sequence.

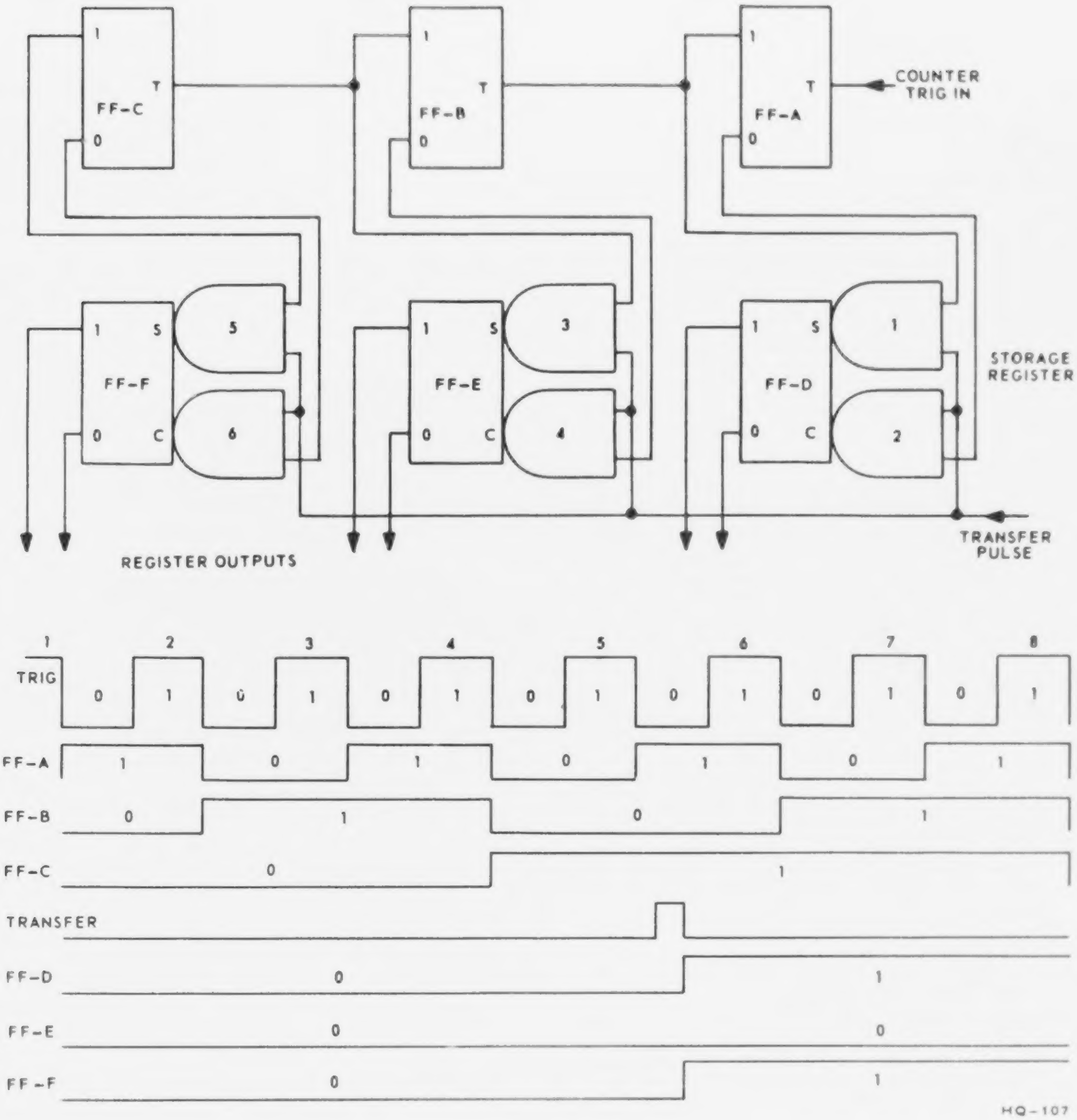


Figure 1-36. Storage register, parallel-in/parallel-out.

of information. The units that do all of this storing, shifting, and mathematics are called registers. Registers are made up of bistable devices and range in design from simple one-stage, serial-in, serial-out units, to complicated multipurpose units with many stages.

015. Specify operational procedures for parallel and serial input registers.

Storage Registers. Since most of the registers you will see use flip-flops, this is the kind we will discuss. A flip-flop will lose the data stored in it when power is removed. This is called volatile storage. This occurs because, when power is reapplied, you have no way of knowing which state the flip-flop will assume. Nonvolatile devices, such as the magnetic core, retain the data stored in them even though power is removed. A storage register can be made up of any number of flip-flops, depending upon the number of bits to be stored. Each flip-flop will store one bit at a time—either a binary 1 or a binary 0.

Parallel-in/parallel-out register. This register provides temporary storage between two functional blocks that use parallel data, accepts data in parallel, and transfers data out in parallel. A typical use of this type of register is shown in figure 1-36. In this logic circuit, the content of the counter is sampled at the time the equipment generates a transfer pulse. The register stores the count and transfers it to using circuits when needed.

There are many configurations of flip-flops and gates that can be used to make up this same type of register. The

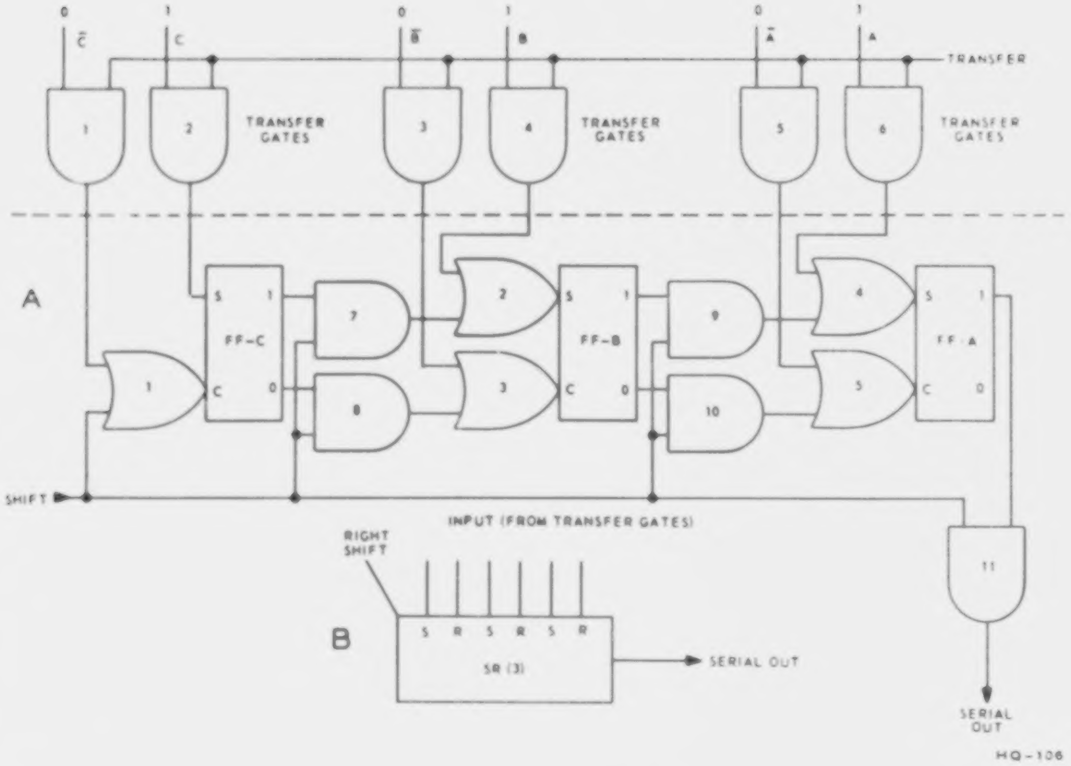


Figure 1-37. Storage register, parallel-in/serial-out.

exact configuration used depends to a large extent upon the amount of interchangeability provided between register flip-flops and counter flip-flops within particular equipment. In this figure, the register flip-flops have an AND-gate at each input. This is typical of most multiuse flip-flops. In fact, flip-flops in several types of equipment in your career ladder use two AND-gates at each input; others have two AND-gates at each input, plus additional reset inputs.

In this logic diagram the counter consists of FF-A, FF-B, and FF-C; the storage register consists of FF-D, FF-E, and FF-F. Notice that the ONE side and ZERO sides of the counter flip-flops are connected to the SET and CLEAR inputs of their respective register flip-flops through AND-gates 1 through 6. The second input to each of these gates is the transfer pulse.

If a transfer pulse occurs just after the counter reaches a count of 1 0 1, the output on the ONE sides of FF-A and FF-C are high, conditioning one leg of AND-gate 1 and one leg of AND-gate 5. Thus, when the transfer pulse occurs, it passes through the transfer gates to set FF-D and FF-F to the ONE state; and AND-gate 4 is conditioned by the high outputs from the ZERO side of FF-B. Therefore, the transfer pulse passes through this gate to set FF-E to the ZERO state. The count 1 0 1 has now been transferred to the register without affecting the counting of the counter.

The count stored in the register is now available to any circuit needing it. The voltage levels available at the ONE and ZERO outputs of the flip-flops can be fed to count detection matrices, digital-to-analog converters, or to any circuit that needs them to solve its problem. Note the waveform in figure 1-36; the count remains in the register until another transfer pulse is generated to read in another count.

When another transfer pulse reads in the new count from the counter, it changes the state of the register flip-flops to represent the new count. Since the transfer gates sample both sides of the counter flip-flops, no clear pulse is needed to clear the register of old data prior to write-in of new data.

Notice one other feature of this circuit. The transfer pulse is delayed slightly with respect to the pulses counted by the counter. This allows the counter flip-flops to assume a stable between-count state prior to sampling the counter configuration.

Parallel-in/serial-out register. Most digital operations are carried out in parallel circuits. Thus, when all necessary operations result in an answer that is in binary form, that binary number of configuration is normally in a parallel register awaiting use. If this number is to be used to actuate print hammers to print out the information it represents, or if it is used to position the beam of a CRT to display the data as a radar picture, it is usually transferred in parallel to decoders and digital-to-analog converters. When the data must be transmitted over telephone lines or microwave links to a data processor or a computer, it must be converted from parallel to serial form. This conversion is made by parallel-in/serial-out registers.

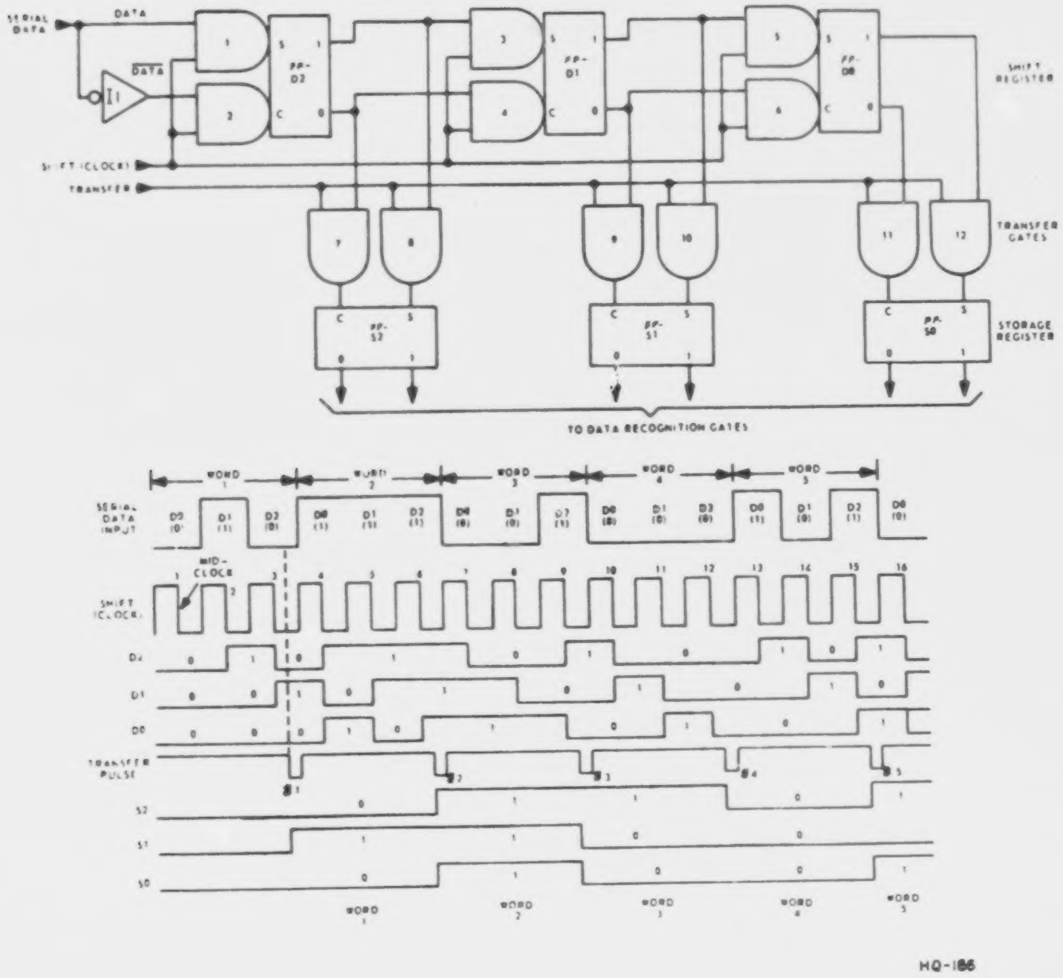

SERIAL DATA
DATA
$\overline{\text{DATA}}$
I1
FF-D2
FF-D1
FF-D0
SHIFT REGISTER
SHIFT (CLOCK)
TRANSFER
TRANSFER GATES
FF-S2
FF-S1
FF-S0
STORAGE REGISTER
TO DATA RECOGNITION GATES
WORD 1
WORD 2
WORD 3
WORD 4
WORD 5
SERIAL DATA INPUT
MID-CLOCK
SHIFT (CLOCK)
D2
D1
D0
TRANSFER PULSE
S2
S1
S0
HQ-186

Figure 1-38. Storage register, serial-in/parallel-out (detailed).

Figure 1-37,A, shows a register that accepts data in parallel through AND-gates 1 through 6, and shifts it out serially, bit by bit, through AND-gate 11. The actual register circuits are composed of three flip-flops—A, B, and C; AND-gates 7 through 10; and OR-gates 1 through 5. In practical circuits, these gates are part of the flip-flop and are not shown on functional diagrams. By showing them as separate functional circuits, we hope to give you a clear picture of the operation of the register. Figure 1-37,B, depicts the register as it is shown in simplified MIL-STD 806B logic.

Now study the circuit for a few minutes. Look at the inputs to the transfer gates. For explanation purposes, assume that the input is A B $\overline{C}$; then see what happens.

The first action is the application of a TRANSFER pulse to AND-gates 1 through 6. AND-gates 1, 4, and 6 are conditioned as follows:

AND 1 = C • TRANSFER
AND 4 = B • TRANSFER
AND 6 = A • TRANSFER

The transfer pulse passes through these AND-gates and through OR-gates 1, 2, and 4, setting the register to 0 1 1. The following paragraphs describe the action of the shift pulses:

a. The first shift pulse:

(1) Passes through AND-gate 11 as the first ONE-bit in the serial output.

(2) Passes through AND-gate 9 and OR-gate 4 to keep FF-A in the ONE state.

(3) Passes through AND-gate 8 and OR-gate 3, setting FF-B to the ZERO state.

(4) Passes through OR-gate 1 to insure that FF-C remains in the ZERO state. The register now contains the number 0 0 1, and a ONE has been shifted onto the serial output line.

b. The second shift pulse:

(1) Passes through AND-gate 11 as FF-A is still in the ONE state. This shift pulse becomes the second ONE-bit on the serial output line.

(2) Passes through AND-gate 10 and OR-gate 5 to set FF-A to the ZERO state.

c. The third shift pulse finds AND-gate 11 disabled and the output becomes ZERO for the third time period. The binary 0 1 1 in the register has now been placed in serial form.

Serial-in/parallel-out register. When data is to be transmitted over relatively long distances, it is uneconomical to use a line for each bit in a message, as is required for the parallel transfer of data. The equipment that receives this serially transmitted data must accept it bit by bit as it comes in on the line, but must convert it to parallel data for use in parallel operations within the equipment. To perform this serial-to-parallel conversion, serial-in/parallel-out registers are used.

A typical register of this type is shown in figure 1-38. It is designed to accept a three-bit word in serial form and, when the total word is in the register, to transfer it to the parallel register. Circuits of this type normally have more than three stages; however, if you understand how this register (fig. 1-38) works, you can understand registers of this type with any number stages.

Look at the waveforms. Notice that the serial data input consists of five three-bit words, with each word containing the bits—D0, D1, and D2. Serial data is applied to FF-D2 via AND-gates 1 and 2. The input to AND-gate 2 is inverted by 11; thus, it is $\overline{\text{DATA}}$. DATA provides a conditioning level to AND-gate 1 when the data bit is a ONE, and $\overline{\text{DATA}}$ provides a conditioning level to AND-gate 2 when the data bit is a ZERO. Shift pulses are applied simultaneously to all register input gates. The downclock of the shift pulse occurs in the middle of the data pulse and shift-in occurs at that time. A transfer pulse occurs following the downclock of every third shift pulse. Now let us see what happens as each bit of word 1 is applied.

The first bit applied is D0, a logic ZERO. AND-gate 2 is conditioned by DO • SHIFT PULSE. At midclock time, the shift pulse down clocks, the output of AND-gate 2 goes negative, and FF-D2 is cleared (set to the ZERO state). If FF-D2 were previously in the ZERO state, no action takes place. Bit D0, a logic ZERO, is now stored in FF-D2.

AND-gate 4 is conditioned by $\overline{\text{FF-D2}}$ and the second shift pulse. At the downclock of the second shift pulse, the output of AND-gate 4 goes negative, clearing FF-D1 to the ZERO state. With the next bit (D1) a ONE bit, AND-gate 1 is conditioned by D1 • SHIFT. At the downclock of the second shift pulse, the output of AND-gate 1 also goes negative, setting FF-D2 to the ONE state. The first two data bits have now been stored in the register.

AND-gate 6 is conditioned by $\overline{\text{FF-D1}}$ and the third shift pulse. At the downclock of this shift pulse, the output of AND-gate 6 goes negative, clearing FF-D0 to the ZERO state. AND-gate 3 is also conditioned (by FF-D2 • SHIFT); and its output also goes negative with the downclock of the shift pulse, thus setting FF-D1 to the ONE state. The third data bit , D2, is a logic ZERO and FF-D2 is cleared to the ZERO state by the output of AND-gate 2. The first word, 0 1 0, is now stored in the shift register.

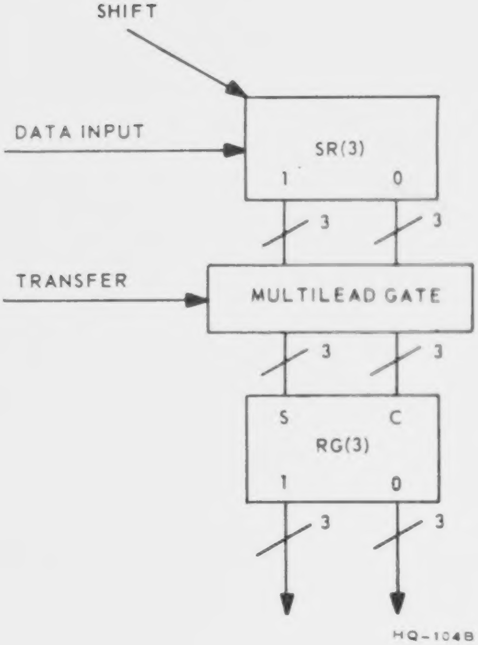


Figure 1-39. Storage register, serial-in/parallel-out (basic).

Transfer pulse number 1 is now applied to transfer AND-gates 7 through 12. Since the condition in the shift register is 0 1 0, AND-gate 7, AND-gate 10, and AND-gate 11 are conditioned. At the downclock of the shift pulse, these gates are deconditioned, their outputs go negative, and the word is transferred to the storage register. FF-S2 is cleared, FF-1 is set, and FF-S0 is cleared. Word number 1 is now in the storage register, where it is available for use until the next transfer pulse transfers in a new word.

This serial-in/parallel-out register, the transfer gates, and the parallel-in/parallel-out register can be represented in simplified form (see fig. 1-39). This form of logic drawing is used where detail is not needed and only basic logic functions are shown. Data input is shown coming into the left side of the block labeled "SR." The SR(3) identifies this block as a three-stage shift register. The shift arrow shows that shift is to the right. The slash marks with the number 3 on each output of the shift register indicate that three ONE-side outputs and three ZERO-side outputs from the shift register are applied to the multilead gate. The presence of the transfer line indicates that all gates transfer when this pulse is applied. The remainder of the drawing is self-explanatory. Compare it with the drawing in figure 1-38 and note how simply functions can be expressed when there is no interest in the detail of how these functions are accomplished.

Serial-in/serial-out register. To enter or extract a binary number in a serial-in/serial-out register requires an operation known as "shifting." The shift function has many applications and is *not* limited to a serial input-output register. The various uses of the shift function will

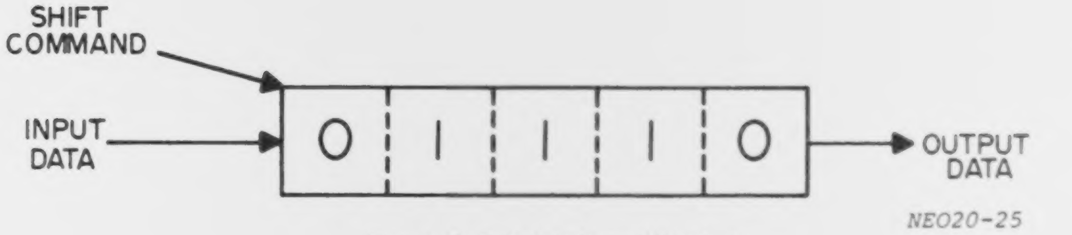

SHIFT COMMAND
INPUT DATA
0
1
1
1
0
OUTPUT DATA
NEO20-25

Figure 1-40. Series-in/series-out shift register.

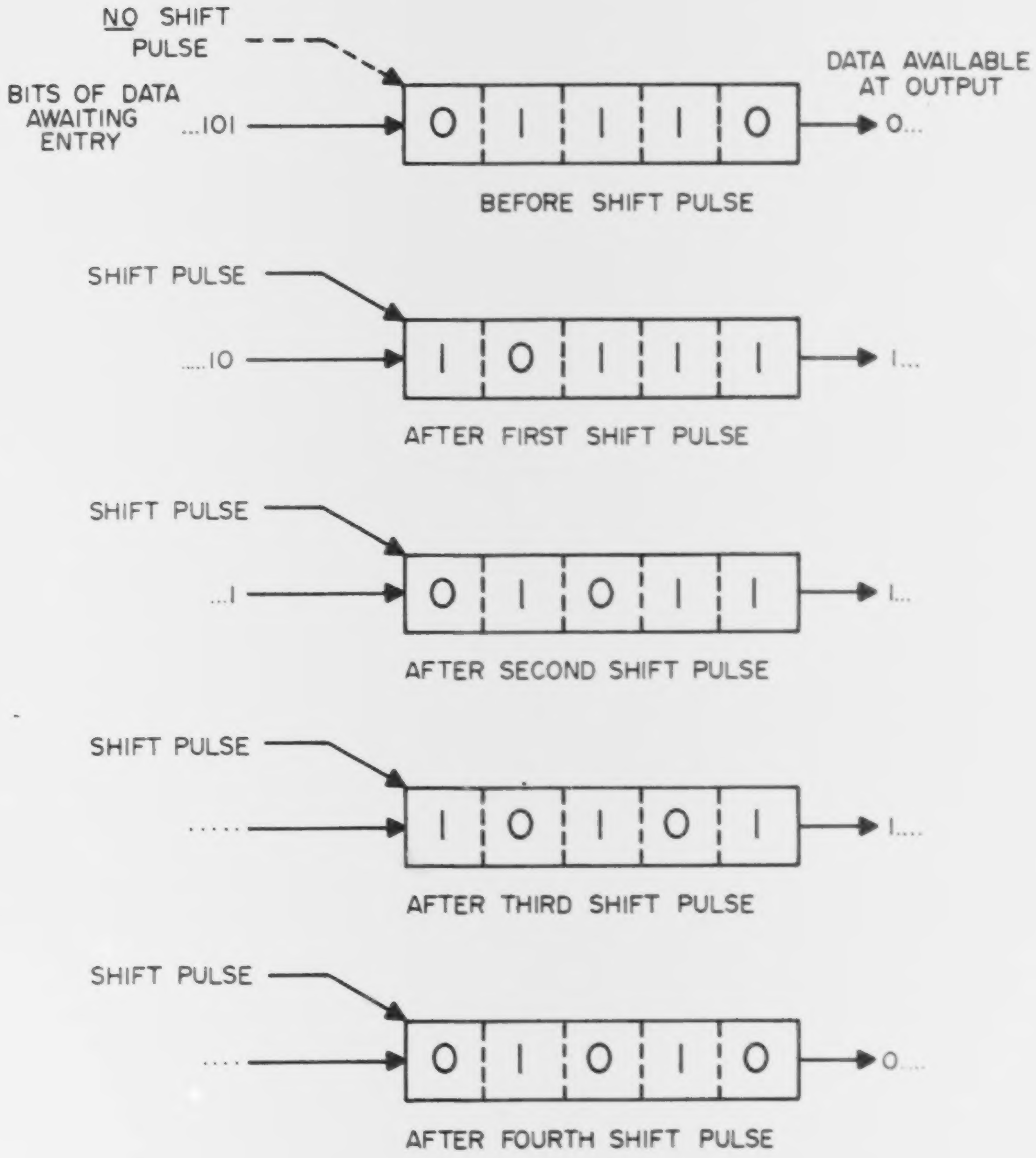

NO SHIFT PULSE
BITS OF DATA AWAITING ENTRY
...101
0 1 1 1 0
DATA AVAILABLE AT OUTPUT
0...
BEFORE SHIFT PULSE
SHIFT PULSE
.....10
1 0 1 1 1
1...
AFTER FIRST SHIFT PULSE
SHIFT PULSE
...1
0 1 0 1 1
1...
AFTER SECOND SHIFT PULSE
SHIFT PULSE
.....
1 0 1 0 1
1....
AFTER THIRD SHIFT PULSE
SHIFT PULSE
....
0 1 0 1 0
0....
AFTER FOURTH SHIFT PULSE

Figure 1-41. Examples of shift sequence.

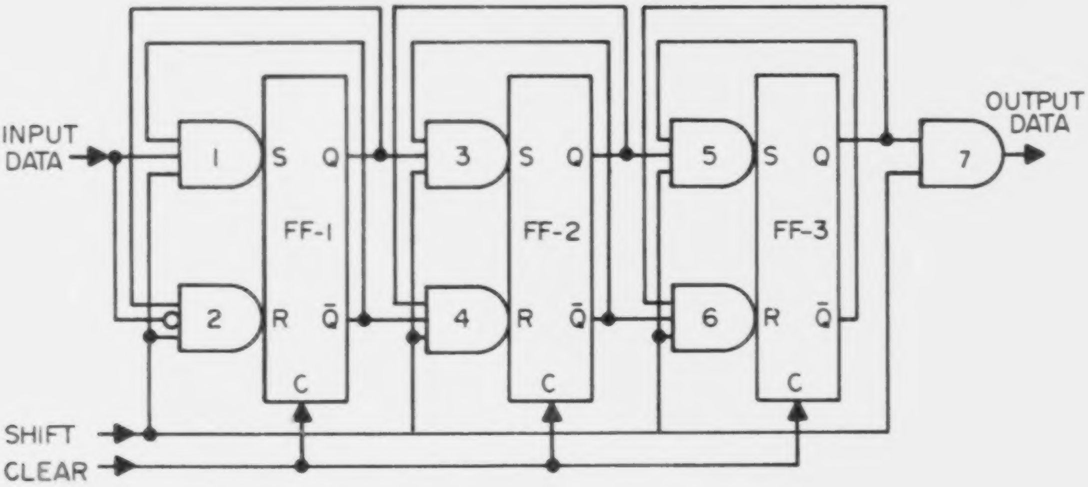


Figure 1-42. Series-in/series-out right shift register.

become clear to you as you read this text. A register that uses the shift function is commonly called a *shift register*.

Figure 1-40 symbolizes a serial-in, serial-out 5-bit shift register. The "shift" command is the control pulse. The binary configuration 01110 represents data already stored in the register. If the stored data is no longer needed, the register can be reset or cleared prior to entering new data. Figure 1-41 shows some examples of the shift sequence when a binary 101 is entered and the stored data is extracted. The transfer/storage operation is as follows: (Again, refer to fig. 1-41.)

(1) The first binary pulse (1) is applied to the input, but it will not be transferred into the register until the first shift pulse occurs. The first bit of the *stored* data is always available at the output and is extracted when the shift pulse occurs.

(2) When the first shift pulse occurs, the input bit is transferred into the first storage location. At the same time, *all* of the stored data is shifted *one place* to the right.

(3) The second input pulse (0) is applied and is now awaiting entry.

(4) When the second shift pulse occurs, the second bit is transferred in, and all of the stored data is again shifted to the right.

(5) This operation continues until all of the input data is stored or all of the stored data is extracted.

(6) Even when there is no data at the input, continuous application of the shift pulse will keep shifting any stored data to the right until the register contains all 0's; then the shift pulse no longer has any effect.

Now that you have an overall concept of how a shift register operates, let's use the diagram illustrated in figure 1-42 to examine the shift operation in more detail. Figure 1-42 illustrates a serial-in/serial-out, 3-bit right-shift register. The C (CLEAR) input performs the same function as the R (RESET) input, but the two are electrically isolated; thus, they are shown separately. Note that the shift input is applied to *all* of the AND-gates. It is important to know that the "switching" time of a flip-flop is greater than the time duration of the shift pulse. Thus, the shift pulse is no longer present by the time a flip-flop changes state. This change of state conditions specific AND-gates, but they cannot produce a high output until another shift pulse occurs.

Assume that the register in figure 1-42 has been cleared by the application of a binary 1 to the CLEAR input. This produces a high (1) at each $\overline{Q}$ output and a low (0) at each Q output. The flip-flops are now reset or considered to be in the 0 state.

The Q and $\overline{Q}$ outputs of each flip-flop are connected back into opposite inputs (R and S) via the AND-gates. This connection provides external complemented inputs for each flip-flop.

The transfer/storage operation of a binary 101 is as follows:

(1) The first input pulse (1) is applied to AND-gates 1 and 2. The state indicator on AND-gate 2 indicates that the gate will be inhibited by the input pulse, which results in a low (0) output from AND-gate 2, regardless of the other two inputs. However, AND-gate 1 has two highs (the input and $\overline{Q}$) and will produce a high (1) output when the shift pulse is applied. All of the other AND-gates have one low (0) input present from the Q output; thus, the shift pulse will not affect them.

(2) When the shift pulse occurs, the high (1) from AND-gate 1 will cause FF-1 to set (Q is now high and $\overline{Q}$ is low). The first bit (1) is now stored in FF-1. The second pulse (0) is applied and is awaiting entry.

(3) AND-gate 2 now has two highs (the low at the state indicator input and Q). AND-gate 3 also has two highs (Q of FF-1 and $\overline{Q}$ of FF-3). All of the other AND-gates have a low input.

(4) When the shift pulse occurs, the high output from AND-gate 2 causes FF-1 to change back to a 0 state, and AND-gate 3 causes FF-2 to switch to a 1 state. In effect, the first bit has been shifted to the right one place and the second bit has been shifted in and stored. The third bit (1) is now awaiting entry.

(5) AND-gate 1 is again properly conditioned by two highs (the input and $\overline{Q}$ of FF-1). AND-gate 4 has two highs ($\overline{Q}$ of FF-1 and Q of FF-2), and AND-gate 5 also has two highs (Q of FF-2 and $\overline{Q}$ of FF-3). This means that all of the flip-flops will change their output state when the next shift pulse is applied.

(6) Application of the shift pulse will allow the last bit to be transferred in and also shift the register contents one place to the right. Binary 101 is now stored in the register.

If it was desired to store another number in this register, the present data could be cleared or simply shifted out. However, let's assume that the binary number 101 must be shifted out and stored in another register for future use.

The output (a binary 1 or 0) is produced when the shift pulse is applied. In figure 1-42, the Q output of FF-3 is presently producing a high (1) to AND-gate 7. A shift pulse will allow AND-gate 7 to transfer the 1 out. At the same time, FF-1 will change to a 0 state, FF-2 will change to a 1 state, FF-3 will change to a 0 state. The register now contains a binary 010.

The next shift pulse will not affect AND-gate 7 because the Q output of FF-3 is now low (0). The low output of AND-gate 7 represents the second output binary bit (0). This shift pulse does not affect FF-1 because it is in the 0 state, and there is no input pulse. However, FF-2 will change to a 0 state, and FF-3 will change to a 1 state. The register now contains a binary 001.

The next shift pulse will allow AND-gate 7 to transfer out a binary 1, and FF-3 will change to a 0 state. The stored data (101) has been shifted out in this form: 1 0 1. Additional shift pulses will have no effect on the register because all of the AND-gates now have a LOW input. This circuit only had a right-shift capability, but some are designed to shift left while others have both right- and left-shift capability.

Exercises (015):

1. On figure 1-36, if a transfer pulse is generated after the sixth count trigger, what flip-flops will be set in the storage register?

2. On figure 1-36, how is the information read out of this storage register?

3. On figure 1-36, if the register flip-flops do not have a reset pulse, how is new information stored?

4. Which functions are enabled to shift a 101 into the register on figure 1-37?

5. What is the purpose of serial-in/parallel-out registers?

6. How does information serially get converted for parallel use?

7. What does SR(3) mean in figure 1-39?

8. In figure 1-38, when does a transfer pulse occur?

9. What is another name for a serial-in/serial-out register?

10. On figure 1-42, what will be the effect of the second shift pulse if there is no data input and the register has a 001 stored?

016. Identify types of shift registers and specify their operational procedures.

Shift Registers. You have learned that the serial-in/serial-out storage register is often referred to as a shift register. However, there is more to shift registers than this single circuit. A shift register is a device capable of receiving, rearranging, and retaining binary data which can be used later in the computer. It can receive data either in serial or parallel form, and data may be taken from the shift register in serial or parallel form. When information is taken out in serial form, it may be shifted to the right or to the left, depending upon the design of the circuit. Shifting is useful in many operations, such as scaling, multiplication, division, comparing data bits, and sequencing a change of events. The shift register also serves as a storage register when it is used to store data for certain periods of time. Some of the types of transfers/shifts associated with shift registers are:

a. Serial-In/Serial-Out Register. One bit is shifted in or out each time a shift pulse is applied.

b. Parallel-In/Serial-Out Register. All data is transferred in at the same time, but only one bit will be transferred out when each shift pulse occurs.

c. Serial-In/Parallel-Out Register. In this circuit, only one bit is shifted in at a time, but when the data is needed, all bits are transferred out at the same time.

The location of a shift pulse at the left corner of the symbol (fig. 1-43) indicates that the shift is from left to right. If the shift input is located at the right corner of the symbol, the shift is from right to left.

Shift Register Operation. The operation of shift registers is similar to that of storage registers, except shift registers have interconnecting lines and a shift pulse to shift data through the register.

Parallel-in/serial-out register. Figure 1-44 illustrates a typical shift register with the input taken from a storage register. The shift register has a parallel input and a right-shift serial output.

Using the diagram of the shift register in figure 1-44, notice that the output of each flip-flop in the shift register is fed directly to the input of the following flip-flop. A shift register can have many more than three flip-flops, but the connections remain the same throughout.

Before the read-in (transfer) pulse is applied, assume flip-flops A, B, and C are in the ZERO state and the storage register contains a binary count of five (101). With the above conditions existing, the transfer is applied to AND-gates 1, 2, and 3. At the time the transfer pulse downclocks (T0), flip-flops A and C are set to the ONE state. Flip-flop B remains in the ZERO state since AND-gate 2 does not have two high inputs. The shift register and storage register now contain the same binary configuration of 101 as shown by the waveforms.

The output of flip-flop C is high and is one input to AND-gate 8. When the shift pulse goes high at time T1, both inputs to AND-gate 8 are high and the output goes high. When the downclock of the shift pulse at time T1, flip-flop A changes to the ZERO state, flip-flop B changes to the ONE state, flip-flop C changes to the ZERO state, and the output goes low. Thus, one bit has been shifted out of the register. At time T1, the one bit in flip-flop A was transferred to flip-flop B; the ZERO bit in flip-flop B was transferred to flip-flop C; and the ONE bit in flip-flop C was gated out of AND-gate 8. This leaves a binary configuration of 010 in the shift register.

With 010 in the shift register, the only flip-flops that are activated for a change of state are flip-flops B and C. The output AND-gate is held closed since flip-flop C is in the ZERO state. Thus, with the downclock of the T2 shift pulse, flip-flop A remains in the ZERO state, flip-flop C changes to the ONE state, and no output signal is produced. However, the count in the shift register has moved one more place to the right, and a zero bit has been shifted through AND-gate 8. This leaves a binary configuration of 001 in the shift register. Flip-flop C and AND-gate 8 are now activated. When the shift pulse is applied, an output from AND-gate 8 appears. When the downclock of T3 occurs, flip-flop A and flip-flop B remain in the ZERO state, and flip-flop C goes to the ZERO state. At this time, shift out is complete. You can see that one shift pulse is necessary to shift out each binary bit.

Let us review the action of the shift register.

(1) The storage register had binary configuration of 101.

(2) The shift pulse T1 produced a one-bit output and shifted the configuration to the right, with a remaining configuration of 010.

(3) Shift pulse T2 shifted the configuration to the right for the second time and produced a zero-bit output with a remaining configuration of 001.

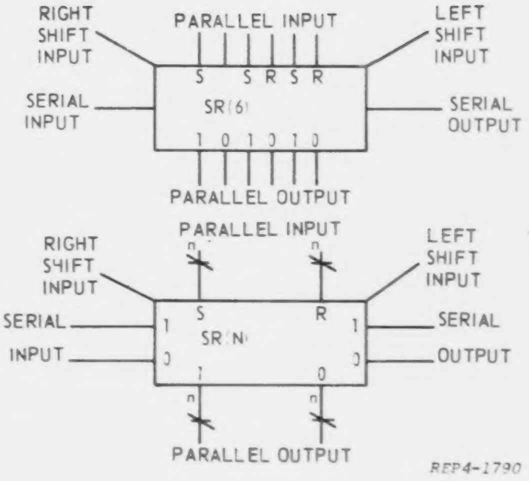


Figure 1-43. Register input/output designations.

(4) Shift pulse T3 shifted the configuration to the right for the third time and produced a one-bit output with a remaining configuration of 000.

The shift register symbol represents a register with provisions for displacing or shifting the contents of the register one stage at a time to the right or left by means of the SHIFT-pulse input.

Serial-in/parallel-out shift register. Figure 1-45 is a logic diagram of a serial input/parallel output shift register, and a parallel-input/parallel-output storage register. The waveform chart shows the various actions of the circuit. To explain the operation, $011_{(2)}$ will be shifted into the shift register, then transferred to the storage register.

Assume that all flip-flops in the shift register are CLEAR and that all flip-flops in the storage register are SET as shown by the waveforms. Clear pulse A clears the storage register (flip-flops D, E, and F). When the input data pulse and the shift pulse are applied at the same time, AND-gate 1 will produce an output pulse to set FF-A. The third leg of AND-gate 1 was activated by the binary one from the ZERO side of FF-A. The shift register now contains $100_{(2)}$.

When the second shift pulse is applied, another data pulse is present at the input. However, FF-A cannot be affected because AND-gates 1 and 2 are deactivated for the duration of the shift pulse. AND-gate 1 is deactivated by the binary zero from the ZERO side of FF-A. AND-gate 2 is deactivated by the inverted data pulse from the inverter. AND-gate 3 will produce an output pulse because of the binary 1 from FF-A, the binary 1 from FF-B, and the shift pulse. The pulse from AND-gate 3 will set FF-B. The register now contains $110_{(2)}$.

When the third shift pulse arrives, the data-pulse line contains a binary 0, so AND-gate 1 will be deactivated. The inverter will invert the binary 0 to a binary 1 and activate one leg of AND-gate 2. A second leg of AND-gate 2 will be activated by the binary 1 from the ONE side of FF-A. So when the shift pulse is applied, AND-gate 2

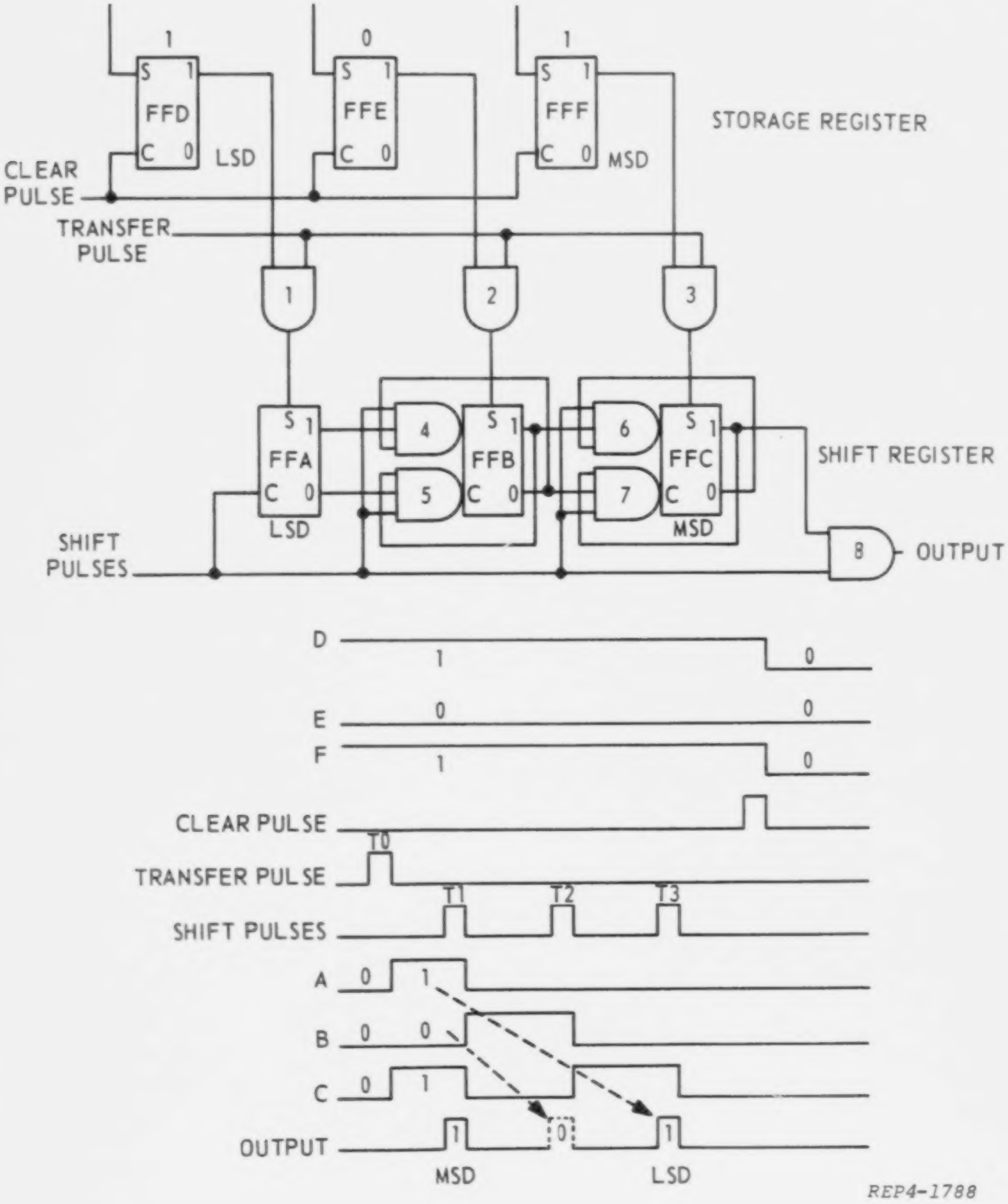

1
0
1
S 1
FFD
C 0
LSD
S 1
FFE
C 0
S 1
FFF
C 0
MSD
STORAGE REGISTER
CLEAR
PULSE
TRANSFER
PULSE
1
2
3
S 1
FFA
C 0
LSD
4
5
S 1
FFB
C 0
6
7
S 1
FFC
C 0
MSD
SHIFT REGISTER
SHIFT
PULSES
8
OUTPUT
D
1
0
E
0
0
F
1
0
CLEAR PULSE
T0
TRANSFER PULSE
T1
T2
T3
SHIFT PULSES
A
0
1
B
0
0
C
0
1
OUTPUT
1
0
1
MSD
LSD
REP4-1788

Figure 1-44. Shift register operation.

will produce an output pulse and clear FF-A. FF-B will remain set because AND-gates 3 and 4 remain deactivated. However, AND-gate 5 will be activated and produce an output pulse to set FF-C. The register now contains $011_{(2)}$.

When the read-in pulse (same as a transfer pulse) occurs, the contents of the shift register, $011_{(2)}$, are transferred to the storage register. Both registers now contain the same data.

Shifting Operations. Up to this point, you have only been exposed to right shifters. However, shifts may be done in either direction—right or left. Also, it is possible to shift only a part of the data at any one time, depending on the design of the circuitry.

Each time a binary 1 is shifted toward the LSD, its value becomes half of what it was before the shift. As an example, if the binary number $100_{(2)}$ is shifted right one place, the new number is $010_{(2)}$. The original value of the

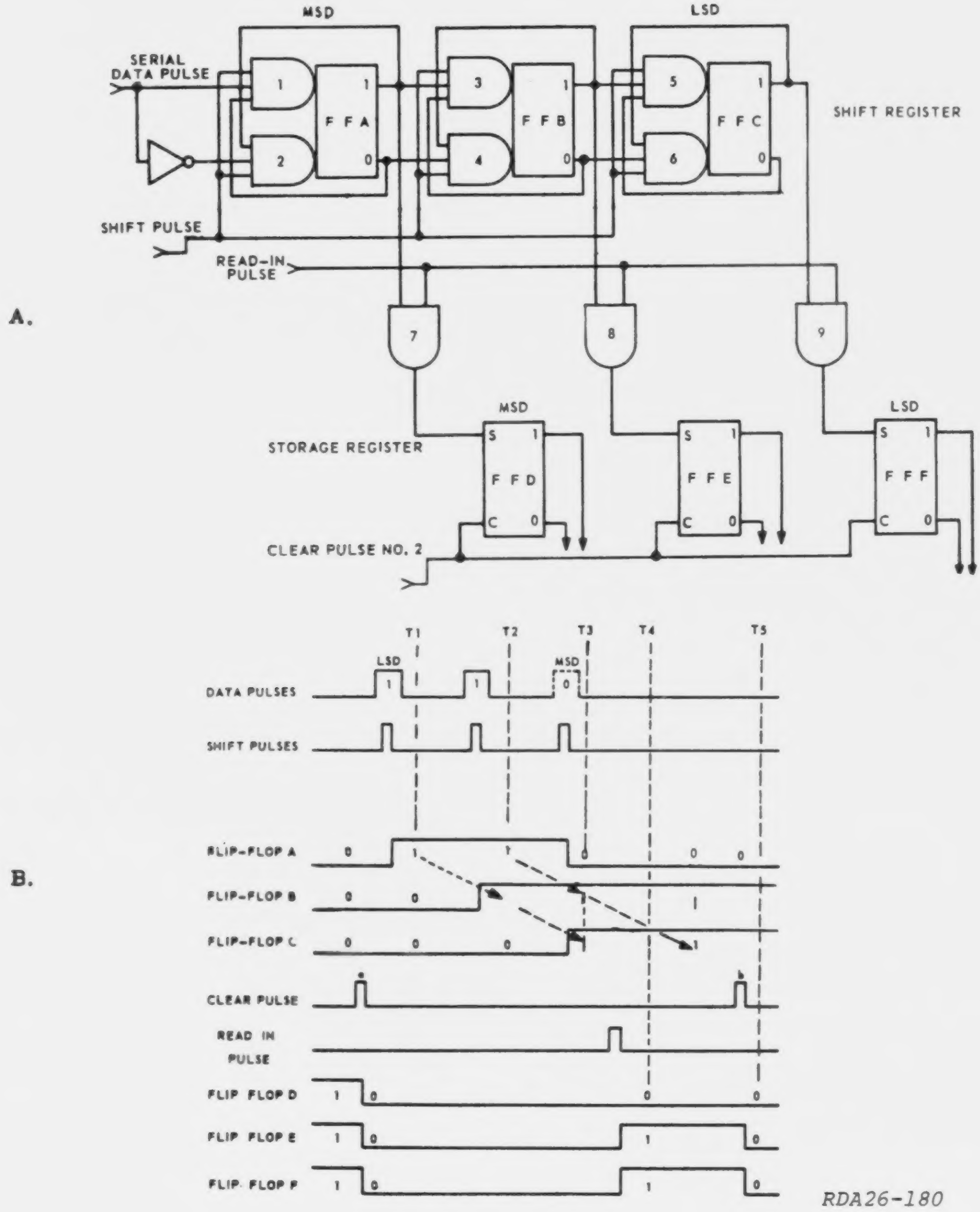

A.
MSD
LSD
SERIAL DATA PULSE
SHIFT REGISTER
F F A
F F B
F F C
SHIFT PULSE
READ-IN PULSE
STORAGE REGISTER
F F D
F F E
F F F
CLEAR PULSE NO. 2
B.
T1
T2
T3
T4
T5
DATA PULSES
SHIFT PULSES
FLIP-FLOP A
FLIP-FLOP B
FLIP-FLOP C
CLEAR PULSE
READ IN PULSE
FLIP FLOP D
FLIP FLOP E
FLIP FLOP F
RDA26-180

Figure 1-45. Serial-in/parallel-out operation.

number was 4, but after the shift toward the LSD, its new value is 2, which is one-half of the original value. Just reverse this procedure and you will see that each time the number is shifted toward the MSD, its value will double.

Shifts are normally one of two types—arithmetic or logical. The number of places in which data is shifted will be controlled by a counter as you will see later. Let's first look at the arithmetic shift.

Arithmetic shift. The arithmetic shift, in most computer systems, will shift only the magnitude of the number without changing the sign (positive or negative) of the number. The computer is able to tell whether a number is positive or negative by the "sign bit." In most computers, the number is negative when the sign bit is a binary 1 and positive when the sign bit is a binary 0.

Look at figure 1-46. This is a sample arithmetic shift. The arrows indicate a left shift, end off. In other words, when the shift pulse is applied, the entire contents of the register (B1-B15), with exception of the sign bit, are

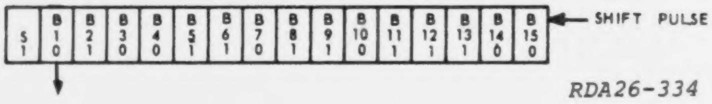


Figure 1-46. Sample arithmetic shift.

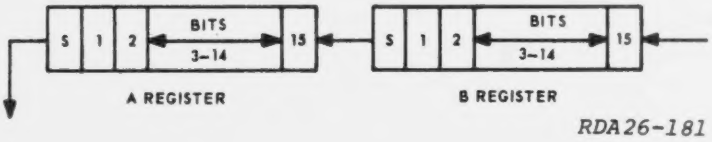


Figure 1-47. Sample double logical shift.

shifted left one place, and the data which was in B1 is shifted out and lost. The sign bit did not shift or change.

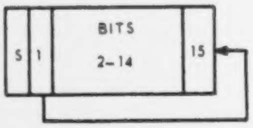
Logical shift. The logical shift is normally the same as the arithmetic shift *except* that the sign bit will also be moved. Figure 1-47 shows a sample double logical shift from one register to another. Like the arithmetic shift, the logical shift shown here is only a sample and may not be done like this in all machines. You must know the operation of each machine to determine how the shifts are made.

Shift combinations. The examples in figure 1-48 are, again, only sample shift functions. They may not be done the same way in all computer systems. Shifting operations using only one register are referred to as *single* and the operations using two registers are called *double.* Each of these are single shifts, but each one may be combined with another register for double shifting operations.

Digital Integrated Circuit Shift Registers. Registers, too, are often found as digital integrated circuits (DICs). The DIC presented is only meant to be representative of those that are available in the field. Space does not permit publication of the full line; however, this integrated circuit will demonstrate the flexibility of the many single-chip registers presently in use.

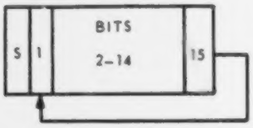
One of these is the five-bit shift register/TTL MSI (multifunction shift register). Types SN5496 and SN7496 are shown in figures 1-49A and 1-49B, along with an expanded view diagram for simplicity. This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed. Sequential operation information is detailed in figure 1-49. Some of the functions are N-bit serial-to-parallel converter, N-bit parallel-to-serial converter, and N-bit storage register.

3.Single, left, arithmetic, end around.


BITS
2-14
S
1
15

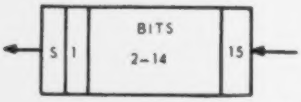
RDA26-185

4.Single, right, arithmetic, end around.


BITS
2-14
S
1
15

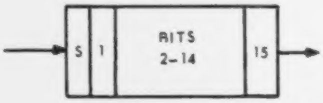
RDA26-186

5.Single, left, logical, end off.


BITS
2-14
S
1
15

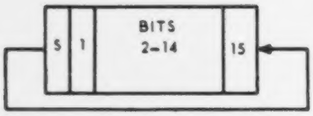
RDA26-187

6.Single, right, logical, end off.


BITS
2-14
S
1
15

RDA26-188

7. Single, left, logical, end around.


BITS
2-14
S
1
15

RDA26-189

Figure 1-48. Examples of shift functions.

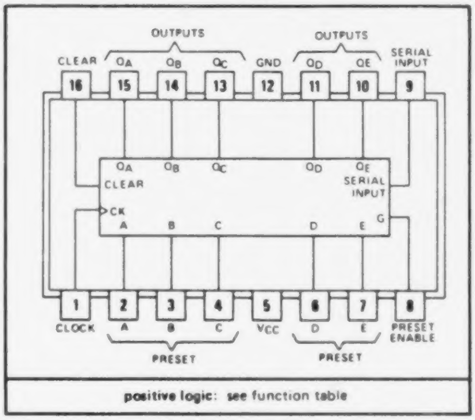
TYPES SN5496, SN54L96, SN7496, SN74L96
5-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7211821, DECEMBER 1972

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

TYPE	PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
'96	25 ns	240 mW
'L96	50 ns	120 mW

'96 . . . J, N, OR W PACKAGE
'L96 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

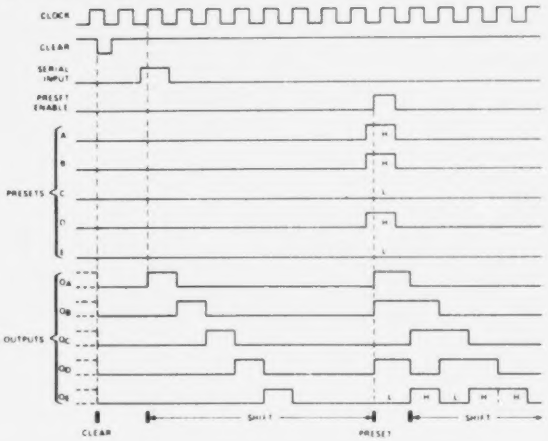
FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	PRESET ENABLE	PRESET					CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
		A	B	C	D	E							
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

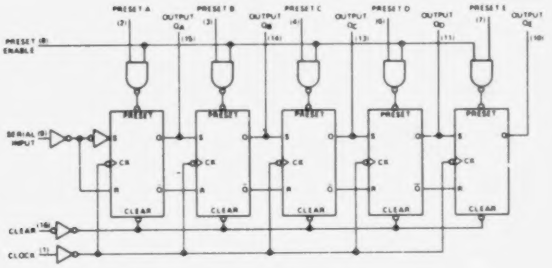
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc = the level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, etc = the level of Q_A, Q_B, etc, respectively before the most-recent ↑ transition of the clock.

Figure 1-49A. SN5496, SN7496 five-bit shift registers.

typical clear, shift, preset, and shift sequences



functional block diagram

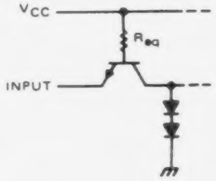

PRESET A (2)
OUTPUT Q_A (15)
PRESET B (3)
OUTPUT Q_B (14)
PRESET C (4)
OUTPUT Q_C (13)
PRESET D (6)
OUTPUT Q_D (11)
PRESET E (7)
OUTPUT Q_E (10)
PRESET ENABLE (8)
SERIAL INPUT (9)
CLEAR (16)
CLOCK (1)
PRESET
S
CK
R
Q
$\bar{Q}$
CLEAR

—◇ . . . dynamic input activated by transition from a high level to a low level.

schematics of inputs and outputs

'96

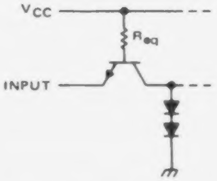
EQUIVALENT OF EACH INPUT


V_{CC}
R_{eq}
INPUT

INPUT	R_{eq} NOM
Preset enable	800 Ω
All others	4 kΩ

'L96

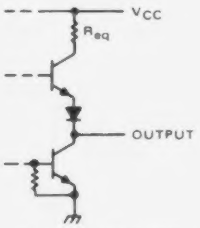
EQUIVALENT OF EACH INPUT


V_{CC}
R_{eq}
INPUT

INPUT	R_{eq} NOM
Preset enable	1.6 kΩ
All others	8 kΩ

'96, 'L96

TYPICAL OF ALL OUTPUTS


V_{CC}
R_{eq}
OUTPUT

'96: R_{eq} = 130 Ω NOM
'L96: R_{eq} = 260 Ω NOM

NEO20-151

Figure 1-49B. SN5496, SN7496 five-bit shift registers (contd).

Exercises (016):

1. What type of register is found in figure 1-50 below?

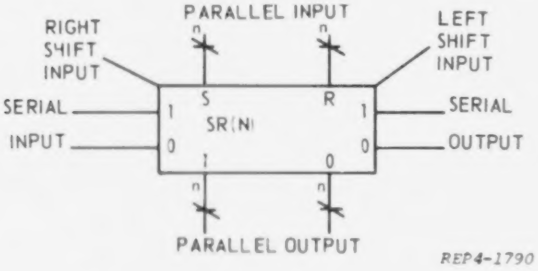

PARALLEL INPUT
n
n
RIGHT SHIFT INPUT
LEFT SHIFT INPUT
SERIAL INPUT
S
R
SR(N)
1
0
1
0
1
0
SERIAL OUTPUT
n
n
PARALLEL OUTPUT
REP4-1790

Figure 1-50. Register (objective 016, exercise 1).

2. What type of register is found in figure 1-51?

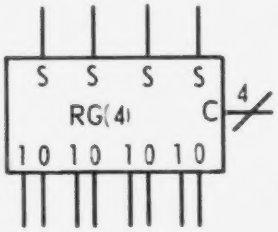

S S S S
RG(4)
C
4
1 0 1 0 1 0 1 0

Figure 1-51. Register (objective 016, exercise 2).

3. How does the logical shift normally differ from the arithmetic shift?

4. How many types of shifts are used by most computers?

5. In a left-shift register, with the LSD on the right, a binary bits value will be changed in what manner by each shift?

6. What pulse moves information into and through a parallel output shift register?

7. What pulse moves the information out of the parallel output register?

017. Specify characteristics of the different methods of register transfer.

Methods of Register Transfer. In the following paragraphs, we will discuss the methods of transferring data and the terminology involved in this process. First, you should know what we mean by the term "transfer." It is the moving of data from one place to another. For our purposes, we are concerned about two basic types of transfers: single-line transfer and double-line transfer. A single-line transfer is a transfer network capable of moving only the ones or zeros stored in a register. There are two classifications of single-line transfer networks: one-side transfer and zero-side transfer.

One-side transfer. A one-side transfer network is shown in figure 1-52. The one-side outputs of the X register are fed into the transfer network consisting of gates A, B, C, and D. To move the contents of the X register into the Y register without altering the data, it is necessary to first clear the Y register. With the application of the transfer pulse, the flip-flops in the Y register will be set if the corresponding flip-flops in the X register are in the one

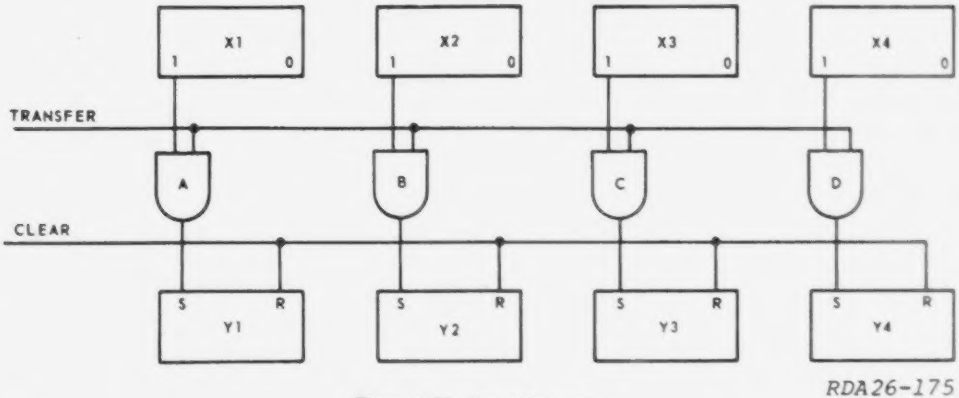

X1
X2
X3
X4
1
0
TRANSFER
A
B
C
D
CLEAR
S
R
Y1
Y2
Y3
Y4
RDA26-175

Figure 1-52. One-side transfer.

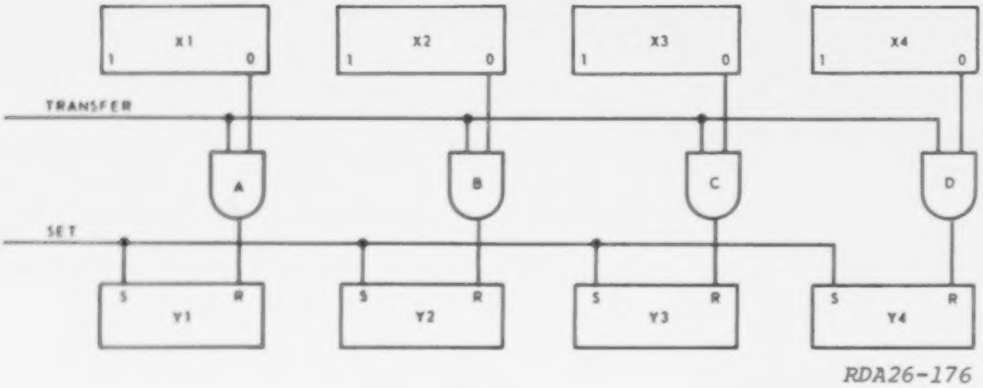


Figure 1-53. Zero-side transfer.

state. It is not necessary to transfer the zeros because the receiving register is cleared before the transfer, thus the name "one-side transfer." In summing up, we can say:

(1) The register flip-flops are cleared before transfer.

(2) Connections are made in the one side of the flip-flops.

(3) When the transfer pulse occurs, a one is transferred into the Y register if the corresponding flip-flop in the X register is in the one state.

Zero-side transfer. A zero-side transfer is shown in figure 1-53. The zero-side transfer uses the same configuration as the one-side transfer except that the zero-side outputs are fed into the transfer network. Note that the Y register must first be set (all ones) before the transfer pulse is applied. In summing up the zero-side transfer:

(1) The register flip-flops are set before transfer.

(2) When the transfer pulse occurs, a zero will be transferred into the Y register if the corresponding flip-flop in the X register is in the zero state.

(3) Connections are made to the zero side of the flip-flops.

Double-line transfer. A transfer network capable of moving, in one operation, both the ones and the zeros stored in a register is called a double-line transfer. Figure 1-54, shows a double-line transfer network. Although this configuration uses twice as many gates as the single-line transfer network, only one control signal is required. Since there is both a set and reset input applied to the receiving register, there is no requirement for a clear or set pulse. This type of network is often referred to as force feeding since data is forced into the receiving register regardless of its previous content.

Complementary transfer. The complementary transfer is a variation of the double-line transfer. Figure 1-55, shows how a complementary transfer is accomplished. After application of the transfer pulse, the contents of the X register will be found in the one's complement form in the Y register.

Exercises (017):

Indicate whether the following statements are true or false. If false, provide the correct statement.

____ 1. The two types of single-line transfer are one- and zero-side transfers.

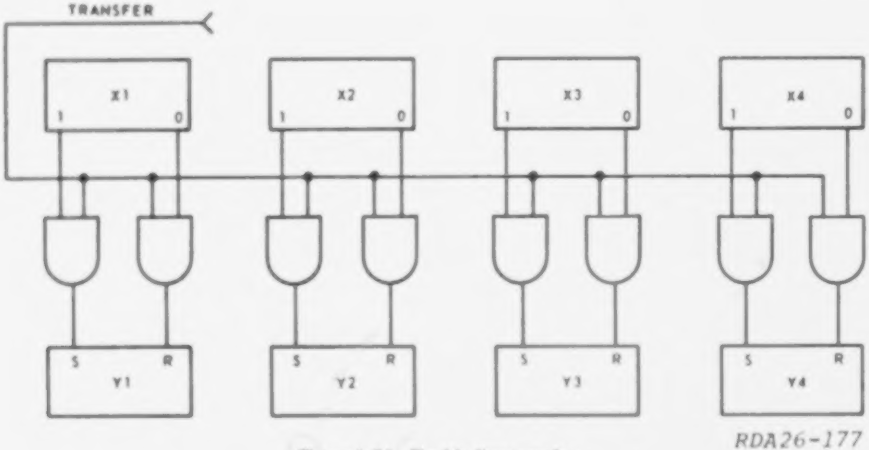
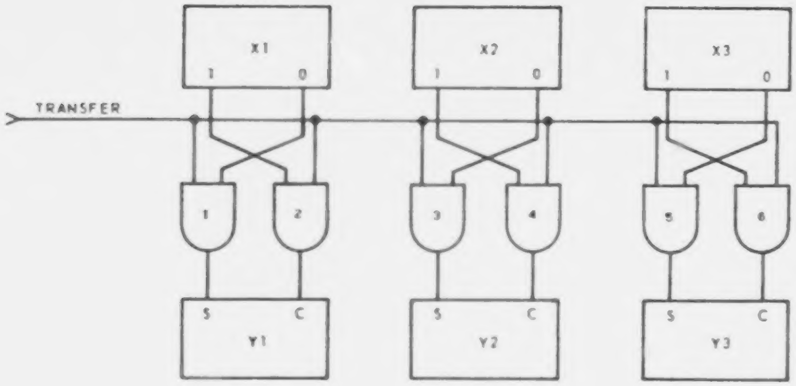


Figure 1-54. Double-line transfer.



RDA26-178

Figure 1-55. Complementing transfer.

____ 2. A single-line transfer capable of moving only zeros would be called a one-side transfer.

____ 3. The term "force feeding" is often used with reference to single-line transfer.

____ 4. In a one-side transfer, the transferred data will not be altered if the Y register is cleared before transfer.

____ 5. A double-line transfer does not require a clear or set pulse.

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Answers for Exercises

Reference:

001 - 1. ZERO output equals a high or 1; ONE output equals a low or 0.
001 - 2. CLEAR or ZERO state.
001 - 3. SET or ONE state.
001 - 4. Limit logic voltage level changes to 0 volts and − 10 volts.
001 - 5. AND-gate for the C side input of the flip-flop.
001 - 6. Q3 and Q4.
001 - 7. The downclock.

002 - 1. High pulse to the SET input causes a low to the bottom OR-gate which provides a high at the one output.
002 - 2. By a high at the CLEAR input.
002 - 3. The high output of the bottom AND-gate keeps the top AND-gate inhibited to maintain the high or one output from the bottom AND-gate.
002 - 4. Latch will be set by a high on the SET input which inhibits the top AND-gate and enables the bottom AND-gate to provide a high or one output.

003 - 1. Pulse steering.
003 - 2. They will change states.
003 - 3. None.
003 - 4. Complementing or toggle.
003 - 5. Q6 and Q7.
003 - 6. ONE.
003 - 7. Q4 and Q6.

004 - 1. JK master-slave flip-flops, synchronous or asynchronous toggle flip-flops, and D flip-flops.
004 - 2. Some of the more common ones are binary counters, shift registers, and ring counters.
004 - 3.
  a. Clock pulse is used to synchronize the operation of the JK flip-flop.
  b. ONE-side output from JK flip-flop circuit in the CLEAR state.
  c. ZERO-side output from JK flip-flop circuit in the CLEAR state.
  d. Input trigger from J flip-flop circuit.
  e. CLEAR changes the state of the JK flip-flip to its RESET state and replaces the data inputs with a low, causing the $\overline{Q}$ output to go high and Q output to go low.
  f. Input trigger from K flip-flop circuit.

005 - 1. 14-pin and 16-pin DIP.
005 - 2. Approximately 3 volts.
005 - 3. .8 volt or less.

005 - 4.
  (1) Isolate the slave from the master.
  (2) Enter information from AND-gate input to the master.
  (3) Disable the AND-gate inputs.
  (4) Transfer the information from the master to the slave.

006 - 1. Serial or parallel.
006 - 2. Up-counters or down-counters.
006 - 3. The number of stages.
006 - 4. Modules of 16.
006 - 5. Decimal 15.
006 - 6. 64 counts.

007 - 1. 13.
007 - 2. All flip-flops will be in the ZERO state.
007 - 3. When FF-C changes from the ONE state to the ZERO state.
007 - 4. Use the ZERO-side output to provide inputs to feed succeeding stages.
007 - 5. The down-counter starts at 15, counts down to 0, and resets to 15.
007 - 6. When FF-A goes to the ONE state.

008 - 1. Parallel counter.
008 - 2. The parallel counter is faster.
008 - 3. This depends on how the counter is wired up or down.
008 - 4. A parallel counter.
008 - 5. SET or ONE state.
008 - 6. Fifteen.
008 - 7. Twelve.
008 - 8. The input pulse if fed to all flip-flops.
008 - 9. The output is taken from the ZERO-side of the flip-flops.

009 - 1. Up-down counter. It determines the direction of the count.
009 - 2. Change the setting of the control flip-flop by changing SW1.
009 - 3. ZERO state.

010 - 1. Ring counter.
010 - 2. It is designed so that the last stage feeds back to the input stage to automatically start the count over.
010 - 3. 0010. For FF-A, FF-B, FF-C, and FF-D respectively.

011 - 1. When FF-D sets, it inhibits AND-gate 2 and also inhibits the operation of FF-C.
011 - 2. By inhibiting AG-2 and using AG-2 to trigger FF-D, when the twelfth clock pulse is received, all flip-flops will be reset.
011 - 3. As mentioned previously, count blocking resets all flip-flops at CP-12, whereas count adding advances the flip-flop count from 8 to 12 and continues to count to 16.
011 - 4. Normally, binary counting takes place through count 7. At count 8, FF-A, FF-B, and FF-C all reset and FF-D sets. FF-D set causes FF-C to set again. FF-C and FF-D set equals binary count 12.
011 - 5. Count 12.

012 - 1. Mod-10 counter.
012 - 2. By either blocking or adding six counts.
012 - 3. 1001, which is 9.
012 - 4. 1110, which is 14.

013 - 1. The clear pulse sets the control FF to the ONE state. When the first clock pulse changes the control FF to the ZERO state, this triggers FF-A to the ONE state.
013 - 2. FF-A in the ONE state and the control FF changing from the ZERO to the ONE state.
013 - 3. Eight clock pulses.
013 - 4. FF-C in the ONE state, FF-B in the ZERO state, and the control FF changing from ZERO to ONE.
013 - 5. The state that the control FF is in when SS1 or SS2 conditions one of AG-1 through AG-4.

013 - 6. Control FF in the ONE state and the downclock from SS2.

014 - 1. TTL high-speed decade counter.
014 - 2. By having all flip-flops simultaneously clocked so that the outputs change coincidentally with each other when instructed by the steering logic.
014 - 3. The outputs may be preset to any state by entering the desired data at the data inputs while the load input is low.
014 - 4. The output counting spikes normally associated with asynchronous counters are eliminated.
014 - 5. Four dual-rank master slave flip-flops.

015 - 1. FF-E and FF-F.
015 - 2. A flip-flop is not gated. The contents of the storage register are always available because the outputs of the flip-flop are not gated.
015 - 3. The ONE and ZERO sides of the counter flip-flop are both applied to the transfer gates. This will cause the storage flip-flops to follow the inputs.
015 - 4. AG-2, AG-3 and OR-3, AG-6 and OR-4.
015 - 5. It is used to receive serially transmitted data, bit by bit as it comes in on the line and to convert it to parallel data for use in parallel operations within the equipment.
015 - 6. The data is entered into a shift register serially and then transferred to a storage register with parallel outputs.
015 - 7. Three-stage shift register.
015 - 8. Following the downclock of every third shift pulse.
015 - 9. Shift register.
015 - 10. First pulse shifts out the (1) and the second pulse has no effect.

016 - 1. Shift register.
016 - 2. Storage register.
016 - 3. In the logical shift, the sign bit will be moved. In the arithmetic shift, it will not.
016 - 4. Two.
016 - 5. Doubles.
016 - 6. Shift.
016 - 7. Transfer.

017 - 1. True.
017 - 2. False. A one-side transfer can only move ones; a zero-side transfer is the one that moves only zeros.
017 - 3. False. Double-line transfer is often referred to as force feeding since it forces data into the receiving register regardless of its previous content.
017 - 4. True.
017 - 5. True.

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10005 530 005 8112 DIGB

MODULE 10005

DIGITAL TECHNIQUES

UNIT 5

Combination Logic and Converters

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Preface

THE PERFORMANCE of an operation within an electronic computer or switching system may require that digital quantities be compared, added, subtracted, decoded, encoded, and converted before the desired result is obtained. Combinational logic circuits are gates and inverters connected in such a way that their output is a function of the inputs to the circuit. This unit to Module 10005, *Digital Techniques,* provides a study of several combinational logic circuits which you may encounter in the maintenance of electronic equipment.

Code numbers appearing on figures are for preparing agency identification only and should be of no concern to the student.

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Acknowledgement

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Figure No.	*Title*
1-47	SN 5486, SN7486 quadruple two-input exclusive-OR gates.
1-48	SN5442, SN5443, SN5444, SN7442, SN7443, SN7444 4-line-to-10-line decoders.
1-49	S5483, N7483 four-bit binary full adder (look-ahead carry).
1-50	S5485, N7485 four-bit magnitude comparators.
1-51A	SN54150, SN54151, SN74152, SN74151, SN74152 data selectors/multiplexers.
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NOTE: In this unit, the subject matter is developed by a series of student-centered objectives. Each of these carries a three-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see whether your answers match those in the back of this unit. If your response to an exercise is incorrect, review the objective and its text.

1-1. Decoders and Encoders

Computers are designed to operate on data which is in binary form, either 1 or 0. In most computers, it is not practical to enter numbers and other information into the computer in binary form. Using binary form would require the programmer to spend too much time in the detailed effort of accurately representing large numbers of complicated alphabets and symbols.

Likewise, it is not usually desirable to present the final computer output in binary form since this would require too much time to read and interpret. Therefore, it is necessary to perform conversion on both the input and output information. Figure 1-1 illustrates this conversion.

001. Identify basic decoders with their operational characteristics.

Basic Functions. Computers are generally equipped with *encoders* (a device that codes in a group of coded signals) and *decoders* (a device that enables a system to decode a group of coded signals).

In this section, we will discuss the basic principles applicable to both devices. Since the decoding and encoding functions dealing with binary-to-decimal, binary-to-octal, and binary-to-hexadecimal coding are so similar, we will cover the characteristics applicable to decoding.

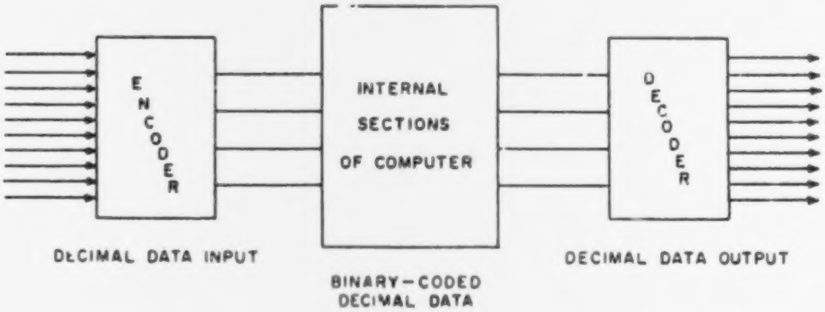


Figure 1-1. Basic principles of encoding and decoding.

In any analysis of decoding circuits, the basic thinking must be in terms of binary numbers. Positive or negative logic may be used to secure a binary output. In positive logic, the logic 1 is the most positive voltage. Logic 0 will be a voltage that is less positive than the 1 state. When negative logic is used, logic 1 is the most negative voltage output and logic 0 will be a voltage that is less negative.

You previously learned that the binary number system includes two symbols (1 and 0). The decimal system uses the digits 0 through 9, the octal system uses the numbers 0 through 7 for the eight digits, and the hexadecimal system uses numbers and letters 0 through 9 and A through F to designate the 16 digits required. The same quantity can be expressed in each of these systems using different symbols or groupings of symbols. The number 13_{10} equals 15_8, D_{16}, or 1101_2.

Converting a binary-coded output into any of the other numbering systems requires a special kind of translator called a *decoding circuit*. A decoding circuit is a device which translates a combination of input signals into one output signal. There is a converse operation, too, where we convert decimal keyboard inputs to binary combinations for storage in computer memory. We also use an *encoding circuit* to translate one of a group of signals into a combination of binary-coded signals. This objective limits the discussion to the characteristics of decoding circuits only.

Binary and decimal decoding. To illustrate how a typical decoding circuit operates, we discuss a simple example with two binary inputs. The decoder must detect all possible combinations of input conditions, and then produce a separate, distinct output for each condition. With two inputs, each having either a high or low state, the decoder must generate a minimum of four (2^2) outputs. Refer to the circuit in figure 1-2.

The simple decoding circuit in figure 1-2 has four AND-gates since it has to produce a separate output for each specific combination of inputs. Note that some of the input lines contain inverting amplifiers. These are required for correct decoder operation.

Assume that inputs "A" and "B" are both in a low state. The inputs to AG-1 are inverted to highs, causing output 1 to be high. However, gates 2, 3, and 4 each have at least one low input, causing their outputs to remain low for this particular input condition. The circuit produces a high on output 1 if, and only if, both inputs A and B are in a low state at the same time.

With another specific input condition — A input low and B input high — gate 1 has one low input (B), gate 2 has one low input (A), gate 3 has two high inputs, and gate 4 has one low input (A). With this specific input combination, only output 3 is high.

The other two possible input conditions (A high, B low; A and B both high) cause high outputs on gates 2 and 4, respectively. The circuit in figure 1-2 satisfies the definition of a decoder; it produces a single, one-of-four output for each specific input condition. Refer now to figure 1-3.

In figure 1-3, the decoder circuit is slightly modified. It still has two inputs, but uses flip-flops as input signal sources. The need for inverters is eliminated by using the "0" outputs from the flip-flops. Other than these changes, this decoder operates the same as the circuit discussed earlier.

Assume that the flip-flops are storing a binary 01; that is, F/F1 (binary 1) is set ("1" side high, "0" side low), and F/F2 (binary 2) is clear ("1" side is low and "0" side high). For this input combination, output 1 is high and the other three outputs are low, just as in the previous first example. Again, the decoder produces a single output for each of four (two flip-flops, each capable of two states) input conditions.

Now, if the basic decoding circuit is expanded to included 10 gates connected to 4 binary-coded flip-flops, a binary-to-decimal decoder is constructed. It produces a single output for each of 10 input conditions, 0 through 9. Refer to the circuit shown in figure 1-4.

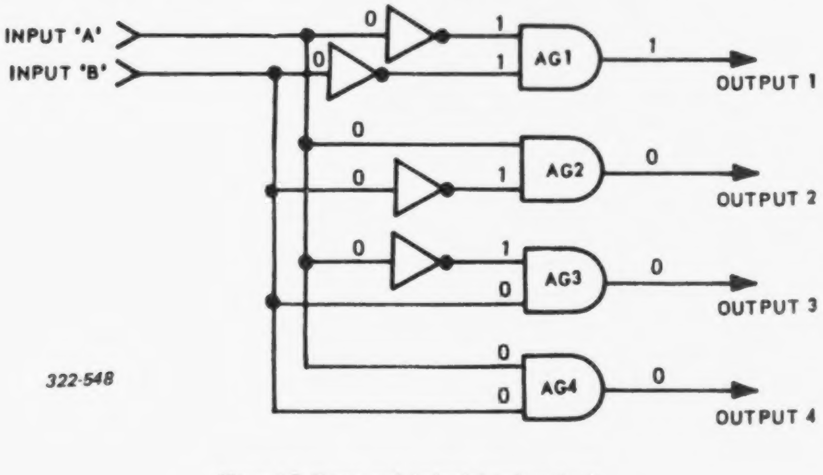
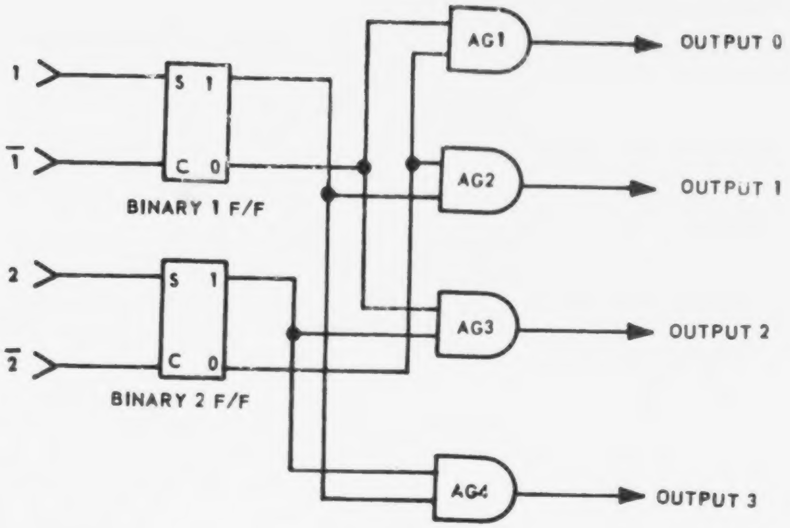
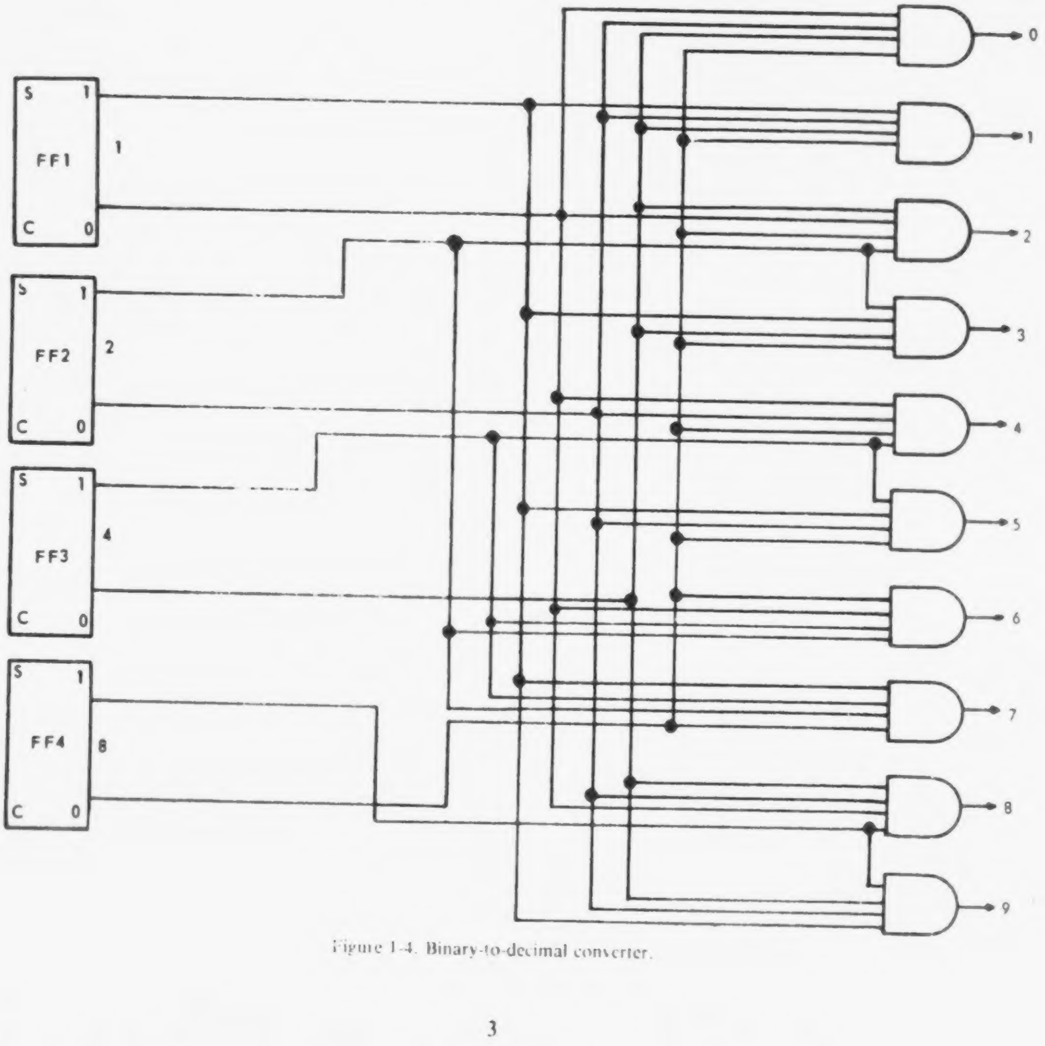


Figure 1-2. Binary and decimal decoding circuit.



AG1
OUTPUT 0
1
S 1
$\overline{1}$
C 0
AG2
OUTPUT 1
BINARY 1 F/F
2
S 1
AG3
OUTPUT 2
$\overline{2}$
C 0
BINARY 2 F/F
AG4
OUTPUT 3

Figure 1-3. Four-output decoder.



S 1
FF1
1
C 0
S 1
FF2
2
C 0
S 1
FF3
4
C 0
S 1
FF4
8
C 0
0
1
2
3
4
5
6
7
8
9

Figure 1-4. Binary-to-decimal converter.

Binary-to-octal decoding. When decoding binary digits to either octal or hexadecimal digits, the decoding gates may be of any basic type, depending upon the manufacturer of the unit. However, the most commonly used gating circuits use the inhibited AND-gate as shown in figure 1-5. This is part of a 0–7 storage register and decoder logic diagram. Remember that converting binary digits to octal digits requires the grouping of three binary digits (with the capability of 0 to 7 count) to produce one octal digit. Follow the schematic in figure 1-5 for the decoding of binary 101 to an octal output of 5 ($101_2 = 5_8$).

A simple method of analysis (and the one we use in this lesson) is to determine the requirements of the desired output and trace back to the source inputs. To produce an octal 5 from the decoder, there must be three low enabling inputs to the number 5 inhibited AND-gate. The top low input traces back to the 0 output of F/F1. It is in the *set* state; therefore, the required low is enabling the gate. The middle low input traces back to the 1 output of F/F2. It is in the *clear* state and the required low is applied to the gate. The bottom enabling low traces back to the 0 output of F/F3. The set state there produces the required enabling low and the gate requirements are met, with a 101_2 input producing a 5_8 output. To prove the truth of the circuit, trace any high output from the register to the remaining output gates. Each high disables one or more of the gates and no high output is produced.

Binary-to-hexadecimal decoding. To convert binary digits to a hexadecimal digit, again, as in the previous paragraph, you must think in terms of binary counting. Remember, it requires groupings of four binary digits to produce one hexadecimal digit. Figure 1-6 has been taken from a 0–15 storage register and decoder logic diagram. Follow the schematic in the figure as binary 1010 is decoded to the single-digit, base 16 number. Conversion of $1010_2 = A_{16}$.

Since inhibited AND-gates are also used for the outputs in this decoder, to secure a high from the A gate requires three enabling lows. The top low is traced back to flip-flop 1 where a clear state supplies the needed low from the 1 output. The middle low is supplied from the 0 side of F/F2 and the set state there meets the low requirement. The bottom low is supplied through N3 NAND-gate that is double NOTted. The low inputs to N3 are supplied by the 0 side of F/F4 (set state) and the 1 side of F/F3 (clear state). The three needed lows are supplied by the binary register when it is storing binary 1010. Any other gate is disabled by a high from one of the flip-flops.

To decode either octal or hexadecimal digits to binary digits, a reverse procedure is followed and a circuit such as figure 1-7 might be used. Notice that OR-gates are used in this circuit and this practice is common in decoding to binary digits. You should recognize this as a hexadecimal-to-binary decoder because of the 16 possible input combinations. Think in binary digits and trace a number (such as 1011_2) back to the hexadecimal input.

A circuit similar to figure 1-7 could also be used in decimal-to-binary conversion by using 10 input combinations and designing the OR-gate inputs to receive assigned decimal value voltages.

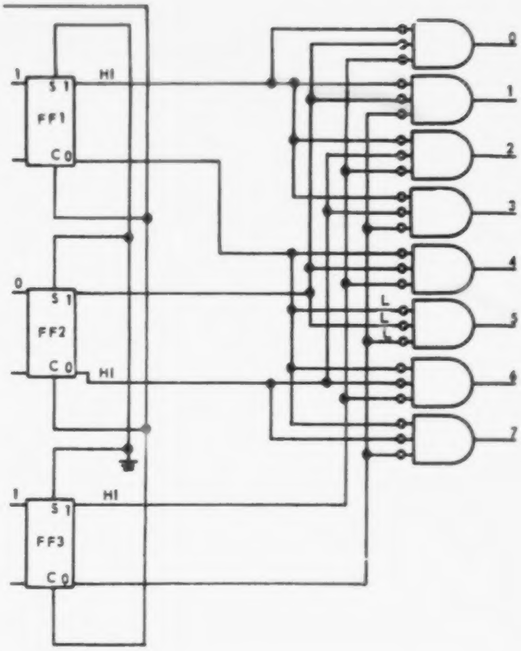


Figure 1-5. Binary register and octal decoder circuit.

Exercise (001):

1. Select the correct word from column B to complete each statement listed in column A. Each item in column B may be used only once.

Column A

(1) The 1 and 0 are the two ________ used in the binary number system.

(2) The quantities 1111_2 and F_{16} are ________ .

(3) Binary arithmetic circuits require ________ components than decimal circuits.

(4) A/An ________ circuit translates a combination of inputs into a signle one-of-a-group output.

(5) A/An ________ circuit translates one-of-a-group inputs to a combination output.

(6) The binary and decimal decoding circuit produces a low on the output of AG2, AG3, and AG4 of figure 1-2 when inputs A and B are ________ .

For questions 7 through 11 use figure 1-4 and select the flip-flops that must be set to produce the specific decimal output for the decimal numbers.

(7) 9_{10} = ________ .

(8) 1_{10} = ________ .

(9) 0_{10} = ________ .

(10) 7_{10} = ________ .

(11) 5_{10} = ________ .

(12) The register in figure 1-5 is called
(12) a ________ register.

(13) The most commonly used gate in a binary-to-octal decoder is the ________ gate.

(14) Binary digits must be in groups of ________ for conversion to octal digits.

(15) Decoding circuit analysis is most easily done by first defining the specific output ________.

(16) Conversion to a hexadecimal digit requires grouping of ________
The register in figure 1-6 is
(17) known as a ________.
________ .

(18) A high input to any gate in figure 1-6 will ________ the gate.

(19) When converting base 16, 10, or 8 digits to binary digits, the ________ gate is most commonly used.

Column B

a. Decoding.
b. Symbols.
c. Fewer.
d. Low.
e. Equivalent.
f. Encoding.
g. High.
h. Hi and lo.
i. F/F1 and F/F2.
j. F/F1 and F/F3.
k. F/F1, F/F2, F/F3.
l. F/F2 and F/F4.
m. F/F1 and F/F4.
n. F/F1.
o. None.
p. Requirements.
q. More.
r. NAND.
s. AND.
t. 3.
u. 0-5 storage.
v. 0-7 storage.
w. 5.
x. 4.
y. 7.
z. 0-15 storage.
aa. Enable.
bb. Disable.
cc. OR.
dd. NOR.

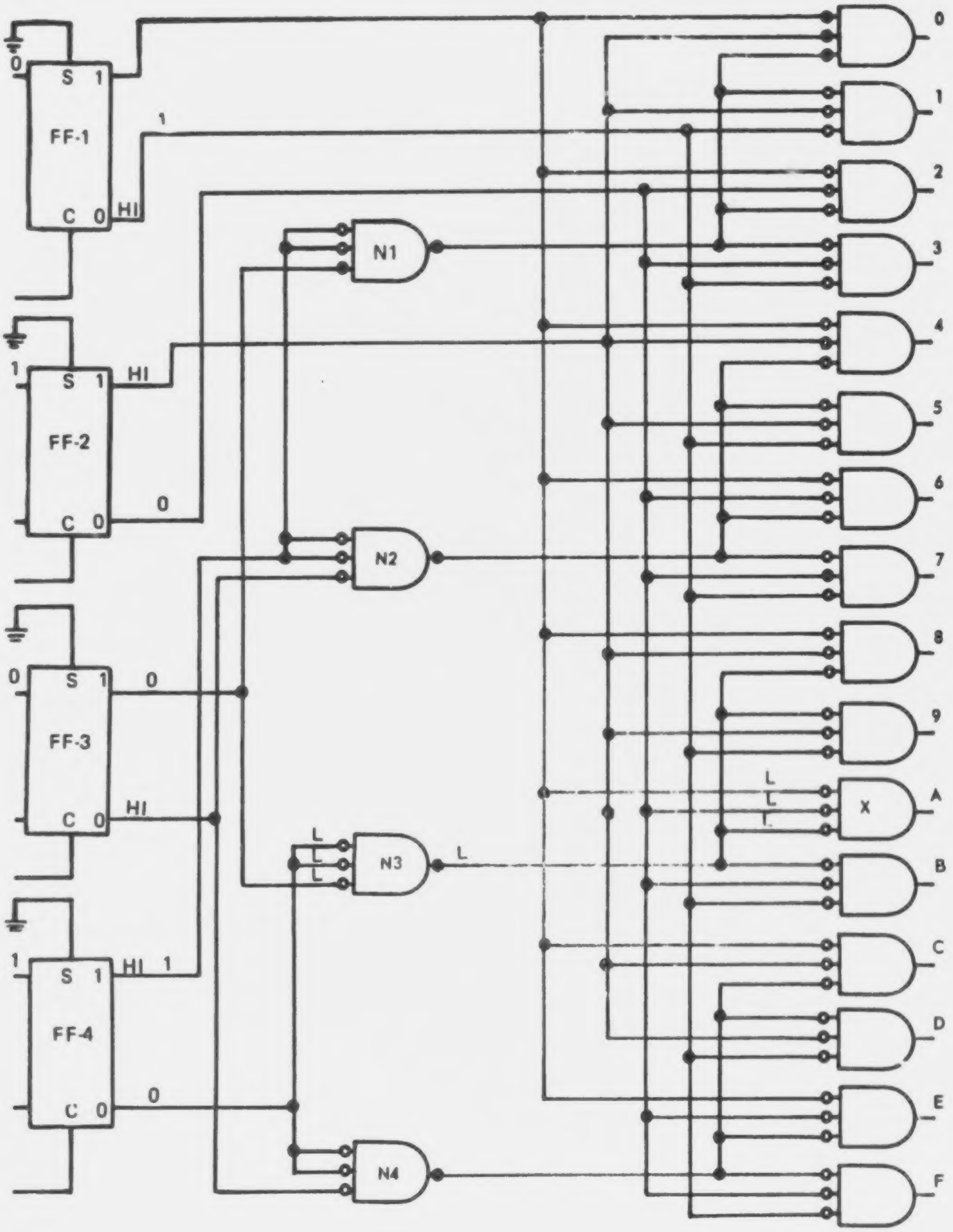

0
S 1
FF-1
C 0
HI
1
N1
1
S 1
HI
FF-2
C 0
0
N2
0
S 1
0
FF-3
C 0
HI
L
L
L
N3
L
1
S 1
HI 1
FF-4
C 0
0
N4
0
1
2
3
4
5
6
7
8
9
L
L
L
X
A
B
C
D
E
F

Figure 1-6. Binary register and hexadecimal decoder circuit.

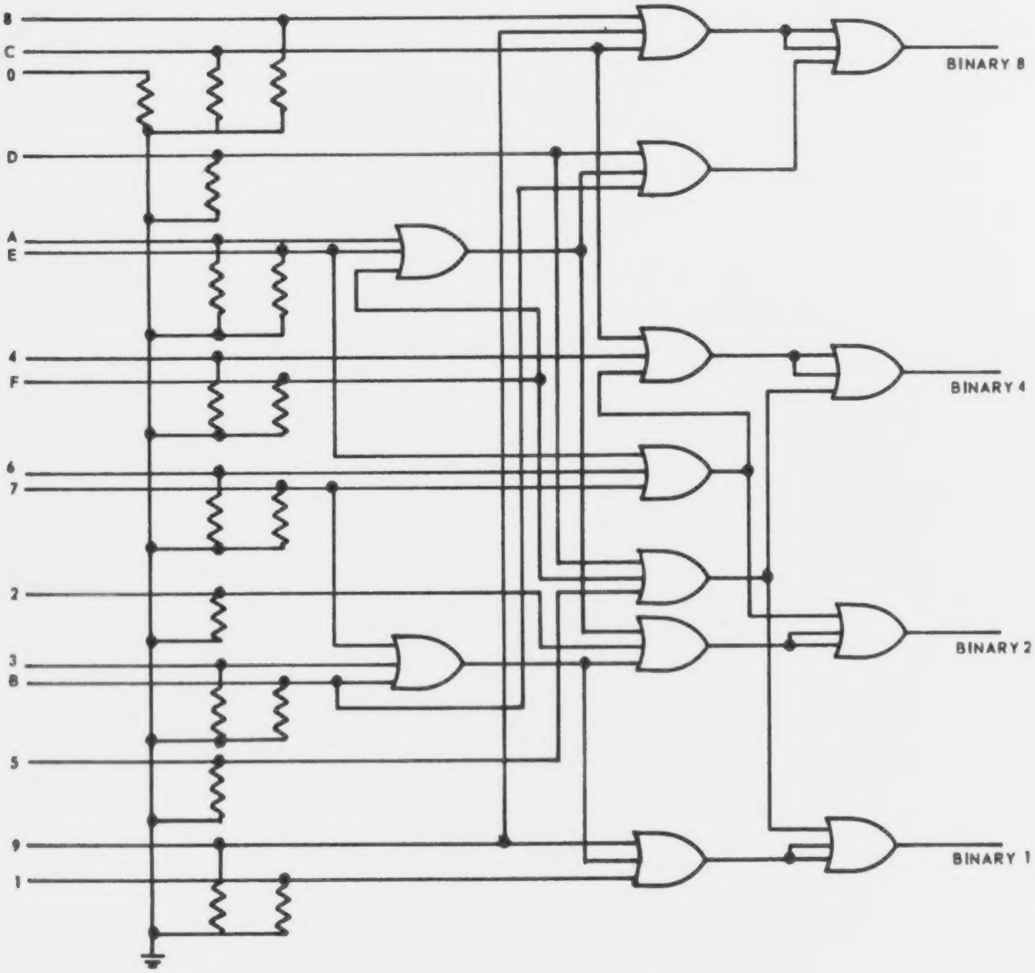

8
C
0
D
A
E
4
F
6
7
2
3
B
5
9
1
BINARY 8
BINARY 4
BINARY 2
BINARY 1

Figure 1-7. Hexadecimal-to-binary decoder.

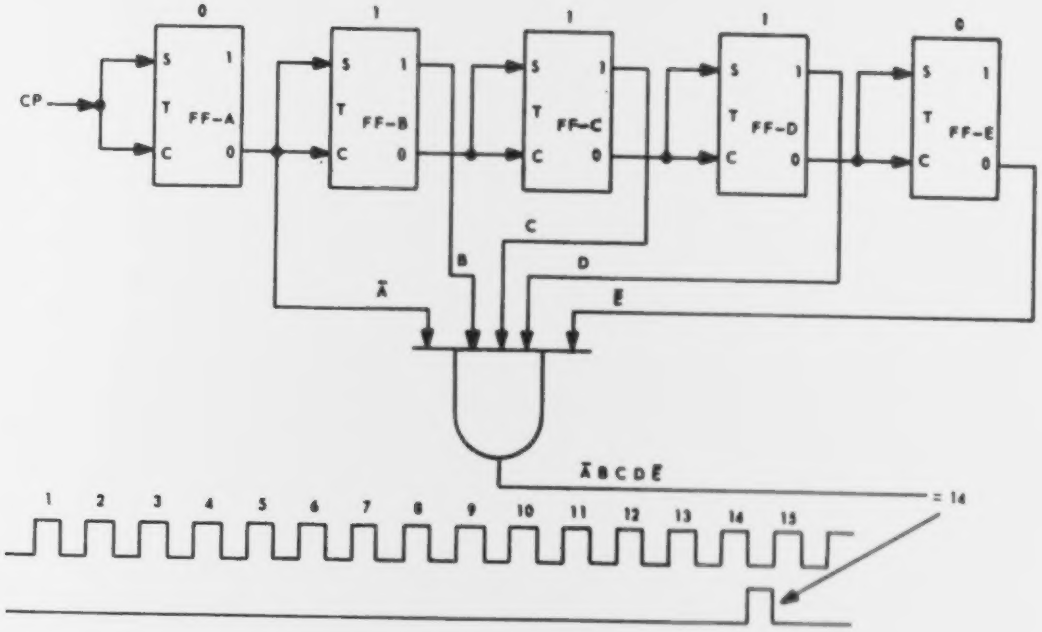

0
1
1
1
0
CP
S 1
T FF–A
C 0
S 1
T FF–B
C 0
S 1
T FF–C
C 0
S 1
T FF–D
C 0
S 1
T FF–E
C 0
C
B
D
Ā
E
ĀBCDE
= 14
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Figure 1-8. Count detection of 14.

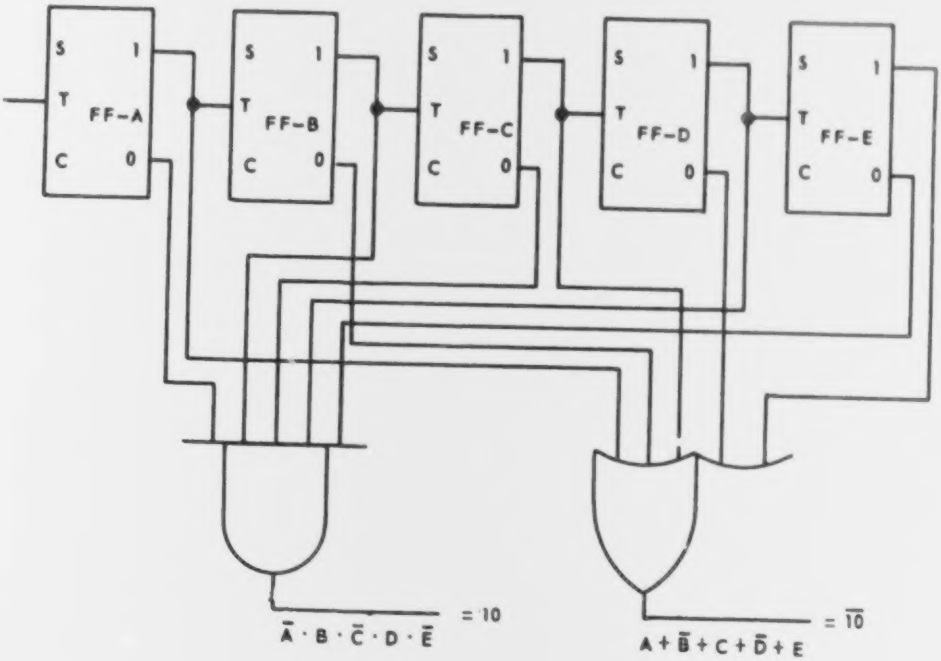

S 1
T FF–A
C 0
S 1
T FF–B
C 0
S 1
T FF–C
C 0
S 1
T FF–D
C 0
S 1
T FF–E
C 0
$\bar{A} \cdot B \cdot \bar{C} \cdot D \cdot \bar{E}$ = 10
$A + \bar{B} + C + \bar{D} + E$ = $\overline{10}$

Figure 1-9. Count detection of 10 or $\overline{10}$.

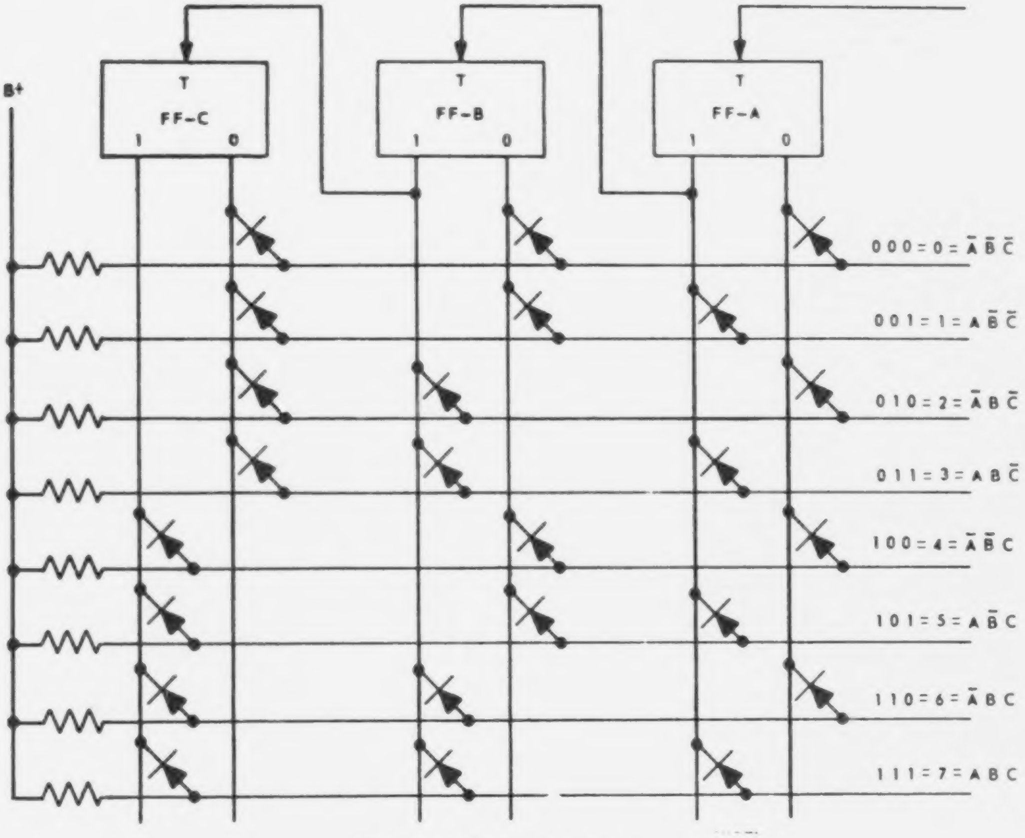

B+
T
FF-C
1
0
T
FF-B
1
0
T
FF-A
1
0
000 = 0 = $\bar{A}\,\bar{B}\,\bar{C}$
001 = 1 = $A\,\bar{B}\,\bar{C}$
010 = 2 = $\bar{A}\,B\,\bar{C}$
011 = 3 = $A\,B\,\bar{C}$
100 = 4 = $\bar{A}\,\bar{B}\,C$
101 = 5 = $A\,\bar{B}\,C$
110 = 6 = $\bar{A}\,B\,C$
111 = 7 = $A\,B\,C$

Figure 1-10. Diode matrix decoder.

002. State the operational characteristics, advantages, and disadvantages of diode- and relay-constructed decoders.

AND- and OR-Gate Decoders. Figure 1-8 shows a serial up-counter with a simple AND-gate decoder. Notice that the AND-gate produces a positive pulse output when count 14 is present in the counter. This pulse may be used for any control function that must occur at count 14.

Figure 1-9 shows the same serial counter with an AND-gate and an OR-gate. The AND-gate produces an output when the count of 10 is present in the counter; the OR-gate produces an output at all counts except the count of 10. The output from the AND-gate would most likely be used as an enabling gate for some other digital circuit. The most likely use for an OR-gate output would be as an inhibit gate to inhibit some other circuit action at the count of 10.

Although both of these examples of the use of AND- and OR-gates for decoding show their use as count detectors, this is not the only function for which they are used. By their very nature, AND- and OR-gates are primarily decoders, since they produce outputs when certain conditions exist in the equipment.

Diode Matrix Decoders. When a large number of AND- and OR-gates are used to detect a series of counts or a series of binary configurations, common practice is to show them schematically as a rectangular diode matrix. This form of circuit is shown in figure 1-10. A three-stage serial up-counter is shown connected to eight AND-gates. Each AND-gate produces a pulse of one count width when a particular count is present in the counter.

Look at the first set of diodes. The cathodes of the diodes are connected to the ZERO sides of the flip-flops. This causes a positive output to appear on the first line when the configuration 0 0 0 appears in the counter.

Now, look at the second set of diodes. They produce an output when the configuration 0 0 1 is rpesent in the counter. This configuration represents count 1; this count is expressed in Boolean notation as $A\,\overline{B}\,\overline{C}$. Notice that the cathode of the diode connected to F/FA is

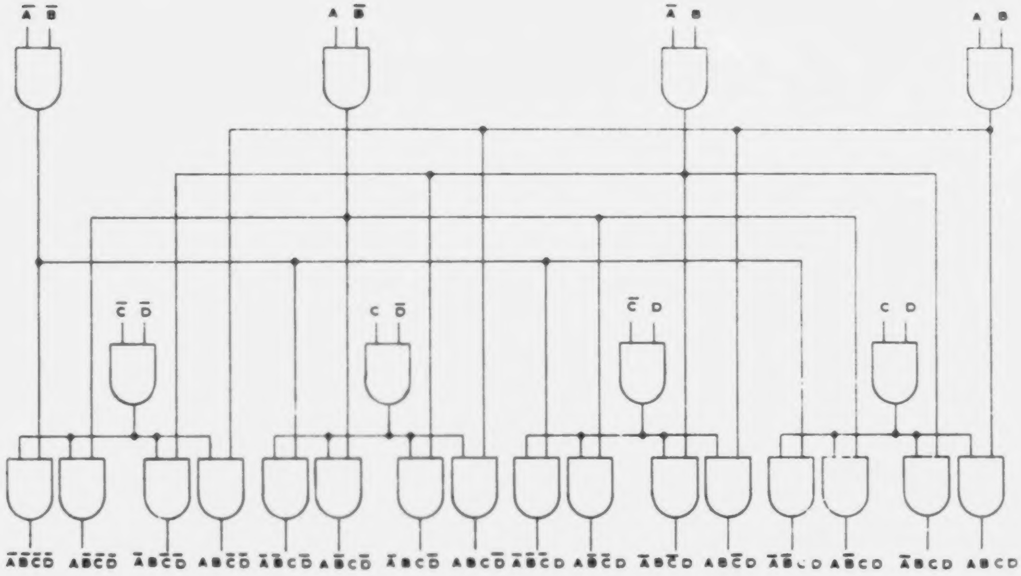

$\bar{A}\bar{B}$
$A\bar{B}$
$\bar{A}B$
AB
$\bar{C}\bar{D}$
$C\bar{D}$
$\bar{C}D$
CD
$\bar{A}\bar{B}\bar{C}\bar{D}$
$A\bar{B}\bar{C}\bar{D}$
$\bar{A}B\bar{C}\bar{D}$
$AB\bar{C}\bar{D}$
$\bar{A}\bar{B}C\bar{D}$
$A\bar{B}C\bar{D}$
$\bar{A}BC\bar{D}$
$ABC\bar{D}$
$\bar{A}\bar{B}\bar{C}D$
$A\bar{B}\bar{C}D$
$\bar{A}B\bar{C}D$
$AB\bar{C}D$
$\bar{A}\bar{B}CD$
$A\bar{B}CD$
$\bar{A}BCD$
$ABCD$

Figure 1-11. Pyramid AND-gate decoder.

connected to the ONE side, and the cathodes of the other two diodes are connected to the ZERO side of their respective flip-flops.

From the illustration, you should be able to recognize that the matrix represents eight 3-input AND-gates. Thus to detect eight different counts with this type of circuit, it requires 8 × 3 = 24 crystal diodes. For every stage added to a counter, the number of diodes required to detect all counts increases. The number required is $n \times 2^n$, where n = number of stages in the counter or register feeding the matrix. As you can see, the number of diodes required rises rapidly as the number of stages increases. For example, a 10-stage counter would require $10 \times 2^{10} = 10 \times 1024 = 10{,}240$ crystal diodes to detect all possible counts. To reduce the number of crystals required, AND-gates are often connected in the form of a pyramid. This type of arrangement is called *pyramid* AND-gates, or *treed* AND-gates.

Pyramid AND-Gate Decoders. A rectangular matrix fed by a four-stage counter requires $4 \times 2^4 = 64$ crystals to detect all possible binary configurations; however, by arranging AND-gates in a pyramid, the number of crystals required may be reduced to 48.

A pyramid AND-gate is shown in figure 1-11. Notice that the circuit consists entirely of two-input AND-gates. In this arrangement, the outputs of the two least significant counter stages (A and B) are ANDed together, and the two most significant stages (C and D) are ANDed together. This produces eight outputs, which are then ANDed together in 16 two-input AND-gates to produce 16 possible outputs. Count the number of AND-gates required to detect 16 different numbers. There are 24 of them. Since each AND-gate contains two crystals, the number of crystal diodes used is 24 × 2 = 48. By this means, the circuit elements have been reduced by 25 percent. Pyramid AND-gates are used primarily for detecting counts and for decoding multibit binary numbers.

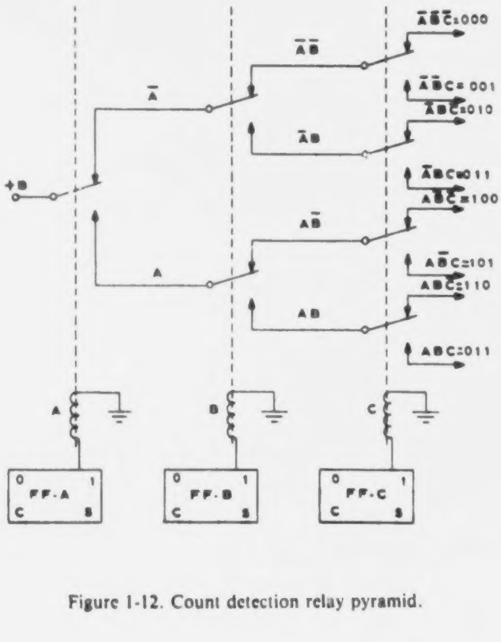

$\bar{A}\bar{B}\bar{C}$=000
$\bar{A}\bar{B}C$= 001
$\bar{A}B\bar{C}$=010
$\bar{A}BC$=011
$A\bar{B}\bar{C}$=100
$A\bar{B}C$=101
$AB\bar{C}$=110
ABC=011
$\bar{A}\bar{B}$
$\bar{A}$
$\bar{A}B$
$A\bar{B}$
A
AB
+B
A
B
C
0
1
FF-A
C
S
0
1
FF-B
C
S
0
1
FF-C
C
S

Figure 1-12. Count detection relay pyramid.

Relay Decoders. Circuits that require more current at the output than can be developed by diodes often use relays as decoders. Some of the circuits that make use of relay decoders are power controls, test function selection circuits, and print selectors where the decoded signal must determine what print on a print hammer is to strike the paper.

Figure 1-12 shows a series of relays interconnected to form a decoder. A similar circuit is used in equipment in your career ladder to select printer solenoids and, in turn, to determine what number is to be printed. Assume that the binary configuration 1 0 1 is present in the flip-flop register. Circuit actions are described in the following paragraphs.

The ONE in F/FA causes relay A to be energized, thus switching its contacts and applying B+ to line A. The ZERO in F/FB allows the B relay to remain in its deenergized state. Thus, the B+ is connected to the $\overline{B}$ line. The signal now represents A $\overline{B}$. The ONE in F/FC energizes relay C, switching the relay contacts and connecting B+ to the output line labeled A B C. Therefore, the line selected by the relay contacts has a high voltage on it, representing a ONE. If a printer solenoid is connected to each line, the binary configuration 1 0 1 selects line 5 and causes the number 5 to be printed.

Instruction (Command) Generation. Count detection networks can also be constructed to perform as an instruction generator in a computer to control the sequence of operations. One such instruction generator is shown in figure 1-13. The circuit shown consists of a counter connected to AND-gate detectors. The outputs of these AND-gates could be used in the computer to trigger certain operations in a program. Assume that the counter contains a count of zero. With this count, the zero side outputs of all three flip-flops are high.

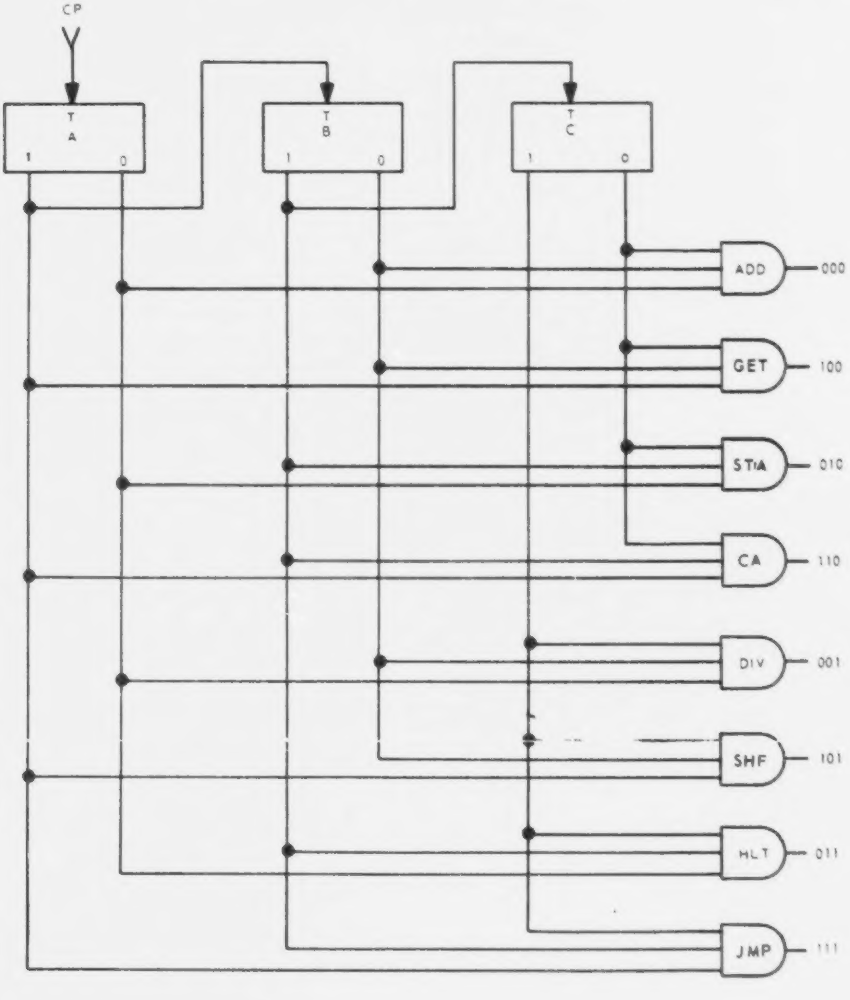


Figure 1-13. Instruction generator.

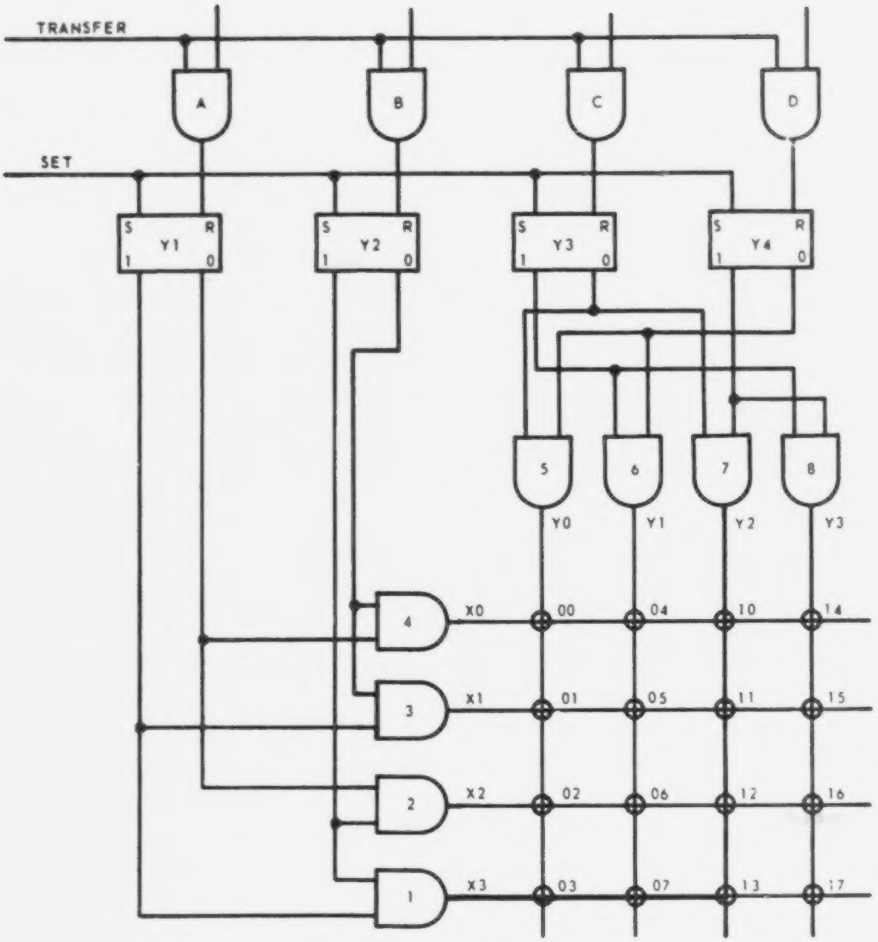


Figure 1-14. Address selection matrix.

Checking each of the gates in the matrix, the top gate is the only one that is fully satisfied. There is a high from F/FA on the bottom leg, a high from F/FB on the center leg, and a high from F/FC on the top leg. Therefore, the top AND-gate will detect a count of zero and produce a pulse output which could be used to initiate an *add* sequence in the computer.

If the counter is triggered by a clock pulse (CP), the counter will step to the next count. With a count of 1 in the counter, the only gate that is satisfied is the one labeled "GET." If you continue through the operation, you will see that only one gate will produce an output at any one time.

Address Detection. A logic diagram of a simple address selection matrix is shown in figure 1-14. The four-bit address register is capable of storing each of the memory addresses $00_{(8)}$ through $17_{(8)}$. Flip-flops Y3 and Y4, along with detectors 5 through 8, are used to select the Y coordinate. Flip-flops Y1 and Y2, along with detectors 1 through 4, select the X coordinate. The intersection of the X and Y lines identifies the address location. For example, insert the binary address 1101, which is 15 octal, into the Y register. With flip-flops Y1, Y3, and Y4 set, AND-gates 3 and 8 until they intersect. Memory address $15_{(8)}$ is selected. Note that this is the same address as was loaded into the Y register.

Exercises (002):

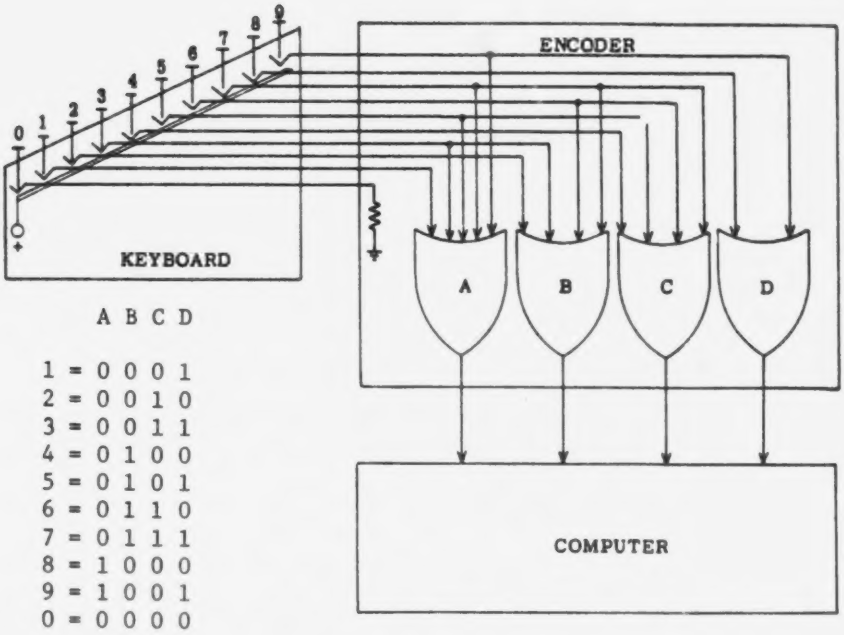
1. Using figure 1-8, write the Boolean equation for the AND-gate if the circuit were to be designed to detect count 12.

2. On figure 1-9, when will the OR-gate produce a high?

3. How many crystal diodes would be required to represent all possible counts if the counter shown in figure 1-10 were expanded to six stages?

4. What is the advantage of a pyramid AND-gate decoder over a diode matrix?

5. When would a relay pyramid be used?



	A	B	C	D
1 =	0	0	0	1
2 =	0	0	1	0
3 =	0	0	1	1
4 =	0	1	0	0
5 =	0	1	0	1
6 =	0	1	1	0
7 =	0	1	1	1
8 =	1	0	0	0
9 =	1	0	0	1
0 =	0	0	0	0

Figure 1-15. Encoder.

003. Given a schematic diagram of an encoder, state the function of the circuit and the output states of its OR-gates under given conditions.

Encoders. The encoder is a network or system of gates in which only one input is excited at a time and each input produces a combination of outputs. The encoder is not to be confused with the decoder taken up in the previous material. The decoder translates the computer language to some conventional form, such as the decimal numbering system. The encoder translates conventional forms of information (such as the decimal numbering system) into a form acceptable by the computer.

Figure 1-15 illustrates a simple encoder. The input to the encoder is a keyboard whereby the operator can insert decimal numbers into the computer. As the keys are depressed, the spring contact moves down and makes contact with the bar with the positive potential applied. The spring contact then passes the positive potential to the encoder. The encoder unit takes the output from the decimal keyboard and converts the decimal number to an equivalent binary number. The computer can then process the binary number as programmed.

For example, let's assume that the number 6 key is depressed. This causes a positive potential to leave the keyboard and enter the encoder. Analyzing the encoder, note that only OR-gates B and C receive the positive potential. Thus, OR-gate A has a LOW output, OR-gate B has a HIGH output, OR-gate C has a HIGH output, and OR-gate D has a LOW output. With OR-gate A as the LSD, the output is 0 1 1 0, which equals a binary 6.

Remember that an encoder is a device usually found at the input of a system designed to convert the input information into a form acceptable by the system.

Exercises (003):

1. Use the schematic diagram in figure 1-15. What is the function of this encoder circuit?

2. What is the output operational state of each OR-gate in the encoder with a keyboard selection of 7?

1-2. Adders and Subtractors

This section will discuss the mechanization and operation of single and multistage adders and subtractors. The discussion will include serial and parallel borrow structures, end-around carry, end-around borrow, and sectionalized multistage adders and subtractors.

004. Define different types of adders, state adder circuit characteristics, and solve problems involving adders.

Types of Adders. An adder may be defined as a computer device that can form the sum of two or more numbers or quantities. Hence, a binary adder is a circuit that can combine two or more binary numbers in such a fashion as to produce a sum.

Quarter-adder. A study of the truth table for the exclusive-OR circuit reveals that, if carries are ignored, the circuit functions as an adder, producing a summation of its inputs. For example:

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 0$$

In the last equation, the sum is actually $10_{(2)}$ (a summation of 0 and a carry of 1). However, no provisions are made for dealing with the carry, so it is ignored or dropped.

The mechanization and operation of exclusive-OR circuits (sometimes referred to as *quarter-adders)* was covered in unit 3.

Half-adder. The first form of half-adder to be considered is that used in serial-adders. Such a circuit is shown in figure 1-16,A. Figure 1-16,B, is the truth table for the circuit. A study of this truth table reveals that the circuit is actually an exclusive-OR circuit configured to produce both a sum (S) and a carry (C) output.

Figure 1-17,A, is the more conventional representation of a half-adder and is the circuit commonly used in parallel-adders. Figure 1-17,B, is the truth table for this circuit; as you can see, it is identical to the one shown in figure 1-16,B. Hence, this circuit is also an exclusive-OR circuit modified to produce both a sum (S) and carry (C) output. Since flip-flops usually serve as the input source for this circuit, both X and Y and their complements are readily available. Hence, there is no need to provide a means for complementing any of the inputs in order for the circuit to function properly.

Full-adder. A full-adder considers the possibility of a carry from a previous column. Figure 1-18 shows that a full-adder, in effect, consists of two half-adders. One half-adder adds the addend and augend in a particular column. The other half-adder adds the resulting sum to a carry from the previous stage. As a result of these two additions, a sum-and-carry output are produced for that particular column. A truth table for a full-adder with three inputs is shown in table 1-1. The truth table shows that there are four combinations that produce a sum with no carry and four combinations that produce a sum and carry. They are as follows:

Sum with 0 carry = $\overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C$
Sum with 1 carry = $ABC + AB\overline{C} + A\overline{B}C + \overline{A}BC$

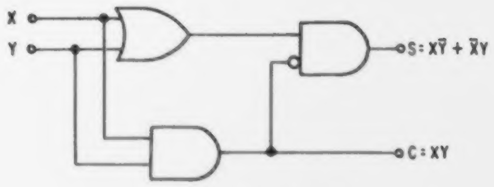
In order for the computer to add numbers containing several binary bits, it is necessary to connect adder stages together. The method of connecting the adders is determined by the particular computer requirements. They can be connected in parallel, serial, or a combination of the two. Parallel operation offers the advantage of higher processing speeds while serial operation requires less circuitry. In parallel operation, the numbers are added in all columns at the same time. In serial operation, each column of the two numbers is added sequentially.

Serial-adder. The full-adder circuit shown in figure 1-19 is designed to advance a carry (in serial-addition) through as many columns as necessary. This action is accomplished by circulating a carry digit through the carry feedback circuit (A2, CR2, and D1) each time a 1 condition exists at the A2 output. The following example will illustrate this feature.

Consider the addition of 111 and 011, as shown. The serial columns are applied at times t_0, t_1, and t_2, respectively. OR circuit, G1, produces a 111 input to one terminal of the inhibitor, I1, with one pulse applied during each time interval. AND circuit, A1, produces an inhibitory input to I1 during time intervals t_0 and t_1 so that the output of I1 is 100.

The carry digits (011) from A1 are also fed through CR1 (an isolating diode) to delay line, D1, where each digit is delayed one bit time. The output (110 corresponding to time intervals t_2, t_1, t_0, reading from right to left) is applied to the lower input terminal of G2, causing the output of this circuit to be 110 during the time intervals shown.

Note that the input to G2 during the intervals t_2, t_1, and t_0 is also applied to one terminal of AND circuit A2, and that the first carry output (110) is applied to the other terminal. Thus, A2 produces a 100 output during intervals t_2, t_1, and t_0.

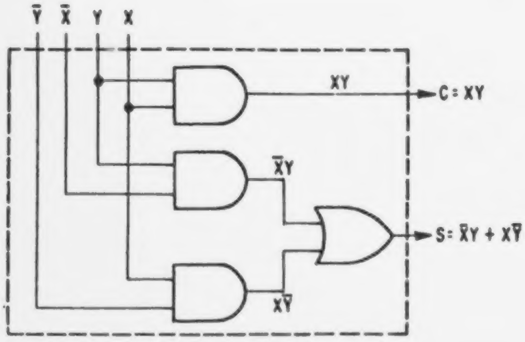


A. LOGIC DIAGRAM

INPUTS		OUTPUTS	
X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

B. TRUTH TABLE

Figure 1-16. Half-adder used in serial addition circuit.



A. LOGIC DIAGRAM

INPUTS		OUTPUTS	
X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

B. TRUTH TABLE

Figure 1-17. Half-adder used in parallel addition circuit.

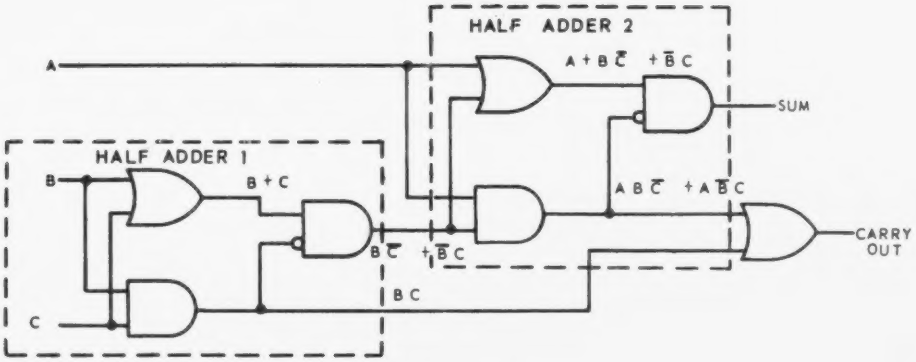

HALF ADDER 2
A
$A + B\overline{C} + \overline{B}C$
SUM
HALF ADDER 1
B
$B + C$
$AB\overline{C} + A\overline{B}C$
CARRY OUT
$B\overline{C} + \overline{B}C$
BC
C

Figure 1-18. Full-adder.

TABLE 1-1

TRUTH TABLE FOR FULL ADDER

Boolean	$\overline{ABC}$	$A\overline{BC}$	$\overline{A}B\overline{C}$	$\overline{AB}C$	ABC	$AB\overline{C}$	$A\overline{B}C$	$\overline{A}BC$
Augend A	0	1	0	0	1	1	1	0
Addend B	0	0	1	0	1	1	0	1
Carry In C	0	0	0	1	1	0	1	1
Sum	0	1	1	1	1	0	0	0
Carry	0	0	0	0	1	1	1	1

The 1 output of A2 during period t_2 causes the 1 input to I2 during the t_2 interval to be inhibited, and the output of I2 during this period is 0. The I2 during intervals t_0 and t_1 appears uninhibited. Thus, the output from t_2 t_0 is 010.

The presence of a 1 in the A2 output indicates that a carry is yet to be added to one of the remaining columns before the true sum can be produced. The carry digit is fed through CR2 to D1, where it is delayed and shifted into the period t_3. The second output of D1 (shown as

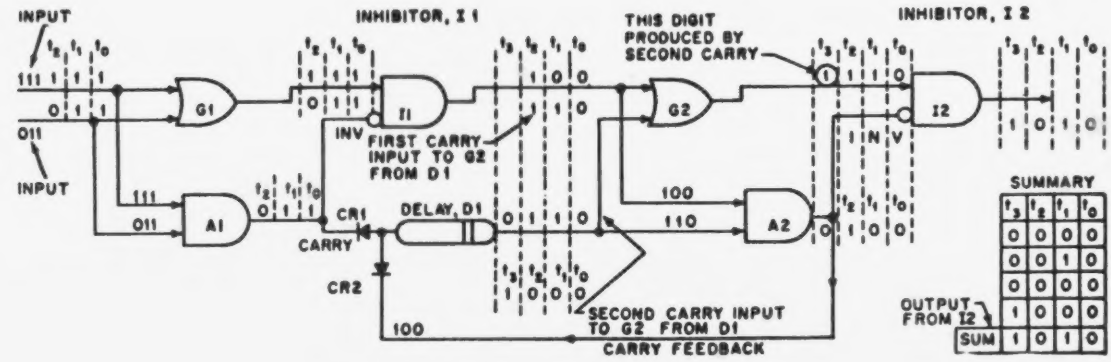


Figure 1-19. Serial-adder for accumulating multiple-carry digits.

the second carry input to G2) is passed through G2 during the t_3 interval and combined with the serial train already at the output. This action produces the true sum (1010) of the binary inputs at G1. Note that a carry has been advanced from the first column to the fourth. In a similar manner, this circuit can advance the carry through any number of columns as required.

Parallel-adder. Figure 1-20 shows several half-adders connected to add binary numbers in parallel. This means that all the bits of a binary number in one register may be added to all the bits of a binary number in another register at the same time. The inputs A1, A2, A3, and A4 represent the outputs from one register (A register). Inputs B1, B2, B3, and B4 represent the outputs from the other register (B register).

The voltage levels of these inputs are gated through the adder and a resultant binary sum is sensed at the output gates which are marked "sum 1, sum 2, sum 3, and sum 4." An output at the carry gate indicates a carry from the MSD position. This carry is either added to the next stage or to the LSD, depending upon the design of the adder. Note that the inputs in figure 1-20 are as follows:

A = 1011 B = 1001 Sum = 10100

The inputs A1 and B1 are added together, and the result is felt at the output of AND-gate D as a zero for sum 1. Also, the binary one output from AND-gate E indicates a carry being generated from bits A1 and B1. This carry is applied to OR-gate F and AND-gate K. Bits A2 and B2, both being a binary zero, result in a zero from AND-gate J. This zero is added with the carry from bits A1 and A2 at AND-gate K, giving a zero output from AND-gate K. OR-gate F is activated by the carry from AND-gate E. Gate G is enabled by the binary one output from OR-gate F and the binary zero output from AND-gate K. This gives a result of one for sum 2. Gate M will have a zero output because both inputs are low.

Bits A3 and B3 result in a zero output from AND-gate T and one from OR-gate Q. These signals satisfy AND-gate R to produce a binary one output. Gate S is inhibited by the binary zero from gate M and gate N is enabled by the binary one from gate R. This combination results in a binary one output for sum 3. Gate U has a binary zero output which results in zero carry to the next higher stage. Bits A4 and B4, both being binary ones, result in a binary one output from gates X and C1. The binary one from gate C1 inhibits one leg of gate Y which, in combination with the zero carry from the previous stage, will result in a binary zero for sum 4. The binary one from gate C1 causes AND-gate D1 to produce a carry of one to the next higher stage. The sum outputs will be recorded in another register or be force fed back into either the A or B register for temporary storage. The number of bits which can be added at any one time is determined only by the amount of circuitry in the adder.

Exercises (004):

1. Define adder.

2. What is a half-adder?

3. What constitutes a full-adder?

4. What type of adder requires a delay line?

5. What causes overflow?

6. The following questions are based on the operation of the full-adder shown in figure 1-19. Assume that the inputs to the adder are:

	t_3	t_2	t_1	t_0
Upper input	0	1	1	0
Lower Input	0	0	1	0

   a. What is the output of A1 at t_2, t_1, and t_0, respectively?

   b. What are the upper and lower inputs, respectively, to A2 and t_2?

   c. A carry is generated at the output of A2 and is fed back to G2 through delay D1. When does it appear at the lower input to G2?

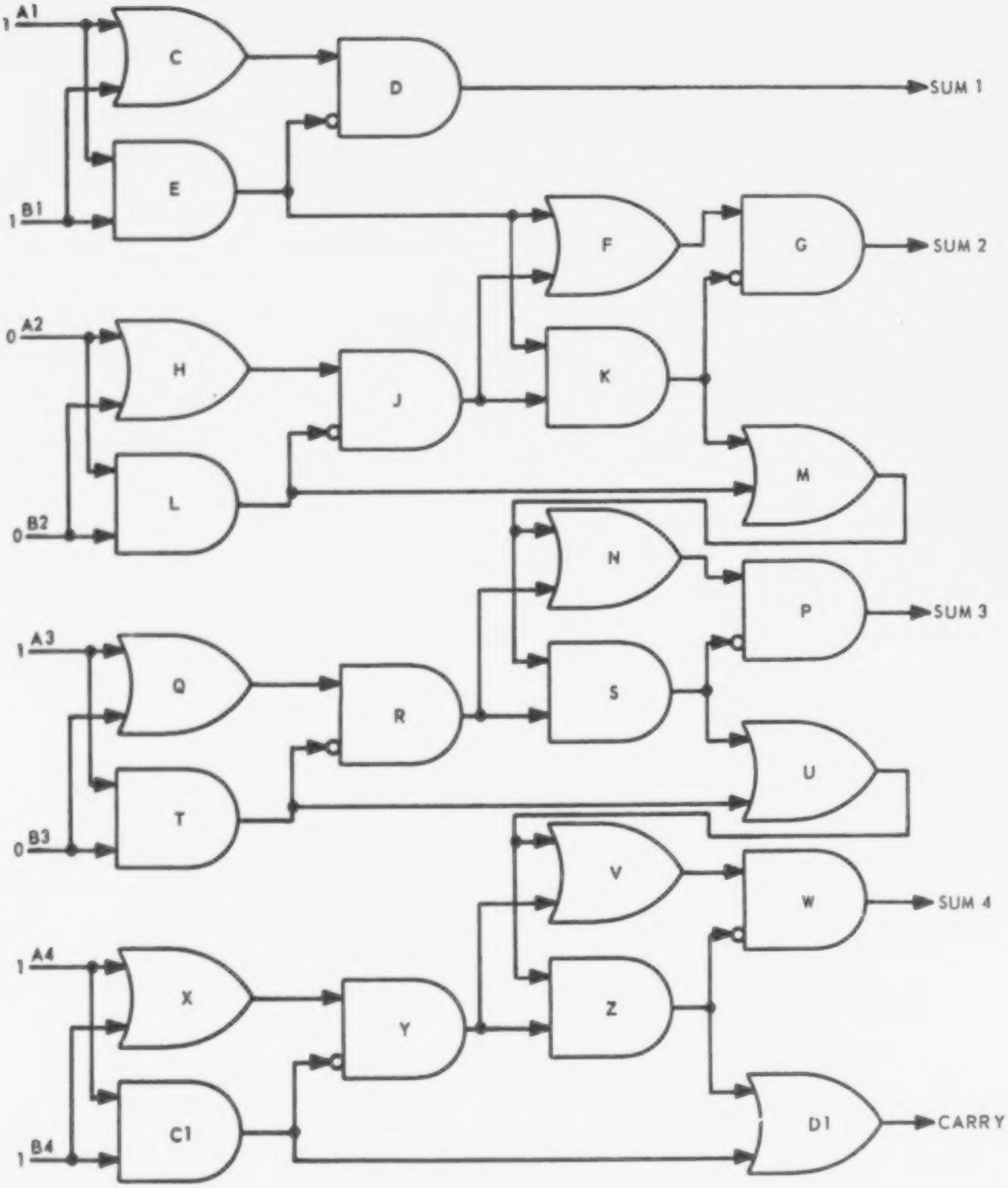

1 A1
1 B1
0 A2
0 B2
1 A3
0 B3
1 A4
1 B4
C
D
E
F
G
H
J
K
L
M
N
P
Q
R
S
T
U
V
W
X
Y
Z
C1
D1
SUM 1
SUM 2
SUM 3
SUM 4
CARRY

Figure 1-20. Parallel-adder.

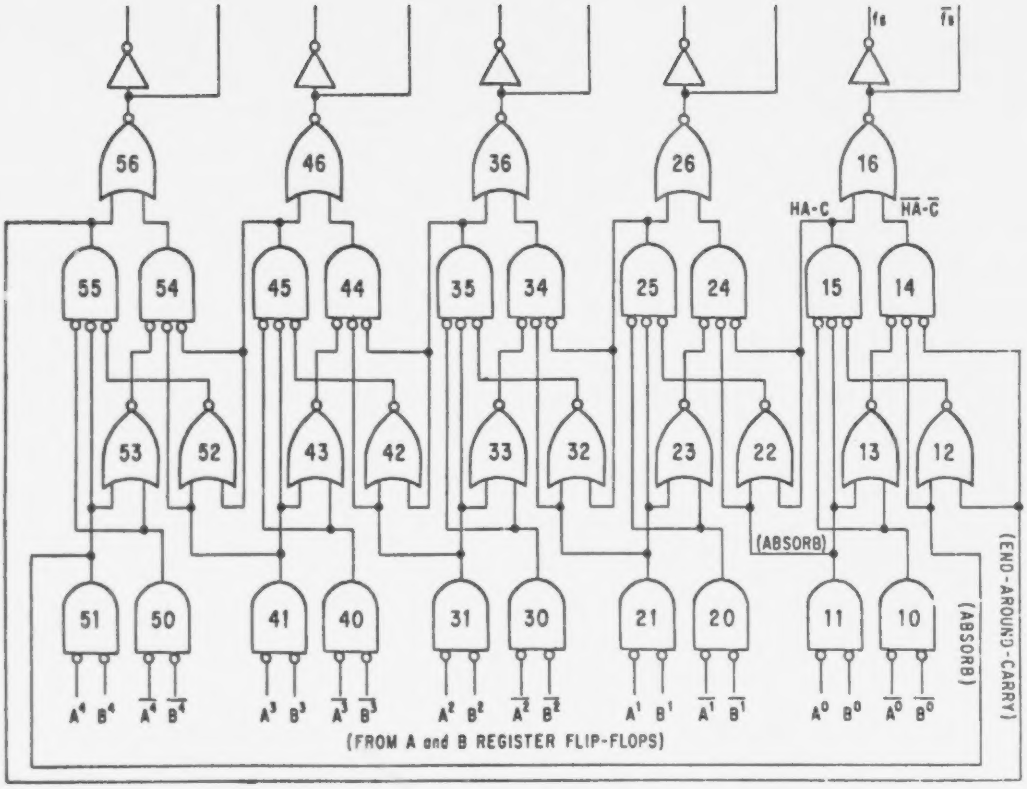

fs
$\overline{fs}$
56
46
36
26
16
HA-C
$\overline{\text{HA-C}}$
55
54
45
44
35
34
25
24
15
14
53
52
43
42
33
32
23
22
13
12
(ABSORB)
51
50
41
40
31
30
21
20
11
10
(ABSORB)
(END-AROUND-CARRY)
A^4 B^4 $\overline{A^4}$ $\overline{B^4}$
A^3 B^3 $\overline{A^3}$ $\overline{B^3}$
A^2 B^2 $\overline{A^2}$ $\overline{B^2}$
A^1 B^1 $\overline{A^1}$ $\overline{B^1}$
A^0 B^0 $\overline{A^0}$ $\overline{B^0}$
(FROM A and B REGISTER FLIP-FLOPS)

Figure 1-21. Adder circuit utilizing a serial carry structure.

		Ci							Co				
A^0	B^0	51	55	10	12	13	14	16	11	15	fs	INPUT	OUTPUT
0	0	0	0	0	0	1	1	1	1	0	1	$\bar{A}$ $\bar{B}$ Ci	fs $\overline{Co}$
0	0	0	1	0	1	1	0	0	1	0	0	$\bar{A}$ $\bar{B}$ $\overline{Ci}$	$\overline{fs}$ $\overline{Co}$
0	0	1	0	0	1	1	0	0	1	0	0		
0	0	1	1	This Combination Cannot Exist									
0	1	0	0	0	0	0	0	0	0	0	0	$\bar{A}$ B Ci	$\overline{fs}$ Co
0	1	0	1	0	1	0	0	1	0	1	1	$\bar{A}$ B $\overline{Ci}$	fs $\overline{Co}$
0	1	1	0	0	1	0	0	1	0	1	1		
1	0	0	0	0	0	0	0	0	0	0	0	A $\bar{B}$ Ci	$\overline{fs}$ Co
1	0	0	1	0	1	0	0	1	0	1	1	A $\bar{B}$ $\overline{Ci}$	fs $\overline{Co}$
1	0	1	0	0	1	0	0	1	0	1	1		
1	1	0	0	1	0	1	1	1	0	0	1	A B Ci	fs Co
1	1	0	1	1	1	1	0	0	0	0	0	A B $\overline{Ci}$	fs Co
1	1	1	0	1	1	1	0	0	0	0	0		

Figure 1-22. Listing of possible conditions for stage 2°.

005. Explain the operation of adders using serial carry by identifying the outputs for specified conditions.

Serial-Adders. Adders may be designated with either serial or parallel carry structures. Each has its own advantages and disadvantages. Serial structures are perhaps the easiest and least expensive to mechanize, primarily because they require that a carry generated in one stage of the adder be carried only to the next higher order stage (or, in the case of end-around carry, from the highest order stage to the lowest order stage).

Figure 1-21 shows an adder using a serial carry structure with provisions made for end-around carry. Since, in this circuit, the adder inputs are connected directly to the outputs of the A and B registers with no provisions made for gating the signals, the fs outputs of the adder should at all times reflect a summation of the values contained in the registers.

For example, assume that the values presently contained in the registers are A = 10101_2 and B = 10111_2. With these values in the registers, the following flip-flops will be set: A^4, A^2, A^0, B^4, B^2, B^1, and B^0. When these flip-flops are set, they will cause HIGHS to appear at the following adder inputs: A^4, B^4, $\overline{A}^3$, $\overline{B}^3$, A^2, B^2, $\overline{A}^1$, B^1, A^0, and B^0. Now we will examine how the addition is accomplished by the adder circuit. (NOTE: The operation of all stages of the adder is interdependent and simultaneous. That is, the operation of each stage of the adder is dependent on the next lower order stage and, since the carry structure forms a closed loop due to the provisions made for end-around carry, the operation of each stage is to a degree dependent on the operation of all other stages. Since each stage of the adder operates in a like fashion, only the operation of one stage will be described in detail.)

Consider now the operation of stage 2^0 of the adder. The HIGHS at A^0 and B^0 inputs are applied to AND-gate 11, causing it to be disabled and have a LOW output. This LOW is applied directly to OR-gate 13 and to AND-gate 15. This LOW has no effect on the operation of OR-gate 13; however, it serves as a partial enable to AND-gate 15.

Consider now the LOWS at the $A^{\overline{0}}$ and $B^{\overline{0}}$ inputs. These LOWS fully enable AND-gate 10, causing it to have a HIGH output. This HIGH is applied directly to OR-gate 13 and to AND-gate 15. This HIGH enables OR-gate 13, causing it to output a HIGH, and will disable AND-gate 15, causing it to have a low output.

The inputs to OR-gate 12 are initially assumed to be LOW. With LOWS at both inputs, OR-gate 12 will be disabled and output a HIGH. The LOWS at the inputs to OR-gate 12 will be disabled and output a HIGH. The LOWS at the inputs to OR-gate 12 serve as enabling inputs to AND-gate 14. The LOW output from OR-gate 13 provides an enable for AND-gate 14. AND-gate 14 is now fully enabled, causing it to have a HIGH output.

The LOW output from OR-gate 12 will have no effect on the operation of AND-gate 15, since it was already disabled by the HIGH from AND-gate 10. The LOW from AND-gate 15 has no effect on the operation of OR-gate 16. The HIGH from AND-gate 14, however, will enable OR-gate 16, causing it to have a LOW output. This LOW will provide the fs output for stage 2^0. The LOW at the output of OR-gate 16 is, in turn, inverted to a HIGH by the inverter/amplifier to provide the fs output for the stage.

The summation provided by this stage is as follows:

$$\begin{array}{rl} 1 & A^0 \\ \underline{+1} & B^0 \\ 10 & \\ \underline{+1} & \text{end-around carry} \\ \underline{1}1 & \text{fs} \\ & \text{carry to next stage} \end{array}$$

Hence, under the conditions described, stage 2^0 will provide a summation of 1 and carry of 1.

Stage 2^1, in like fashion, provides the following summation:

$$\begin{array}{rl} 0 & A^1 \\ \underline{+1} & B^1 \\ 1 & \\ \underline{+1} & \text{carry from previous stage} \\ \underline{1}0 & \text{fs} \\ & \text{carry to next stage} \end{array}$$

Stage 2^2 provides:

$$\begin{array}{rl} 1 & A^2 \\ \underline{+1} & B^2 \\ 10 & \\ \underline{+1} & \text{carry from previous stage} \\ \underline{1}1 & \text{fs} \\ & \text{carry to next stage} \end{array}$$

Stage 2^3 provides:

$$\begin{array}{rl} 0 & A^3 \\ \underline{+0} & B^3 \\ 0 & \\ \underline{+1} & \text{carry from previous stage} \\ \underline{0}1 & \text{fs} \\ & \text{carry to next stage} \end{array}$$

Stage 2^4 provides:

$$\begin{array}{rl} 1 & A^4 \\ \underline{+1} & B^4 \\ 10 & \\ \underline{+0} & \text{carry from previous stage} \\ \underline{1}0 & \text{fs} \\ & \text{carry to next stage} \end{array}$$

Presented in more conventional form, the adder provides the following summation:

$$\begin{array}{rl} 111 & \text{— carry} \\ 10101_2 & \text{A} \\ +\,10111_2 & \text{B} \\ \hline 101100 & \\ \\ +\qquad 1 & \text{end-around carry} \\ \hline 01101_2 & \text{fs} \end{array}$$

NOTE: Since an end-around carry was, in fact, developed, the initial assumption with respect to the inputs to OR-gate 12 is correct.

In an adder using a serial carry structure, such as the one shown in figure 1-21, the possibility arises that a false carry may be generated. For example a carry stage 2^0 is indicated whenever the output of AND-gate 15 is LOW. Now consider that the output of AND-gate 15 will be LOW for either of the following conditions: $A^{\overline{0}}B^{\overline{0}}$ or A^0B^0. The condition A^0B^0 is the one that generate a carry. The condition of $A^{\overline{0}}B^{\overline{0}}$, therefore, generates a false carry. If provisions are not made to prevent the false carry from getting to the next higher order stage, the false carry will be treated as a carry. In this case, the output of AND-gate 11 is used for this purpose. That is, the output of AND-gate 11 is used as a gating or absorb signal to condition the higher order stage so that it will accept or absorb only the proper carry. Figure 1-22 lists all possible conditions that could exist for stage 2^0 of the adder shown in figure 1-21.

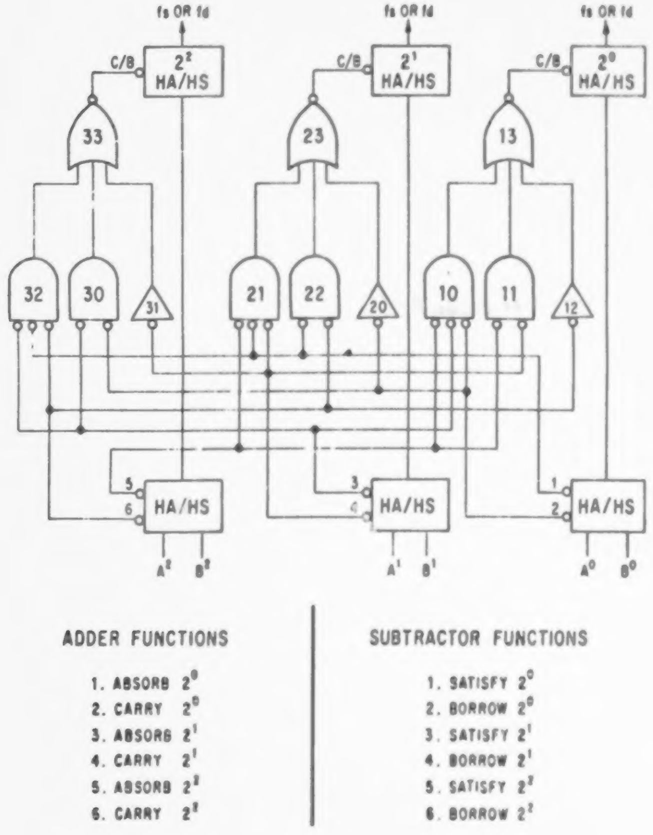

fs OR fd
C/B
2²
HA/HS
2¹
2⁰
33
23
13
32
30
31
21
22
20
10
11
12
5
6
3
4
1
2
HA/HS
A²
B²
A¹
B¹
A⁰
B⁰
ADDER FUNCTIONS
1. ABSORB 2⁰
2. CARRY 2⁰
3. ABSORB 2¹
4. CARRY 2¹
5. ABSORB 2²
6. CARRY 2²
SUBTRACTOR FUNCTIONS
1. SATISFY 2⁰
2. BORROW 2⁰
3. SATISFY 2¹
4. BORROW 2¹
5. SATISFY 2²
6. BORROW 2²

Figure 1-23. Parallel carry/borrow structure.

The use of a serial carry structure in an adder results in a problem known as the carry-ripple problem. This problem exists because the carry, when generated, must be advanced through each stage of the adder until it is absorbed, and it requires a somewhat fixed time for each stage to respond to its inputs. Thus, the more stages involved, the longer it will take for the adder to stabilize and present a reliable output. It can thus be seen that there are two factors determining the minimum time that must be allowed for such an adder to stabilize. These are average response time per stage and the number of stages.

Many schemes have been devised to overcome the carry-ripple problem, among which are the use of parallel carry structures. This method will be discussed in the next objective.

Exercises (005)

Questions 1 through 5 are based on the operation of the adder circuit, figure 1-21. Assume the following inputs: A = 11011 and B = 10011.

1. What is the output of AND-gate 15?

2. AND-gate 25 will have, after inversion, a 0 from OR-gate _______ and AND-gate _______ and a 1 from AND-gate _________ .

3. The output of AND-gate _________ is used as an absorb signal from stage 2^2.

4. In an end-around carry circuit, the carry from the AND-gate _________ is applied to OR-gate 12 and _________ _________ .

5. The output A^0B^0 generates a _________ from _______________ _______________ .

6. The use of serial carry results in a problem known as _________ _________ .

006. Concerning the operation of adders using parallel carry, identify inputs, outputs, and signal applications.

Parallel-Adders. In an adder using a parallel carry structure, a carry generated in one stage of the adder is simultaneously presented to all other stages. Then, depending on the conditions existing in each of the other stages, the carry may be absorbed by one or more of them.

Figure 1-23 depicts a three-stage adder/subtractor that uses a parallel carry/borrow structure. When operating as an adder, the circuit will function as in the following examples.

Example 1: Assume that the values to be added are:

$$A = 000_2$$
$$B = 000_2$$

With these values in the A and B registers, circuit conditions will be as indicated in the first row of the table shown in figure 1-24.

Referring to figure 1-242, columns A^2, B^2, A^1, B^1, A^0 and B^0 are the inputs to the half-adder at the bottom of figure 1-23. Columns 1 through 6 are the half-adder outputs. Columns 10, 11, 12, 13, 20, 21, 22, 23, 30, 31, 32, and 33 refer to the outputs of the gates having the same numbers in figure 1-23. AND columns 2^2, 2^1, and 2^0 refer to the adder outputs.

Example 2: Assume that the values to be added are:

$$A = 010_2$$
$$B = 011_2$$

With these values in the A and B registers, circuit conditions will be as indicated in the fourteenth row of the table shown in figure 1-24.

Example 3: Assume that the values to be added are:

$$A = 001_2$$
$$B = 111_2$$

With these values in the A and B registers, circuit conditions will be as indicated in the twenty-fourth row of the table shown in figure 1-24.

A^2	B^2	A^1	B^1	A^0	B^0	1	2	3	4	5	6	10	11	12	13	20	21	22	23	30	31	32	33	2^2	2^1	2^0
0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0
0	0	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	1	0	0	1	0	1	0	1	1	0	0
0	0	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	1	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	1	0	1	1	0	0	1	0	1	1	0	0	0	0	1	0	0	1	0	1	0	1	1	0	0
0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0
0	0	1	1	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1
0	0	1	1	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1
0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	0	1	1	1	0	1	1	1	0
0	1	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
0	1	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
0	1	0	0	1	1	0	0	1	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0	1	1	0
0	1	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
0	1	0	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0	1	0	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1	1	1	0	1	0	1	0	1	0	0	1
0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
0	1	1	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1	1	1	0	1	0	1	0	1	0	0	1
0	1	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	1
0	1	1	1	0	1	1	0	0	0	1	0	0	0	1	1	1	0	0	1	1	1	0	1	0	1	0
0	1	1	1	1	0	1	0	0	0	1	0	0	0	1	1	1	0	0	1	1	1	0	1	0	1	0
0	1	1	1	1	1	0	0	0	0	1	0	0	0	1	1	1	0	0	1	1	1	1	1	0	1	1
1	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
1	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
1	0	0	0	1	1	0	0							0	0	1	0				0	0	0	1		
1	0																									

Figure 1-24. Partial truth table for circuit in figure 1-23.

Exercises (006):

Questions 1 through 3 are based on the operation of the parallel carry structure shown in figure 1-23. Assume that the inputs are: A = 011 and B = 010.

1. What are the inputs to OR-gate 13?

2. What does the output of OR-gate 13 represent?

3. What is the input to HA2^2?

4. To what stages is signal 4 applied?

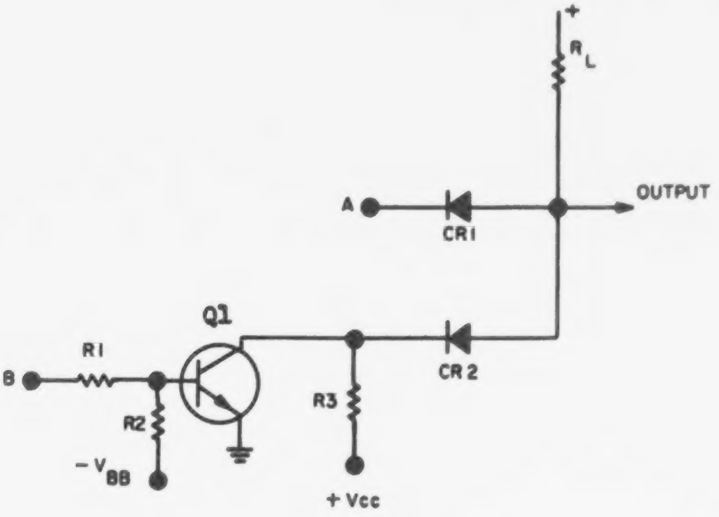
007. Define the different types of subtractor circuits; state the basic limitation of quarter-subtractors.

Types of Subtractors. Basically, a subtractor is a device that accepts the minuend and subtrahend digits at its inputs and produces a difference and borrow at its outputs.

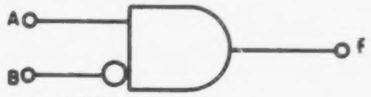
Quarter-subtractor. A study of the truth table for the inhibitor circuit, figure 1-25, reveals that if borrows are ignored, the circuit functions as a subtractor. For example:

$$0 - 0 = 0$$
$$0 - 1 = 0$$
$$1 - 0 = 1$$
$$1 - 1 = 0$$

Due to circuit limitations, an erroneous resultant will be produced when attempting to use a simple inhibitor to perform the arithmetic operation indicated in the second equation. To produce a true difference, some means must be incorporated to generate a borrow whenever the subtrahend is greater than the minuend. The mechanization and operation of the inhibitor circuit, also known as a quarter-subtractor, was covered in Unit 3.



A. CIRCUIT SCHEMATIC



B. LOGIC DIAGRAM

INPUT		OUTPUT
A	B	f(A,B) = A$\bar{B}$
0	0	0
0	1	0
1	0	1
1	1	0

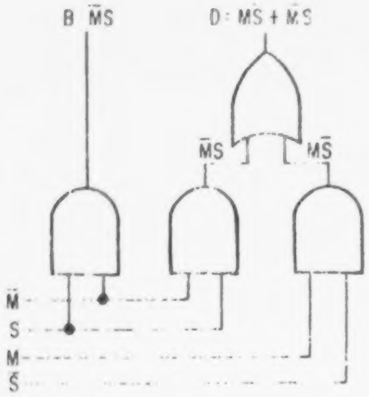
C. TRUTH TABLE

Figure 1-25. The inhibitor circuit.

Half-subtractor. A truth table presenting the conditions arising from the subtraction of two binary digits is shown in figure 1-26,A. Since it does not take into account borrows from a previous order, it is the truth table for a process known as *half-subtraction.*

MINUEND (M)	0	1	0	1
SUBTRAHEND (S)	0	0	1	1
DIFFERENCE (D)	0	1	1	0
BORROW (B)	0	0	1	0

A. TRUTH TABLE



B. LOGIC DIAGRAM

Figure 1-26. Half-subtractor.

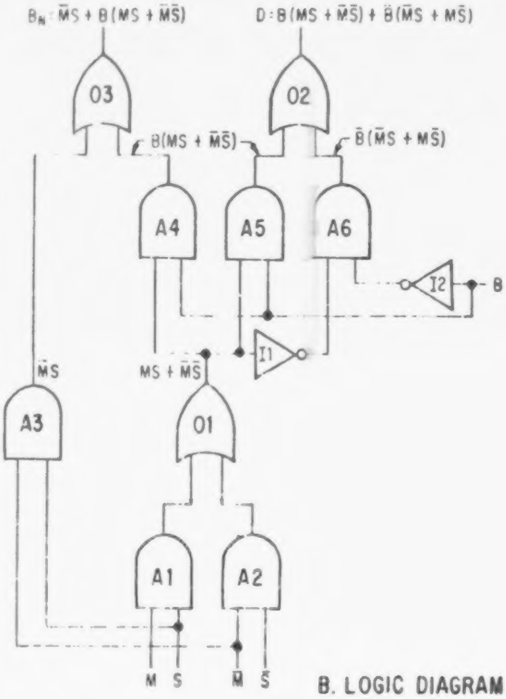
One means for mechanizing the half-subtract process is presented in figure 1-26,B. This circuit is practically identical to that for the half-adder presented in figure 1-17,A. The only difference is in the connection of the inputs and in the terminology used. The operation is the same, bearing out the proposition that since the add and subtract operations are the reverse of each other, the same circuit could be used to perform both.

Full-subtractor. As was true with the addition process, more than one column is usually involved in the subtraction process. Thus, the usefulness of the table shown in figure 1-26,A, is limited, although valid. When more than one column of digits containing a minuend and subtrahend are to be subtracted, each digit of the minuend is decreased by the amount of the subtrahend in that column. If the minuend is reduced to a value less than zero, then the minuend in the next higher order column must be reduced by 1 and a value equivalent to this 1 added to the minuend in the column being subtracted. This is the process most commonly used when you are manually manipulating numbers and is a process also widely used in computer circuits.

Now consider the representative subtractor circuit of figure 1-27. The table of figure 1-27,A, showsn the M (minuend), S (subtrahend), B (borrow from a previous order), D (difference), and Bn (new borrow; that is, the borrow generated in the column being subtracted).

M	0	1	0	1	0	1	0	1
S	0	0	1	1	0	0	1	1
B	0	0	0	0	1	1	1	1
D	0	1	1	0	1	0	0	1
B_N	0	0	1	0	1	0	1	1

A. TRUTH TABLE


$B_N = \bar{M}S + B(MS + \bar{M}\bar{S})$
$D = B(MS + \bar{M}\bar{S}) + \bar{B}(\bar{M}S + M\bar{S})$
03
02
$B(MS + \bar{M}\bar{S})$
$\bar{B}(\bar{M}S + M\bar{S})$
A4
A5
A6
I2
B
I1
$\bar{M}S$
$MS + \bar{M}\bar{S}$
A3
01
A1
A2
M
S
$\bar{M}$
$\bar{S}$

B. LOGIC DIAGRAM

Figure 1-27. Representative subtractor circuit.

Assume a condition where M, S, and B are all HIGH (true) or (1). Under this condition, from the table of figure 1-27,A, you can expect that the D and Bn outputs will also be HIGH (1). The action to produce these outputs is as follows:

With M and S HIGH, the A1 AND-gate will have a HIGH output. The resulting HIGH will activate OR-01 which represents the true or HIGH state of $MS + \overline{MS}$. This output serves as a ONE enabling input to AND-gate A4 and A5. The HIGH (1) borrow input causes AND-gates A4 and A5 to become fully enabled, to produce a HIGH output at D via OR-gate 02, representing the true state of the difference function

B(MS + MS), and a HIGH output at BN via OR-gate 03, representing the true or HIGH (1) state of the borrow function B($MS + \overline{M}\overline{S}$). Thus, both the difference and borrow outputs are HIGH (1).

Now consider the action when M is LOW (0), S is HIGH (1), and B is LOW (0). By design, the output of AND-gate A3 goes HIGH when $\overline{M}$ is HIGH (1), and S is HIGH (1). The HIGH output of AND-gate A3 activates OR-gate 03 and its output goes HIGH to represent a borrow (Bn) from the next higher order. The inputs ($\overline{M}S$) do not enable AND-gate A1 or A2, causing the output of OR-gate 01 output to be LOW for the function of $MS + \overline{M}\overline{S}$. This LOW output inhibits AND-gate A4 and A5, and is inverted by amplifier I1. The HIGH I1 output must, therefore, represent the complement of $MS + \overline{M}\overline{S}$, which is $\overline{M}S + M\overline{S}$. The HIGH I1 output serves as one enabling input to AND-gate A6. The LOW at B is inverted to a HIGH by amplifier I2. The HIGH I2 output, therefore, represents the complement of B, which is $\overline{B}$. This HIGH signal, along with the HIGH output from I1, enables AND-gate A6. The HIGH output of AND-gate A6, representing the function $\overline{B}(\overline{M}S + M\overline{S})$, causes OR-gate 02 to have a HIGH output. This output represents a HIGH (1) difference output for the assumed inputs.

Exercises (007):

1. What is a half-subtractor?

2. What is a full-subtractor?

3. What is another name for a quarter-subtractor?

4. What is the basic limitation of a quarter-subtractor?

008. Regarding operation of subtractors using serial borrow, specify the outputs of certain components in a described circuit?

Serial-Subtractors. Subtractors, like adders, may be constructed with either serial or parallel borrow structures. Borrows are treated most like carries, and adder circuits can, with minor modifications, be made to perform as subtractors.

Consider now the subtractor circuit shown in figure 1-28. Except for the input and output connections, this circuit is identical to the adder circuit shown in figure 1-21. Again, no provisions are made for gating the register outputs; hence, the subtractor outputs should at all times reflect the difference between the values contained in the A and B registers.

Exercises (008):

Assume that the subtractor circuits shown in figure 1-28 have as inputs: A = 11001_2 and B = 11011_2.

1. With the values given what is the output of AND-gate 10?

2. What is the output of AND-gate 20?

3. What is the output of AND-gate 24?

4. What is the output of the circuit?

009. Specify operating characteristics and circuit conditions of subtractors using parallel carry.

Parallel Subtractors. Consider again the circuit shown in figure 1-23. This circuit can be made to subtract by complementing the subtrahend prior to proceeding with the addition. When it is subtracting, the borrows are treated like carries; that is, a borrow generated in one stage is simultaneously presented to all other stages and, depending on conditions, will be absorbed by one or more of them. The absorb signal will, when subtracting, be designated as a satisfy.

Example 1: Assume that A = 010_2 and B = 110_2 and that B is to be subtracted from A. When the contents of B are complemented, circuit conditions will be as indicated in row 10 of the table shown in figure 1-24.

Example 2: Assume that A = 111_2 and B = 110_2 and that A is to be subtracted from B. When A is complemented, circuit conditions will be as indicated in row 18 of the table shown in figure 1-24.

Example 3: Assume that A = 100_2 and B = 110_2 and that B is to be subtracted from A. When B is complemented, circuit conditions will be as indicated in row 34 of the table shown in figure 1-24.

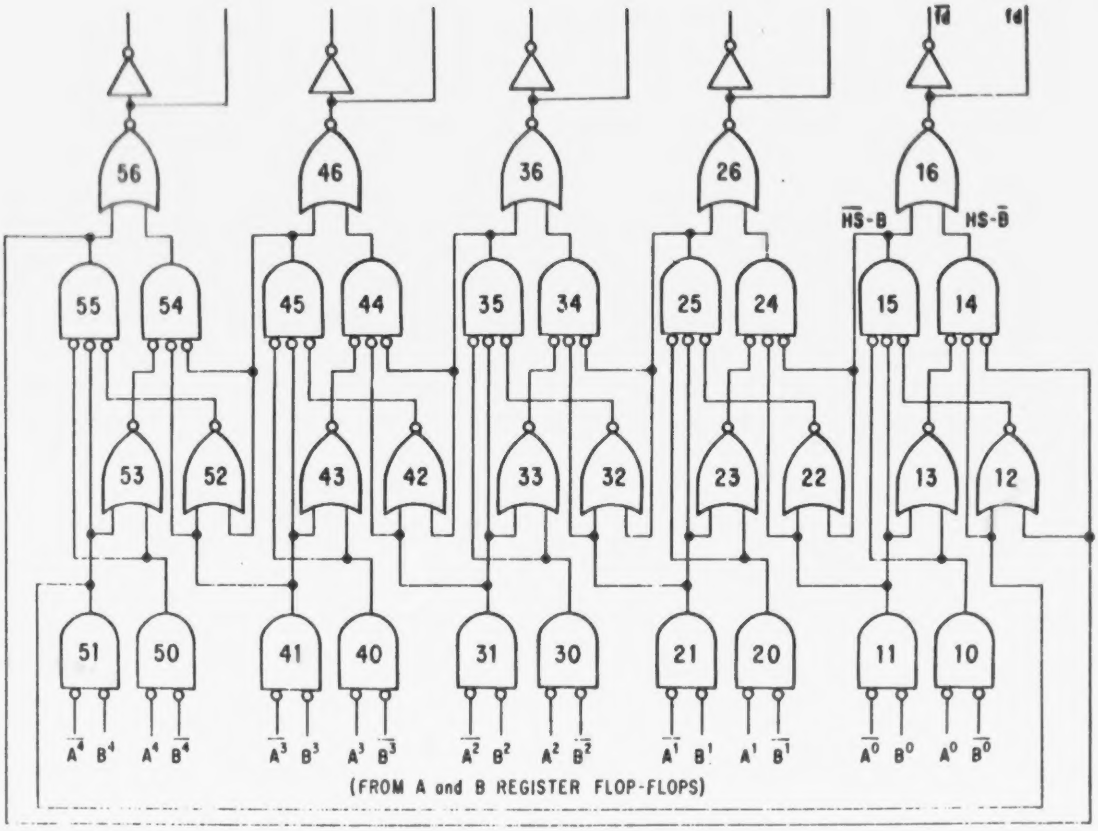

$\overline{fd}$
fd
56
46
36
26
16
$\overline{HS}$-B
HS-$\overline{B}$
55
54
45
44
35
34
25
24
15
14
53
52
43
42
33
32
23
22
13
12
51
50
41
40
31
30
21
20
11
10
$\overline{A^4}$ B^4 A^4 $\overline{B^4}$
$\overline{A^3}$ B^3 A^3 $\overline{B^3}$
$\overline{A^2}$ B^2 A^2 $\overline{B^2}$
$\overline{A^1}$ B^1 A^1 $\overline{B^1}$
$\overline{A^0}$ B^0 A^0 $\overline{B^0}$
(FROM A and B REGISTER FLOP-FLOPS)

Figure 1-28. Subtractor circuit utilizing borrow structure.

Exercises (009):

1. How can a parallel-adder be made to subtract?

2. A borrow generated in the second stage of a subtractor using parallel borrow is applied to __________ __________ __________ .

3. In figure 1-23, the __________ satisfy signal is applied to AND-gates 10, 11, and 21.

4. Refer to figures 1-23 and 1-24 to answer the following: Assuming that A = 111_2 and B = 110_2, with A to be subtracted from B, when A is complemented, circuit conditions are indicated in row _______________ of the table (fig. 1-24).

1-3. Comparators

A *comparator* is a device used to compare two values or numbers to determine whether they are like or unlike. Common forms of comparison are:

- Comparison of two sign bits, plus or minus.
- Adders (covered in the last section).
- Comparison of two numbers for identity.

The simplest form of comparator is one that checks two bits of data and indicates whether they are like or unlike. In a more complicated cause, we may need to compare the count in a counter with the data in a register and take action when the two counts are identical or different.

010. Define terms that relate to comparator circuits.

Comparator Basics. Before we discuss comparators, parity, and error checking circuitry, you must become

familiar with certain terminology. Each type of equipment has coined terms that convey particular meaning to the people trained on the individual equipment. Therefore, you may encounter other terms which may be added to this list. The following definitions apply to circuits discussed in this section:

***a.* Bit. A bit is a binary digit. It may have an significant position and is expressed as a ONE or a ZERO.**

***b.* Binary number. A binary number is a group of one or more binary digits that represent a decimal number.**

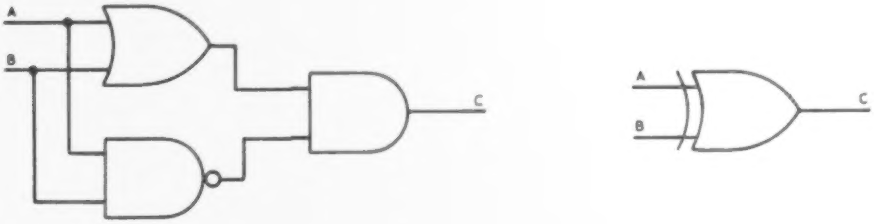
c. Record. A record is a group of one or more binary digits, such as a binary number, a character, a half-word, a word, a part of a message, a message, or a tape record.

d. Parity. Parity establishes equality with respect to a standard. This produces uniformity in either the oddness or evenness of the ONE bits in a record.

e. Odd record. An odd record (odd parity) is a record that must contain an odd number of ONE bits, including the parity bit, or be in error.

f. Even record. An even record (even parity) is a record that must contain an even number of ONE bits, including the parity bit, or be in error.

One of the simplest comparator circuits is the exclusive OR-gate. The exclusive OR-gate has an important characteristic which makes it readily adaptable to perform comparator functions. Figure 1-29 shows an exclusive OR-gate and its truth table. If two unlike values are fed into an exclusive OR-gate, it produces a binary one output. But if the values are alike (equal), the output will be a binary zero. In other words, the exclusive OR-gate detects unlike inputs.



A	B	C
1	1	0
0	0	0
1	0	1
0	1	1

Figure 1-29. Exclusive OR-gate.

Sign Bit Comparator. Before an addition of two binary numbers is performed, the computer must be able to determine the sign (+ or —) of the two numbers. If the sign bits are the same, the numbers are added directly. If the sign bits are not the same, additional steps are required. Figure 1-30 shows a sample comparator which monitors the sign bit flip-flop of two registers. Exclusive OR-gate one produces a binary one output only when the sign bits are unlike. Exclusive OR-gate two produces a binary one output only when the signs are the same. The indication of like or unlike signs is then applied to control circuits where decisions are made as to what operations must be performed and what the sign of the answer will be.

If the sign bits of both numbers are binary ones, the sign bit flip-flops of both registers will be SET. The high output from the one side of F/FX is applied to pin 1-1 of gate 1 and pin 2-1 of gate 2. The high output from the one side of F/FY is applied to pin 1-2 of gate 1. The low output from the zero side of F/FY is applied to pin 2-2 of gate 2. Since gate 1 has two high (equal value) for inputs, its output will be a binary zero; but gate 2 will have a binary one output because of its unlike inputs. The high output from gate 2 indicates that the sign bits are alike. (Note the table of combinations in fig. 1-30).

Let's use another example where the sign bits are unlike. Assume that the F/FX sign bit is a binary one and the F/FY sign bit is a binary zero. In this case, F/FX will be set and F/FY will be clear. With F/FX set, a binary one will be felt off the one side and applied to pin 1-1 of gate 1 and pin 2-1 of gate 2. Since F/FY is clear, a binary zero will be felt off the one side and applied to pin 1-1 of gate 1. A binary one from the zero side of F/FX will be felt on pin 2-2 of gate 2. Gate 1 now has a high and a low for inputs which will give a high output. Gate 2 has two low inputs which will give a low output. The high output from gate 1 tells us that the sign bits were unlike.

Exercises (010):

1. What is a bit?

2. What is a record?

3. What is an even record?

4. Define parity.

5. How does an exclusive OR-gate function as a comparator?

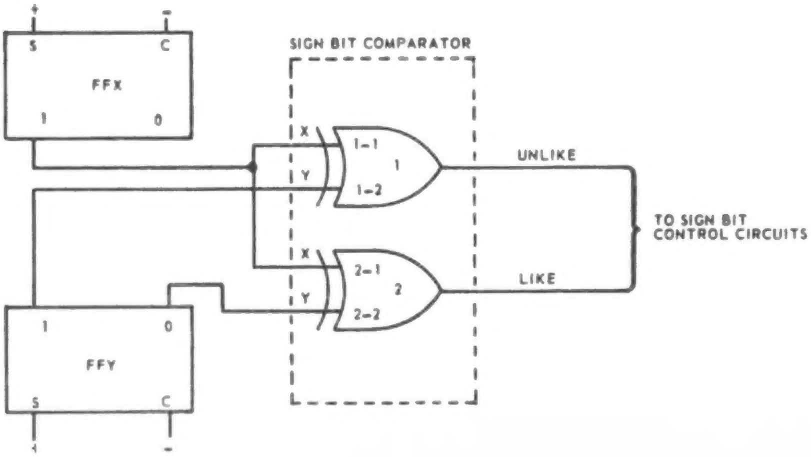

+
-
S
C
FFX
1
0
SIGN BIT COMPARATOR
X
Y
1-1
1-2
1
UNLIKE
X
Y
2-1
2-2
2
LIKE
TO SIGN BIT CONTROL CIRCUITS
1
0
FFY
S
C
+
-

Table of Combinations			
		Gate 1	Gate 2
X	Y	UNLIKE	LIKE
+	+	0	1
-	+	1	0
+	-	1	0
-	-	0	1

Figure 1-30. Comparator.

011. Specify the operation, purpose, and types of parity circuits.

Parity Checking Circuits. Parity means likeness. So when the word "parity" is used in relation to computers, all it means is that the data moved from some place, such as a memory location, should be like it was when it was originally put into that location. In other words, if a word containing an odd number of binary ones is sent to memory, then it should still have an odd number of binary ones when it is removed at a later time. The only way to know whether a number has an odd or even number of binary ones before it goes into memory is to check it and assign an additional binary one if needed. Then when it is removed from memory, it is checked to insure that either the even or odd number of binary ones are still present. The circuit used to assign parity (make each number either even or odd in binary ones) is called parity-generating circuit. The circuit used to check or verify parity is called a parity-checking circuit.

Computers are capable of several thousand operations per second, and thousands of individual components are constantly involved in these operations. Since the data is being processed at high speeds, it is reasonable to assume that errors may occur in transfers of data among the computer's units. Information (or data) bits may be "dropped" or "picked up" although there is no equipment failure. Therefore, it is necessary that some means of equipment self-checking be built into the computer. Parity-checking circuits serve this purpose.

A system can operate on even or odd parity. If odd parity is established when the computer is designed, then all words going into or coming out of storage must have an odd number of binary ones or they will be in error. If even parity is used, the words must have an even number of binary ones. There are two types of parity-checking circuits: parallel and serial. We will first look at the parallel version.

Parallel parity-checking circuit. The purpose of a parity-checking circuit is to determine the validity of each computer word after it has been taken from a storage medium or been transmitted over transmission lines. A parity-checking circuit must be capable of:

- Determining whether the number of binary ones in a computer word is even or odd.
- Generating an error signal when a word with incorrect parity is detected.

The error signal generated by the parity-checking circuit is used to trigger an alarm so that the operator will know the status of the word, or to initiate some other action within the computer. The parity-checking circuit is used at strategic points going into memory and coming out of memory and to or from terminal equipment.

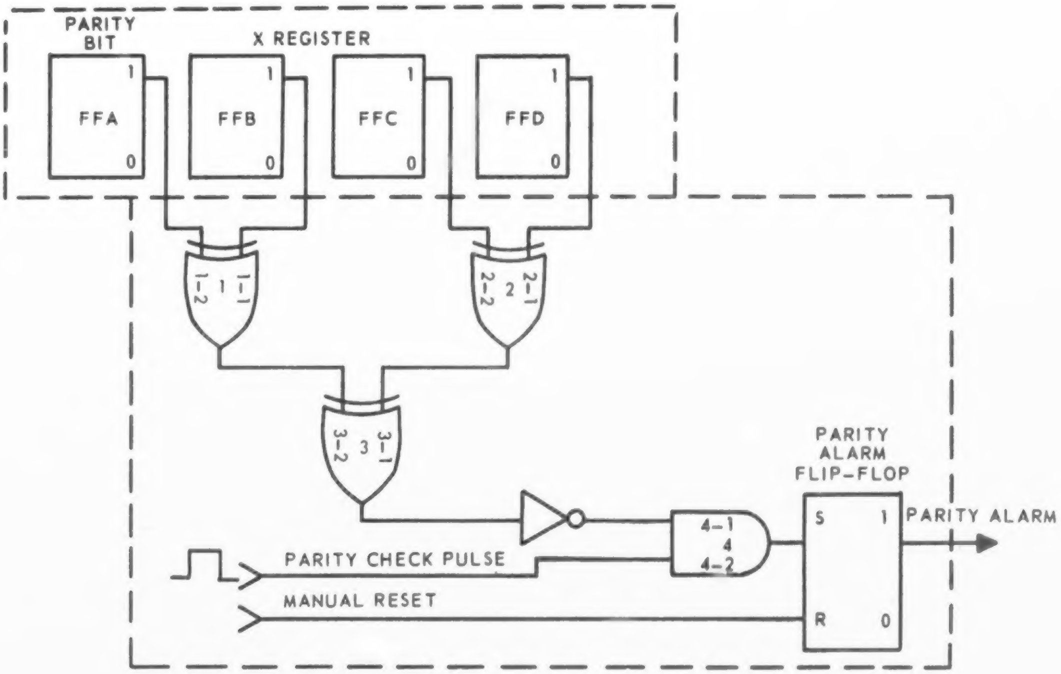


Figure 1-31. Parallel parity-checking circuit.

A parallel parity-checking circuit is shown in figure 1-31. This circuit checks for odd parity. An alarm will be activated when a word with an even number of binary ones is checked. With odd parity assigned to all words, the circuit will check for uniformity. If a word is found to have even parity, the error may have occurred either in storing or in transferring from one place to another.

Let's look at the circuit and see how it works. The original computer word in memory is 1011. It has an odd number (3) of binary ones, indicating that parity is correct. Assume that, in the transfer from memory, one of the binary ones was lost (bit D). When the word is transferred to the X register, F/FA (parity bit flip-flop) and F/FC will SET, F/FB and F/FD remain CLEAR. The register configuration is now 1010. The outputs of the X register are applied to the parity-checking circuit which consists of logic gates and an alarm flip-flop. With F/FA SET, a high will be felt off its one side and applied to pin 1-2 of gate 1. F/FB is CLEAR, so a low from its one side will be applied to pin 1-1 of gate 1. With one high and one low input, exclusive OR-gate 1 will produce a high output to pin 3-2 of gate 3. With F/FC SET and F/FD CLEAR, gate 2 will also produce a high output. The high from gate 2 is applied to pin 3-1 of gate 3. This now makes both inputs to gate 3 high, which will give a low output. The low output from gate 3 is inverted (to a high) and applied to pin 4-1 of gate 4. When the parity check pulse is applied to pin 4-2, gate 4 will produce an output pulse and SET the alarm flip-flop indicating that a parity error has been detected. If a word having correct parity had been checked, gate 4 would have been inhibited at the time the parity check pulse was applied, so the alarm flip-flop would remain CLEAR. As shown by the diagram, the alarm flip-flop can be manually CLEARED (reset) to resume normal checking operation.

Serial parity-checking circuit. A sample parity-checking circuit used to detect parity errors in a serially transmitted word is shown in figure 1-32. From a circuit standpoint, the serial method of checking parity is the simplest of all. It works on the principle that if a flip-flop is initially CLEAR and is triggered an odd number of times, it ends up SET. If it is triggered an even number of times, it ends up CLEARED. The circuit shown is designed to check for even parity but may be changed to check for odd parity by simply designing the circuit to initially SET F/FA.

The X register is a right shift, end-off, shift register. After each check pulse (T1 through T4), a shift pulse is applied to move the data in the shift register one place to the right. F/FA is CLEAR because it was cleared by the previous check operation. F/FB is manually CLEARED to reset the alarm circuits.

If the X register contains the binary configuration shown on the diagram, the binary zero in X2 at T1 time applies a low voltage to pin 1-1 of gate 1. The T1 check pulse is applied through the OR-gate to pin 1-2 of gate 1. The output of gate 1 remains high because of the low input from X2. This will not cause F/FA to change states.

The first shift pulse occurs and all data in the X register is moved one position to the right. Xp is CLEARED and Xs, X1, and X2 are SET. The X2 output, which is now high, is applied to pin 1-1 of gate 1. So when T2 is applied through the OR-gate to pin 1-2, gate 1 will produce an output pulse. The pulse from gate 1 will SET F/FA (see waveforms) which puts a binary one on in 2-1 of gate 2.

The second shift pulse occurs, and all data in the X register again moves one position to the right. Xp and Xs are now CLEAR and X1 and X2 are SET. The high output from X2, and the T3 check pulse, will cause gate 1 to again produce an output pulse. This output pulse from gate 1 will cause F/FA to CLEAR.

When the third shift pulse occurs, the data in the X register will again be shifted one place to the right. This CLEARS Xp, Xs, and X1; and SETS X2. When check pulse T4 occurs, the high from X2 and T4 will cause gate 1 to produce an output pulse to set F/FA. With F/FA set, a high is applied to pin 2-1 of gate 2. So when T4 is applied to pin 2-2, gate 2 will produce an output pulse to SET F/FB. The output from the one side of F/FB indicates that a parity error has occurred. The T4 check pulse was also used, after being delayed, to clear F/FA. F/FB must be cleared manually.

As stated before, this circuit checks computer words for even parity. The example word we used had an odd number of binary ones. We were looking for an even number, so an alarm was activated. The last half of the waveform chart shows the action with an even number of binary ones in the computer word. So, if you follow the chart, you will see that an alarm is not activated when a word with even parity is checked.

Parity-generating circuits. Parity-generating circuits are used in a system at points where words are going into storage. Any given word may not have correct parity. Therefore, correct parity must be assigned before the new word can be stored into memory.

Figure 1-33 shows a typical odd parity-generating circuit. Flip-flop Xp is the parity flip-flop. This circuit first checks the parity of the word. If the parity of the word checked is not correct, an output pulse from AND-gate 6 will change the state of Xp to give an odd number of binary ones. Since you already know how an exclusive OR-gate works, the signals will not be traced through each gate.

Assume that the word 01100 has been entered into the X register from the arithmetic unit or an input-output device. Since this circuit checks for odd parity, you can sede that this word now has incorrect parity. With Xp, X2, and X3 CLEARED and Xs and X1 SET, the end result will be a binary zero output from exclusive OR-gate 4. This binary zero is inverted to a binary one by inverter 5 and applied to one leg of AND-gate 6. When the "assign parity" pulse (generated by control circuits) is applied, both legs of AND-gate 6 will be satisfied.

AND-gate 6 will now produce an output pulse and SET the parity flip-flop (Xp). With Xp SET, the X register now contains 11100. The extra binary one (Xp) was assigned to give the word correct (odd) parity. If a word contains odd parity to start with, there will be a binary one output from gate 4 which will be inverted to disable one leg of AND-gate 6; therefore, Xp will not be changed.

Exercises (011):

1. Parity circuits are a means of ________ ________ built into the computer.
2. Parity check circuits check the __________ of each computer word.
3. Parity checks are made at __________ points within the computer.
4. Exclusive OR-gates may be used in ________ parity-checking circuits.
5. The simplest method of checking parity is the __________ method.
6. The method of parity checking which relies upon setting and clearing a flip-flop an even or odd number of times is the __________ method.
7. Parity-generating circuits are used within computers at points where words are ____________ ____________ ____________ .
8. Correct parity must be assigned ________ the word is stored into memory.

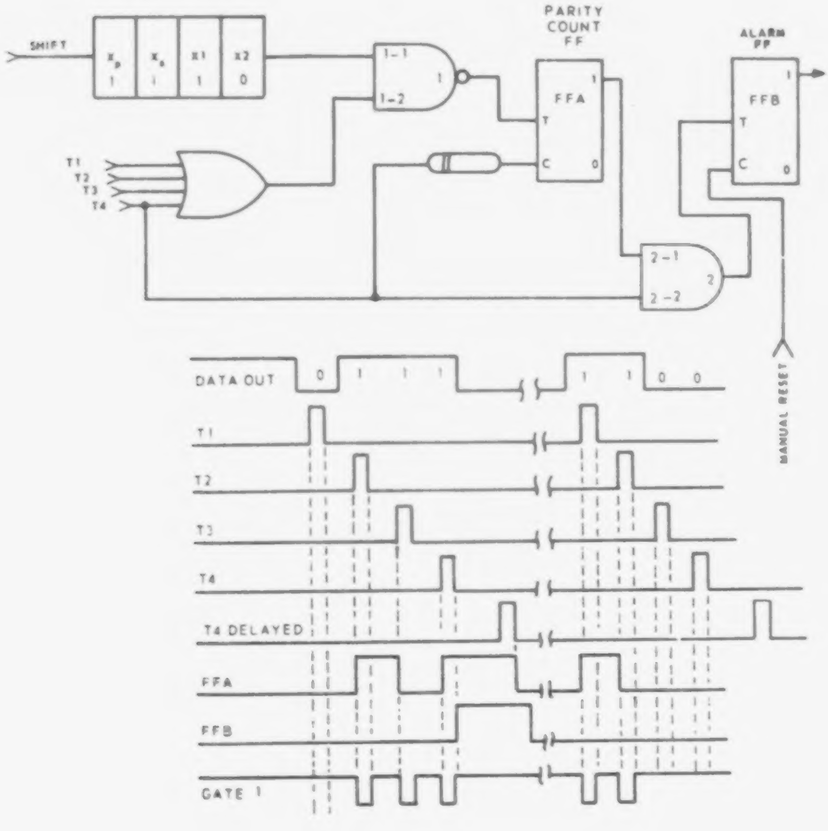

SHIFT
Xp
1
Xs
1
X1
1
X2
0
1-1
1-2
1
PARITY COUNT FF
FFA
T
C
1
0
ALARM FF
FFB
T
C
1
0
T1
T2
T3
T4
2-1
2-2
2
MANUAL RESET
DATA OUT
0
1
1
1
1
1
0
0
T1
T2
T3
T4
T4 DELAYED
FFA
FFB
GATE 1

Figure 1-32. Serial parity-checking circuit.

012. State selected circuit conditions or requirements for checking parity in a parallel record.

Serial Parity Check of a Parallel Record. The previously discussed method of serially checking parity was accomplished bit by bit while the record was being transmitted serially. In the method discussed now, the check is done serially on a record that is undergoing parallel transfer. Foldout 1, in the back of this unit, shows a typical circuit. Notice that this circuit is drawn in positive logic; that is, a logic ONE is represented by a relatively high voltage, and the activating level for the flip-flop is the positive-going clock. Notice also that the circuit is made up of primarily five standard cards, labeled A through E.

Before digging into the details of how parity is checked, let us first find out: (1) how a record is passed through the circuit if parity is correct and (2) how the record is stopped if the parity is incorrect. The flip-flop register (along the bottom of the logic diagram) is a temporary storage register that holds the record while parity is checked. The ONE side of each flip-flop in this register is connected to a two-input AND-gate. These gates, numbered 50, 60, 70, 80, and 90, are the record-transfer gates. If the parity count is good, the transfer pulse existing from AND-gate 101 conditions the other leg of each of the transfer AND-gates; ;and the record is transferred to the next unit. If parity does not check good, AND-gate 101 is not conditioned and does not pass the transfer pulse. As a result, the record does not pass through the transfer gates.

Assume, for the purpose of explanation, that the reset flip-flop pulse has just reset the alarm flip-flop, and the flip-flop register to the CLEAR state; and that immediately following this action, the record 01101 is loaded into the flip-flop register. With this record in the flip-flop register, F/F1 is SET (set to the ONE state), F/F2 is CLEAR (set to the ZERO state), F/F3 is SET, F/F4 is set, and the parity flip-flop is CLEAR. With the alarm flip-flop in the CLEAR state, one leg of AND-gate 100 and one leg of AND-gate 101 are conditioned. At this point, the record is in the flip-flop register awaiting transfer. The next step is to check parity to determine if the record should be transferred.

Parity check of the records starts with the application of a positive-going parity check pulse to the top of leg AND-gate 100. Since the bottom leg of this AND-gate is already conditioned by the alarm flip-flop, the pulse passes through the gate and samples AND-gate 1 and 4 of the first card in the check matrix. Notice that AND-gates 2 and 3 are tied to a negative level. This level disables these two gates so that they cannot interfere with the operation of the matrix.

Since F/F1 is SET, the pulse passes through AND-gate 1 and exits from OR-gate 1. You can see by this action that if F/F1 is SET, the pulse exits from the top OR-gate, indicating odd parity; and if F/F1 is CLEAR, the pulse exits from the bottom OR-gate, indicating even parity. Therefore, we can refer to the top row of OR-gates as the odd row and the bottom row of OR-gates as the even row. The check pulse exiting from OR-gate 1 samples AND-gates 6 and 7.

Since F/F2 is CLEAR, the pulse passes through AND-gate 7 and exits from OR-gate 3. You can see that, when a cleared flip-flop is encountered, the oddness or evenness of the parity count does not change. In other words, the count entering card B is odd; and because F/F2 is CLEAR, the count leaving card B is odd.

The check pulse from OR-gate 3 samples AND-gates 10 and 11. F/F3 is SET, so the pulse passes through AND-gate 10 and exits from OR-gate 6. You can see that, when the pulse encounters a SET flip-flop, the pulse complements its state. In other words, the count entering card C was odd and the count leaving card C was even. The pulse from OR-gate 6 samples AND-gates 13 and 16. F/F4 is SET, so the pulse passes through AND-gate 13 and exits from OR-gate 7, again complementing the count. The check pulse exiting from OR-gate 7 samples AND-gates 18 and 19. The parity flip-flop is CLEAR, so the pulse passes through AND-gate 19 and exits through OR-gate 9. OR-gate 9 is the upper row, which is the odd row.

The pulse from OR-gate 9 is fed through OR-gate 110 to the CLEAR side of the alarm flip-flop. This effectively tells the alarm flip-flop that the parity checked odd, which is the desired result. Normally, as long as parity checks correctly, the alarm flip-flop remains in the CLEAR state. However, this pulse is used to clear the flip-flop in case noise has set it to the alarm state. This pulse also goes to other circuitry to generate a transfer pulse. The transfer pulse comes back and conditions the other leg of AND-gate 101. The pulse exiting from AND-gate 101 strobes the transfer AND-gates, and the record is transferred to the next unit.

Now, let us see what happens when parity is even (in error). For this explanation, we use the record 1 0 0 0 1. The check pulse exiting from AND-gate 100 samples AND-gates 1 and 4. F/F1 is SET, so the pulse passes through AND-gate 1 and exits from OR-gate 1. As discussed previously, when a cleared flip-flop is encountered, the oddness or evenness of the record does not change. With this in mind, you can see that the next three flip-flops are cleared, so the pulse exits from OR-gate 3, OR-gate 5, and OR-gate 7, in sequence. The pulse exiting from OR-gate 7 samples AND-gates 18 and 19. The parity flip-flop is SET, so the pulse passes through AND-gate 18 and exits from OR-gate 10, and stores the evenness of the count in the set side of the alarm flip-flop by setting it to the alarm state. This action inhibits the transfer of the bad record because the request transfer pulse is not generated. With the alarm flip-flop SET, a parity alarm is produced; and AND-gates 100 and 101 have one leg deconditioned.

In summary, the function of this circuit is to detect parity errors of a record temporarily sorted in a check register; the record is undergoing transfer when the check is made. If the parity of the record in question is good, transfer is made. If the record has a bad parity, the transfer is inhibited.

Exercises (012):

1. What is the purpose of F/F1 through F/F4 and the parity of F/F?

2. List the two requirements for the transfer gates to be enabled.

3. When will AND-gate 100 be enabled?

4. What is the result if the alarm F/F does set?

013. State the purpose of the pulse fail and true time comparator circuit, write required Boolean equations, and identify types of errors.

Pulse Fail and True Time Comparator Check Circuit. Electronic switching systems use circuits by this name to check for missing pulses. You will discover many circuits which use the same principle of operation but are referred to by different names as you become familiar with different digital systems.

This type of error detection circuit (shown in foldout 2) is used: (1) to detect the failure of clock pulses (pulses are the time bases of the system), and (2) to compare the coincidence of the system timing pulses with the pulses after they pass through the logic. In this explanation, the missing pulse detector (MPD) only checks for missing clock pulses; however, you may encounter MPD circuits that are used to check the waveshape of pulses.

Foldout 2,A, shows a typical MPD arrangement. The A and B transmit clock pulses feed the two MPDs. The MPD output follows its input. Should the input fail or become erratic, the MPD switches off and generates a clock fail alarm, indicating which clock failed. The outputs from the MPDs feed an OR-gate. Should one clock fail, the other clock still clocks the counter, as in foldout 2,B.

The counter (foldout 2,B) is used to develop the T7 self-check ($T7_s$) pulse. The counter, consisting of three flip-flops (F/F1, F/F2, and F/F3), feeds AND-gate 1. The reset flip-flop input is used to reset the counter to 1 1 1 after an error or when bringing up the comparator. The counter is clocked through the trigger input to F/F1. The following chart gives the counts for a full cycle. The count pertains to the set side of the flip-flops.

Clock Pulse	F/F1	F/F2	F/F3	T7 Self-Check
7	1	1	1	$T7_s$
0	0	0	0	$T7_s$
1	1	0	0	$T7_s$
2	0	1	0	$T7_s$
3	1	1	0	$T7_s$
4	0	0	1	$T7_s$
5	1	0	1	$T7_s$
6	0	1	1	$T7_s$
7	1	1	1	$T7_s$

You can see from the chart that the only time $T7_s$ is a logic ONE is when the counter is in the 1 1 1 state. The output from AND-gate 1 ($T7_s$) feeds the top leg of OR-gates 3 and 4, in the true time generator (foldout 2,C), and the middle leg of exclusive OR-gate 3 (foldout 2,D).

Now, let us look at the true time generator and see how the T7 true ($T7_t$) pulse is developed. The input signals to the generator are $T7_s$, T7 transmitters B ($T7_b$), and T7 transmitter A ($T7_a$). To condition AND-gate 2 and get the output $T7_t$, at least one leg of each OR-gate in the generator must be conditioned.

a. To condition OR-gate 3: $T7_s + T7_a$.

b. To condition OR-gate 4: $T7_s + T7_b$.

c. To condition OR-gate 5: $T7_a + T7_b$. The result of a and b and c is $(T7_s + T7_a) \bullet (T7_s + T7_b) \bullet (T7_a + T7_b)$. You can see that to produce $T7_t$, we must have $T7_s$ and at least one transmitter T7; if we do not have $T7_s$, we must have both transmitters. To complete the equation for $T7_t$, multiply out $(T7_s + T7_a)\ '\ (T7_s + T7_b) \bullet (T7_a \bullet T7_b)$ as follows:

$$\begin{array}{r}
T7_s + T7_a \\
\times\ T7_s + T7_b \\
T7_s + T7_s T7_a + T7_s T7_b + T7_a T7_b \\
\times\ T7_a + T7_b \\
\underset{1}{T7_s T7_a} + \underset{2}{T7_s T7_a} + \underset{3}{T7_s T7_a T7_b} + \underset{4}{T7_a T7_b} \\
+ \underset{5}{T7_b T7_a} + \underset{6}{T7_b T7_s T7_a} + \underset{7}{T7_s T7_b} + \underset{8}{T7_a T7_b}
\end{array}$$

In Boolean algebra, we can combine like functions. Elements 1 and 2 are alike, so they are represented by one AND function $(T7_s \bullet T7_a)$. Elements 3 and 6 become $(T7_s \bullet T7_a \bullet T7_b)$. Elements 4 and 8 become $(T7_a \bullet T7_b)$. Elements 5 and 7 become $(T7_s \bullet T7_b)$. The resultant expression for $T7_t$ is as follows:

$$(T7_s \bullet T7_a) + (T7_s \bullet T7_a\ '\ T7_b) + (T7_a \bullet T7_b) + (T7_s \bullet T7_b)$$

From this expression, you can see that, to generate $T7_t$, at least two input signals must be present and coincident. $T7_t$, $T7_s$, $T7_b$, $T7_a$ are all fed to the coincidence detector (foldout 2D). $T7_t$ feeds the top leg of exclusive OR-gates 1, 2, and 3. $T7_a$ feeds the middle leg of exclusive OR-gate 2, and $T7_b$ feeds the middle leg of exclusive OR-gate 1. $T7_s$ feeds the middle leg of exclusive OR-gate 3. The trigger inputs T1, T2, and T3 feed their respective T inputs in exclusive OR-gates 1, 2, and 3. For the two top legs of each of the exclusive OR-gates in foldout 2D to function as exclusive OR-gates, the trigger (T) input must be a logic ONE.

This coincidence detector develops the NOT function. Take, for example, exclusive OR-gate 1. If $T7_t$ and $T7_b$ and the trigger T1 are coincident, or arrive at the same time, the result is B error NOT (the output from exclusive OR-gate 1 is a logic ZERO). If $T7_t$ and $T7_b$ do not arrive coincident with T1, the output from exclusive OR-gate 1 is also a logic ZERO. To produce a B error, we must have $T7_t$ or $T7_b$ (but not both) coincident with T1. The Boolean equations for the three outputs are as follows:

$$\text{B error} = [(\overline{T7_t} \bullet T7_b) + (T7_t \bullet \overline{T7_b})] \bullet (T1)$$
$$\text{A error} = [(\overline{T7_t} \bullet T7_a) + T7_t \bullet \overline{T7_a})] \bullet (T2)$$
$$\text{Self-check error} = [(\overline{T7_t} \bullet T7_s) + (T7_t \bullet \overline{T7_s})] \bullet (T3)$$

In summary, this error detection circuit first determines if the clocks are generating good pulses. It generates an alarm if either clock fails. Second, the circuit monitors the coincidence of the transmitter A, $T7_a$ pulse; transmitter B, $T7_b$ pulse; T7 self-check, $T7_s$ pulse; and T7 true, $T7_t$ pulse. The good clock pulses step the $T7_s$ generator. For each eight input pulses, one output pulse, $T7_s$, is generated. The true time generator develops one $T7_t$ pulse each time at least two of these inputs are coincident, $T7_a$, $T7_b$, and $T7_s$. The coincidence detector determines if there is an error and generates an alarm indicating which is in error.

Exercises (013):

1. What is the purpose of the circuitry found in foldout 2?

2. Write the Boolean equation for AND-gate 1.

3. Write the Boolean equation for exclusive OR-gate.

4. What error will result if F/F1 fails to set?

014. Specify the operational characteristics of a storage error detection circuit.

Storage Error Detector. This storage error detection circuit is used to detect errors occurring during a memory load cycle. The circuit in figure 1-34 acts as an input store comparator which compares memory input data with stored data to see if it was properly stored. If an error is detected, the memory store sequence is inhibited.

First let us look at the memory. The memory receives a number of five-bit records. The ONE bits from the input records are stored in the specified location in memory.

Now let us find out how the circuit detects storage errors. Let us use the record 1 0 1 1 0. At the memory input, this is $\overline{A}$ B C D $\overline{E}$. The input line is conditioned long enough to complete a load control cycle. The following steps accomplish the load control cycle:

a. The input line is conditioned by the record 1 0 1 1 0.

(1) The lower legs of exclusive OR-gates 1, 3, and 4 are conditioned.

(2) Inputs A_1, $\overline{B}_1$, C_1, D_1, $\overline{E}_1$ are loaded into memory.

b. The load control cycle reads the record out of memory.

(1) Memory outputs A_2, $\overline{B}_2$, C_2, D_2, $\overline{E}_2$ are gated to their respective lines.

(2) The top legs of exclusive OR-gates 1, 3 and 4 are conditioned.

c. With both legs of exclusive OR-gate comparing, the output of all gates is ZERO, giving a no-error condition.

d. If one or more of the exclusive OR-gates do not compare, the output from these gates will be a ONE.

e. The ONE output in step d passes through OR-gate 1 or 2, conditioning AND-gate 1.

f. The storage check pulse conditions the top leg of AND-gate 1, setting F/F1.

g. With F/F1 set, a storage error is generated. Now going back to step b; after the load cycle control reads the record out of memory and the error check is made, the load control cycle restores the record back into memory.

In summary, the circuit is primarily a comparator. If the input record compares with the stored version, the stored record is good. If the two operations do not compare, an alarm is generated.

Exercises (014):

1. If 0 1 1 1 0 was loaded into the memory, what is the memory output to the exclusive OR-gates?

2. If $A_1B_1\overline{C}_1\overline{D}_1E_1$ is loaded, and $A_2\overline{B}_2\overline{C}_2\overline{D}_2E_2$ is read out during the load cycle, how does F/F1 set?

3. How many bits may change between input and output records before a storage error will be detected?

1-4. Analog-Digital Conversion

Computers are classified as either digital or analog. Digital computers count, and analog computers measure. Digital computers are generally more versatile than analog computers. A digital computer performs mathematical computations by expressing numbers in terms of digits that can assume certain values. The results obtained are expressed in digit form. For example, a digital computer may use the binary numbering system and the digits 0 and 1 to express numbers. The digits are assigned certain values, such as +5 volts and 0 volts. Under these conditions, it is necessary only that the computer circuits be able to distinguish between 0 volts and +5 volts. Precision circuitry is not important because, should the signal strength vary, it can always be restored to either 0 volts or +5 volts.

An analog computer converts numbers into physically measurable quantities such as voltages or lengths. As an example, the magnitude of a number on a slide rule is represented by a length on the slide rule. There are as many "signal" values as there are numbers, and the slightest variation in signal value has a definite effect upon the accuracy of the computer.

A physical condition, such as azimuth, is represented most easily by a proportional (analog) voltage. It is, therefore, desirable to use analog voltage in certain circuits in some digital equipment. Since the analog computers are designed to solve a specific problem, in practice, it would be necessary to have as many types of analog computers as there are analogous problems to be solved. A digital computer can solve a variety of different problems; the only requirement being that the problem be stated in a language that the computer understands and that the computer be supplied with sufficient data to solve the problem. The limitations of analog computers and the cited advantages of digital computers, particularly in their ability to process large quantities of data, give rise to the use of analog-digital converters.

015. Specify the operating characteristics of digital-to-analog converters.

Digital-to-Analog Converters. An *analog-to-digital* (A/D) converter is a device which converts physical motion or changes in electrical voltage to a digital output. A *digital-to-analog* (D/A) converter will accomplish just the opposite function. It will change digital quantities into physical motion or into a voltage. Term *analog-digital conversion* refers to both processes and does not specify the direction in which the transformation takes place. Let's look at how both types of converter circuits operate.

The circuit in figure 1-35,A, shows a digital-to-analog converter. This circuit can accept a binary input of voltage levels representing a combination of 1's (high) and 0's (low) and transfer them into an equivalent voltage at the output. Looking at an example where the binary digital input at D1, D2, D3, and D4 is 1111, this could be used to represent an analog voltage of 15 volts (1111 would represent 15 in decimal). Using straight digital binary inputs, 0000 could be 0 volts and each increase of one digit between 0000 and 1111 could step the output voltage by 1 volt. In this way our four-bit D/A converter would provide analog output voltages of 0 through 15 volts. The analog-to-digital (A/D) converter shown in figure 1-35B changes an analog voltage to an equivalent digital value. Using the same example from above of a four-bit binary digital number representing a voltage between 0 and 15 volts, the A/D converter would change a 15-volt analog input to a digital output of 1111 (all highs on the output lines). Likewise, if a 0-volt analog input were applied to the converter, the digital output would be 0000 (all lows on the output lines). Figure 1-35 illustrates the basic principles of operation for the D/A and A/D converters. Now let's take a look at how this conversion is actually accomplished. There are many ways to accomplish D/A conversion. However, the two most common are the use of a weighted resistor network and what is commonly referred to as a binary resistance ladder.

Weighted resistor network. The weighted resistor network is illustrated by the circuit shown in figure 1-36. The digital inputs are represented by the switches S1 through S4. If a switch is open, a logic 0 is generated; if it is closed, a logic 1 is generated. Note that in this circuit, a 1 is the value of the battery and a 0 is equivalent to an open switch or no voltage being applied.

Since we have four switches in this circuit we can produce 16 possible digital inputs; that is, all switches closed 1111, or all switches open 000 and any combination of switch closures between these extremes. The changing resistance values as a result of the digital input will control the output of the op amp. By selecting the proper battery and value for R, this converter can be made to function as the converter of figure 1-35,A. That is, if S1 were the only switch closed, the output of the converter would be −1 volt (the op amp is being used as na inverter). If only S2 were closed the output would be −2 volts. With both switches S1 and S2 closed and S3 and S4 open, the converter output would be a −3 volts. This is the same as the converter operation shown in figure 1-35,A. Instead of using mechanical switches at the converter inputs, an electronic device is generally used. This input device may be the output of a binary bistable multivibrator or one of several possible TTL decade counters. One such commonly used device is the

SN7490 decade counter. With this IC chip, output pins A, B, C, and D replace S1 through S4, respectively. The SN7490 counts to 9 and then resets to 0. Therefore, the D/A converter circuit will generate 0 to 9 volts as analog outputs.

The advantage of the resistor-network method for conversion is that with the network each bit of information uses only one resistor. The network is developed with N number of resistors whose values are R, R/2, R/4, etc., with each input to the network "seeing" a different resistance value. The binary resistance ladder, however, is constructed using two resistance values R and 2R.

Binary resistance ladder. The circuit shown in figure 1-37 is a D/A converter using a binary resistance ladder. Note that each input digital information bit detects the same resistance of 3R (2R and R). Therefore, whether it is the LSB or the MSB, each digital bit supplies the same amount of current to the circut.

As in the circuit of figure 1-36, the mechanical switches S1 through S4 may be replaced with an SN77490 decade counter. To illustrate this, if you took an SN7490 and provided a clock as shown in figure 1-38,A, and then used the A, B, C, and D outputs as inputs to the binary ladder of figure 1-37, the circuit would provide the staircase output shown in figure 1-38,B.

Exercises (015):

1. What is the meaning of the term "analog-digital" conversion?

2. What is the advantage of the weighted resistor network method for D/A conversion?

3. If an SN7490 were used to replace the switches of figure 1-36, what would be the range of the analog voltage output?

4. What is the distinguishing characteristic of the binary resistance ladder?

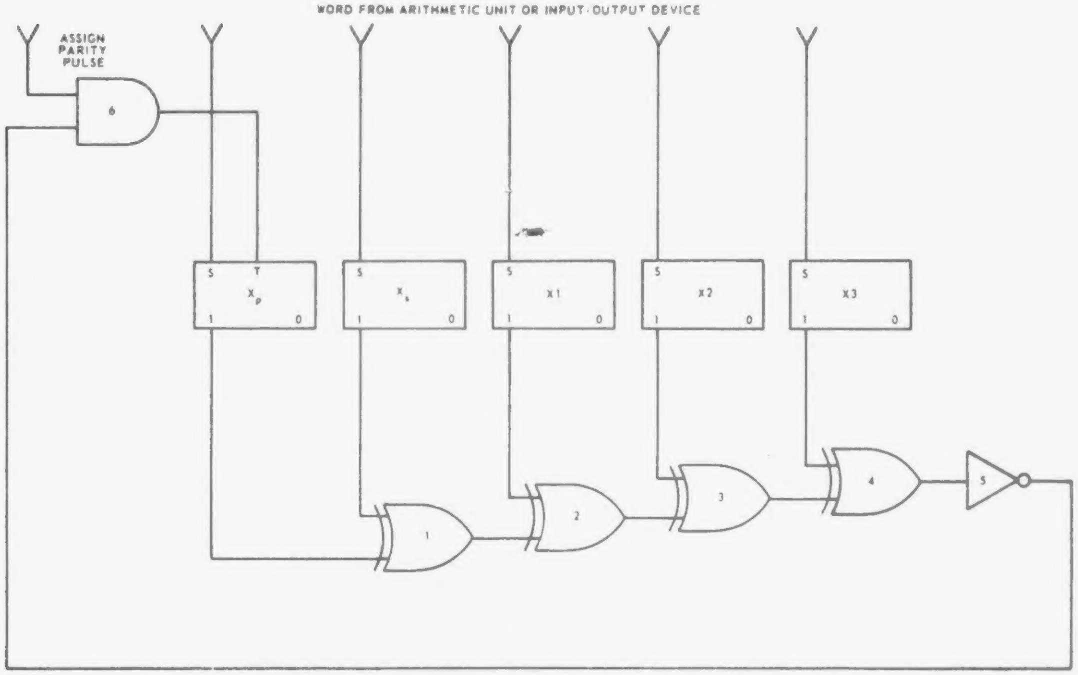


Figure 1-33. Odd-parity generator.

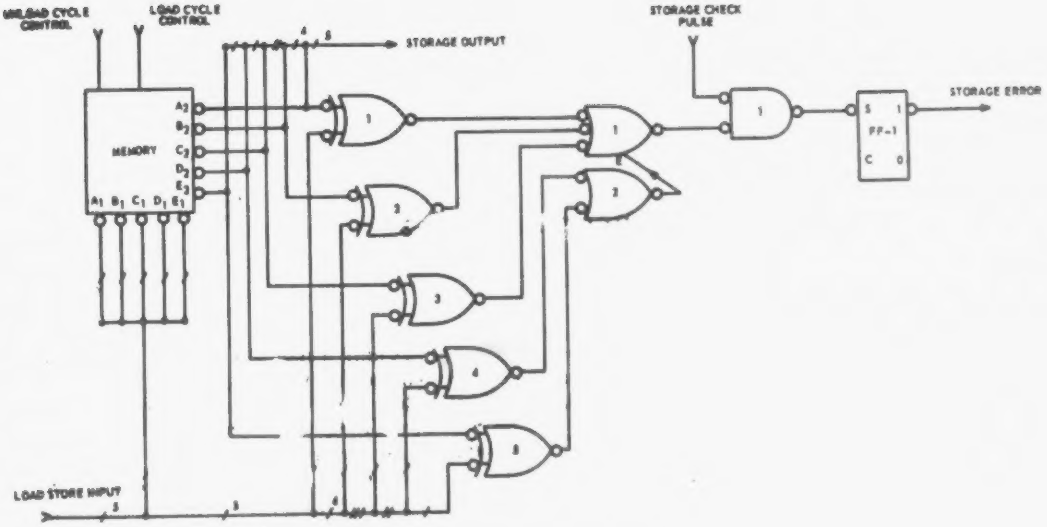

UNLOAD CYCLE CONTROL
LOAD CYCLE CONTROL
STORAGE OUTPUT
STORAGE CHECK PULSE
STORAGE ERROR
MEMORY
A_2
B_2
C_2
D_2
E_2
A_1 B_1 C_1 D_1 E_1
FF-1
S 1
C 0
LOAD STORE INPUT

Figure 1-34. Storage error detection circuit.

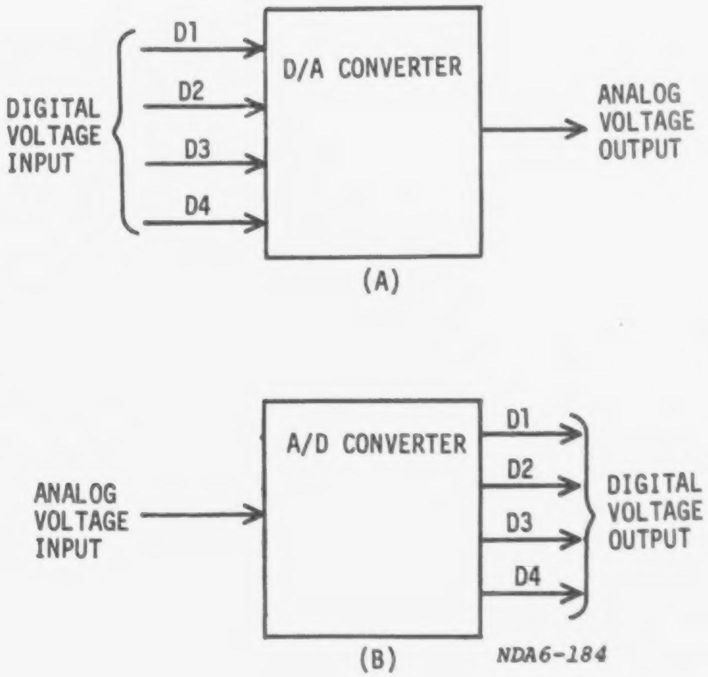

DIGITAL VOLTAGE INPUT
D1
D2
D3
D4
D/A CONVERTER
ANALOG VOLTAGE OUTPUT
(A)
ANALOG VOLTAGE INPUT
A/D CONVERTER
D1
D2
D3
D4
DIGITAL VOLTAGE OUTPUT
(B)
NDA6-184

Figure 1-35. Analog-digital conversion.

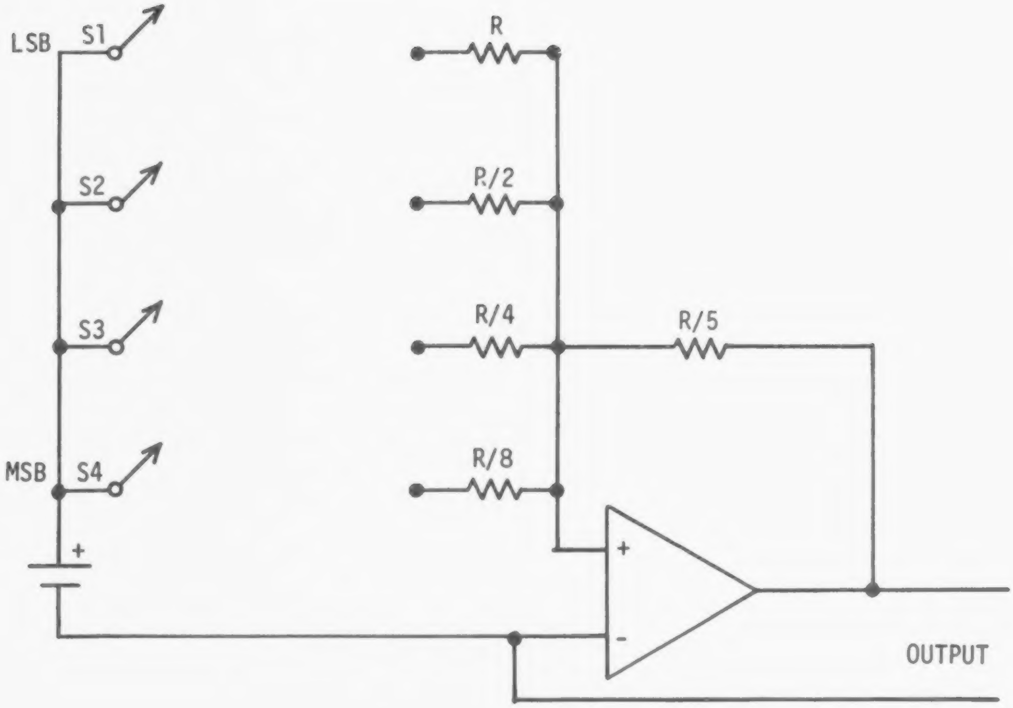


Figure 1-36. Four-bit D/A converter using a resistor network.

016. Specify the operating characteristics of analog-to-digital converters.

Analog-to-Digital Conversion. Not all analog inputs to a computer are in voltage form. Some inputs are mechanical. These inputs can represent speed of linear movement, speed of rotation, position of a shaft, elevation, temperature, pressure, or humidity. Before this information can be used by the digital computer, it must be converted to digital form. Another type of analog-to-digital converter does this job.

Converter disc. A type of converter that converts a mechanical shaft position to a digital number is shown in figure 1-39. This one represents a rotating disc with contact brushes on four channels, and is typical of the many different types of converters used for this purpose. The conducting material in the disc is shown as the dark areas. The disc is arranged into as many channels as there are digits in the largest binary number that is to be coded. A brush is in contact with each channel on the disc. A voltage source is used in the circuit so that, if the brush is in contact with the *conducting* material, a binary *one* is detected. If the brush is in contact with the *nonconducting* material, a binary *zero* is detected. The binary number detected in the position shown in figure 1-39 is 0000. Observe that, for counterclockwise rotation, the illustration shows the binary numbers obtained as the brushes slide on and off the conducting surfaces. Notice that the maximum count is $15_{(10)}$.

Assume that the brushes are attached to a rotating antenna and that the disc is held stationary. When the antenna rotates to 40°, the brushes will be positioned at point "A," and a binary readout of 0001 will be present. As the antenna continues to rotate to 275°, the brushes will be at point "B," and a binary readout of 1100 will be present. The inside track represents the MSD, and the readout changes every 24°. If greater accuracy is required, the number of channels and brushes must be increased.

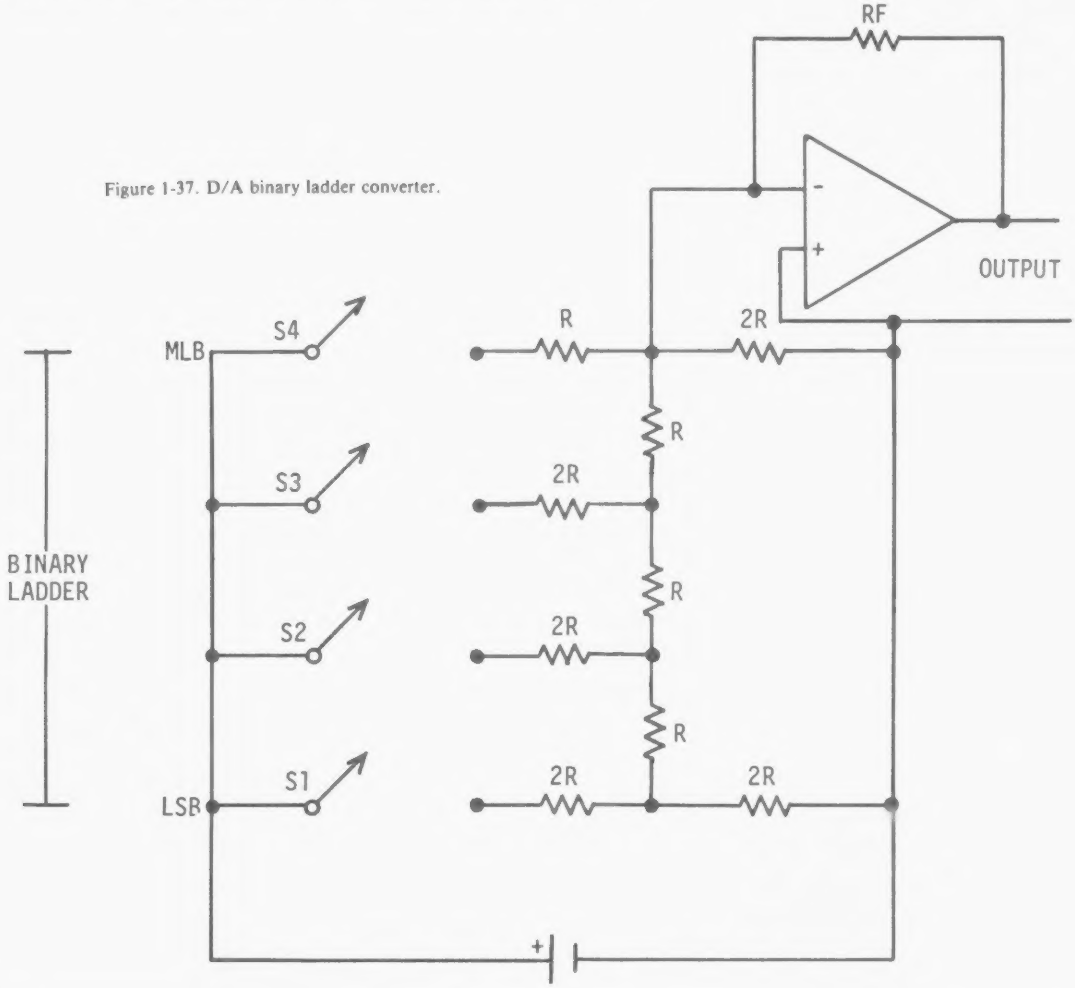
Electronic A/D converters. Probably the most common use of A/D conversion, one to which you will easily relate, is the digital multimeter. The digital multimeter detects an analog input and converts it to a digital signal which drives the circuits that ultimately provide the numeric display.

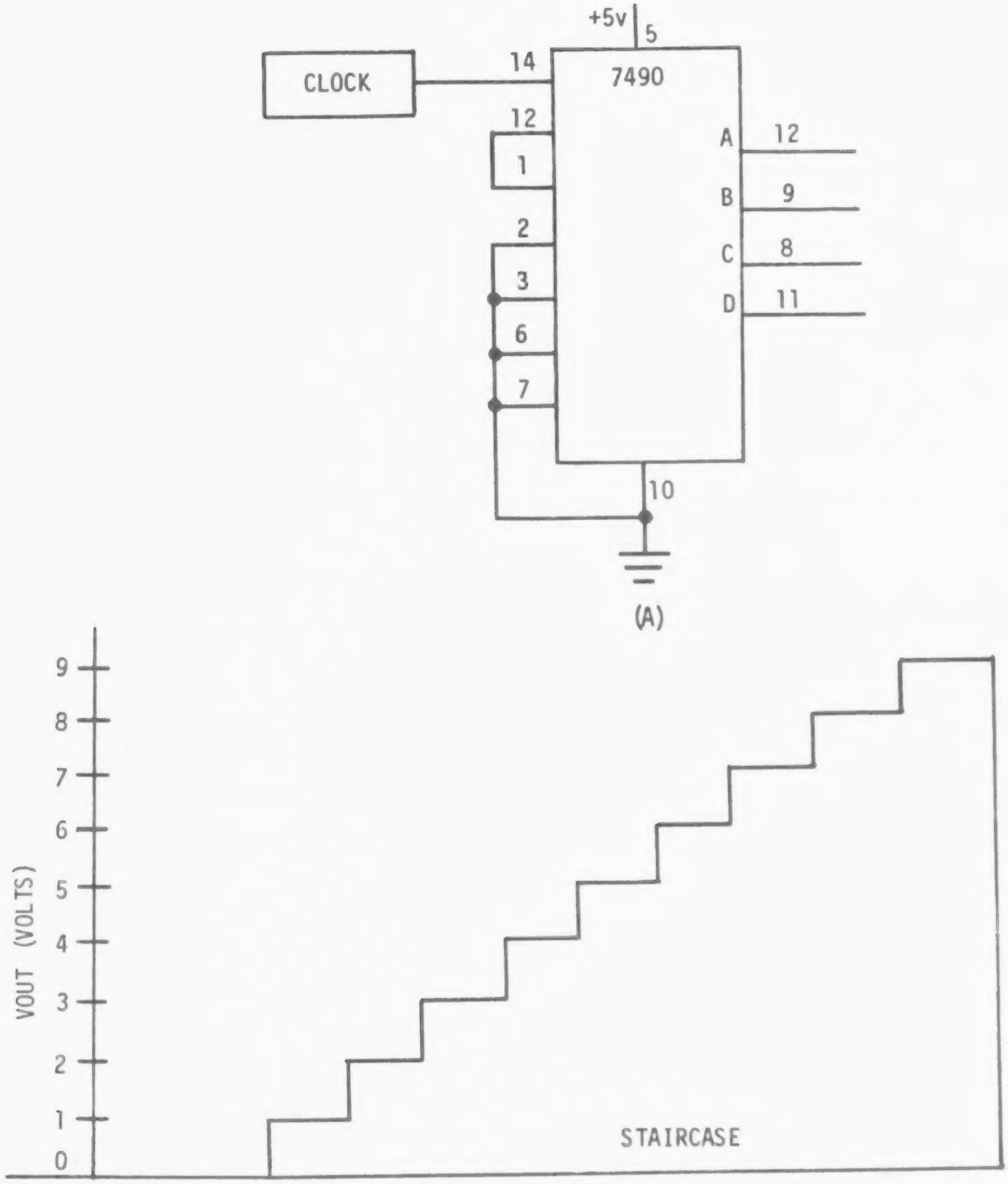
A simple four-bit 0- to 9-volt digital display voltmeter is illustrated by figure 1-40. Much of this circuit you have already studied. Basically you will see a binary ladder, four-bit decade counter, a decoder, an op-amp used as a comparator, and a seven-segment LED numeric display.

The binary ladder is similar to the one shown in figure 1-35, resulting in an output voltage which is increased by 1 volt for each increase in digital value, beginning with 0 and having a maximum output of 9 volts. This particular circuit uses a 20-ms reset clock to the decade counter and the clock produces a count pulse every 0.01 ms. Therefore, it takes 10μsec to cycle digits 0-9 on the display. To better understand this circuit, let's apply a 5-volt analog input to the op-amp and let's also assume that the decade counter has been reset. At this time the binary ladder output is 0 volts (see fig. 1-40). The op-amp output is maximum positive and starts the clock. The clock provides count pulses to the decade counter. The output of the decade counter steps up the voltage in the binary ladder until a count of 0101 (5 volts decimal) is reached. At this the binary ladder output potential will be slightly above the reference voltage of the op-amp. The increase in potential changes the op-amp output to a maximum negative. The negative potential in turn stops the clock and the counter holds the 0101 count until the next reset pulse. At the next reset pulse the counter resets and the cycle begins again. A disadvantage of this circuit is the conversion time (the length of time required by the circuit to convert and read out the data).

Successive Approximation Method. One method of reducing the conversion time is to use what is called a successive approximation counter. An example of this circuit is shown in figure 1-41. The advantage of the successive approximation method is that the conversion time is equal to the time of the clock-pulse multiplied by the number of bits. Referring to figure 1-41, let's again consider a 5-volt analog input to the digital analog converter. The analog-to-digital conversion is accomplished by comparing the analog input voltage to a binary ladder output voltage one bit at a time beginning with the MSB. Using the four-bit successive approximation counter in figure 1-41, we would set and reset the flip-flops representing bit values 8, 4, 2, and 1 beginning with the MSB. With the 5-volt analog input we are using, the MSB flip-flop 8 is set generating an 8-volt output of the binary ladder. Since 8 volts is more than our 5 volts, this flip-flop resets starting the count cycle.

Figure 1-37. D/A binary ladder converter.




+5v
5
CLOCK
14
7490
12
1
2
3
6
7
A
12
B
9
C
8
D
11
10
VOUT (VOLTS)
0
1
2
3
4
5
6
7
8
9
STAIRCASE

(A)

(B)

Figure 1-38. SN7490 TTL decade counter to replace switches of binary ladder.

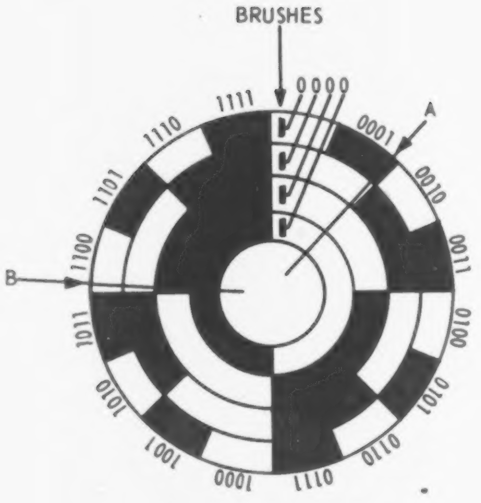


Figure 1-39. Converter disc.

Continuing on the next bit, flip-flop 4 would set generating a 4-volt output of the binary ladder. This is less than our 5-volt input so this flip-flop 4 remains set. The next least significant bit flip-flop 2 sets, again changing the binary ladder output to 6 volts. We now have one volt more than our 5-volt input, so this bit flip-flop 2 is also reset. The next bit is our LSB, causing the LSB flip-flop 1 to set. This results in a 5-volt output of the binary ladder (flip-flop 4 and flip-flop 1). When the output of the ladder and the analog input are equal the count is complete. Note that by comparing only the four bits, this converter has converted our analog input voltage to a digital output to be displayed, in this case by the LED.

Binary-to-Decimal Readout. Conversion other than analog-to-digital and digital-to-analog are required in digital equipment. Often, a visual readout is required in decimal form. This requires a binary-to-decimal conversion and a display device. One such device is the *nixie light,* designed to indicate directly any one of the 10 decimal digits. It is a glow-tube device that converts electrical signals into visual numbers. The nixie light displays a decimal digit directly. The tube is gas-filled and contains 10 cold cathodes and 1 common anode. Each cathode is shaped to form one of the symbols 0 through 9. A positive voltage is applied to the anode, and the selected cathode symbol is grounded. Ionization occurs and causes the symbol to glow. The tubes are available in a variety of sizes, ranging from one-half inch to several inches in diameter. Figure 1-42,A shows two sizes of nixie lights.

Unlike the neon indictor which takes an output directly from a flip-flop, the nixie indicator requires a decoding system to select the desired cathode. Figure 1-42,B shows the decoder network for a count of five (from a three-stage up-counter). The counter is made up of flip-flops A, B, and C. Gate 1 detects a count of five in the counter. The inverter amplifier provides a voltage of the proper polarity and amplitude to drive the nixie indicator. The 10 cathodes are shown as inputs to the nixie tube. Each cathode needs a count detecting (AND) gate and driver like the one shown for cathode 5.

The decoder in figure 1-43 will decode a binary count of 010, 011, or 100. The inputs to the AND-gates can be determined by writing the Boolean equation for the desired count each gate is to detect. If a count of five is to be detected, the equation becomes $A \bar{B} C$. By feeding the one-side output of F/FA, the zero-side output of F/FB, and the one-side output of F/FC to an AND-gate, only a count of five could cause an output. Notice that each AND-gate must have the same number of inputs as there are flip-flops in the counter. It would require four flip-flops and 10 AND-gates to decode 0 through 9.

Seven-Segment Displays. These devices are used to display digits 0–9 and occasionally special letters by illuminating two or more segments. Figure 1-44 illustrates a LED display of the type used in the digital multimeter in figure 1-40. The segments or light emitting elements may be incandescent filament wires, light-emitting diodes (LED), gas discharge glow diodes, or liquid crystal.

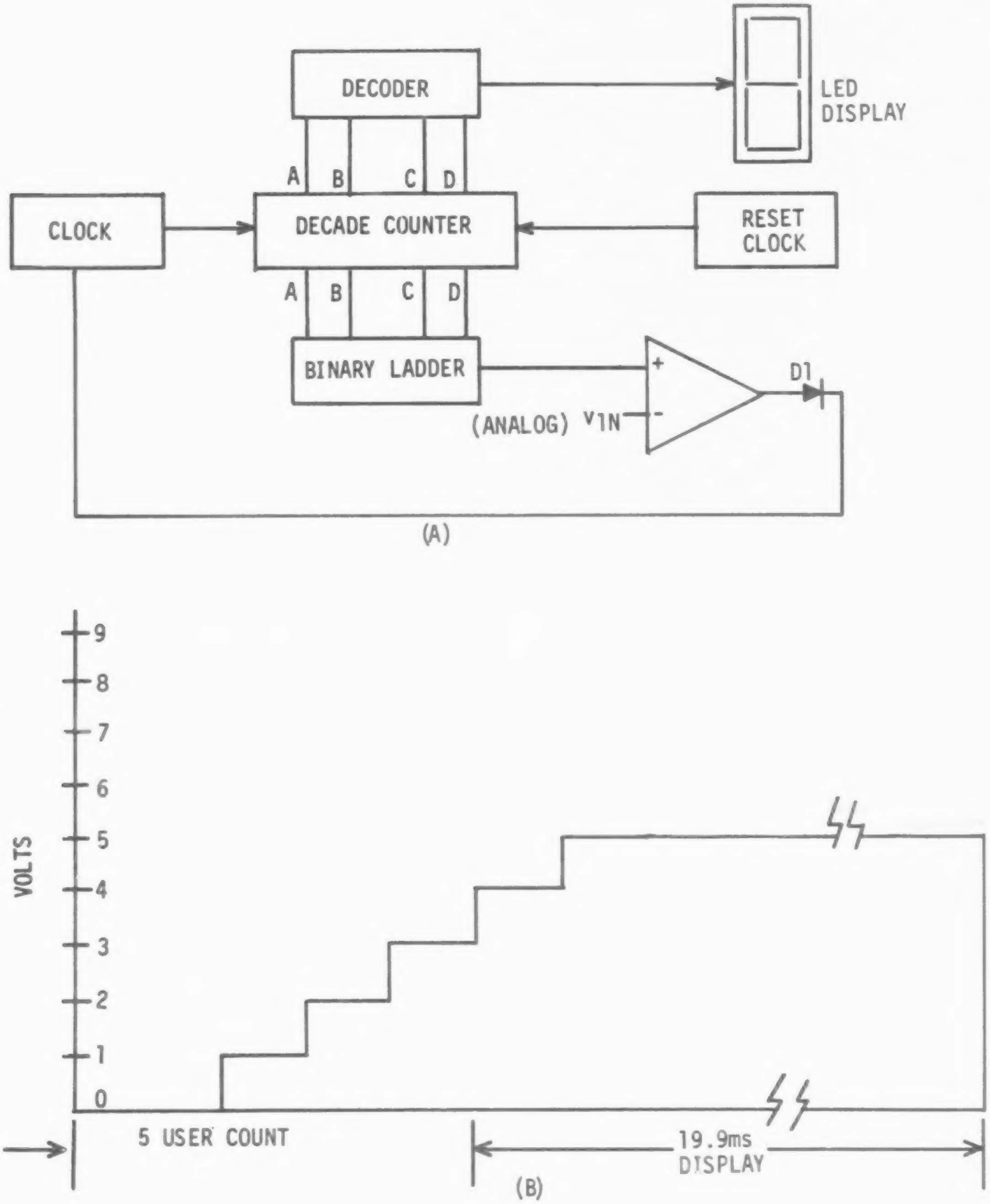

DECODER
LED DISPLAY
A
B
C
D
CLOCK
DECADE COUNTER
RESET CLOCK
A
B
C
D
BINARY LADDER
+
-
D1
(ANALOG) VIN
(A)
VOLTS
9
8
7
6
5
4
3
2
1
0
5 USER COUNT
19.9ms DISPLAY
(B)

Figure 1-40. Simple 0–9-volt digital voltmeter.

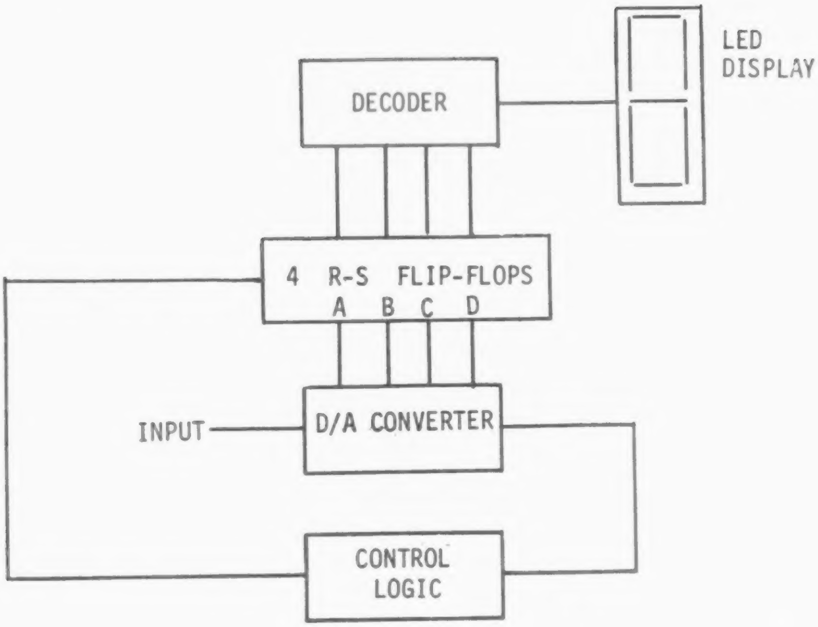
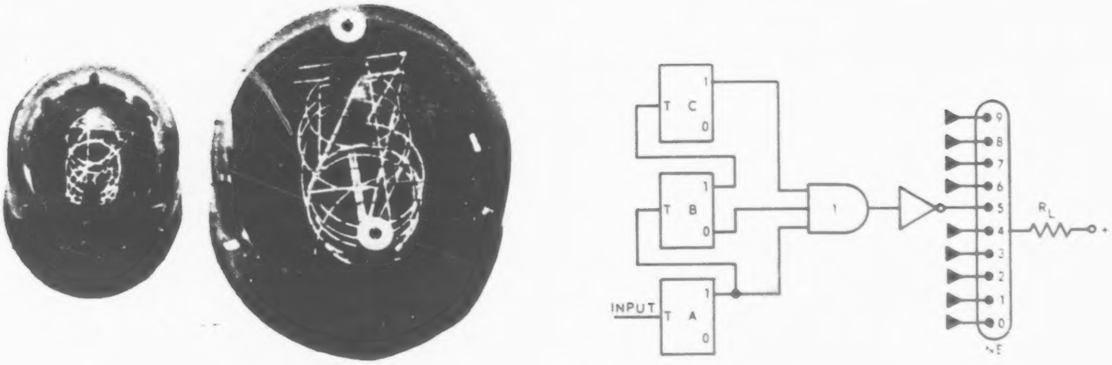

DECODER
LED DISPLAY
4 R-S FLIP-FLOPS
A B C D
INPUT
D/A CONVERTER
CONTROL LOGIC

Figure 1-41. Successive approximation converter.


T C
T B
T A
INPUT
1
0
9
8
7
6
5
4
3
2
1
0
R_L
NE

[A]

[B]

Figure 1-42. Count five nixie decoder.

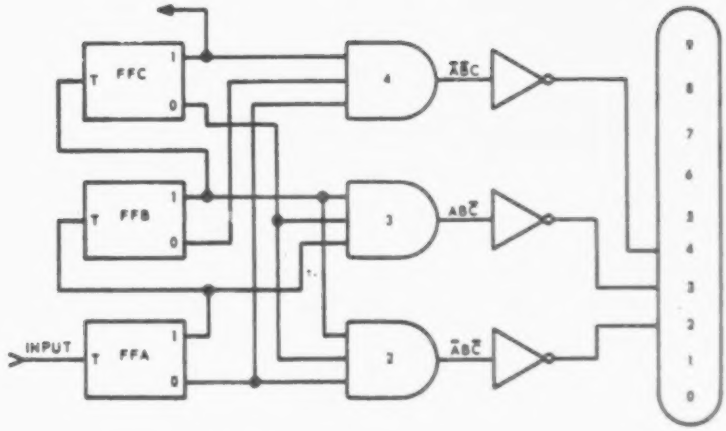


Figure 1-43. Count two, three, and four decoder.

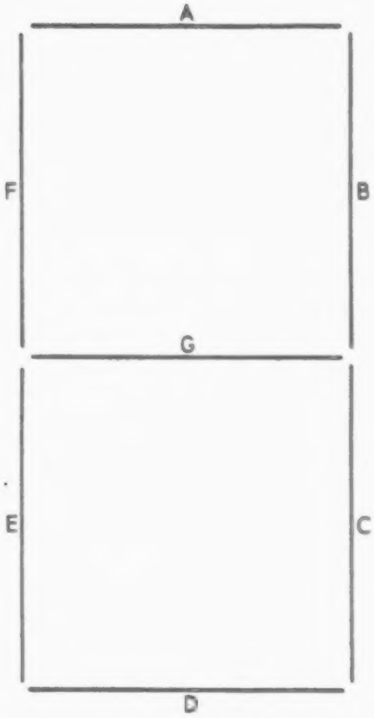


Figure 1-44. LED display (seven segment).

Incandescent filament segments use a thin tungsten wire that glows to a bright white light when current passes through it. The segments are mounted in a single plane with a filter window in front to provide the digit coloring.

The light-emitting diode is a special semiconductor junction which uses certain impurities to cause emission of a visible light when it is forward biased. Depending on the impurities, the emitted light may be yellow, green, or red. LEDs require less power, many operating from a 1.5-volt source, making them practical for battery operated equipment.

In the case of a gas-discharge glow diode, the segment element is the cathode of a special gas-discharge diode. When a high voltage is applied to the element, the gas surrounding the element is ionized and emits a red-orange glow.

Liquid crystal displays draw the least current of those discussed above. They are made in two types, *transmissive* (backlighting) and *reflective* (ambient lighted). Each segment has a thin layer of liquid crystal sandwiched between two clear glass plates. Each glass plate has a conductive coating and is connected to the energizing source. When energized, the properties of the liquid crystal material in the segment change, causing the light transmission from either backlighting or from reflective lighting. One disadvantage of this device is that it must have external ambient light.

Exercises (016):

1. What is an analog-to-digital converter?

2. How is the binary number represented by each segment of a coded disc readout?

3. How is greater accuracy achieved with the converter disc?

4. In figure 1-40, when is the output of the amplifier maximum negative?

5. In figure 1-40, when does the counter begin its cycle?

6. In figure 1-41, what stops the count when using successive approximation?

7. How is conversion time computed in a successive approximation converter?

8. What is a nixie light?

9. Which seven-segment display is practical for battery operated equipment?

10. Which seven-segment display must have a light source?

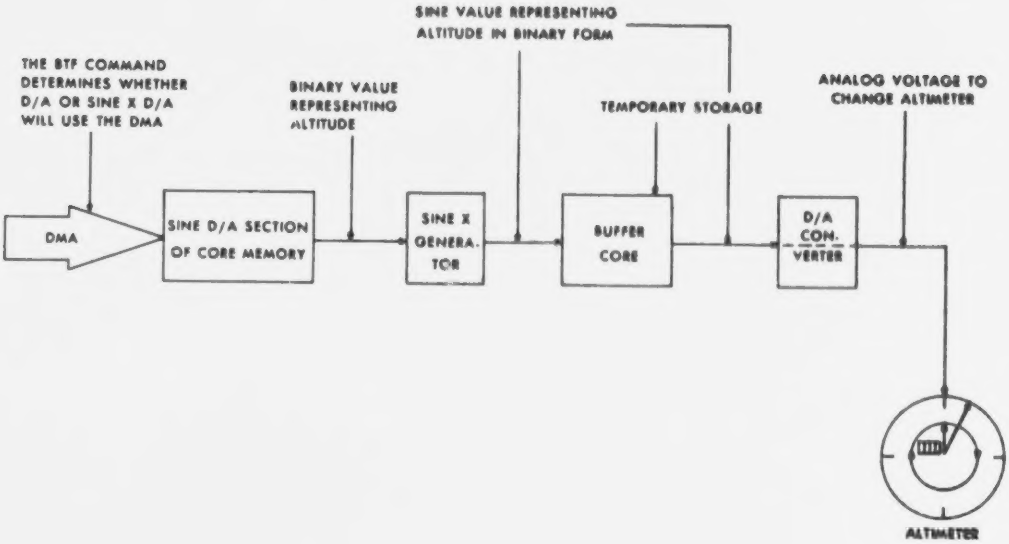

SINE VALUE REPRESENTING
ALTITUDE IN BINARY FORM
THE BTF COMMAND
DETERMINES WHETHER
D/A OR SINE X D/A
WILL USE THE DMA
BINARY VALUE
REPRESENTING
ALTITUDE
TEMPORARY STORAGE
ANALOG VOLTAGE TO
CHANGE ALTIMETER
DMA
SINE D/A SECTION
OF CORE MEMORY
SINE X
GENERA-
TOR
BUFFER
CORE
D/A
CON-
VERTER
ALTIMETER

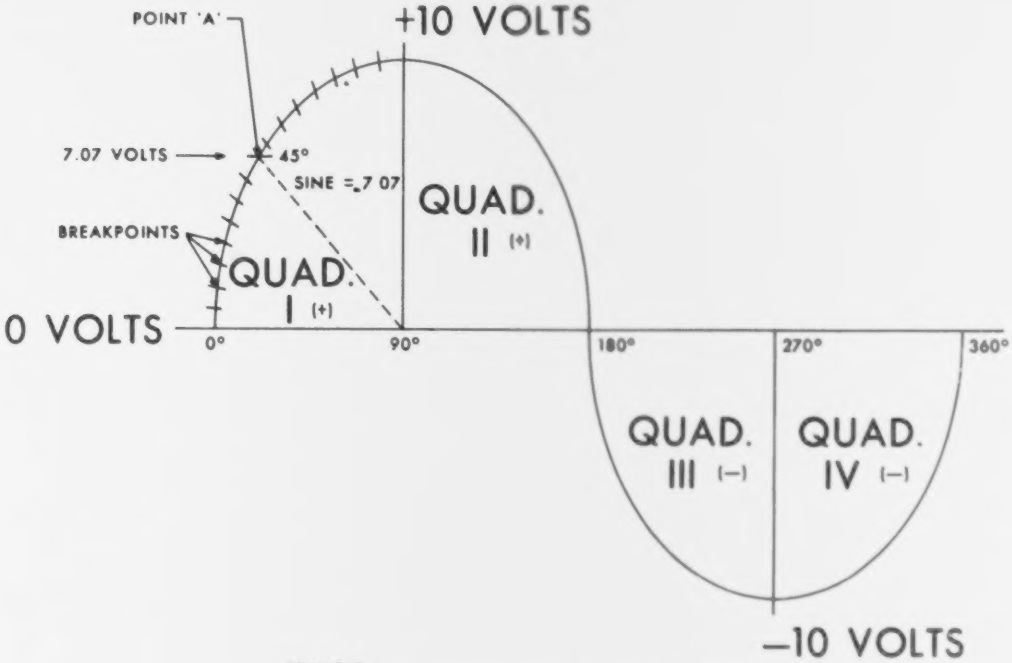
Figure 1-45. D/A conversion with the sine X generator.

017. State the purpose of the sine X generator and state basically how it works.

Sine X Generator. Digital-to-analog conversion, or the conversion of computer binary data to analog data, may be accomplished using the sine X method. In this particular discussion we are again using a general-purpose computer. The sine D/A conversion system in the GP computer uses a buffer core memory. Buffer core memory is a small core memory consisting of 2,048 words, 24 bits in length. It is primarily used to store target data for the DTG (digital target generator). However, the first portion of the buffer core memory is used for D/A conversion, which we discussed previously, and sine D/A conversion. This section is called working storage.

The term "sine X" is taken from fundamental trigonometry. A sine wave can be generated by rotating a vector through 360° from the X axis and plotting the sines of all an gles generated by the rotation. Therefore, the approximate value of the sine of any angle can be read from the graph of the sine of X, which is the sine curve.

The sine X generator is actually a subsystem of the linkage system. It takes a linear digital input and converts it to a representtive value of the sine X function of the input. A signal representing altitudes is an example of a linear input. Now refer to figure 1-45. Assume that the BTF (block transfer) instruction command selects the sine X generator to use the DMA. (Bits 2, 3, and 4 of the dried memory access (DMA) control word determine which device will use DMA.) The binary value representing altitude is then transferred from the sine D/A section of core memory to the sine X generator. The sine X generator changes the incoming binary value to a sine value. This sine value, in binary form, is then transferred to the buffer core memory. Here it is temporarily stored until called for by a special priority system. The sine value, still in binary form, then goes to the D/A converter where the actual conversion to an analog voltage takes place. The analog voltage is then available to position an indicator such as the altimeter. This analog voltage is somewhere between a positive 10 volts and a negative 10 volts. Notice that the sine X generator is feeding an instrument with indicator needles that rotate through 360°. The sine X generator is used to feed this type of instrument



EXAMPLE:
A BINARY VALUE WHICH HAS BEEN LOCATED AT POINT 'A' BY DECODING THE BIT POSITIONS WOULD HAVE A VALUE OF THE SINE OF 45°. THIS VALUE IS .707 OR .7 OF 10 VOLTS OR 7.07 VOLTS

Figure 1-46. Sine X conversion example.

because the conversion from digital to analog is easier for the computer from an engineering standpoint.

The sine X generator approximates the sine X by interpolating on straight line segments between known values on a sine curve. Our problem then is to convert a digital value to its sine value, which would be an exact position on the sine curve. The digital value will then correspond to the correct analog voltage after the actual D/A conversion occurs.

An example of changing a binary value to a sine value is shown in figure 1-46. This binary value has been located to point A by decoding the bit positions of a binary word. In this example we have assumed that the bit positions have a value of 45°. The sine of 45° is 0.707; therefore, after going through the D/A converter the sine value would be equal to 7.07 volts. Other points on the curve would convert in the same manner. For exmple, 90°, which has a sine value of one, would equal 10 volts.

The sine wave is initially broken down into four quadrants, as shown in figure 1-46. The first and second quadrants have positive signs; the third and fourth quadrants have negative signs. Each quadrant is further broken down into 16 equal segments. Each segment is further divided into 64 equal increments. The binary data from the computer must be decoded to find the exact location on the sine curve where it is to be positioned. This position then determines the analog voltage, as shown in figure 1-46.

The bits coming into the sine generator are decoded as follows:

- Bits 0 through 4 are not used in conjunction with the sine generator.
- Bit 5 determines the sign of the sine curve.
- Bits 5 and 6 determine the quadrant.
- Bits 7 through 10 determine the segment of the quadrant.
- Bits 11 through 16 determine the position within the segment.

The sine X conversion operation may be summarized by the following statements: The incoming digital word is decoded into a breakpoint (fig. 1-46) and corrections by the sine X generator as listed above. The breakpoint and corrections represent an exact point on a hypothetical sine curve. After the incoming word is decoded by the sine X generator and located on this hypothetical sine curve, the sine X generator sends the sine value, in binary form, to the buffer core memory. The buffer core memory temporarily stores this value. The data then goes from the buffer core memory to the D/A converter for the actual converstion to an analog voltage.

Exercises (017):

1. Where does the term "sine X" come from?

2. How can you graph the approximate sine of any angle?

3. What is the purpose of the sine X generator?

4. In the computer discussed in the text, for what is the buffer core memory used?

5. What converter feeds an instrument which has indicator needles rotating through 360 degrees?

6. Into what major segments is the sine wave broken down?

7. Which are positive and which are negative?

8. How is each quadrant further broken down?

9. How are the bits going into the sine X generator broken down?

1-5. TTL IC Combinational Logic

A comparison of the circuits and the functions performed by the combinational logic circuits you have studied in this unit will reveal two interesting facts. First is that many circuits can be used for more than one function. Consider the many applications of the exclusive OR-gate or compare an adder to a subtractor circuit. Second, the more complex the function to be performed the more components required in the circuit. The designers of integrated circuits take into consideration both of these characteristics.

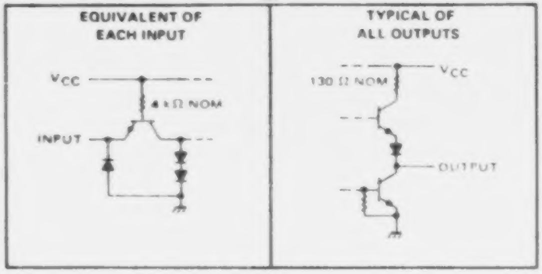
018. Specify the distinctive characteristics of various digital integrated circuits which perform the functions of combinational logic circuits.

TYPES SN5486, SN54L86, SN54LS86, SN54S86, SN7486, SN74L86, SN74LS86, SN74S86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

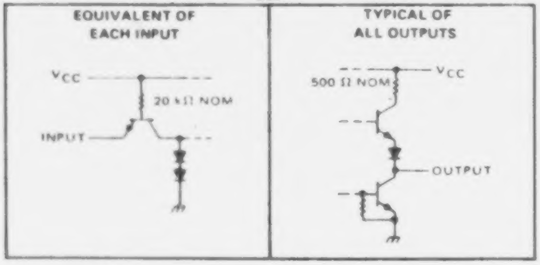
BULLETIN NO DL-S 7211825, DECEMBER 1972

schematics of inputs and outputs

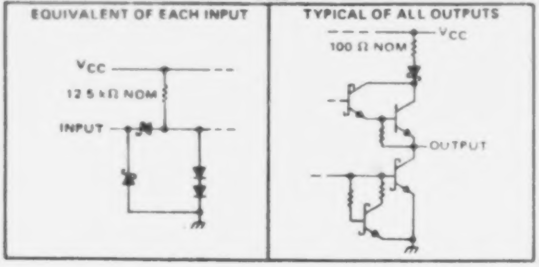
'86


EQUIVALENT OF EACH INPUT
VCC
4 kΩ NOM
INPUT
TYPICAL OF ALL OUTPUTS
130 Ω NOM
VCC
OUTPUT

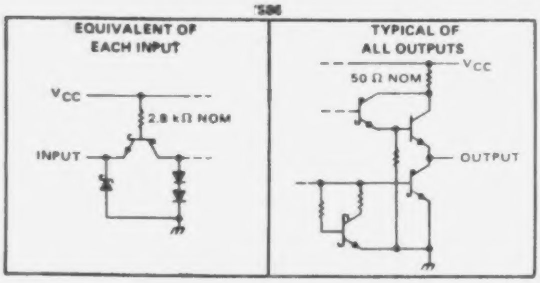
'L86


EQUIVALENT OF EACH INPUT
VCC
20 kΩ NOM
INPUT
TYPICAL OF ALL OUTPUTS
500 Ω NOM
VCC
OUTPUT

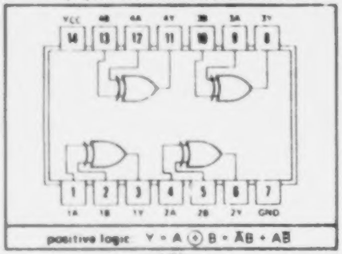
'LS86


EQUIVALENT OF EACH INPUT
VCC
12.5 kΩ NOM
INPUT
TYPICAL OF ALL OUTPUTS
100 Ω NOM
VCC
OUTPUT

'S86

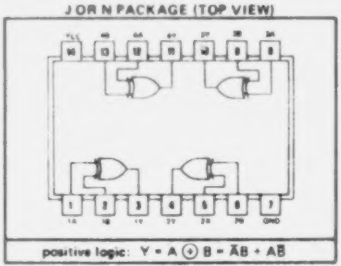

EQUIVALENT OF EACH INPUT
VCC
2.8 kΩ NOM
INPUT
TYPICAL OF ALL OUTPUTS
50 Ω NOM
VCC
OUTPUT

'86, 'LS86, 'S86
J, N, OR W PACKAGE (TOP VIEW)


VCC
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND

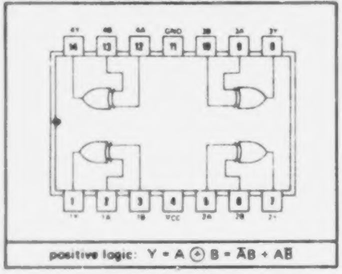
positive logic: Y = A ⊕ B = $\bar{A}B + A\bar{B}$

'L86
J OR N PACKAGE (TOP VIEW)


VCC
4B
4A
4Y
3Y
3B
3A
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2Y
2A
2B
GND

positive logic: Y = A ⊕ B = $\bar{A}B + A\bar{B}$

'L86
T PACKAGE (TOP VIEW)


4Y
4B
4A
GND
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1Y
1A
1B
VCC
2A
2B
2Y

positive logic: Y = A ⊕ B = $\bar{A}B + A\bar{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'L86	55 ns	15 mW
'LS86	10 ns	30.5 mW
'S86	7 ns	250 mW

Figure 1-47. SN5486, SN7486 quadruple two-input exclusive OR-gates.

Many combinational logic circuits are available using medium-scale integration (MSI) and large-scale integration (LSI). The operations remain basically the same, but are accomplished much faster using less space and power. Therefore, digital integrated circuitry has become the choice of the designers when constructing new equipment. The most widely used form of integrated digital logic circuits (DIC) is the TTL or transistor transistor logic chips. TTL is best represented by the SN54/74 series of DICs originally developed by Texas Instruments Operation. Today there are several manufacturers of these DICs which use the same numbering system.

The following digital integrated circuits are presented with the appropriate functional explanations, diagrams, and truth tables. They are from either *The TTL Data Book for Design Engineers* or *Supplement to the TTL Data Book for Design Engineers,* CC–411 and CC–416, published by the Texas Instruments Corporation, Dallas, Texas. Because of the well organized manner of presentation, we have not deviated from their format. Both of the books are excellent references when you might have a question on some new device and are unable to locate the information in the appropriate technical manual.

The digital integrated circuits presented here are only meant to be representative of the available digital integrated circuits in the field. Space does not permit publication of the full line presently in use, and there are newer special function DICs continually being developed.

Quadruple Two-Input Exclusive OR-Gates. Types SN5486 and SN7486 are shown in figure 1-47. These monolithic devices function with the Boolean expression: $Y = \bar{A}B + D\,A\bar{B}$. When the input states are complementary, the output goes to a logic 1. Additional information is given in figure 1-47.

4-Line-to-10-Line Decoders (1 of 10). Types SN5442, SN5443, SN5444, SN7442, SN7443, and SN7444 are shown in figure 1-48. The functions which can be performed by this type of decoder are: BCD-to-decimal decoding, excess-3-to-decimal decoding, 4-line-to-16-line decoding, and 3-line-to-8-line decoding. These monolithic decimal decoders consist of eight inverters and ten 4-input NAND-gates. You will notice that in this case the top view of the package shown in figure 1-48 gives no clue as to what is really inside. This is of no real consequence, because you would be unable to repair the individual units within the package if they should fail. For specific operation for any input logic configuration, you should consult the truth table shown in figure 1-48.

Four-Bit Binary Full-Adder (Look-Ahead Carry). Types S5483 and N7483 are shown in figure 1-49. It is a four-bit binary full adder used for adding two four-bit binary numbers. A look-ahead carry circuit is included to provide minimum carry propagation delays. Refer to figure 1-49 for the truth table and functional logic diagram for specific functional analysis and operation.

Four-Bit Magnitude Comparators. S5483 and N7485 are shown in figure 1-50. They perform magnitude comparison of straight binary and straight BCD codes. Three fully decoded decisions about two 4-bit words (A and B) are made and are externally available at three outputs. The functional block diagram and truth tables are also shown in figure 1-50.

Data Selectors/Multiplexers. Types SN54140, SN54141, SN54152, SN74150, SN74151, and SN74152 are shown in figure 1-51. You will note that three separate diagrams are shown for the specifically numbered circuits. Each of these types can perform similar functions. Some of the functions are: Select 1 of 16 (or 1 of 8 data sources, serve as a five-variable function generator (SN54150, SN74150), perform parallel-to-series conversion, and permit multiplexing from N lines to one line. These are fully compatible with TTL, DTL, and other MSI circuits. Each of these monolithic data selectors/multiplexors contains inverter/drivers to supply fully complementary, on-chip, binary decoding data selection to the AND/OR/INVERT gate. The SN54151/74151 features complementary outputs, whereas the SN5415 0/74150 and SN54152/74152 have inverted outputs only. The SN54150 and SN54151/74151 circuits are provided with a strobe input which, when taken to a logic 0, enables the function of these multiplexers. This allows gating of information at a specific time. The truth table for SN54151/SN74151 and SN54152/SN74152 units is shown in figure 1-51,B. The truth table can be used to prove the configurations which can be gated through from the data input point while using the functional logic diagrm shown in figure 1-51,A. The consequent output at points Y and W can be worked out through logic analysis.

Eight-Bit Odd/Even Parity Generators/Checkers. SN74180 parity generator/checker is shown in figure 1-52, along with appropriate truth table and functional logic diagram. These universal, monolithic, eight-bit parity generators/checkers feature odd/even output and control inputs to facilitate operation in either odd or even parity applictors. The word-length capability is easily expanded by cascading. Typical applications are shown for these parity circuits being used to degenerate and check parity.

Exercises (018):

1. Which integrated circuit discussed in the text will function as a quarter-adder?

2. What integrated circuit discussed in the text may be used for excess-three-to-decimal decoding?

3. How is word length capability expanded for parity checking with the SN74180 DIC?

TTL
MSI

TYPES SN5442A THRU SN5444A, SN54L42 THRU SN54L44, SN7442A THRU SN7444A, SN74L42 THRU SN74L44 4-LINE-TO-10-LINE DECODERS (1-OF-10)

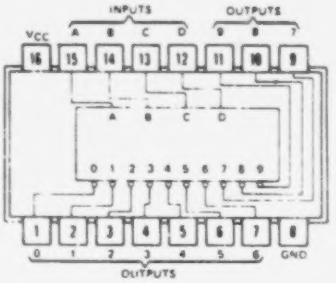
BULLETIN NO. DL-S 7211861, DECEMBER 1972

'42A, 'L42 . . . BCD-TO-DECIMAL
'43A, 'L43 . . . EXCESS-3-TO-DECIMAL
'44A, 'L44 . . . EXCESS-3-GRAY-TO-DECIMAL

- Also for Application as
  - 4-Line-to-16-Line Decoders
  - 3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A, '43A, '44A	140 mW	17 ns
'L42, 'L43, 'L44	70 mW	49 ns

SN54'/SN74' . . . J, N, OR W PACKAGE
SN54L'/SN74L' . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A and 'L42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt.

The 'L42, 'L43, 'L44 decoders are designed specifically for power critical or battery-operated systems. The '42A, '43A, and '44A decoders are intended for higher performance systems, especially new designs, where power is not critical. For ultra-high performance and/or speed critical memory decoders, the SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

FUNCTION TABLE

NO.	'42A, 'L42 BCD INPUT				'43A, 'L43 EXCESS-3-INPUT				'44A, 'L44 EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

Figure 1-48. SN5442, SN5443, SN5444, SN7442, SN7443, SN7444 4-line-to-10-line decoders.

TTL
MSI

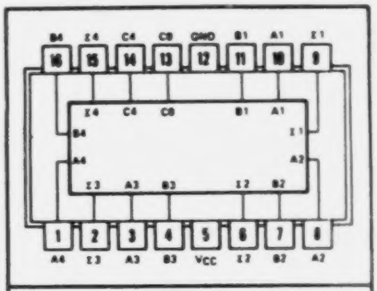
TYPES SN5483A, SN54LS83, SN7483A, SN74LS83
4-BIT BINARY FULL ADDERS

BULLETIN NO. DL-S 7211863, DECEMBER 1972

- **For applications in:**
  - **Digital Computer Systems**
  - **Data-Handling Systems**
  - **Control Systems**
- **SN54283/SN74283 Are Recommended For New Designs as They Feature Supply Voltage and Ground on Corner Pins to Simplify Board Layout**

TYPE	TYPICAL ADD TIMES TWO 8-BIT WORDS	TYPICAL ADD TIMES TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER 4-BIT ADDER
'83A	23 ns	43 ns	310 mW
'LS83	89 ns	165 ns	75 mW

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. The adders are designed so that logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion. Designed for medium-to-high-speed, the circuits utilize high-speed, high-fan-out transistor-transistor logic (TTL) but are compatible with both DTL and TTL families.

The '83A circuits feature full look ahead across four bits to generate the carry term in typically 10 nanoseconds to achieve partial look-ahead performance with the economy of ripple carry.

The 'LS83 can reduce power requirements to less than 20 mW/bit for power-sensitive applications. These circuits are implemented with single-inversion, high-speed, Darlington-connected serial-carry circuits within each bit.

Series 54 and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS are characterized for 0°C to 70°C operation.

FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L / WHEN C2 = L			WHEN C0 = H / WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A3, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54', SN54LS' Circuits	−55°C to 125°C
SN74', SN74LS' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the '83A, this rating applies between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4. For the 'LS83, this rating applies between the following pairs: A1 and B1, A1 and C0, B1 and C0, A3 and B3.

Figure 1-49. S5483, N7483 four-bit binary full adder
(look-ahead carry)

functional block diagrams

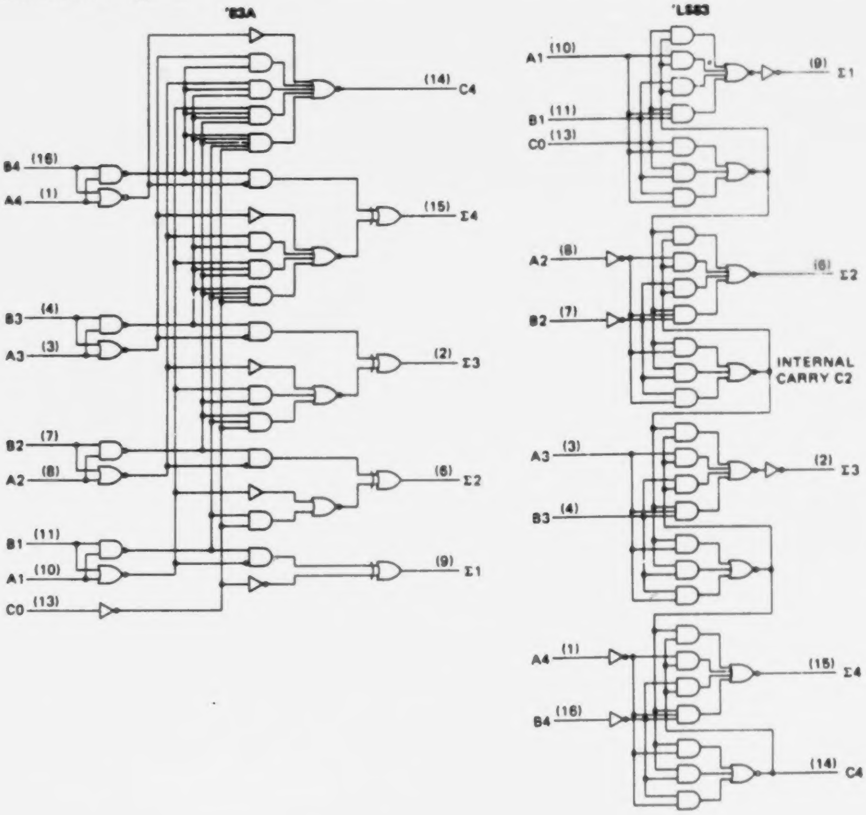

'83A
B4 (16)
A4 (1)
B3 (4)
A3 (3)
B2 (7)
A2 (8)
B1 (11)
A1 (10)
C0 (13)
(14) C4
(15) Σ4
(2) Σ3
(6) Σ2
(9) Σ1
'LS83
A1 (10)
B1 (11)
C0 (13)
(9) Σ1
A2 (8)
B2 (7)
(6) Σ2
INTERNAL CARRY C2
A3 (3)
B3 (4)
(2) Σ3
A4 (1)
B4 (16)
(15) Σ4
(14) C4

Figure 1-49. S5483, N7483 four-bit binary full adder
(look-ahead carry) (cont'd)

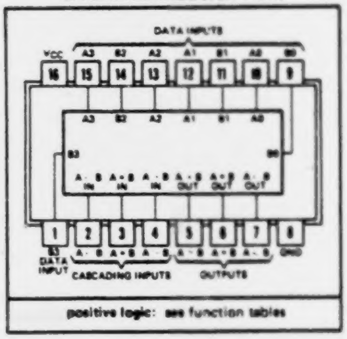
TTL
MSI

TYPES SN5485, SN54L85, SN54S85, SN7485, SN74L85, SN74S85 4-BIT MAGNITUDE COMPARATORS

BULLETIN NO. DL-S 7211810, DECEMBER 1972

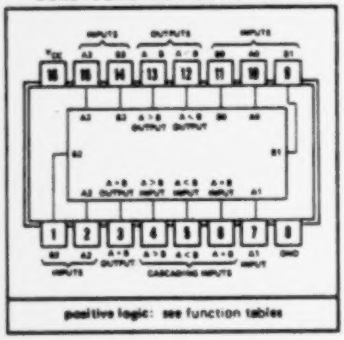
TYPE	TYPICAL POWER DISSI-PATION	TYPICAL DELAY (4-BIT WORDS)
'85	275 mW	23 ns
'L85	20 mW	90 ns
'S85	365 mW	11 ns

'85, 'S85
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)


DATA INPUTS
VCC
A3
B2
A2
A1
B1
A0
B0
16
15
14
13
12
11
10
9
B3
A < B IN
A = B IN
A > B IN
A > B OUT
A = B OUT
A < B OUT
1
2
3
4
5
6
7
8
B3 DATA INPUT
CASCADING INPUTS
OUTPUTS
GND

positive logic: see function tables

'L85
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)


INPUTS
OUTPUTS
INPUTS
VCC
A3
B3
A > B
A < B
B0
A0
B1
16
15
14
13
12
11
10
9
A > B OUTPUT
A < B OUTPUT
B2
A = B OUTPUT
A > B INPUT
A < B INPUT
A = B INPUT
1
2
3
4
5
6
7
8
B2
A2
A = B OUTPUT
A > B
A < B
A = B
A1 INPUT
GND
CASCADING INPUTS

positive logic: see function tables

description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input and additionally for the 'L85, low-level voltages applied to the A > B and A < B inputs. The cascading paths of the '85 and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

'85, 'S85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

'L85

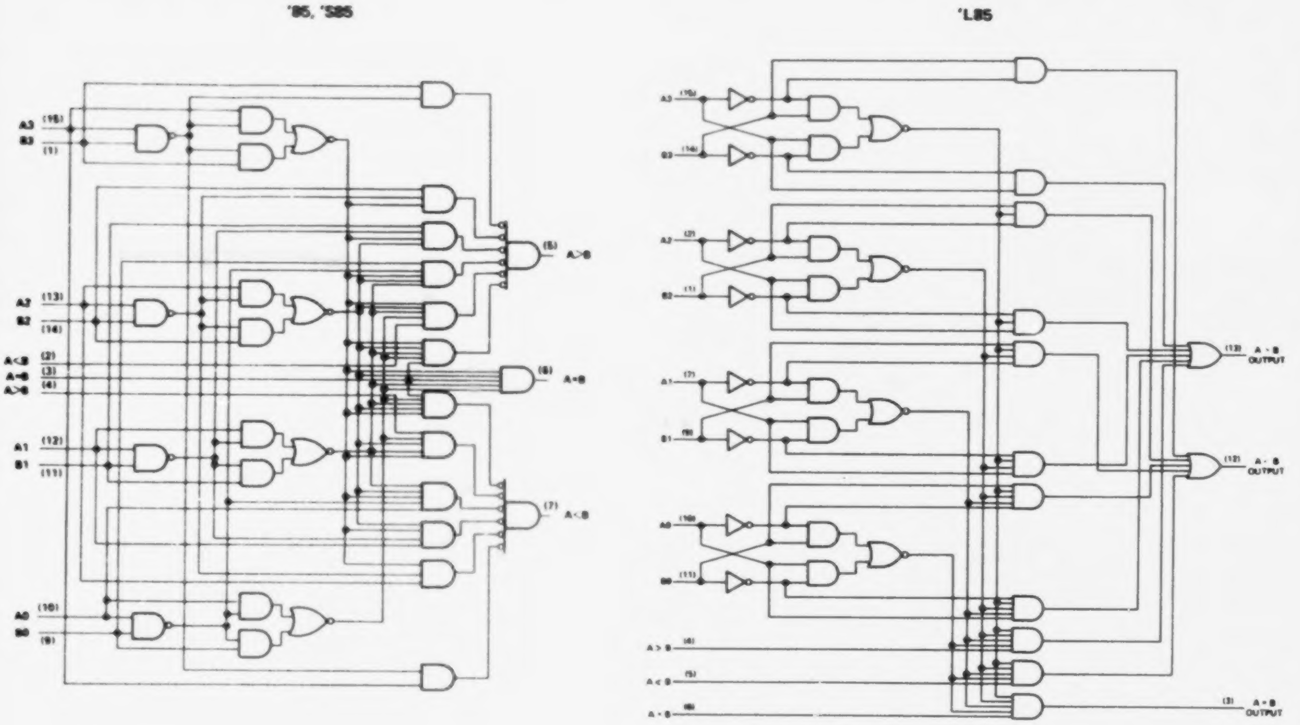
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

Figure 1-50. S5485, N7485 four-bit magnitude comparators.

TYPES SN5485, SN54L85, SN54S85,
SN7485, SN74L85, SN74S85
4-BIT MAGNITUDE COMPARATORS

functional block diagrams


A3 (15)
B3 (1)
A2 (13)
B2 (14)
A<B (2)
A=B (3)
A>B (4)
A1 (12)
B1 (11)
A0 (10)
B0 (9)
(5) A>B
(6) A=B
(7) A<B
A3 (15)
B3 (14)
A2 (2)
B2 (1)
A1 (7)
B1 (8)
A0 (10)
B0 (11)
A > B (4)
A < B (5)
A = B (6)
(13) A > B OUTPUT
(12) A < B OUTPUT
(3) A = B OUTPUT

'85, 'S85

'L85

Figure 1-50. S5485, N7485 four-bit magnitude comparators (cont'd).

TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74152A, SN74LS151, SN74LS152, SN74S151 DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7211819, DECEMBER 1972

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL and DTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
'150	11 ns	200 mW
'151A	8 ns	145 mW
'152A	8 ns	130 mW
'LS151	11 ns†	30 mW
'LS152	11 ns†	28 mW
'S151	4.5 ns	225 mW

†Tentative data

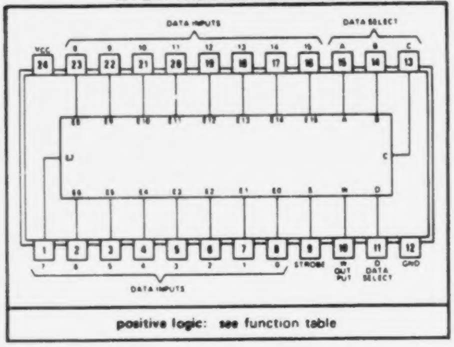
description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

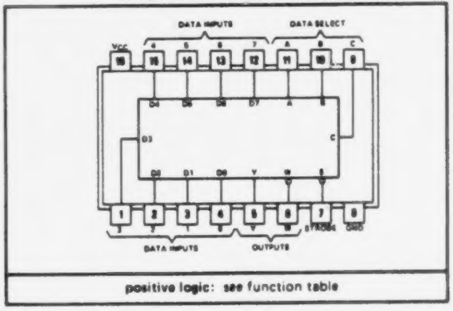
The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

'150
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)


DATA INPUTS
DATA SELECT
VCC
8
9
10
11
12
13
14
15
A
B
C
24
23
22
21
20
19
18
17
16
15
14
13
A
B
C
D
W
S
1
2
3
4
5
6
7
8
9
10
11
12
7
6
5
4
3
2
1
0
STROBE
W OUTPUT
D DATA SELECT
GND
DATA INPUTS

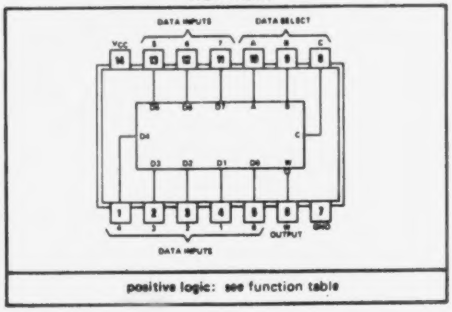
positive logic: see function table

'151A, 'LS151, 'S151
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)


DATA INPUTS
DATA SELECT
VCC
4
5
6
7
A
B
C
16
15
14
13
12
11
10
9
D4
D5
D6
D7
A
B
D3
C
D2
D1
D0
Y
W
S
1
2
3
4
5
6
7
8
3
2
1
0
Y
W
STROBE
GND
DATA INPUTS
OUTPUTS

positive logic: see function table

'152A, 'LS152
W FLAT PACKAGE
(TOP VIEW)


DATA INPUTS
DATA SELECT
VCC
5
6
7
A
B
C
14
13
12
11
10
9
8
D5
D6
D7
A
B
D4
C
D3
D2
D1
D0
W
1
2
3
4
5
6
7
4
3
2
1
0
W
OUTPUT
GND
DATA INPUTS

positive logic: see function table

Figure 1-51A. SN54150, Sn54151, SN74152, SN74151, SN74152
data selectors/multiplexers.

TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74152A, SN74LS151, SN74LS152, SN74S151
DATA SELECTORS/MULTIPLEXERS

logic

'150

FUNCTION TABLE

INPUTS					OUTPUT
SELECT				STROBE	W
D	C	B	A	S	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

'151A, 'LS151, 'S151

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

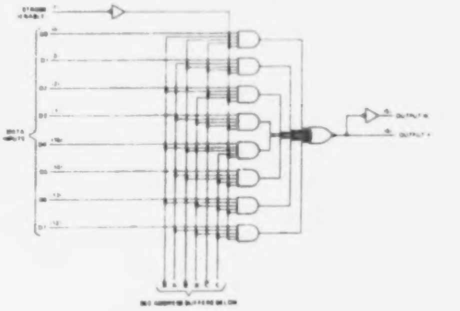
'152A, 'LS152

FUNCTION TABLE

SELECT INPUTS			OUTPUT W
C	B	A	
L	L	L	$\overline{D0}$
L	L	H	$\overline{D1}$
L	H	L	$\overline{D2}$
L	H	H	$\overline{D3}$
H	L	L	$\overline{D4}$
H	L	H	$\overline{D5}$
H	H	L	$\overline{D6}$
H	H	H	$\overline{D7}$

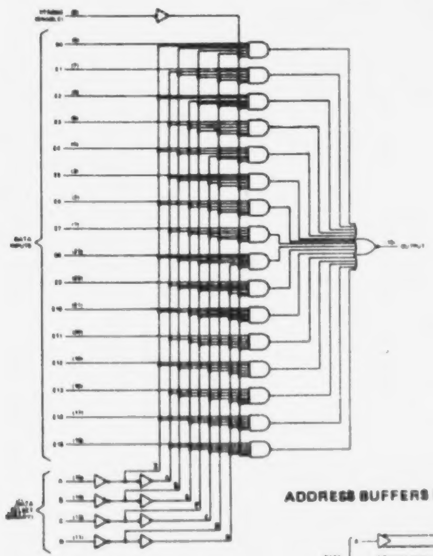
H = high level, L = low level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 . . . D7 = the level of the D respective input

'151A, 'LS151, 'S151

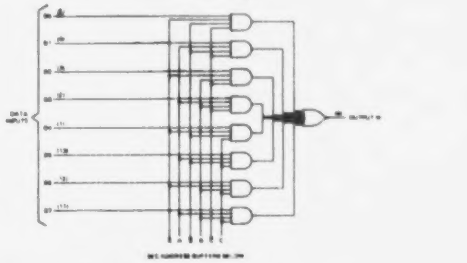


functional block diagrams

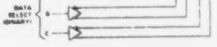
'150



'152A, 'LS152



ADDRESS BUFFERS FOR '151A, '152A



ADDRESS BUFFERS FOR 'LS151, 'S151, 'LS152

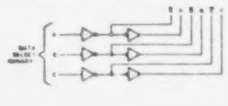


Figure 1-51B. SN74151 data selector.

TTL
MSI

TYPES SN54180, SN74180
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

BULLETIN NO. DL-S 7211814, DECEMBER 1972

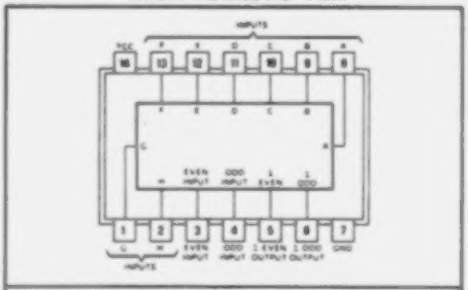
logic

FUNCTION TABLE

INPUTS			OUTPUTS	
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = high level, L = low level, X = irrelevant

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)


INPUTS
VCC
F
E
D
C
B
A
14
13
12
11
10
9
8
G
H
EVEN INPUT
ODD INPUT
Σ EVEN
Σ ODD
1
2
3
4
5
6
7
EVEN INPUT
ODD INPUT
Σ EVEN OUTPUT
Σ ODD OUTPUT
GND

positive logic: see function table

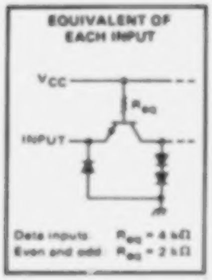
description

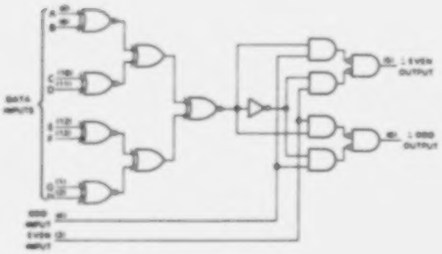
These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, utilize familiar Series 54/74 TTL circuitry and feature odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

The SN54180/SN74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74180 is characterized for operation from 0°C to 70°C.

functional block diagram


EQUIVALENT OF EACH INPUT
VCC
Req
INPUT
Data inputs Req = 4 kΩ
Even and odd Req = 2 kΩ


A
B
C
D
E
F
G
H
DATA INPUTS
Σ EVEN OUTPUT
Σ ODD OUTPUT
ODD INPUT
EVEN INPUT

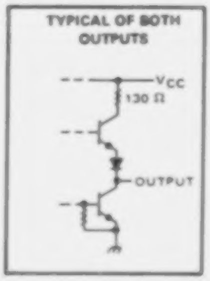

TYPICAL OF BOTH OUTPUTS
VCC
130 Ω
OUTPUT

Figure 1-52. SN74180 eight-bit odd/even parity generators/checkers.

Bibliography

ECI Courses

CDC 30455, Volume 2, *Television Equipment Repairman.* Extension Course Institute, Gunter Air Force Station, Alabama 36118.

CDC 30870, Volume 2, *Space Systems Command and Control Equipment Operator/Technician.* Extension Course Institution, Gunter Air Force Station, Alabama 36118.

CDC 34154, Volumes 4 and 5, *Digital Flight Simulator Specialist.* Extension Course Institute, Gunter Air Force Station, Alabama 36118.

Books

The TTL Data Book for Design Engineers (CC-411). Dallas, Texas: Texas Instruments Incorporated.

Supplement to the TTL Data Book for Design Engineers (CC-416). Dallas, Texas: Texas Instruments Incorporated.

NOTE: None of the items listed in the bibliography are available through ECI. If you cannot borrow them from local sources, such as your base library or local library, you may request one item at a time on a loan basis from the AU Library, Maxwell AFB AL 36112, ATTN: ECI Bibliographic Assistant. However, the AU Library generally lends only *books* and a limited number of *AFMs*. TOs, classified publications, and other types of publications are *not* available. Refer to current indexes for the latest revisions of and changes to the official publications listed in the bibliography.

Answers For Exercises

Reference:

001 - 1. (1) Symbols.
(2) Equivalent.
(3) Fewer.
(4) Decoding.
(5) Encoding.
(6) Low.
(7) F/F1 and F/F4.
(8) F/F1.
(9) None.
(10 F/F1, F/F2, and F/F3.
(11) F/F1 and F/F3.
(12) 0-7 storage.
(13) NAND.
(14) 3.
(15) Requirements.
(16) 4.
(17) 0-15 storage.
(18) Disable.
(19) OR.

002 - 1. $\bar{A}\ \bar{B}\ C\ D\ \bar{E}$.
002 - 2. At all times during count 10 when the output will be low.
002 - 3. 384.
002 - 4. The number of circuit elements can be substantially reduced.
002 - 5. When a circuit requires more current than diodes can handle.

003 - 1. To convert decimal numbers into an equivalent binary number that a computer can process.
003 - 2. OR-gates A, B, C high; OR-gate D low.

004 - 1. A comparator which forms the sum and carry of two or more numbers.
004 - 2. It is a circuit that has two inputs, representing addend and augend; and two outputs, representing sum and carry.
004 - 3. Two half-adders.
004 - 4. Serial-adder.
004 - 5. Addition resulting in a number too large for the sum register to hold.
004 - 6. a. 010.
b. 1, 1.
c. At T_1.

005 - 1. 0.
005 - 2. 22; 20; 21.
005 - 3. 21.
005 - 4. 55; AND-gate 14.
005 - 5. 1; AND-gate 10.
005 - 6. Carry ripple.

006 - 1. 0 from the inverter amplifier 13, 0 from AND-gate 11, and 0 from AND-gate 10.
006 - 2. The carry output.
006 - 3. 0.
006 - 4. All other stages.

007 - 1. A subtractor circuit that generates a borrow but does not take into account borrows from a previous order.
007 - 2. A subtractor circuit that receives and considers a borrow generated in the previous order.
007 - 3. Inhibitor.
007 - 4. It does not generate a borrow.

008 - 1. 0.
008 - 2. 1.
008 - 3. 1.
008 - 4. 11101.

009 - 1. By complementing the subtrahend (by changing the input lines) prior to adding.
009 - 2. All other stages. (A borrow generated on any stage is applied to al other stages; hence the name "parallel borrow.")
009 - 3. 2^3.
009 - 4. 18.

010 - 1. A binary digit; it may have any significant position and is expressed as a ONE or ZERO.
010 - 2. A group of one or more binary digits, such as a binary number, a character, a half-word, a word, a part of a message, a message, or a tape record.
010 - 3. A record that must contain an even number of ONE bits including the parity bit, or be in error.
010 - 4. The quality of uniformity in either the oddness or evenness of the ONE bits in a record.
010 - 5. The fact that if two unlike inputs produce a binary ONE output or two like or equal inputs will produce a binary ZERO output. It compares or detects unlike inputs.

011 - 1. Self-check.
011 - 2. Validity.
011 - 3. Strategic.
011 - 4. Parallel.
011 - 5. Serial.
011 - 6. Serial.
011 - 7. Going into storage.
011 - 8. Before.

012 - 1. The flip-flop forms a temporary storage register that holds the record while parity is being checked.
012 - 2. The corresponding flip-flop in the register must be set and a good parity signal must be generated.
012 - 3. If the alarm F/F is cleared and a parity check pulse is received.
012 - 4. The transfer gate will be inhibited and the record will not be transferred.

013 - 1. To detect the failure of clock pulses and to compare the coincidence of the system timing pulses with the pulses after they pass through the logic.
013 - 2. $T7_c = (F/F1) \cdot (F/F2) \cdot (F/F3)$.
013 - 3. B error $= [\,(T7_t \cdot T7_b) + (T7_t \cdot T7_b)]$.
013 - 4. Self-check error.

014 - 1. $\bar{A}_2$, B_2, C_2, D_2, $\bar{E}_2$.
014 - 2. Exclusive OR-gate 2 will enable, OR-gate 1 will enable, AND-gate 1 enables with a storage check pulse, and F/F1 sets.
014 - 3. One bit being improperly stored will cause a storage error.

015 - 1. This term refers to both digital-to-analog and analog-to-digital conversion and does not specify the direction in which the conversion takes place.
015 - 2. Each bit of information uses only one register.
015 - 3. 0-9 volts.
015 - 4. Only one value resistor is used and each bit detects the same resistance of 3R.

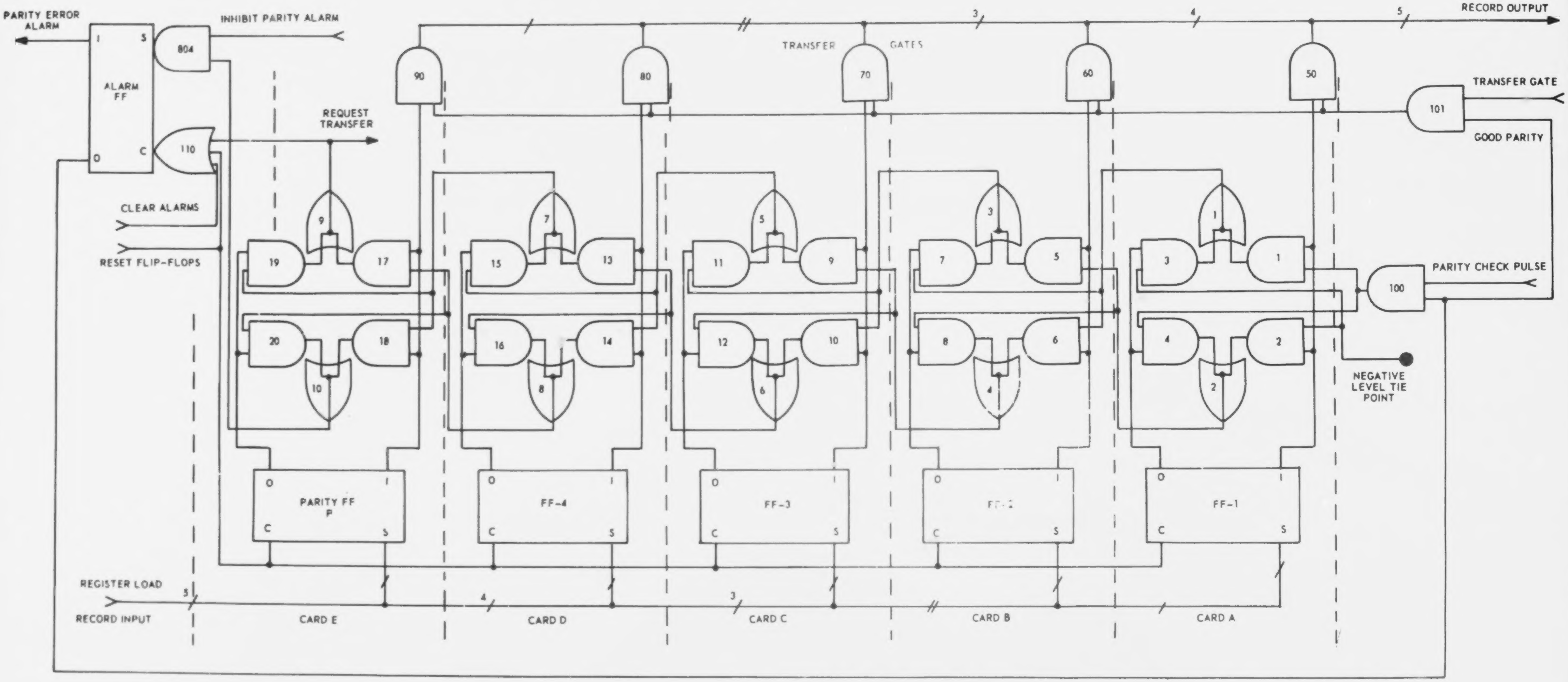
016 - 1. A device that receives an analog input and supplies a digital output.
016 - 2. By interpreting the shaded and light areas in the segment containing the brushes, reading from the innermost to the outermost circle. Read a "0" for each light area and a "1" for each dark area.
016 - 3. By increasing the number of channels nd brushes.
016 - 4. When the binary ladder output equals the input voltage.
016 - 5. Reset pulse and negative potential from the op amp.

016 - 6. When the output of the ladder equals the analog input.
016 - 7. The time of the clock pulse multiplied by the number of bits.
016 - 8. A glow-tube device that converts electrical signals into visual numbers.
016 - 9. LED.
016 -10. Liquid crystal.

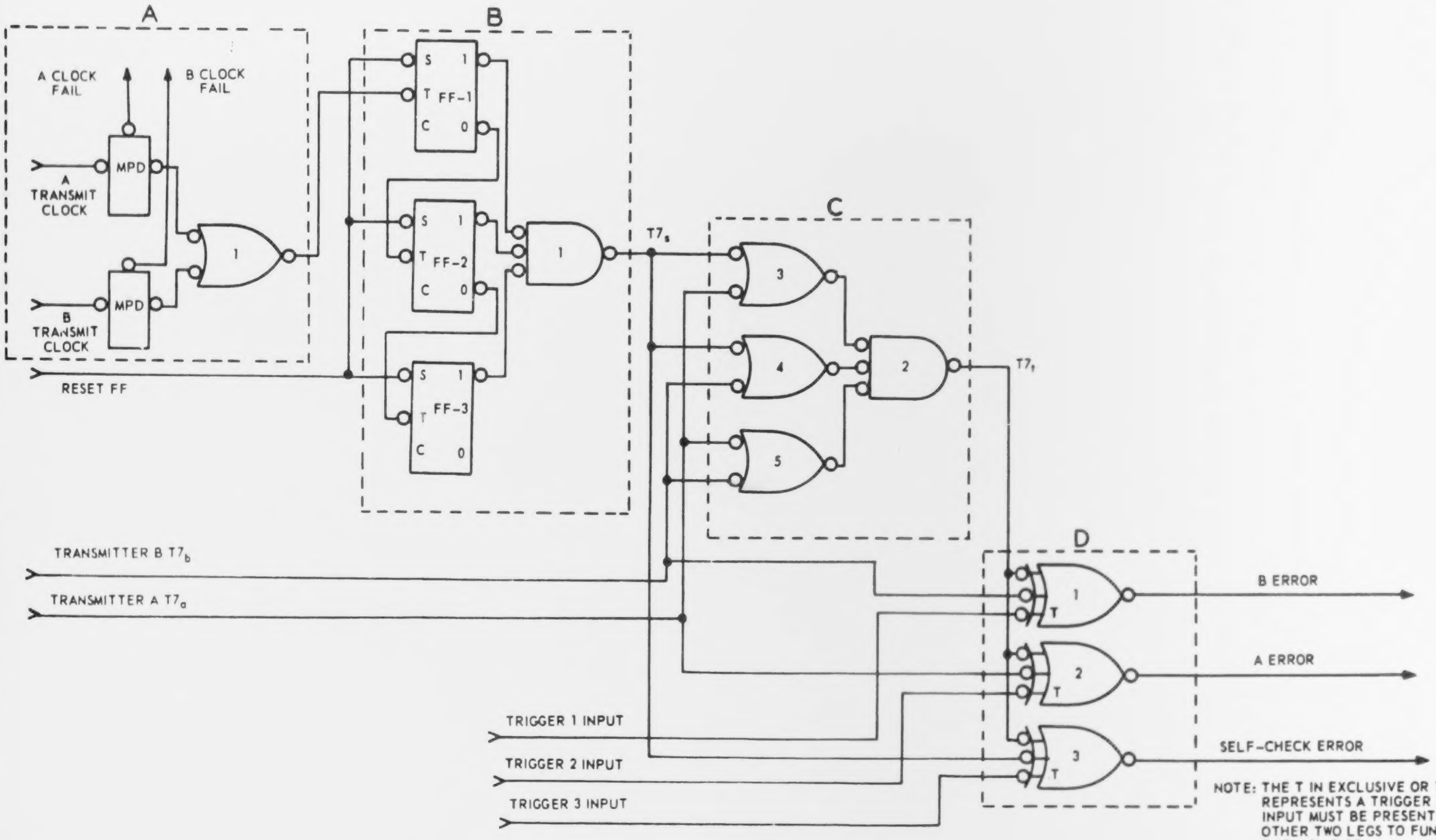
017 - 1. From fundamental trigonometry.
017 - 2. By rotating a vector through 360° from the X axis and plotting the sines of all angles generated by rotation.
017 - 3. It takes a linear digital input and converts it to a representative value of the sine X function of the input.
017 - 4. For temporary storage of the sine value, in binary form.
017 - 5. The sine X generator.
017 - 6. Quadrants.
017 - 7. Quadrants 1 and 2 are positive, and 3 and 4 are negative.
017 - 8. Into 16 equal segments, each of which has 64 equal increments.
017 - 9. Bits 0–4 are not used in conjunction with sine generator. Bit 5 determines the sign of the sine. Bits 5 and 6 determine the quadrant. Bits 7-10 determine the segment of the quadrant. Bits 11-16 determine the position within the segment.

018 - 1. SN5486/SN7486.
018 - 2. SN5443A, SN54L43, SN7443A, or SN74L43.
018 - 3. By cascading the required number of integrated circuits.

1982-546-034/614 AUGAFS,AL(824564)5300


PARITY ERROR ALARM
ALARM FF
1
S
0
C
804
INHIBIT PARITY ALARM
110
REQUEST TRANSFER
CLEAR ALARMS
RESET FLIP-FLOPS
RECORD OUTPUT
TRANSFER GATES
90
80
70
60
50
101
TRANSFER GATE
GOOD PARITY
PARITY CHECK PULSE
100
NEGATIVE LEVEL TIE POINT
19
17
20
18
9
10
15
13
16
14
7
8
11
9
12
10
5
6
7
5
8
6
3
4
3
1
4
2
1
2
PARITY FF P
FF-4
FF-3
FF-2
FF-1
O
I
C
S
REGISTER LOAD
RECORD INPUT
CARD E
CARD D
CARD C
CARD B
CARD A
3
4
5

Foldout 1. Serial parity check of a parallel record.


A
A CLOCK FAIL
B CLOCK FAIL
MPD
A TRANSMIT CLOCK
MPD
B TRANSMIT CLOCK
1
RESET FF
B
S
T
C
1
0
FF-1
FF-2
FF-3
1
T7$_s$
C
3
4
5
2
T7$_t$
TRANSMITTER B T7$_b$
TRANSMITTER A T7$_a$
TRIGGER 1 INPUT
TRIGGER 2 INPUT
TRIGGER 3 INPUT
D
1
2
3
T
B ERROR
A ERROR
SELF-CHECK ERROR

NOTE: THE T IN EXCLUSIVE OR 1, 2, AND 3 REPRESENTS A TRIGGER INPUT. THIS INPUT MUST BE PRESENT FOR THE OTHER TWO LEGS TO FUNCTION AS AN EXCLUSIVE OR.

Foldout 2. Pulse fail and true time comparator check circuit.

30554 02 S39 8112

10005 530 006 8112 DIGB

MODULE 10005

DIGITAL TECHNIQUES

Unit 6

Computers, Peripherals and Storage Media

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Preface

ALL FACETS OF the electronics industry are currently experiencing tremendous growth due to technological advancements. Technical innovations in the computer industry are a case in point. This unit to Module 10005, *Digital Techniques*, covers the major equipment and technologies used to implement digital systems.

Chapter 1 covers the basic computer, minicomputers, microcomputers, and the microprocessor. Chapter 2 covers the input and/or output devices which comprise a computer system's peripheral equipment. Chapter 3 discusses the various types of media used to store instructions and data for a data processing system.

Code numbers appearing on figures are for preparing agency identification only and should be of no concern to the student.

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Material in this unit is technically accurate, adequate, and current as of April 1981.

Acknowledgment

THE FIGURES and text listed below have been reproduced by permission of John Wiley & Sons, Inc., publisher of the book, *Computer Storage System and Technology,* by Richard Matick.

Figure 2.2-1, General Organization of Storage Systems, page 72.

Figure 7.2-1, Schematic of Direct Access Systems, page 477.

Text from page 73 on Storage System Requirements.

Figures 1-4 and 1-5 in this unit and portions of the text on microprocessors have been reproduced by permission of the MOS Technology, Inc., from their manuals:

6500-15B	KIM-1 Microcomputer	Module User Manual
6500-10A	Microcomputer Family	Hardware Manual
6500-50A	Microcomputer Family	Programming Manual

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Chapter

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NOTE: In this unit, the subject matter is developed by a series of student-centered objectives. Each of these carries a three-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see whether your answers match those in the back of this unit. If your response to an exercise is incorrect, review the objective and its text.

Computers

IN LESS THAN 40 years, the electronic computer has evolved from the behemoth ENIAC and its 18,000 vacuum tubes to the handheld calculator with its internal microcomputer. The time required for a computer calculation has decreased from the 0.2 millisecond (ms) in ENIAC to a few microseconds or less for the microcomputer of today. Integrated circuit (IC) electronics is the primary reason for these reductions in size and the increase in speed of today's digital computer.

1-1. Computer Architectures and Terms

A computer may be room size for a large system capable of many data processing functions, or it could be a desk-top minicomputer with fewer capabilities to satisfy a smaller systems requirement. The microprocessor has enabled us to insert a computer into any system or device which requires a digital data handling capability. It can be done cheaply and with a minimum of hardware. In this chapter we'll discuss the basic computer, minicomputers, microcomputers, and microprocessors.

001. Identify the basic components of a computer with their function.

Basic Computer Architecture. Many different types of digital computers have been built, ranging in cost from a few hundred to several million dollars. All digital computers have certain common characteristics, no matter how much they vary in size, speed, or function. In fact, some of their most basic properties are found in every device which aids in calculation. These properties exist with paper and pencil, a mechanical calculator, an abacus, or an electronic computer.

The diagram in figure 1-1 is so general in nature that it can be used to represent the characteristics of data processing machines ranging from the desk calculator to the most intricate and high-speed electronic data processing equipment. In the case of the desk calculator, the input is a numeric keyboard which is manually operated to enter data. In order to perform mathematical operations, the data to be processed is first stored within the calculator. Control over the

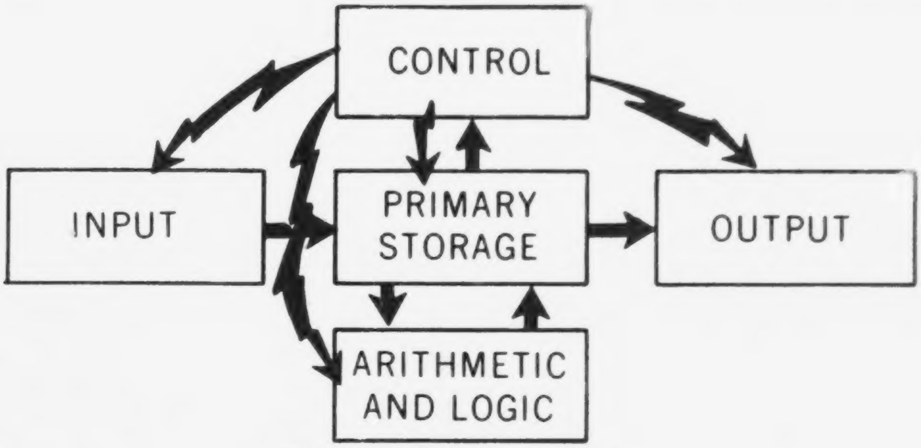

Figure 1-1. Logical sections of a computer.

processing of data is obtained by the manually activated keys. A digital computer, however, is automatically controlled by a prescribed sequence of instructions written by a programmer and stored internally. The output unit will display the results of the computations which have been performed by the calculator or computer.

The basic parts of a digital computer as outlined in figure 1-1 are further defined in figure 1-2. The I/O or input/output interface circuits of the computer will access the devices needed to perform a particular function. There are many types of peripheral equipment used to input data to a computer system. A few of these are listed under *input media*. Likewise, a number of different *output media* are used to get the results of a computer operation. These peripheral devices will be further defined in Chapter 2.

The major portion of a digital computer is the central processing unit, or CPU. The CPU consists of the control section, the arithmetic logic unit (ALU), and the primary storage for the CPU, or *memory*. The *control section* will consist of logic used to implement the instructions supplied by the computer program. Memory will consist of magnetic core, thin film or semiconductor, data storage elements. The ALU will perform all the calculations necessary on the data being processed.

Input/output (I/O). The I/O unit of a digital computer is an interface between the computer and all peripheral devices. The I/O contains logic which will convert peripheral data rates and formats to those compatible for internal processing by the computer. Some data conversions are also done by the peripherals themselves.

Whenever an input or output device wishes to communicate with the computer, an *interrupt* is generated. The interrupt tells the computer that an input or output of data is required. Interrupts generally have a set priority in which they will be handled by a data processor. The computer will, depending on the priority of the interrupt, halt processing of internal data to accept or output data. This will occur through the I/O unit of the computer. Once a data input or output has been handled, the computer will return to its normal, internal, data processing functions.

Control. The control section of a computer has the function of interpreting or decoding the instructions stored in memory and then sending signals to the rest of the parts telling them what to do. It is the nerve center of the machine. In figure 1-1 we see a solid line between memory and control, indicating that instructions are sent to and from memory and control. The other lines from control to the various units are signals sent to control their operations based on the instruction which the control unit interprets.

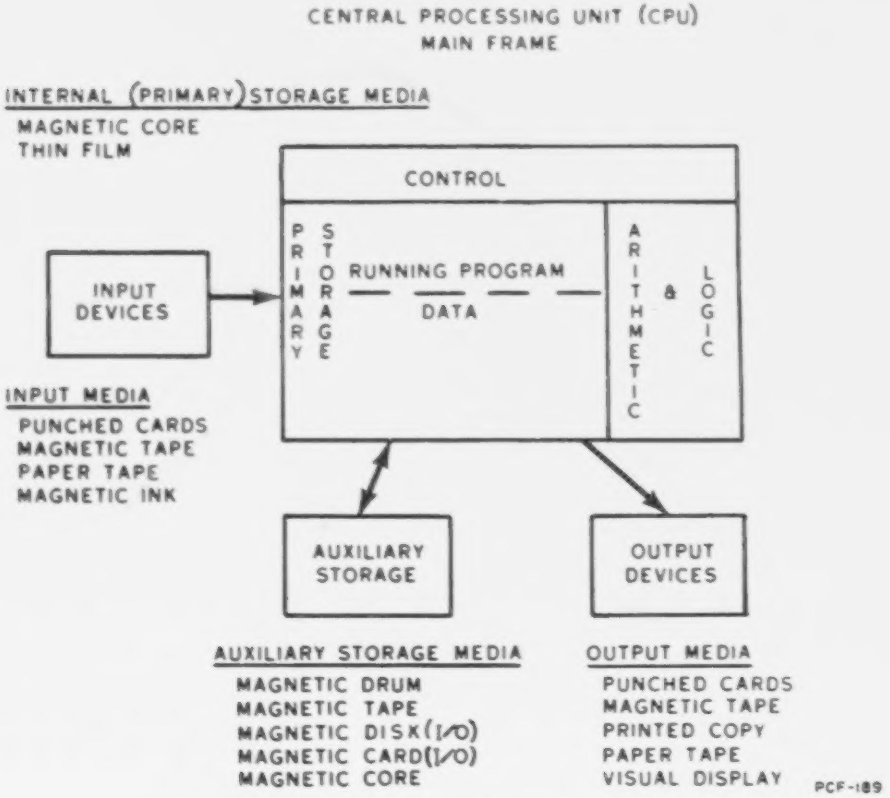
CENTRAL PROCESSING UNIT (CPU)
MAIN FRAME
INTERNAL (PRIMARY) STORAGE MEDIA
MAGNETIC CORE
THIN FILM
CONTROL
PRIMARY STORAGE
RUNNING PROGRAM
DATA
ARITHMETIC & LOGIC
INPUT DEVICES
INPUT MEDIA
PUNCHED CARDS
MAGNETIC TAPE
PAPER TAPE
MAGNETIC INK
AUXILIARY STORAGE
OUTPUT DEVICES
AUXILIARY STORAGE MEDIA
MAGNETIC DRUM
MAGNETIC TAPE
MAGNETIC DISK (I/O)
MAGNETIC CARD (I/O)
MAGNETIC CORE
OUTPUT MEDIA
PUNCHED CARDS
MAGNETIC TAPE
PRINTED COPY
PAPER TAPE
VISUAL DISPLAY
PCF-189

Figure 1-2. Functional components of a digital computer.

The control unit consists of either random logic which will implement the program instructions or a *microprogram* which will do the same thing. The microprogram will usually be a bipolar read-only memory (ROM), which contains a set of *microinstructions*. Using a microprogram will reduce the amount of hardware needed to control the data processing functions of the computer. A second advantage of the microprogram is that it is easy to add or change program functions by changing the ROM.

The control unit of a computer that is microprogrammed accepts a main program instruction and then uses a set of microinstructions in the microprogram to accomplish the function requested. A unique feature of the microprogram is that there is no program counter. The address of microinstructions in the ROM will be determined by bit assignments in the main program instruction. There is, however, a program counter for the main computer program. The major benefits derived from using the microprogram for the control function are to reduce the size, cost, and complexity of the control unit and to speed computer operations.

Arithmetic logic unit (ALU). The ALU consists of registers (fig. 1-3) where all arithmetic and most logical operations are performed. This unit usually has the capabilities of performing the arithmetic operations of addition, subtraction, multiplication, and division. Most of these operations can be broken down into the simple arithmetic process of addition. Recall that subtraction can be carried out by adding the complement of the subtrahend to the minuend, multiplication by repeated addition and shifts, the division by repeated subtraction and shifts.

The logical operations make it possible for the computer to make decisions as the result of comparisons of one item to another. The stored program will specify the alternate actions to be taken as a result of the comparison. For example, in a simplified inventory control operation when an item of stock is withdrawn, the balance on hand (called A) is decreased. This balance on hand (A) is compared against a predetermined reorder point (B); and if A is less than B, the item is reordered. Thus, many small logical decisions are used to accomplish the job.

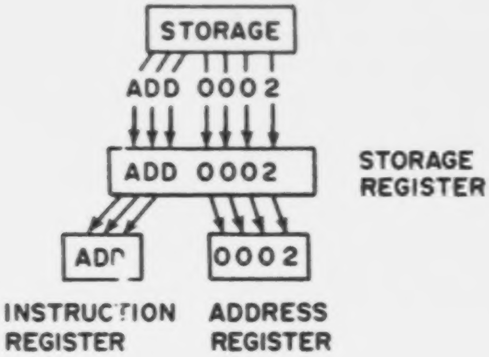

Figure 1-3. Register.

The arithmetic unit must also be capable of recognizing both positive and negative numbers and modifying its operation accordingly. Another important requirement of this unit is to generate signals needed to perform specific operations (within the ALU) when arithmetic instructions are decoded.

A knowledge and understanding of counters, registers, gates, and full- and half-adders are a necessity in order to understand the function of the ALU. These have all been discussed in detail in previous units. The ALU may be implemented by using standard logic or through the use of large-scale integrated circuits which are specifically dedicated to the ALU function.

Memory. Storage consists of internal memory (primary storage), which is an integral part of the processing unit of the computer, and auxiliary storage, which is provided by peripheral equipment. Most data processing systems demand both types of storage in order to contain as much data as the largest application would require and the necessary instructions for the use of this data.

A number of different internal storage media have been used over the years since the development of the electronic computer. The first computers used mechanical relays, storage tubes, and vacuum-tube flip-flops for memory elements. Magnetic core memory was developed during the 50's and has become the predominant main memory storage element. Today, more and more computers are using semiconductor memory because of its low cost, small size, and large capacity. Core memory and semiconductor memory are both used to provide main memory in many newer computers.

A second group of storage media is provided by peripheral devices such as magnetic tapes, drums, disks, paper tape, and punchcards. These media are all a form of external or auxiliary storage.

Auxiliary storage is not an integral part of the central processing unit, but is connected to the CPU via the I/O. Auxiliary storage differs from primary storage in several aspects. First, auxiliary storage supplements memory and can contain both data and instructions; but its contents must be read into primary storage to be used. This means that instructions stored in auxiliary storage must be read into memory and then executed by the CPU. Second, the time necessary for a machine to recall information from a single location is longer for auxiliary storage than for primary storage. This is a measure of what is known as *access time*. Each storage medium has a particular amount of time that it takes to transfer data. The access time will be determined by device speed and whether or not it uses random or sequential access. Finally, auxiliary storage usually has a larger capacity than primary storage and costs less. This means that large quantities of data are stored in auxiliary storage, read into primary storage in small segments, and processed there as they are needed.

Exercise (001):

1. Match the following statements (column A) with the terms that they most closely identify (column B).

Column A	*Column B*
____(1) It is an internal storage media.	a. I/O.
____(2) A microprogram can implement this function.	b. ALU.
	c. Control.
____(3) Data transfers occur here when an interrupt is generated.	d. Magnetic core.
____(4) Will perform a comparison for the CPU.	
____(5) Contains both data and instructions.	
____(6) It is the nerve center.	
____(7) Performs certain logical functions.	

002. Define the terms "minicomputer," "microcomputer," and "microprocessor."

The difference between a minicomputer and microcomputer is sometimes disputed, but it is generally accepted that the major difference is a microprocessor! In other words, the microcomputer uses a microprocessor, whereas the minicomputer does not.

Minicomputers. A minicomputer is generally of the desk-top variety and uses standard logic to implement all functions. The "mini" usually has limited storage but can have access to a wide assortment of peripheral devices. Word size is usually limited to 16 bits versus 32 to 64 bits per computer word for large systems.

Minicomputers were a logical progression from the large, room-size computer, due to the increasing availability of medium- and large-scale integrated circuits. Integrated circuit technology has permitted a tremendous decrease in the size of digital computers, and the "mini" is one result. Minicomputers allow a system to be built at a much lower cost to meet the needs of many small system users. Not everybody needs a room full of computer equipment to satisfy their system requirements! The minicomputer with its small size, low cost, and limited capability has fulfilled an important role for civilian and military users.

Microcomputers. The "micro" is a computer system built with a microprocessor as its primary logic element. It is a logical progression from the "mini," brought about by the ingenuity of IC designers and technological innovation.

The development of large scale integration (LSI) and very large scale integration (VLSI) has made it possible to evolve quite elaborate computers on just one or two semiconductor chips. Small pocket calculators in use today contain the equivalent of thousands of transistors. A microprocessor is considered to have the equivalent of 8,000 to 10,000 transistors. The distinguishing feature between the calculator chip and the microprocessor is that the microprocessor is *programmable*. Microprocessors are made using MOS (metal-oxide-semiconductor) technology primarily.

The term "microcomputer" is defined as a computer system based on a microprocessor and contains all the memory and interface hardware necessary to perform calculations, data conversions, and data transfers. Microcomputer is sometimes called minicomputer, LSI computer/processor, or picocomputer; but microcomputer is the most generally accepted term. The microprocessor is the heart of any microcomputer. It is defined as the central processing unit (CPU) fabricated as one integrated circuit (single chip) that performs the task of executing program instructions.

The past several years have seen the development of an exciting new concept in electrical design. Conventional system design is rapidly being revolutionized by the LSI and VLSI programmable microprocessor. The microprocessor started out as a relatively simple, difficult-to-use programmable device capable of handling simple control or computational problems. However, it has since matured into a powerful, inexpensive, easy-to-use device capable of controlling all but the most complex of systems.

Exercises (002):

1. What is the term used to describe a programmable CPU which has all logic located on an LSI chip?

2. What is a minicomputer?

3. Define the term "microcomputer."

1-2. A Microcomputer System

Figure 1-4 illustrates the basic organization of a microcomputer system. If you compare this block diagram with that of the basic computer in figure 1-1, you'll see what units of the microcomputer are equal in function to the basic units.

003. Define terms and specify the characteristics of a microcomputer system and its components.

A Basic System. The microcomputer contains two memory units. One is the program memory, or ROM (read-only memory), where the microprogram for the microprocessor can be stored. Second is the data memory, or RAM (random access memory), where data and instructions are stored for use by the microprocessor during its operations. The ROM is nonvolatile, and therefore the microprogram is permanently stored. The RAM is volatile and loses its data whenever power is removed unless, as is true with some

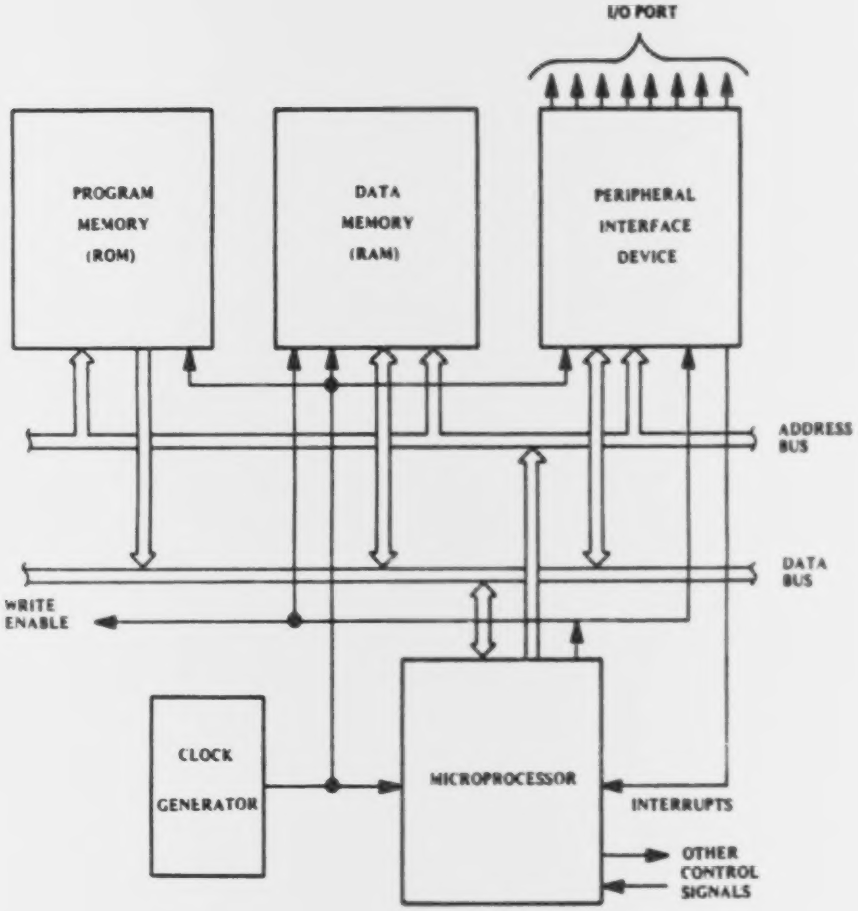

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Figure 1-4. Organization of a microcomputer system (courtesy of MOS Technology, Inc.).

microcomputers, a battery pack is installed to retain data in the RAM.

Next we have the I/O or peripheral interface device. This is usually another microprocessor chip called the peripheral interface adaptor, or PIA. It will provide an interface between the microprocessor and peripheral devices such as a video or plasma display terminal, cassette or magnetic tape, and/or a disk.

Finally in figure 1-4, we have the microprocessor which is our CPU. It will contain our control unit and the ALU. Depending on the microprocessor used, word lengths of 8 to 16 bits are most common. Microprocessors can have a different word length internally. Some microprocessors on the market today use a 16-bit word internally and an 8-bit word externally. The newest microprocessors being developed and produced have 32-bit internal word lengths and a 16- or 32-bit external word length.

The microcomputer is a system which can be characterized as very simple in its detail and very complex in its overall operation. It carries out rather complex tasks by performing a large number of simple operations. Control of the system is primarily the responsibility of the processor. By putting out addresses to program memory, it controls the sequence of operations performed; by interpreting and executing the instructions which it receives from the program memory, it controls the actual operations carried out by the system.

The processor causes the system to perform the desired operations by reading the first instruction in the program and performing the very simple task dictated by the specific pattern of bits in this instruction (referred to as "executing" that instruction). It then goes on to the next instruction in the program and executes it. This simple operation of fetching an instruction and executing it is performed over and over, each time on the next instruction in sequence. In this way, the program instructs the processor to bring about the desired system operation.

Before entering into a detailed discussion of microcomputer operation, it would be useful to define a few terms and to introduce a few concepts concerning addressing. This should assist you in understanding the detailed discussions which follow.

Bit. The term "bit" is a general term referring to anything that can be assigned a binary value of 0 or 1. Thus, an 8-bit data bus is a set of eight lines which can be assigned a value of logic 0 or logic 1. On these lines, the logic values are represented by two different voltages or currents. Similarly, a 16-bit binary display can be built with 16 individual lamps. The logic 1 is represented by the lamp being on.

Address space. The concept of an address space is very useful in understanding microcomputer systems. The term "address space" refers to the total set of addresses which the microprocessor can generate. For example, if a processor had only four address lines, it could generate the addresses 0–15 (binary 0000 to binary 1111). This would not be adequate for any microcomputer operation; consequently, the typical processor has between 12 and 16 address lines. Since each line can assume a value of 0 or 1, these devices can usually address from 4,096 to 65,536 separate addresses.

Address page. The concept of a *page* in memory is very important in 8-bit microcomputer systems. The internal organization of an 8-bit processor is around 8-bit registers, 8-bit parallel data paths, etc. Most arithmetic operations, logic operations, etc., take place on 8 bits of data at a time. Likewise, the 16-bit counter which determines which instruction is being executed is actually divided into two 8-bit busses. One contains bits 0–7 (low-order address bits), and the other contains bits 8 to 15 (high-order address bits). With this in mind, one can think of the address space as consisting of 256 blocks (high-order address bits); each block consists of 256 specific address locations. Each block is referred to as a "page" of memory. The high-order 8 bits of the address (ADH), therefore, indicate on which page the address is located; and the low-order 8 bits (ADL) indicate a specific address on that page. The first page in memory (ADH = 00) is referred to as page 0. The next higher order page (ADH = 01) is referred to as page 1, etc.

Microcomputer Components. The block diagram in figure 1-4 shows the basic components which comprise all microcomputer systems. Each of these blocks may consist of one or more integrated circuits; and, in fact, the functions may be combined into single chips. However, the basic operation of each remains the same.

Clock generator. The clock generator produces a continuous waveform which is normally used to control all signal transitions within the system. It acts as the "heart" of the system. In the typical microcomputer system, the address bus will change during one-half of the clock cycle, and the data will be transferred during the second half. In addition to interpreting the address, data, and control lines, the processor and support chips must also examine the system clock to know when to put out data or when to latch in data generated by another device.

Program memory. The program memory stores the sequence of instructions which comprises the system program. Like any memory, this input puts a pattern of 1's and 0's on the data bus in response to the address on the address-bus input. Each unique address selects a set of 8 binary bits and places this data on the data bus. Note that it does not matter where the address is generated or where the data is used; the memory simply obeys the rule that, given an address, it will put the corresponding 8 bits of data on the data bus.

A unique characteristic of most microprocessor-based systems is that the program is usually stored in "READ-ONLY" memories. The data is stored in a fixed pattern of bits in the memory. Since the data is stored permanently in the device, the data will not be lost when power is disconnected from the chip. In addition, it is only necessary to insert the device into its socket to provide the system program. The term "read-only memory" refers to the fact that, in system operation, it is impossible for the processor to cause data to be stored in the device. The processor can only "read" the data that was stored in the device during the manufacturing process. "Reading" a memory involves the simple process of supplying an address to the device to obtain the corresponding 8 bits of data on the data bus.

Data memory. For temporary storage of input data, the results of arithmetic operations, etc., the microcomputer uses a read/write memory, commonly referred to as the RAM (random access memory). The processor can store data in the RAM (called "writing" the RAM), or it can read back the data it has stored. As in the ROM, each address corresponds to eight memory cells. However, in the RAM the data must be placed into the memory by the processor. Turning off the power to the chip will cause the loss of all data stored there. The data is said to be "volatile." Data in the ROM is not lost when power is disconnected from the device; the data is therefore referred to as "nonvolatile."

"Writing" data into the RAM takes place when the write-enable signal goes to the write state. At this time, the data on the data bus will be stored into the eight memory cells corresponding to the address on the address bus. The processor can *read* this same data by supplying the proper address and keeping the write-enable line in the "read" state.

Input/output. The input/output unit contains the circuits which interface the printer, keyboard, displays, etc., to the processor. These allow the processor to read data from the keyboard, to test the state of sensors and switches, and to display or to print the results of internal operations.

No matter where data is generated, it must be in the form of 1's and 0's before the processor can work with it. Likewise, actions to be initiated by the processor must be triggered by 1's and 0's transferred by the processor to a set of output lines.

The transfer of data from the processor to an output device is usually accomplished by "writing" the data out in much the same manner as the processor writes data into the RAM. Each set of eight input or output lines (referred to as "PORT") is given an address, and the processor simply writes data to that address. For each "1" written out to the peripheral port an output is set high, and for each "0" the corresponding output is set low.

Although the basic concept of peripheral control is simple, the actual implementation of these interfaces can involve many sophisticated techniques designed to allow the processor to maximize its ability to control peripherals and perform internal operations concurrently.

Microprocessor. At first glance it may seem strange to discuss the support chips in the microprocessor-based system before mentioning the processor. However, this approach is necessitated by the fact that most of the inputs and outputs on the processor are aimed at properly controlling the support chips and peripheral devices discussed above.

The address bus, the bidirectional data bus, and the write-enable line allow the processor to exercise direct control over the rest of the system. The address bus puts out addresses to control the source or destination of data transfers. These addresses are derived from various sources within the processor. Addresses for data transfers between the processor and RAM are usually derived directly from the program or are calculated from the data in the program and data in internal registers. The bidirectional data bus serves as a path for transferring data into and out of the processors. The direction of the data transfer is determined by the write-enable line.

Another special function found in microcomputer systems as well as other computer systems is the *interrupt*. As mentioned previously, when an interrupt signal is generated by a peripheral device, the operation of the processor will be directly affected. When the interrupt is received by the CPU, the CPU will complete its current instruction and then, under program control, will respond to the interrupt. The importance of this function is that it allows the processor to execute the system program without requiring the system program to monitor the status of each peripheral device. The software which handles the operation of each peripheral will be executed only when required.

With reference to *software*, two definitions are needed at this point. *Software* is the computer program(s) written by the programmer which causes a computer system to perform a specified operation. The program that is permanently stored in the ROM is called *firmware* and contains the microinstructions which implement software instructions in a microcomputer system. Any program stored in the ROM is generally called firmware. Software is easily changed; firmware is not.

Exercises (003):

1. What memory unit within a microprocessor system is used for storing any microinstructions?

2. What device is used to communicate between the microcomputer and a disk?

3. How many address lines are required if there are 4,096 addresses?

4. How are addresses for data transfers between the processor and the RAM derived?

5. What is firmware?

6. Is data in the ROM lost when power is disconnected?

7. What is meant when we say that the RAM is volatile?

8. What is meant by address space of a microprocessor?

004. Specify operating characteristics of microprocessors.

The microprocessor is an LSI chip containing most of the circuitry required to build a programmable, stored program, digital computer. The chip is usually mounted in a 40- or 64-pin dual in-line package (DIP). By interconnecting the microprocessor (μP) with memory, interface circuits, and/or other microprocessor chips, a microcomputer is the result.

One of the more widely used microprocessors is the MCS6502 designed by MOS Technology, Inc. We shall use the 6502 as an example of the type of microprocessors (μPs) being used in the civilian and military market. We'll discuss the characteristics of the 6502 and look at an internal block diagram for this chip. Next, we'll discuss the various parts of the 6502 and their functions. Later in this chapter we'll compare three other μPs with the 6502.

The MCS6502. Figure 1-5 illustrates the internal block diagram for the 6502 chip. As you can see, many functions are performed by the integrated circuitry

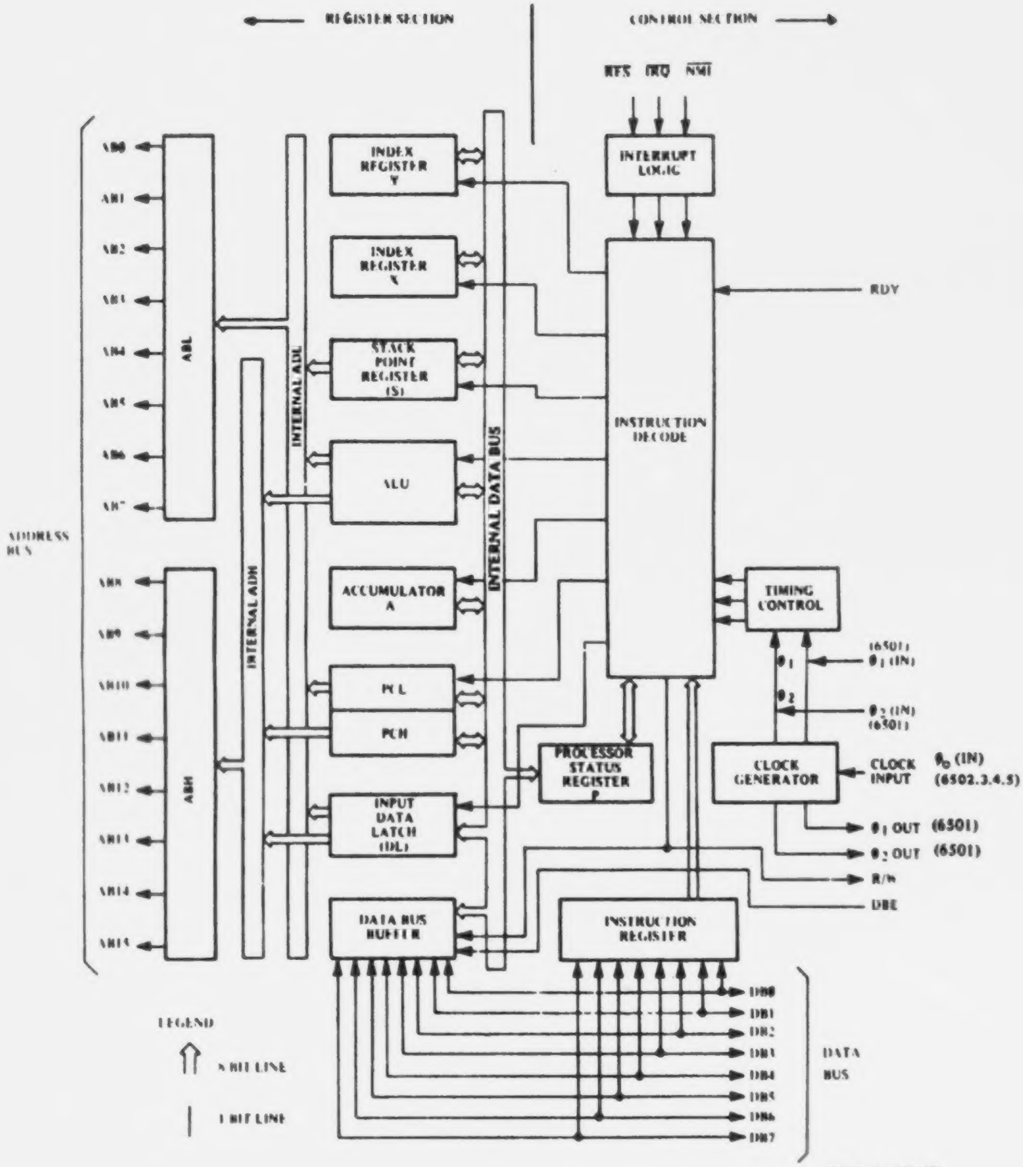
REGISTER SECTION
CONTROL SECTION
RES
IRQ
NMI
INTERRUPT LOGIC
INDEX REGISTER Y
INDEX REGISTER X
STACK POINT REGISTER (S)
ALU
ACCUMULATOR A
PCL
PCH
INPUT DATA LATCH (DL)
DATA BUS BUFFER
INSTRUCTION DECODE
INSTRUCTION REGISTER
PROCESSOR STATUS REGISTER P
TIMING CONTROL
CLOCK GENERATOR
RDY
ABL
ABH
INTERNAL ADL
INTERNAL ADH
INTERNAL DATA BUS
ADDRESS BUS
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
AB12
AB13
AB14
AB15
(6501) Φ1 (IN)
Φ2 (IN) (6501)
CLOCK INPUT
Φ0 (IN) (6502.3.4.5)
Φ1 OUT (6501)
Φ2 OUT (6501)
R/W
DBE
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DATA BUS
LEGEND
8 BIT LINE
1 BIT LINE

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Figure 1-5. MCS6502 internal block diagram (courtesy of MOS Technology, Inc.).

within this 40-pin DIP. The 6502 is easy to interface, operates off a single +5-volt power supply, and doesn't require an external clock generator. The IC uses an 8-bit data word both internally and externally. The high logic level for the chip must be at least 2.4 volts and the low logic level is 0.40 volt or less. These logic levels are compatible with TTL and, therefore, no conversion circuits are required when interfacing with TTL devices. The 6502 is an n-MOS device, which means that n-channel MOSFETs are the active elements on the chip. The nominal clock frequency is 1 MHz. Cycle time is 1 μs at a clock frequency of 1 MHz. Up to 65K bytes of external memory may be addressed with the 16 address lines. A 64K-byte RAM data memory and a 1K-byte ROM program memory are used for storage of data and instructions.

The internal organization of the 6502 can be split into two sections. In general, the instructions obtained from program memory (see fig. 1-4) are executed by implementing a series of data transfers in one section of the chip—the *register section*. The control signals which actually cause the data transfers to take place are generated in the other section—*control.* Instructions enter the processor on the data bus, are latched into the instruction register, and are then decoded along with timing signals to generate the register control signals.

The *timing control unit* keeps track of the specific cycle being executed. This unit is set to "T0" for each instruction fetch cycle and is advanced at the beginning of each *phase one* clock pulse. Each instruction starts in T0 and goes to T1, T2, T3, etc., for as many cycles as are required to complete the execution of the instruction. Each data transfer, etc., which takes place in the register section is initiated by decoding the contents of both the instruction register and the timing counter.

Additional control signals which affect the execution of the instructions are derived from the interrupt logic and from the processor status register. The *interrupt logic* controls the interface between the 6502 and peripheral devices to insure that the processor recognizes and services the device.

The *processor status* register contains a set of latches which control certain aspects of μP operation. The register will indicate the results of arithmetic and logic operations, the status of data generated by the 6502, or the status of data brought in from the outside.

At 1 MHz, the data which comes into the processor from the program memory, the data memory, or from the peripheral devices appears on the data bus during the last 100 nanoseconds of *phase two* clock. No attempt is made to actually operate on the data during this short period. Instead, it is simply transferred into the *input data latch* for use during the next cycle. The data latch serves to trap the data on the data bus during each phase two pulse. It can then be transferred onto one of the internal busses and from there into one of the internal registers. For example, data being transferred from memory into the accumulator (A) will be placed on the internal data bus and will then be transferred from the internal data bus into the accumulator. If an arithmetic or logic operation is to be performed using the data from memory and the contents of the accumulator, data in the input data latch will be transferred into the ALU. At the same time the contents of the accumulator will be transferred onto a bus in the register section and from there into the second input to the ALU. The results of the arithmetic or logic operation will be transferred back to the accumulator on the next cycle by transferring first onto the bus and then into the accumulator. All of these data transfers take place during the phase one clock pulse.

The program counter (PCL, PCH) provides the addresses which step the processor through sequential instructions in the program. Each time the processor fetches an instruction from program memory, the contents of PCL are placed on the low-order 8-bits of the address bus, and the contents of PCH are placed on the high-order 8-bits. This counter is incremented each time an instruction or data is fetched from program memory.

The *accumulator* is a general-purpose 8-bit register which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

All logic and arithmetic operations take place in the ALU. This includes incrementing and decrementing of internal registers (except PCL and PCH). However, the ALU cannot store data for more than one cycle. If data is placed on the inputs to the ALU at the beginning of one cycle, the result is always gated into one of the storage registers or to external memory during the next cycle. Each bit of the ALU has two inputs. These inputs can be tied to various internal busses or to a logic 0; the ALU then generates the SUM, AND, OR, etc., function using the data on the two inputs.

The *stack pointer* (S) and the two index registers (X and Y) each consist of eight simple latches. These registers store data which is to be used in calculating addresses in data memory. The stack concept will be explained in detail later.

The *address bus buffers* (ABL, ABH) consist of a set of latches and TTL compatible drivers. These latches store the addresses which are used in accessing the peripheral devices (ROM, RAM and I/O).

The Stack Concept. The "stack" is a specific set of memory locations in the RAM. The stack is used to speed computations and hold data and/or instructions being operated upon by the processor. The stack represents a form of temporary storage used by a computer to make program operations more efficient. The *stack pointer register* is used to indicate or "point" to the location in stack where the next word will be stored to or retrieved from in the stack area of the RAM.

A good use of the stack occurs when we have an interrupt from a peripheral device. For example, suppose a disk wanted to communicate with our microcomputer. Once the processor recognizes the interrupt, the contents of all data registers and the instruction register would be stored in the stack while the processor services the disk. After the disk finishes its communication, the processor would then take the contents of the stack locations it used and place the information back into the registers it came from. The processor would then continue with its program operations.

Anytime the processor stores information to the stack, data is said to be "pushed" on the stack. Data taken from the stack is said to be "popped" off the stack. These terms are *only* used with reference to a stack. The words stored in the stack or retrieved from the stack are done on a "last in, first out" (LIFO) basis. In other words, the last word stored in stack is the first to be taken from the stack.

Tristate Logic. The address bus in the 6502 is a one-way bus. Addresses leaving the microprocessor go in one direction only—toward memory. On the other hand, the data bus is bidirectional. Data and instructions can travel in either direction on the data bus. This could create mass confusion unless we control when data travels on the bus and in which direction. This is done with *tristate* or *three-state* logic.

A standard logic gate has an output of a 1 or 0. A tristate logic gate is capable of an additional output called its high impedance or disconnect state. The tristate gate also has an additional input, called the enable input. Whenever he gate is enabled, an output of 1 or 0 is present. If not enabled, the output is in its high impedance state or essentially open. Therefore, a series of gates can be tied to the data bus at one time. By enabling one set of gates at a time, we prevent data from more than one source from getting onto the data bus at the same time.

Microprocessor Comparison. There are a multitude of microprocessors available which can be used as general-purpose digital microcomputers or special-purpose data processors. Each μP may require one or more *support* chips to implement a microcomputer system. Microprocessors are also available as "slice" CPUs. These usually operate on only 2 or 4 bits of data at a time. By connecting several of these in parallel, 8- or 16-bit words can be processed.

The following table lists three popular μPs in use today besides the MCS6502. As indicated, some require more power sources than others. Second, not all μPs come with a clock on the chip. These factors will have a bearing on the complexity of a system. Some microprocessors are microprogrammed, and most have a *direct memory access* (DMA) capability. DMA is a function which allows data transfers to occur between memory and peripheral devices without interference from the CPU. DMA is done to speed data transfers when data doesn't require manipulation by the processor.

Maker	*μP*	*Word Size*	*Voltage*	*Clock Freq*	*Memory*	*# Pins*	*DMA*
Intel	8080	8 bits	±5, +12	3 MHz	65K	40	Yes
Motorola	6800	8 bits	+5	2 MHz	65K	40	Option
T.I.	9900	16 bits	±5, +12	3 MHz	65K	64	Yes

Exercises (004):

1. What active chip element is used in the 6502 microprocessor?

2. Name the two major sections that comprise the 6502.

3. What signals cause data transfers to take place?

4. What register in the 6502 will indicate the status of logical operations?

5. How is data stored in the "stack"?

6. In comparing tristate logic with standard logic, what is the third state?

Peripherals

IT IS GENERALLY accepted that peripheral equipment for a computer system consists of all the input and/or output equipment used for the transfer of information in or out of the system. Even in a microcomputer, RAM and ROM are considered peripherals if they are separate chips from the microprocessor. The peripheral devices listed below are the predominant I/O devices that will be discussed in this chapter.

- Card punches/readers.
- Paper tape punches/readers.
- Magnetic drums/tapes/disks.
- Keyboards.
- Printers.
- Visual displays.
- Plotters.

Magnetic drums, tapes, and disks are also major storage media and will be discussed again in Chapter 3 of this unit. The remainder of the devices listed above will be detailed in the following sections.

Peripheral devices provide the computer with the facilities necessary for communicating with the users. Input devices such as data terminals, card readers, and magnetic disks supply the computer with data and instructions, while some of these same devices will change the data processed by the computer into a form required for other purposes. The selection of a particular peripheral device will depend on the specific use for which a computer is intended.

2-1. Types of Input/Output Devices

Different types of computers are used for different purposes. The three major areas of application are business, solving scientific problems, and the automatic control of weapons systems. The types of input/output devices used with each application will differ in many respects. In fact, some peripheral devices are designed specifically for one of these applications and, therefore, will not be useful in others. This chapter restricts its coverage to commonly used devices, leaving treatment of specific devices to other texts.

005. Name the basic requirements for peripheral devices and two ways to use computer time more profitably.

General Requirements for Peripheral Devices. Generally, peripheral devices must meet two basic requirements. First, the devices must be able to modify all data so that it is acceptable to the computer during the input phase of the operation and to present data in usable form during the output phase. Second, the devices must operate quickly and efficiently in conjunction with the computer.

Conventional input devices read coded data into computers or other devices from punched cards, punched paper tape, or from magnetic tape. In some special military applications, the computer input is received from special-purpose devices, such as radar sets, gun platforms, missile guidance systems, satellite telemetry, or tactical display consoles. In scientific digital computers, the input device may consist of a keyboard, while the output device may consist of a plotting board or electric typewriter.

Data may be presented at the output in printed form (English or numerals), in plotted form (such as maps and graphs), on punched cards, paper tapes, magnetic tapes, or oscilloscope displays. Outputs in still other forms are available for special applications.

Nearly all input/output devices suffer the same disadvantage—slowness of response. Most computers can process millions of bits of data per second. Input/output devices, particularly those which require some mechanical operation, are hard pressed to manipulate several thousand bits per second. There is, of course, a wide disparity in data exchange rates between the various devices; but the computer is faster than even the fastest of them.

There are various procedures that can help to utilize computer time more profitably. One such procedure, designed to minimize computer idling time, is to program I/O cycles to run concurrently with computation. Another is to use a number of I/O channels and provide multiplexed inputs to the computer from several I/O devices. (Multiplexing, as used here, refers to the ability of the computer to sample the data on a number of input channels while maintaining the intelligence of the data from each channel. The rate of multiplexing is high enough to permit the operator of each I/O device to retain immediate access with the computer.)

Common methods for improving computer usage insofar as can be accomplished by the I/O equipment itself include the use of off-line devices (i.e., devices not under the direct control of the computer), use of electronic switches to multiplex several equipments on one channel, and the use of buffer storage registers in the I/O equipment. Buffer storage is treated later in this chapter.

Exercises (005):

1. What are the two basic requirements for input/output devices?

2. What disadvantage do nearly all input/output devices have in common?

3. Name ways to use computer time more profitably.

006. State how on-line, off-line, and buffer storage devices are used.

On-Line Equipment. On-line equipment generally operates at high processing speeds and is connected directly to a computer. Usually, on-line equipment is used when large amounts of data are being processed and when very little computation is required. It is now feasible to use slower equipment such as typewriters, printers,and keyboards to supplement the high-speed on-line equipment. Of course, the selection of a particular device or combination of devices must be determined by the intended use of the computing system.

Off-Line Equipment. The equipment that prepares (and sometimes processes) data external to the computer is classified as off-line equipment. Some on-line devices can be used off-line, which results in a more flexible system. Some equipment is used off-line exclusively. Sorters and card punches (which prepare data) and tabulators (which process the data) are in this off-line category. The typewriters and other units mentioned earlier are used for off-line applications, but are classified as auxiliary equipment.

Buffer Storage. Buffers serve as intermediate storage devices to facilitate transfer of data between two media whose operating speeds are difficult or impossible to synchronize. It is frequently necessary to read data from cards, paper tapes, keyboards, etc., into the main (primary) computer memory. In most cases, the speed at which input devices can supply data to storage cannot be increased sufficiently to match the ability of the computer to read in the data at electronic speeds. The same incompatibility is encountered in reading data from memory to output devices. A buffer device is, therefore, designed to read in or write out data at speeds compatible with the input or output device and the main computer memory.

Several types of buffers are in use. The simplest type is an arrangement of flip-flop registers into which data can be slowly accumulated but can be released or read out at electronic speeds. By design, data can be read into and out of the registers in either serial or parallel form. The buffer storage must be capable of reading data slowly from the input device, and, at a later time, writing this data at electronic speeds into the main memory. It must also be capable of reading in data at electronic speeds from the main memory and writing this data slowly at the output device.

Exercises (006):

1. What are the two characteristics common to all on-line equipment?

2. When is on-line equipment used?

3. What is off-line equipment?

4. Name three types of equipment used off-line exclusively.

5. How are buffers used with I/O devices?

6. The buffer storage used with an I/O device must be capable of what?

2-2. Recording Media

Nearly all input and output systems use recording media. The most popular forms of recording media have been the printed pages, punched cards, punched paper tape, and magnetic tape. The most important considerations that determine the choice of recording media are:

- Compatibility between input devices and computer.
- Form and quality required of the display data.
- Ease of handling and accessibility of data.
- Permanence, erasability, and durability of record medium.
- Volume of bulk storage capacity, density, and costs associated with storage of data.

- Size, weight, and power consumption of recording equipment.
- Speed of reading and recording, and reliability of data and of the recording equipment.
- Installation, operation, and recording costs.

007. Specify characteristics of punched cards as input media.

Punched Cards. Punched cards are familiar objects to almost everyone. Punched cards are used for timecards, personnel files, inventory files, and many other types of records. They are one of the most widely used input/output media for digital computers.

The advantages of punched cards are:

- A punched-card file may be easily revised, expanded, or contracted.
- A punched-card file can be easily sorted into subfiles, and cards with desired information can be removed easily.
- Individual items in a data file can be more easily manipulated by using punched cards.
- Stored information is permanent.
- Capacity is unlimited.

The disadvantages of punched cards are:

- The card punches are slow and bulky.
- The cards are heavy and take up storage space.

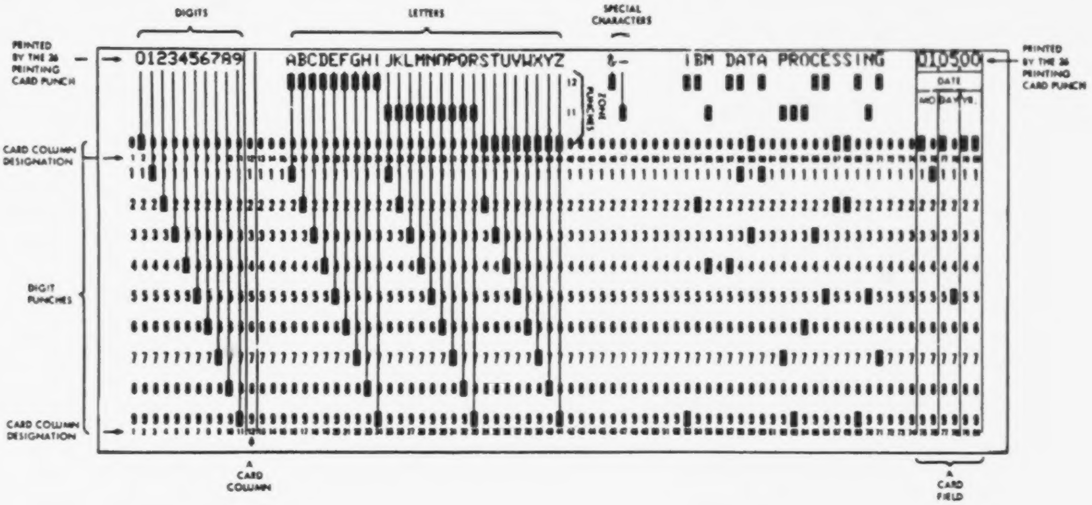
The two most widely used types of punched cards are: (1) the Remington Rand Corporation card and other cards using the RRC card format, and (2) the International Business Machine (IBM) Corporation card and other cards using the IBM card format. The major difference between the two is the number of columns of each. The Remington Rand card has 90 columns, and the IBM card has 80 columns. Since the IBM card format is the most commonly used, we will use it for discussion purposes.

A typical card is of fixed dimensions and is made of a specific quality of paper. Each IBM card has 80 columns, and within each column it has 12 punching positions. Figure 2-1 shows an IBM card, and figure 2-2 shows an AF Form 1500.

Each card has several positions punched. The rows are numbered 0 through 9. Two unnumbered rows may be punched above row 0. These may be referred to as zones (zones 11 and 12 in fig. 2-1); and, when punched with numerical punches, they represent the alphabet.

The numeric characters 0 through 9 are represented by a single punch in a single column. Zero is represented by a single punch in the 0 zone position of the column. The alphabetic characters are represented by two punches in a single column; that is, one numeric punch and one zone punch. Columns A through I use the 12-zone punch and numeric punches 1 through 9. Columns J through R use the 11-zone punch and numeric punches 1 through 9. Columns S through Z use the 0-zone punch and numeric punches 2 through 9. A card may use any format that the particular computer system is designed to use. Some codes used are the standard, row binary, column binary, and Hollerith.

Card Punch. The equipment used to record information onto a card is a card punch. One manual card punch is an electromechanical device which punches information on cards and prints out the information on top of the cards. The punching operation is per-



NEO1 3-232

Figure 2-1. IBM card.

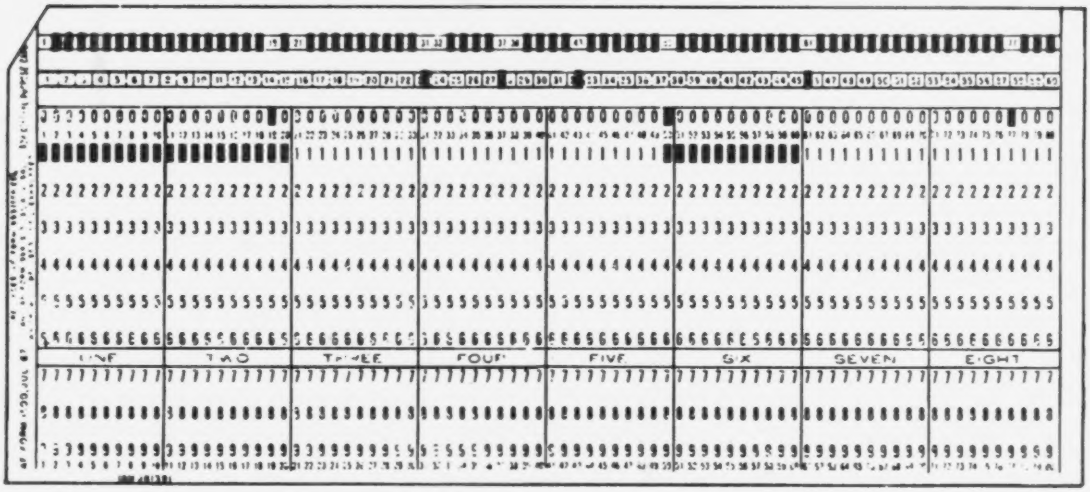

NDA11-12

Figure 2-2. AF Form 1500.

formed by an operator at a keyboard similar to a standard typewriter keyboard. An example of such a manual card punch is shown in figure 2-3.

A card punch for transferring outputs from the computer to cards is shown in figure 2-4. This card punch is operated by the computer through the control unit. The computer generates voltages which operate punch-selecting electromagnets. When the punches operate, they punch out a card-hole pattern corresponding to the computer output information. No manual operation is possible. The computer-operated punch is faster than the manually operated punch. The computer-operated punch can process several hundred cards per minute; the manually operated punch is limited to the three cards per minute and is within normal operator capabilities. In most computers, it is possible to punch information on cards in any of several codes. This may be a built-in feature; if not, it can usually be done by special programming techniques.

A punch feed is shown in figure 2-5. The cards are moved, one at a time, from the card hopper, under a punching station that punches data in the card. After the card is punched, it is moved to a read station. At the read station the punched holes are sensed and the coded information is converted into electrical impulses. These impulses, or digital information (pulse-no-pulse), are then compared to the input data for accuracy. The card then moves into the stacker.

Exercises (007).

1. What is the most commonly used type of punched card format within the Air Force?

2. A punched card is divided into rows, columns, and __________________ .

3. A punch above the 0 row indicates that the information in that column is __________________ .

4. The computer entry punch converts information into a ____________ ____________ ____________ ____________ pattern for computer input.

5. Numerical information is represented on a punched card by a ______________ punch in a ____________ column.

6. What is the most common use for punched card equipment within a computer system?

7. What is the major difference between the two most widely used types of punched cards?

008. State how card readers operate with buffer storage.

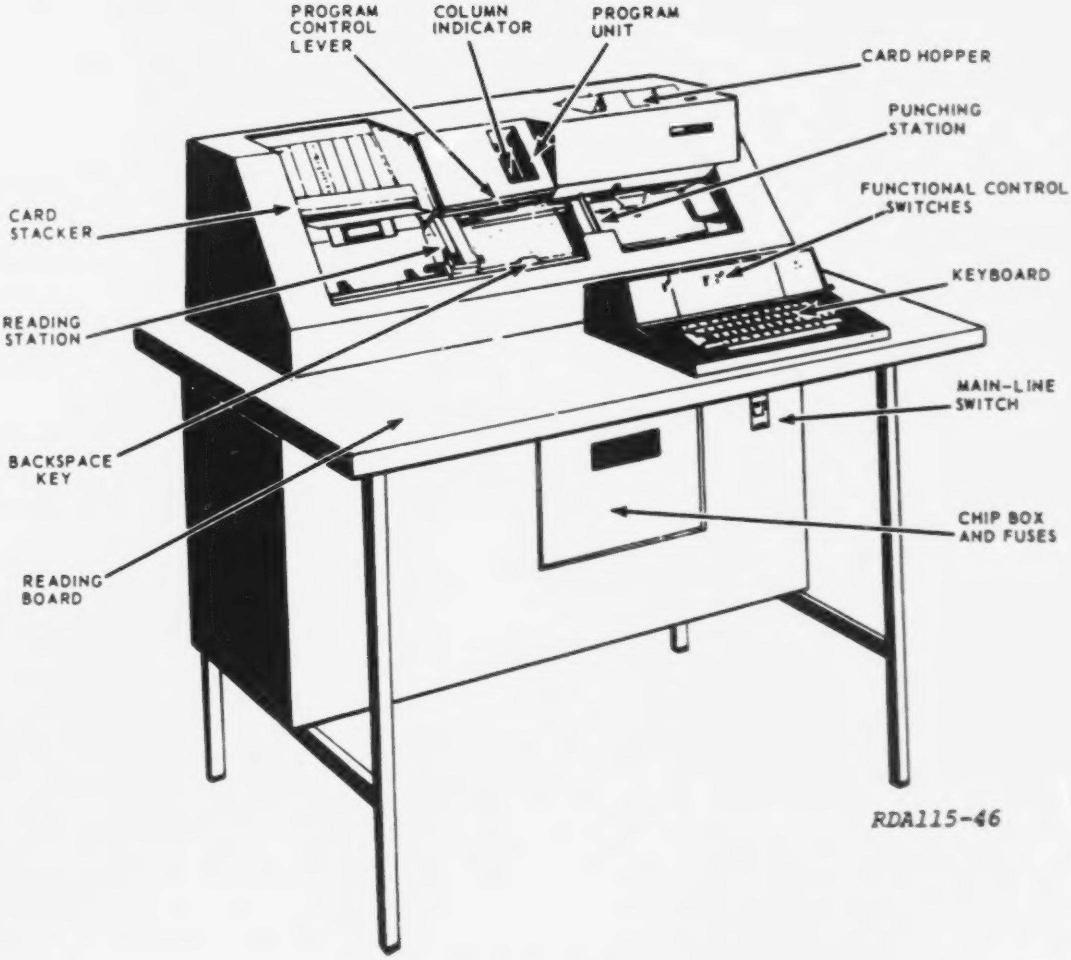


Figure 2-3. Manual card punch.

Using Card Readers with Buffer Storage. Let's look now at a representative method of using card readers with buffer storage. Some card readers are designed for on-line operation with a computer. Furthermore, the computer may be capable of selecting any one of several card readers as the input or output device. The diagram and flow chart in figure 2-6 illustrate one method of reading data from a card reader into the computer memory. Four readers are shown in figure 2-6.

The request for read-in data is generally in the form of a programmed instruction. When the instruction is issued, the control unit produces an input request signal on any one of four input request lines as determined by the instruction. The same instruction (or in some cases a subsequent instruction) will select the desired function, either read or write.

Some readers read the data directly into the computer. This method is slow and does not afford best use of computer time. A more desirable arrangement uses a buffer storage. The card reader passes its input over 80 transfer lines to the storage medium. (Only one of these lines from each reader is shown.) Cores are used as the storage medium in this discussion because of their simplicity.

The storage matrix contains 960 cores (only top rows shown in fig. 2-6), each of which can be in either the 0 or 1 state to represent any combination of holes and no holes contained on the card being read. The data is read in (in parallel form) longitudinally across the matrix so that all 1's in the 9's row of the card are entered first. All 1's in the 8's row are entered next, followed by those in rows 7, 6, 5, 4, 3, 2, 1, 0, 11, and 12, in that order.

A row counter counts each row as it is entered into the matrix. After entering the last row (the 12's row), the row counter indicates that the information is ready for transfer to the computer. If the computer is available to accept the data, it transmits a read enable signal to the card reader to set the read enable circuits. Subsequent instructions will permit the data to be transferred (column by column) into the computer as described later.

The C register provides temporary storage of data en route to the computer. The column counter initiates

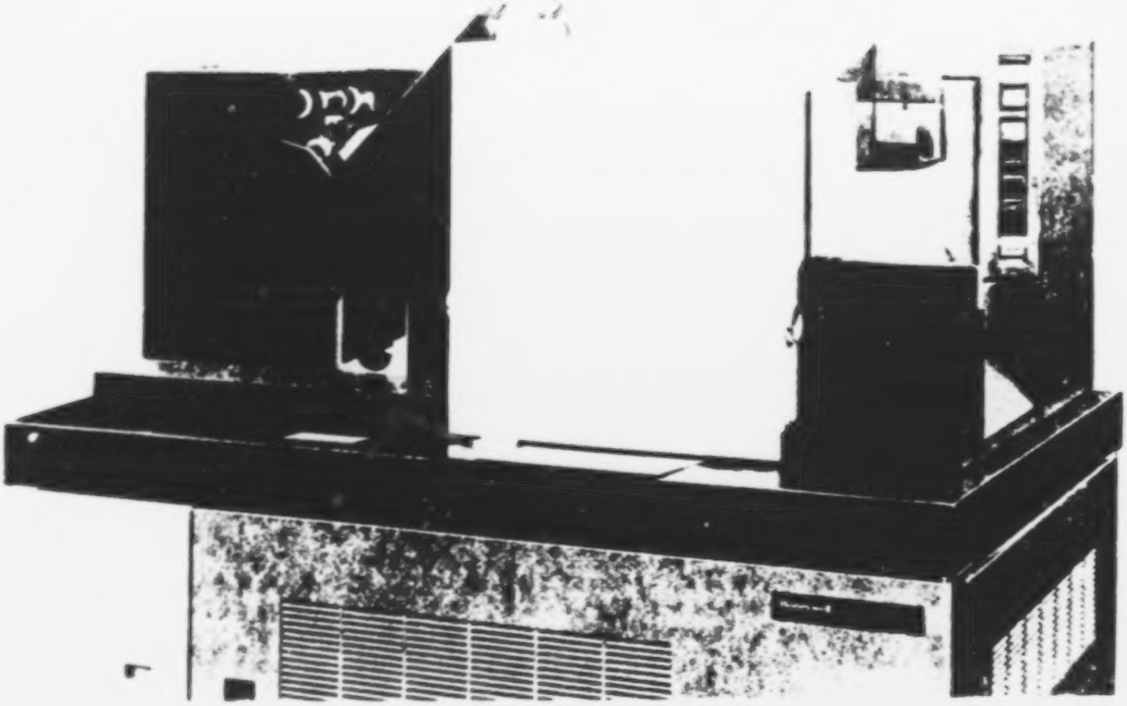


Figure 2-4. Computer controlled card punch.

the "read next card" signal after all 80 columns have been transferred to the computer at high speed. Note that the data is read into the core matrix at the speed of the input device and into the computer at electronic speeds, limited only by the ability of the computer memory to accept and store the data. Thus, the core matrix provides "buffer storage" between the card reader and the main computer memory.

The flow chart (fig. 2-6, B) shows the read-in process. Upon receiving the "input request" signal from the computer, the order to "start card cycle" is issued (A). The "read row" instruction causes the 9's row to be read at the reading station. After the holes and no-holes, or 1's and 0's in the 9's row are read, the "enable row drive and store" instruction causes the drive lines in the matrix (which correspond with holes in the card) to be activated; and their selected cores are switched to the 1 state. All other cores remain in the 0 state. (The memory matrix is cleared before read-in of each card.)

The order "advance row count" places the 8's in the position for read-in. Because the 8's row is the next row to be read, the answer to the question "is row = 12 + 1?" is "no" and a signal is produced to "read row" (row 8 in this case). The process continues, storing the data from the card row by row into the matrix, until all of the card data is transferred to the matrix. The 12's row is the last to be read in.

The answer to the question "is row = 12 + 1?" is "yes." This response causes a command to set the read enable circuits in preparation for the readout of the data from the memory matrix. (Points 1 and 1 are connected.) A command line from the computer carries the signal to cause the readout of one vertical word column of data (12 bits) each time this signal appears on the line. The column counter advances by one each time a 12-bit column is transferred.

If a "no" answer is produced from "count = 80 + 1" circuit and the computer is not ready to accept the next word, a method is provided for storing the word until the computer memory is able to accept it.

After the transfer of all 80 columns, a subsequent order to "advance column count" will produce a "yes" output from the interrogation "count = 80 + 1?" This permits an examination of conditions to determine if the "read input" is still active from the computer. Stated differently, the output asks, "Is the computer

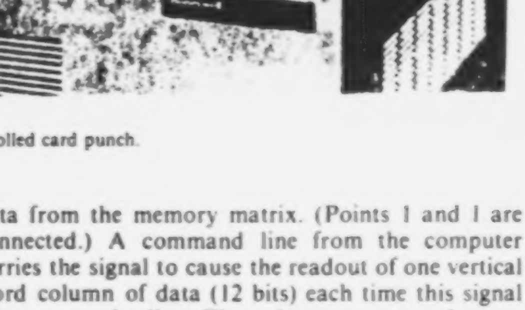


Figure 2-5. Punch feed.

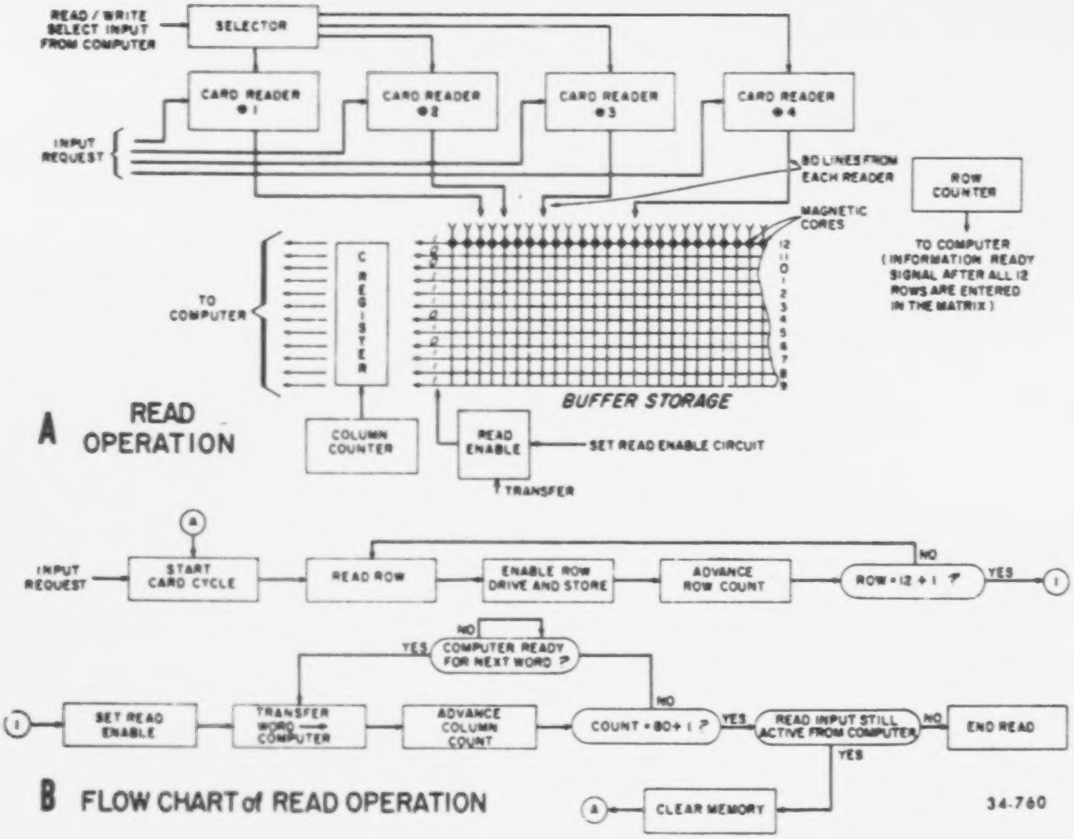

READ / WRITE SELECT INPUT FROM COMPUTER
SELECTOR
CARD READER #1
CARD READER #2
CARD READER #3
CARD READER #4
INPUT REQUEST
80 LINES FROM EACH READER
ROW COUNTER
MAGNETIC CORES
TO COMPUTER (INFORMATION READY SIGNAL AFTER ALL 12 ROWS ARE ENTERED IN THE MATRIX)
TO COMPUTER
C REGISTER
12
11
0
1
2
3
4
5
6
7
8
9
BUFFER STORAGE
A READ OPERATION
COLUMN COUNTER
READ ENABLE
SET READ ENABLE CIRCUIT
TRANSFER
A
INPUT REQUEST
START CARD CYCLE
READ ROW
ENABLE ROW DRIVE AND STORE
ADVANCE ROW COUNT
NO
ROW = 12 + 1 ?
YES
1
NO
YES
COMPUTER READY FOR NEXT WORD ?
NO
1
SET READ ENABLE
TRANSFER WORD → COMPUTER
ADVANCE COLUMN COUNT
COUNT = 80 + 1 ?
YES
READ INPUT STILL ACTIVE FROM COMPUTER
NO
END READ
YES
A
CLEAR MEMORY
B FLOW CHART of READ OPERATION
34-760

Figure 2-6. Card reading operation using buffer storage.

still demanding the read-in of data?" A "yes" answer causes the memory matrix to be cleared and the entire operation to be repeated during the read-in of the next card (points (A) and (A) are connected). A "no" answer initiates "end read," and all card reader operations are discontinued.

To further understand how buffer storage expedites use of computer time, let's consider the overall operation of the computer with and without buffer storage and a buffer controlled sequence. In the flow chart of figure 2-7, the instruction for read-in designates an address at which the read-in must begin (first word address, fwa) and the address of the last word (Lwa). For a read-in instruction, these addresses refer to the location at which the words are to be stored in the main computer memory. For a readout instruction, fwa and Lwa would encompass the total data to be read out. The data is read into or out of memory in sequential order from the "fwa" to the "Lwa."

A subsequent instruction causes the computer to select the "input device," which in this case is presumed to be a card reader. Next, the status of the selected device is determined. If the reader is not available or other conditions are not satisfactory (such as "power switch not on"), a "no" output will result from the "ready" interrogation. In some cases, a light, alarm, or other means of alerting the operator to correct the situation is initiated. If the "ready" interrogation produces a "yes" answer, the command is issued to select "read," meaning that data is to be read into the computer rather than written out.

After all such preparations are completed, the "initiate input operation" is issued and the card reading process begins. If buffer storage is not used (the method described here as NORMAL), the computer will issue the order "input one word." This is followed by a store instruction which places the word in the fwa in storage. The computer now causes a counter to increment the word address (wa), count by 1, and to examine the new address number to determine if the new word is the same as the last word address plus 1. If the answer is "no," the next word is requested. This process repeats itself until the output from the interrogation "fwa = Lwa + 1?" is "yes."

Because the numbers (2) and (2) represent the same point, a "yes" answer causes a command for the computer to resume operations under the influence of the stored program. Note that the computer is not available to perform any other operations while the read-in is in progress.

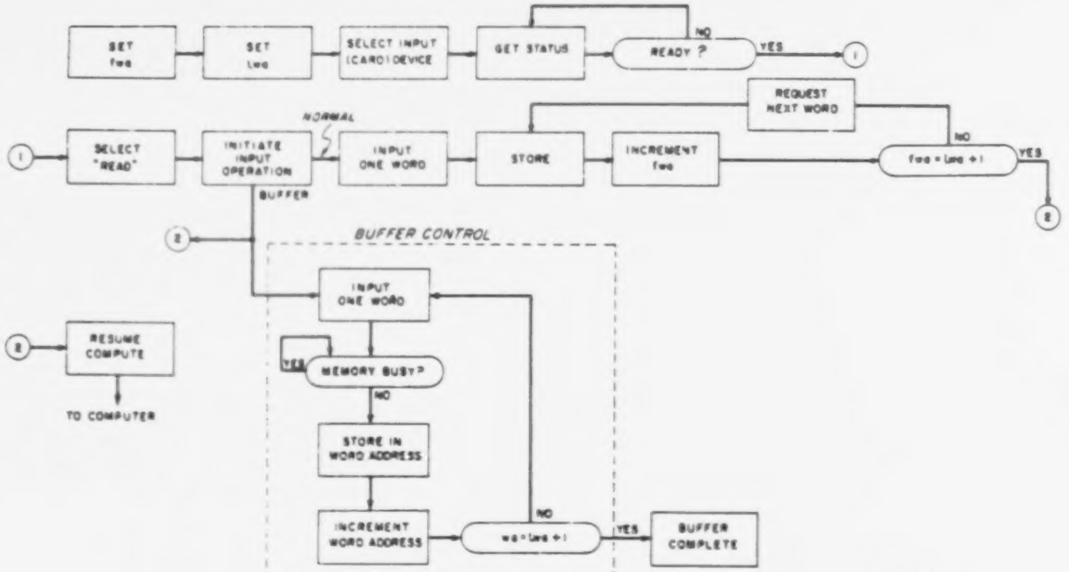

SET fwa
SET Lwa
SELECT INPUT (CARD) DEVICE
GET STATUS
READY ?
NO
YES
1
REQUEST NEXT WORD
NORMAL
SELECT "READ"
INITIATE INPUT OPERATION
INPUT ONE WORD
STORE
INCREMENT fwa
fwa = Lwa + 1
NO
YES
2
BUFFER
BUFFER CONTROL
INPUT ONE WORD
RESUME COMPUTE
TO COMPUTER
YES
MEMORY BUSY?
NO
STORE IN WORD ADDRESS
INCREMENT WORD ADDRESS
wa = Lwa + 1
NO
YES
BUFFER COMPLETE
34-761

Figure 2-7. Flow chart of normal and buffer read-in of card data.

Now consider the action using the buffer method. All conditions and operations are the same up to and including the "initiate input" operation. The fwa and Lwa are stored in a register in the buffer control section so that the buffer operation will stop when the action is completed. As soon as the "initiate input operation" command is issued, a buffer control unit begins to operate and the main computer is released to perform other operations (arithmetic, control, etc.). Buffer control operates independently of the main computer.

After buffer control has caused the read-in of the first word, an interrogation determines if memory is busy. (Memory, and all associated drive and registers, may be busy with some other operation.) If the answer to this interrogation is "yes," no attempt is made by buffer control to enter the data into the main computer storage until memory is available.

After storing the data, a counter increments the word address (wa), and the new address is compared with the previously stored code (Lwa + 1) to see if the last word has already been stored. If the answer is "no," the process repeats until a "yes" output is produced. This "yes" output indicates that the buffer operation is completed. Note in this case that the computer is not directly involved in the buffer operation.

The terms "buffer" and "buffer storage" are used to describe almost any operation that takes place in a computer with the aid of any form of intermediate storage. However, the term "buffer storage" most frequently denotes the type of operation just explained. The word "buffer" generally refers to a device or arrangement of devices or registers that temporarily store data as they are being transferred in the computation process.

Exercises (008):

1. In using a card reader with a buffer storage, how is data read in?
2. How many cores are in the storage matrix?
3. In figure 2-6, what function is performed by the C register?
4. What does the "read row" instruction (fig. 2-6) cause?
5. What happens when the "enable row drive and store" instruction is received by the card reader?
6. When and by how much is the column counter advanced?
7. What is the advantage in using buffer read-in of card data?

009. Specify the characteristics of punched paper tape.

Punched Paper Tape. Paper tape has many of the characteristics of punched cards. It employs the principle of hole-no-hole; requires a mechanical device to move the tape; and employs a brush or photoelectric cell for reading. It is similar to magnetic tape in that it must be read sequentially. The hole patterns are punched into the tape according to a code in which each pattern conforms to specific decimal numbers, alphabetic characters, or special characters. One column of the total possible punching positions (one for each channel) across the width of the tape is used to code these characters. Figure 2-8 shows a section of paper tape illustrating the channels and several coded characters.

The lower four channels on the tape shown in figure 2-8 are labeled 1, 2, 4, and 8 (do not include the feed holes). The vertical sum of the position punches indicates the numeric value of the character. For example, a numeric 2 is represented by a hole punched in channel 2. A numeric 6 is represented by a combination of a 2 and a 4 punch.

The upper four channels on the tape are labeled CHECK, O, X, and END OF LINE (EL). The purpose of the X and O channels is similar to the purpose of the zone positions of punched cards. They are used in combination with the numeric channels to record alphabetic and special characters. The check channel provides for character parity. Take a column with an even number of holes. To make the total number of holes in that column "odd" and give an "odd-count PARITY CHECK," a hole is punched in the CHECK channel. A punch in the EL channel represents a special function character that marks the end of a record on tape. The tape feed code is made up of punches in the X, O, 8, 4, 2, and 1 channels. It is used to indicate blank character positions on tape.

Paper tape is a continuous recording medium. It is limited only by the capacity of the storage component into which the data is to be placed or from which data is received. A punched card, on the other hand, is limited to 80 columns of information.

Paper tapes that have five through eight parallel channels are commonly used. Normally, eight parallel channels are preferred for computer input. Some tapes are made of plain paper. Others are made in the form of a sandwich with aluminum or paper between two thin films of plastic material. Some are oil impregnated and strong fibered for long wear. Mylar tape, an extremely tough and long-lasting plastic tape, is also available. Mylar tape comes in rolls 1,000 feet in length, each roll capable of holding 120,000 characters.

Exercises (009):

1. Paper tape has many of the characteristics of ______________ ______________.
2. Punched paper tape is similar to magnetic tape in that it must be read ______________.
3. A numeric 4 is represented by a hole punched in channel ______________.
4. Channels X and O perform the same function as ______________ positions of a punched card.
5. ______________ tape is used in applications where long life is desired.

010. Specify the uses and operational characteristics of paper tape units.

Paper Tape Devices. Paper tape machines are usually used as an input/output device, although they have been used for memory storage. Information is coded on the basis of a hole-no-hole code. In a typical system, the holes are punched on tape by a manual keyboard and paper-tape punch procedure or by the computer and paper-punch arrangement. Normally, a computer-prepared tape is an output procedure, and a keyboard-prepared tape is an input procedure. A paper-tape unit is shown on the left side of the teletypewriter in figure 2-9.

The paper-tape reader converts the punched paper-tape code into electrical pulses by means of a photoelectric system or by sensing the pattern of hole-no-hole with brushes. The paper-tape reader interprets the punched tape and can be linked to a printout device as well as to the input phase; it can also be used to verify the correctness of a keyboard-prepared tape before the tape is processed as input information. In the input phase, tape is sensed by the reader; and the information, expressed in electrical pulse form, is fed into the computer. Although a paper-tape system is less expensive than a magnetic-tape system, it is a relatively slow method of information processing. Figure 2-10 shows a paper tape punched with a five-channel code.

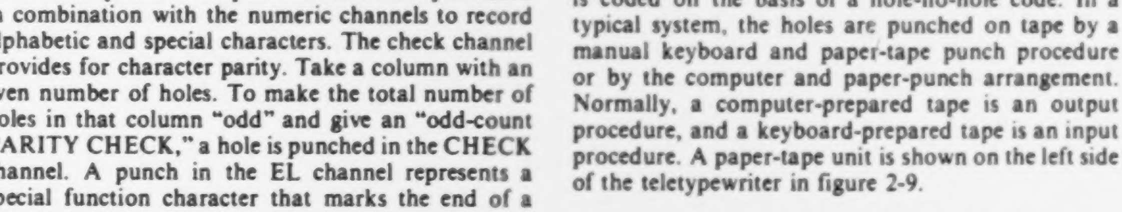

TAPE FEED
SPACE
A B C D E F G H I J K L M N O P Q R S T U V W X Y Z 0 1 2 3 4 5 6 7 8 9
END OF LINE
X
O
CHECK
8
4
2
1

Figure 2-8. Eight-channel punched paper tape.

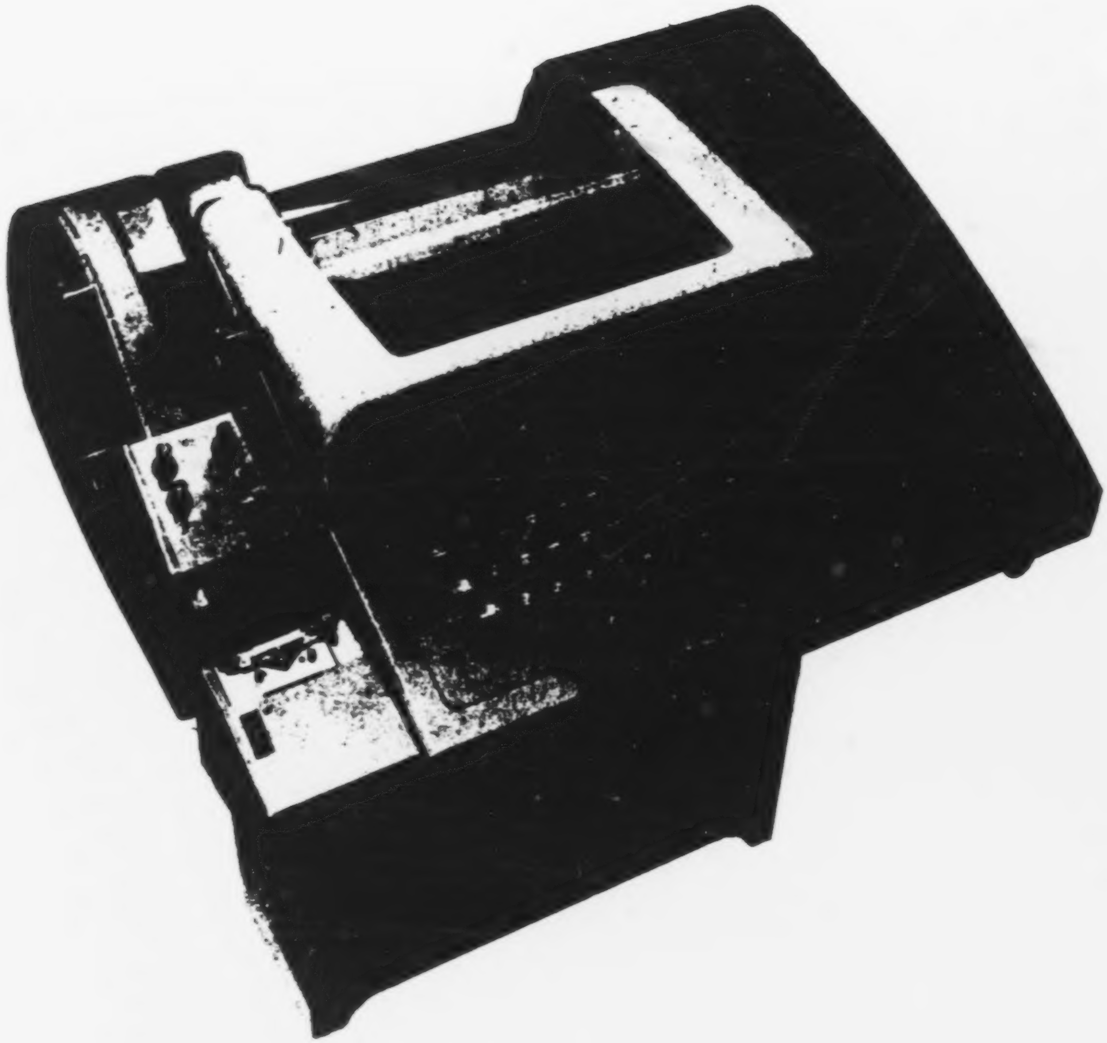


Figure 2-9. Teletype with paper tape unit.

Exercises (010):

1. Paper tape is usually used as an input/output device; however, it may be used for ____________.
2. Normally, a tape prepared on a keyboard is used as an ______________ device.
3. The punched tape reader converts the information stored on the tape to electrical impulses by sensing the hole-no-hole patterns. This is done electrically with a photosensor or mechanically by using ______________.
4. Compared to a magnetic-tape system, a paper-tape system is ______________ and ______________ expensive.

011. Identify terms associated with magnetic drum input/output.

Magnetic Drum. The magnetic drum is a common medium capable of storing from a few thousand characters to millions of characters, depending upon its application. In some computer systems, it is used as internal memory, while in others as an auxiliary storage device. The difference in magnetic drums used for internal memory and those used as external memory is their size. External memory devices are much larger. A magnetic drum is a steel cylinder inclosed in a copper sleeve. The copper surface is plated with a cobalt and nickel alloy. This coating of the drum's surface is the actual storage medium.

If an area of this material is placed in a magnetic field, it becomes magnetized. After the magnetizing force is removed, the magnetism is retained indefinitely. The area affected can be quite small (on one model, it is about 0.071 inch long) so that a large

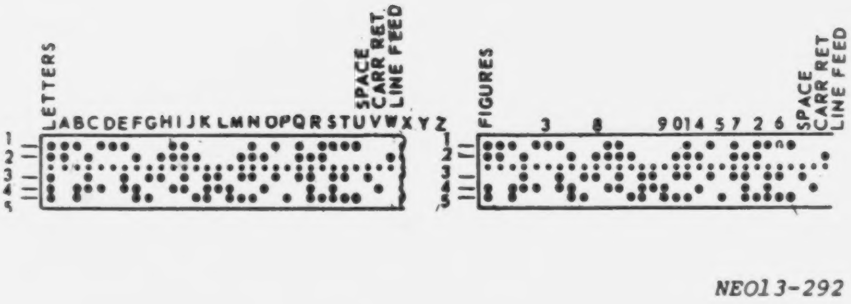


Figure 2-10. Five-channel code.

number of magnetized spots or cells can be placed in a small space. The effect of magnetizing a cell is the same as if a tiny bar magnet were imbedded in the surface of the drum.

As the drum rotates at a constant speed—12,500 rpm in one model—information is written by magnetizing cells as the surface passes a read-write head. The head consists of read and write coils of fine wire wound around a center core. A plastic shim separates the end of the core, providing a magnetic gap. The head assembly is positioned close to the drum so that magnetic lines of force produced by the write head fringe around the gap and flow through the alloy surface (see fig. 2-11).

The cells are magnetized by sending pulses of current through the write coil. The direction of current flow determines the resulting polarity of a cell. Consequently, cells can represent either 1's or 0's, the two digits used for binary recording in all computers. Because the drum is rotating while writing takes place, current must be extremely short to limit the magnetized area. Thus, the size of the cell is almost the same as if the drum were motionless.

When a cell that has been magnetized passes under the read-write head, the magnetic state can be sensed by current induced in the read coil. In this way, information written on the drum can be read back when needed. Reading is not destructive because the condition of a cell is not changed as it passes the head. Unlike core storage, the drum needs no regeneration process; and the information can be read again and again without being erased. Drum storage is, therefore, permanent, and data on its surface remains there indefinitely even after the power to a system is turned off. Information is replaced only when new information is written.

Each drum has a specific number of storage locations, each of which is addressable by the computer. The capacity of each location depends upon the design of the drum and the data representation used. In figure 2-12, each section contains 200 character locations; and each section is addressable (1000–1299). Because reading or writing can occur only when a specified location is passing the heads, access time may vary, depending upon the distance to be traveled by that location to the head. Although the drum has lost some significance as an internal storage medium, present applications use its characteristics as auxiliary storage (an extension of internal memory).

To further explain the magnetic drum mass storage media, the UNIVAC 1057 FAST-RAND IAS will be used. The FAST-RAND IAS (immediate access storage) unit has a capacity of 66 million 6-bit alphanumeric characters. The average access time is 57 milliseconds, and characters are transferred to and from the drum at the rate of 183,000 characters per second.

As illustrated in figure 2-13, the drums are labeled "A" and "B," and each contains 3072 recording paths or tracks around the circumference of the drum. Each drum is serviced by 32 *read-write heads*. Therefore, the two drums contain 6144 tracks serviced by 64 *heads*. All 64 heads are mounted on a movable positioning bar. The heads remain fixed vertically, and the drums rotate at 880 rpm above and below the heads. When the positioning bar is moved, all heads are moved in *unison*. The heads are consecutively numbered from 0 to 63.

The 3072 tracks on each drum are subdivided into 32 groups of 96 tracks each (1 group per head). See figure 2-14. Each track is numbered from 00 to 95 within its group, and each head is capable of being positioned over any one of the 96 tracks. Each track is 1 bit wide, and there are 57 tracks per inch. Since all heads are mounted on a single positioning bar and are moved in unison, notice that all heads are positioned over the same identically numbered track at

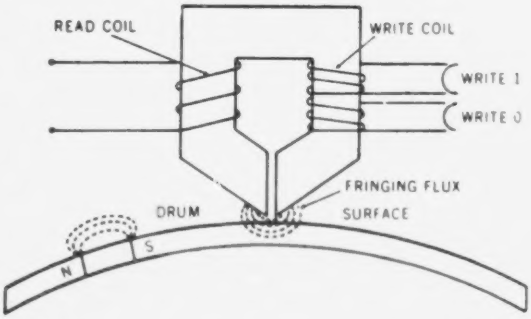


Figure 2-11. Example of magnetic drum recordings.

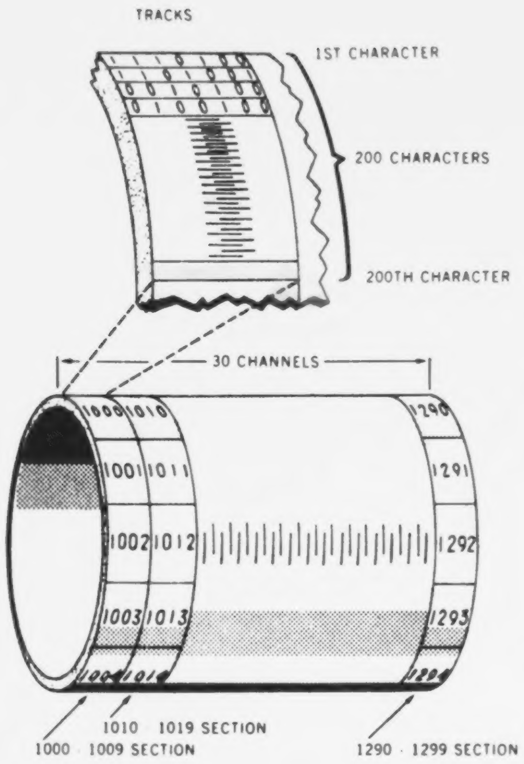


Figure 2-12. Schematic of magnetic drum storage.

any given time, i.e., when any head is over track 00, then all heads are over track 00 within that particular group. From this point on, we will refer to both drums as if they were one unit.

Each of the 6144 data tracks is further subdivided into *data sectors*. There are 64 sectors, numbered 0 to 63, on each track. The sector is the *smallest addressable* unit of data on the *drum*. *If there are 64 sectors per track, 96 tracks per head, and 64 heads,* then there are 64 × 96 × 64, or 393,216 addressable sectors on the drum. Each sector can contain 168 6-bit alphanumeric characters. When a data sector is read from the drum, a 168-character image is transmitted to memory. Likewise, when a data sector is to be written on the drum from memory, 168 characters are transmitted. The general organization of a data sector on FAST-RAND drums is shown in figure 2-15. Each track contains 64 sectors that are addressed octally 00 through 077. The hardware sentinels signal the beginning and end of a sector.

To read data from or to write data onto the drum, an address is decoded in sequence to determine the correct unit, track, head, and sector. Ideally, each record to be stored on the drum would contain its actual address, which would simplify programming. For example, a record whose part or reference number is 01123456 could be stored directly at location unit 1, track 12, head 34, sector 56. Such an arrangement, wherein each data record contains its own unique address, is known as *direct-addressing*. Unfortunately, this method is very seldom possible because of the wide range of numbers and the volume of records involved.

There are various methods referred to as *indirect addressing* used in assigning data records to available storage locations. Grouping of records, look-up tables, functional keys, arithmetic calculations, etc., all have their own advantages and drawbacks; therefore, *appropriate measures must be taken by the programmer to insure that only one record* is assigned to each available address.

Magnetic drums are called mass storage units and are considered random access devices. Although their access time is variable and not as fast as the computer internal core memory, units of storage can be addressed in an essentially random manner by specifying a particular location (address). Mass storage media can be used in handling sequentially organized files; however, their nonsequential or random storage and access capability is of greater significance.

Sequential processing of a magnetic drum file is similar in concept to the technique generally used in handling magnetic tape files; however, significant differences of physical environment exist between magnetic drum storage. A magnetic tape file is defined as an input file or an output file, but not both. When a physical tape record is read, the reel is automatically in proper position to read the next record. At the completion of the program, the input file will contain the same information as it did before the program started. A tape file must be processed sequentially.

In contrast, a magnetic drum file may be used for both input and output because of its record accessing characteristics. A read operation may be performed on the same physical file as a write operation. The usual file update technique is to read a record, store the address of the physical location of that record, process the record, and overwrite the original record with its updated version, using the address stored by the read operation.

In a random file each record is at an address computed by a *randomizing routine*—a program that calculates the address from the item's control number (key field). The order of the records within the storage unit with respect to their control numbers is determined by this formula and, therefore, is generally *not* sequential. To find a record in a random file, its address is simply computed from the control number by the same formula that was used to put it there. If the control numbers of the records in a file used are consecutive numbers without gaps, they may be converted to addresses by simple arithmetic.

Exercise (011):

1. Match the term in column B with the phrase in column A that is most appropriate for that term.

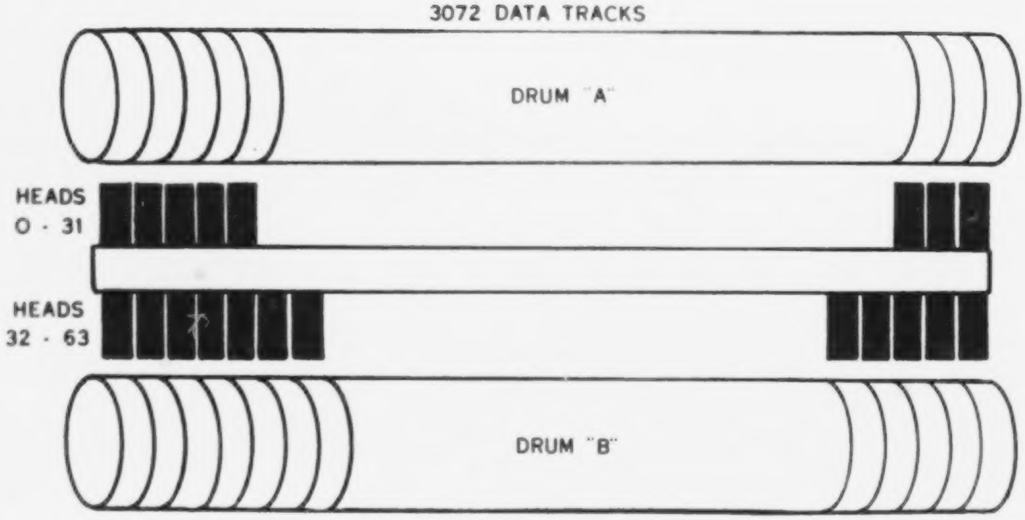


Figure 2-13. Arrangement of read-write heads.

Column A

___ (1) Magnetic storage medium.
___ (2) Information is lost and must be regenerated.
___ (3) Addressable by the computer.
___ (4) Delay caused by a specified location reaching the read-write heads.
___ (5) Recording path around the circumference of the drum.
___ (6) The smallest addressable unit readout of data on the drum.
___ (7) 168 characters.
___ (8) Contains 64 sectors.
___ (9) Each data record has its own unique routine address.
___ (10) Grouping of records, look-up tables, functional keys, arithmetic calculations, etc.
___ (11) Calculates the address from a key field.

Column B

a. Access time.
b. Track.
c. Sector.
d. Cobalt and nickel.
e. Direct addressing.
f. Destructive readout.
g. Storage locations.
h. Indirect addressing.
i. Randomizing routine.

012. Specify characteristics of magnetic tape as a storage medium.

There are two types of tape used with digital computers—magnetic and paper. Both types can be used for either input or output functions. Each type has its own distinctive processing element, and the tapes are not interchangeable.

Magnetic Tape. Magnetic tape usually is a coated plastic tape, about 1/2-inch wide, similar to the tape used in home-style tape recorders. The coating has magnetic properties that enable the tape to be magnetized in discrete units (very small magnetized spots).

Information is represented in the form of a pattern of magnetic bits. In one form of tape recording, a magnetized spot or bit may represent a binary 1; a nonmagnetized spot on the tape may represent a binary 0. A more common system of writing on tape requires 1's to have a change of flux and 0's to hold a steady flux. A large amount of information can be stored on a length of tape. A typical tape is about 2600 feet in length and has a word density of up to 1600 bits per inch.

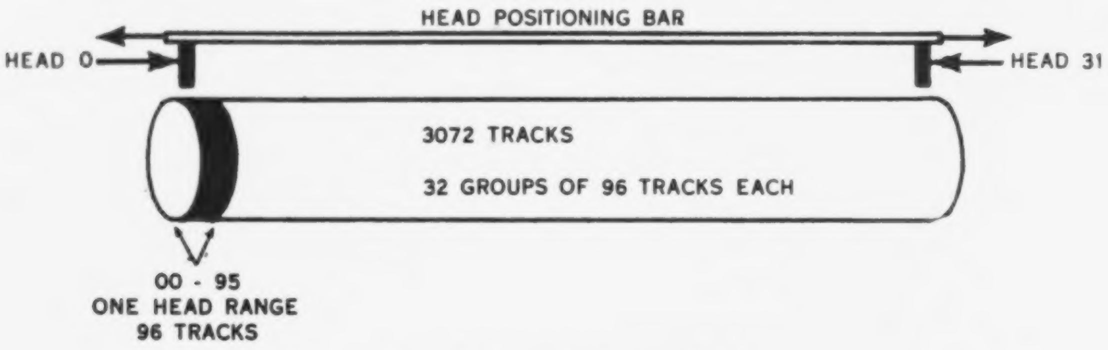


Figure 2-14. Range of one read-write head.

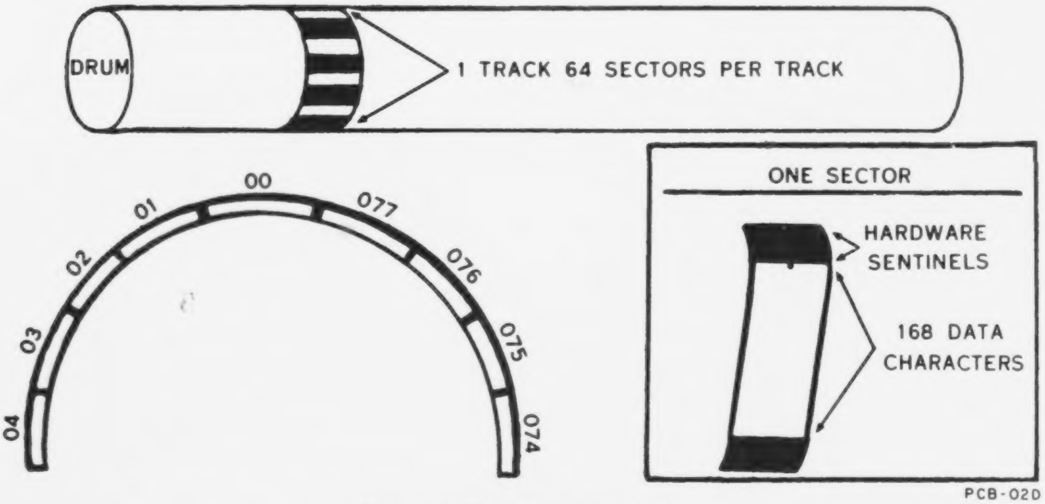


Figure 2-15. Drum storage organization.

Writing and reading magnetic tape. Writing on magnetic tape occurs as the tape is moved across the magnetic gap of a recording or write head. The number of recording tracks in a write head is determined by the code that is used to represent numeric and alphabetic characters. Electrical pulses are sent through recording head coils at desired intervals. The iron oxide coating is magnetized by these pulses. These magnetized areas may be sensed as a 0 or 1. To establish a given code, current will not flow through all the coils at the same time. These patterns represent the data sent from the computer. Figure 2-16 shows a 7-bit alphanumeric code.

The tape moves at high speed across the write heads. Speeds are 75 inches per second and 112.5 inches per second. The write pulses to the write heads are so brief that the spots are magnetized *almost* as if the tape were stationary for the period that the pulse is present.

There are two types of read-write heads used in magnetic tape units. One type has a single gap for each of the channels. Both reading and writing occur at the same gap. Figure 2-17 shows a read-write head which has only one gap. The other, newer type uses two magnetic gaps for each channel. One gap is used for writing, and the other is used for reading. Figure 2-18 shows this type head.

The principles of reading and writing are the same for both type heads. However, the two-gap head has the advantage of being able to read the data shortly after it is written. This allows the data to be checked for errors. To read from the magnetic tape, the tape is passed over the read head. As the magnetized spots pass the gaps, small electrical currents are generated in the coil of the read head. The pulses represent the data that is sent into the computer. Writing on magnetic tape erases old information from the tape. Reading does not do this, so the tape can be read over and over.

Tape unit. The magnetic tape unit is both an input and an output device. The actual reading and writing of information takes place in the unit. One type of tape unit is shown in figure 2-19. The general appearance and use of the different models are similar. The methods of reading, writing, and tape transportation are different. A tape feed unit is shown in figure 2-20.

The tape from the file reel is threaded through the tape-feed mechanism to the take-up (machine) reel. The tape is moved from the left reel to the right reel during writing and reading. The loops of tape on either side of the head allow fast starts and stops without breaking the tape. The tape must start and stop rapidly —with speed in the order of 5 to 10 milliseconds. The tape is accelerated to a high rate of speed by drive capstans. The much heavier reels are able to accelerate at a slower rate by the use of the loops. The reels have to put more tape into the loop before it gets too short or take tape out of the loop before it gets too long. This is done by a servosystem that senses the length of the loops and adjusts them for the correct length. The loops are usually held down to maintain tension on the tape and hold the tape against the head. The loops hang in a vacuum chamber, where the tape fits snugly. The chamber is divided into two parts by the tape. Air is pumped from the bottom part of the chamber. Since the upper part of the chamber is at a different pressure, the tape loop is pushed downward. This keeps the needed tension on the tape. Switches that are actuated by the air pressure sense the length of the loops and send signals to the reel-drive control to adjust the loops properly.

Generally, information is left on the magnetic tape since it will probably be used again in the computer. Sometimes the information is printed out by use of a high-speed printer. Tapes are generally used as large-capacity, slow-access memory storage. They may be considered input/output devices since they are used to initially load information into the computer and to receive information from the computer.

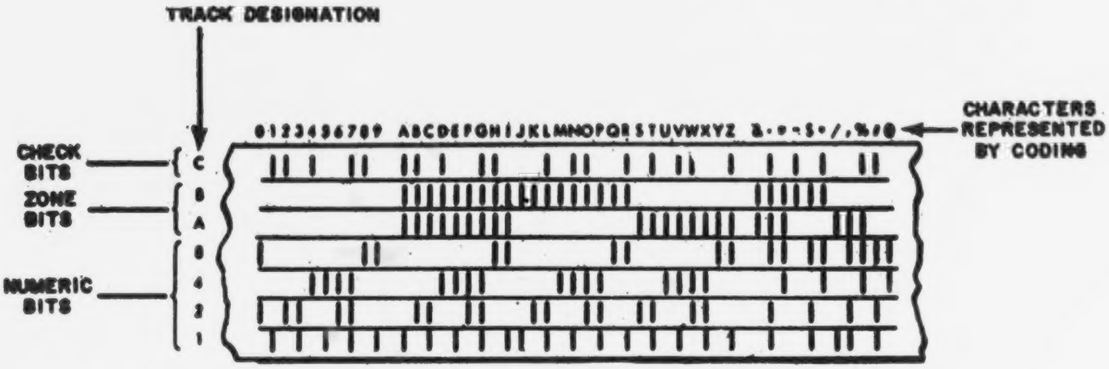

TRACK DESIGNATION
0123456789 ABCDEFGHIJKLMNOPQRSTUVWXYZ &.¤-$*/,%#@
CHARACTERS REPRESENTED BY CODING
CHECK BITS
ZONE BITS
NUMERIC BITS
C
B
A
8
4
2
1

Figure 2-16. Seven-bit alphanumeric code.

Exercises (012):

1. Magnetic tape is used for large-capacity, slow-access ______________ .
2. Writing occurs while the magnetic tape is stopped. (True/False)
3. The number of recording tracks in a write head is determined by the ______________ used to represent characters.
4. The newer types of read-write heads utilize three magnetic gaps per channel. (True/False)
5. Magnetic tape units are used as ______________ and ______________ devices.
6. The loops on either side of the read-write head allow for rapid ______________ and ______________ without breaking the tape.
7. Reading destroys information stored on a computer tape. (True/False)
8. Vacuum chambers are used on some tape units to maintain proper ______________ on the loops.

013. Identify the three categories of magnetic disk units, and specify the characteristics of the magnetic disk.

Categories of Disk Units. Magnetic disk units are fast-access, auxiliary storage devices in which data is stored on rotating magnetic disks. Disks have become the major external memory device for current computer systems. Four factors which have dictated the increasing use of the disk unit are its low cost/bit, high-access speed, large storage capacity, and versatility. Disk units fall into three basic categories or types. Each type of disk unit has characteristics unique to it and also characteristics common to all. We'll briefly discuss disk types and the characteristics of each in this section. A detailed look at the disk as an external memory device will be covered in Chapter 3 under "Storage Media."

The basic recording medium used in disk units is the magnetic disk. The disk is similar in appearance and analogous in operation with the phonograph record. Data is recorded in concentric, magnetic paths called "tracks." The disk or platter in a disk unit is either a *hard* or *floppy* disk. Whether a unit uses a hard disk or a floppy disk will determine the category in which a disk unit resides.

The three major types of disk units are as follows:

(1) The IBM-developed Winchester hard disk—the metallic disks are sealed in the unit, not removable.

(2) The conventional hard disk—the metallic disks are removable through the use of a disk pack.

(3) The "floppy" disk—flexible, plastic, oxide-coated disks, inserted or removed singly.

Magnetic disk units are commonly referred to as "disk drives." Three components are necessary for disk unit operation. First is the electromechanical section used for rotating the disk and loading the recording heads. Second is the disk drive electronics which encodes the data for writing on the disk and also has data decode circuitry for reading from disk. Last, but not least, is the disk controller electronics. The controller may be a separate unit or part of the disk drive. Newer disk drives use a microprocessor as the controller, which is located within the disk unit. The controller, as the name implies, directs the operation of the disk drive so that data transfers occur rapidly and correctly.

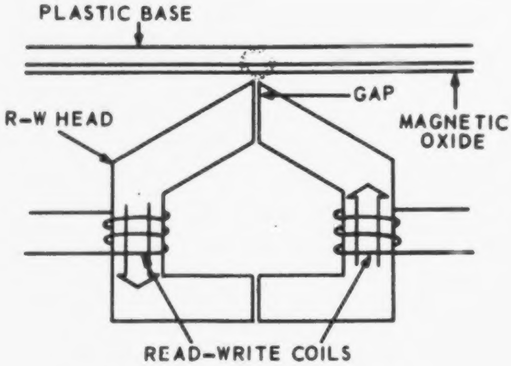


Figure 2-17. Single gap read-write head.

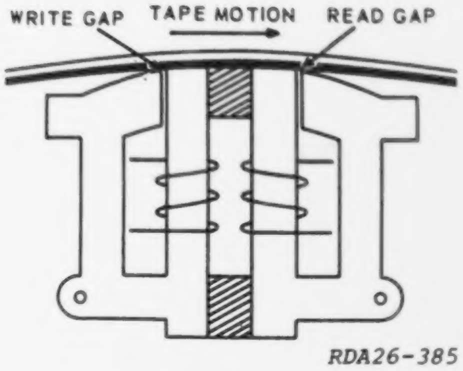


Figure 2-18. Double gap read-write head.

The Disk. The hard disk is usually made of aluminum with a ferric oxide coating, similar to the coating used on magnetic tape. The disk is precisely made to insure uniform thickness and diameter. The standard diameter for a hard disk is 14 inches, although newer Winchester-type disk units use an 8-inch or 5¼-inch disk. The oxide coating is approximately 50 microinches (millionths of an inch) thick.

The floppy disk is made of plastic, coated with a magnetic oxide, and sealed in a cardboard jacket to protect the disk surface. Floppies come in two diameters, the 5¼ inch and the 8 inch. Like the hard disk, the floppy disk is similar to a phonograph record; but it's made of flexible plastic, hence the name "floppy." The packaged floppy disk is also called a *diskette*. The estimated life of a diskette is approximately 2 years.

A magnetic disk is illustrated in figure 2-21. The disk has a number of concentric circles, called *tracks*, where data is stored. The specific number of tracks will be determined by system design. The common number of tracks on many disks is 64 or 128 per side. The disk can be further subdivided into *sectors* which will define more specific areas of the disk. If you think of the disk as a pie, then cut the track area into 8 or 16 pieces of pie; each piece of this "disk pie" would equal one sector. By marking a starting point on the disk in some manner, we can number the sectors from 1 to 8 or 1 to 16. This is how we locate data on a disk. All we need do is specify the sector we want, then specify a track in that sector, and we end up with an address for our data. The starting point we use is called the "index."

A disk may be used singly or can be stacked to allow even greater storage. Disks are stacked on a vertical shaft in what is called a *disk pack* (fig. 2-22). Disk packs enable us to increase data storage in the system, and the pack can be stored for future use after data has been written on it.

The disk pack has circular protective plates mounted above the top disk and below the bottom disk to protect the assembly. A dust cover is provided as an integral part of the removable handle. When inserting a disk pack into the disk drive, the handle locks the disk pack to its spindle which frees the dust cover from the pack. A machine cover must be installed immediately to prevent dust from getting on the disks.

Exercises (013):

1. What type of disk drive unit is the diskette used for a recording medium?

2. Which type of disk unit has the least chance of becoming contaminated?

3. Which type(s) of disk units have the fastest access to data?

4. How do we identify an area of data on a recorded disk?

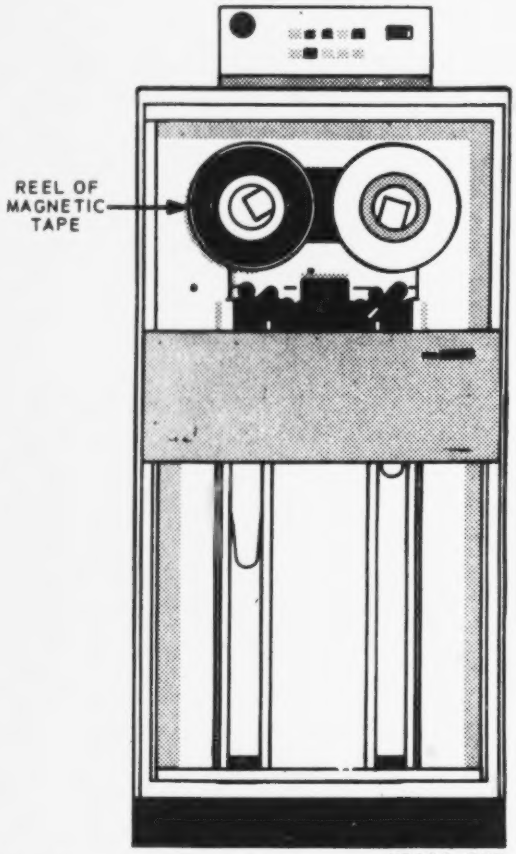


Figure 2-19. Magnetic tape unit.

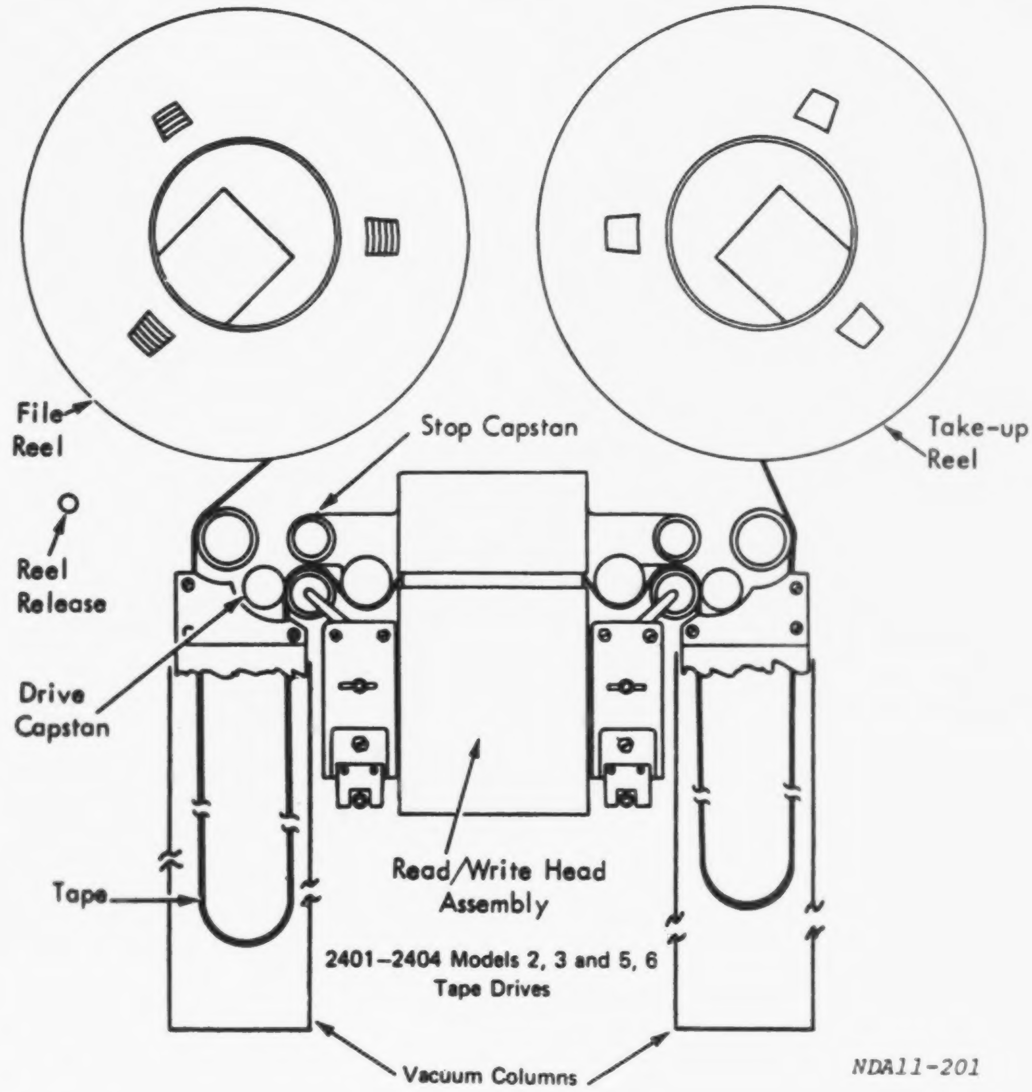

File Reel
Stop Capstan
Take-up Reel
Reel Release
Drive Capstan
Tape
Read/Write Head Assembly
2401–2404 Models 2, 3 and 5, 6 Tape Drives
Vacuum Columns
NDA11-201

Figure 2-20. Tape feed unit.

5. What do we use as the starting point for locating data on a disk?

6. What component within a disk drive interfaces the disk with a CPU?

7. How is data recorded on a magnetic disk?

014. Identify the characteristics that determine a disk drive's capability.

Disk Drive Characteristics. The characteristics of a particular disk drive will affect the four factors mentioned earlier. These factors were cost/bit, speed of access, storage capability, and the versatility of a disk unit. Hard disks offer faster access to data and a larger storage capacity than floppies. A floppy disk allows us to change disks whenever we fill one up with data, whereas the Winchester hard disk won't allow a disk change. A floppy disk unit is cheaper overall, but the cost per bit can be more expensive than the larger hard disk machines. As you will see, there are several disk drive characteristics implied here.

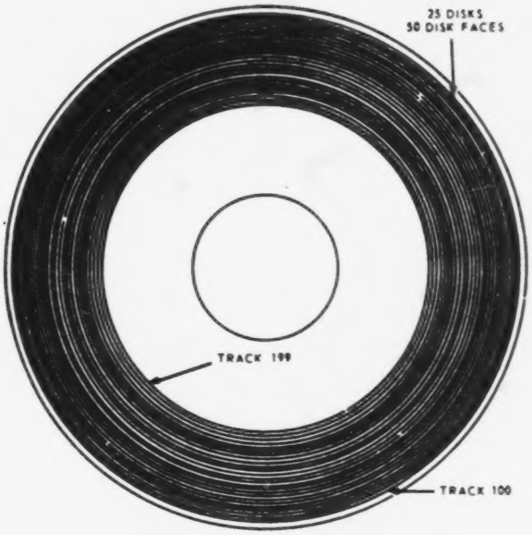


Figure 2-21. Magnetic disk.

The characteristics which are important in determining a disk drive's capability are:

- Speed of disk rotation.
- Moving or fixed head.
- Disk material, size, and number.
- Recording technique.

Now let's describe these characteristics and their effects.

Disk speed. The speed of disk rotation is a determining factor in how fast the access to data on the disk will be. Hard disks rotate at approximately 3000 rpm. Neglecting the time it takes for moving magnetic heads to get in position, access time to a particular track and/or sector is approximately 10 ms at 3000 rpm. The formula for the access time under these conditions is:

$$\text{Access time} = \frac{1}{2} \times \frac{60 \text{ sec/min}}{\text{rpm}}$$

If we take into consideration the time it takes to get the moving head into the correct position, the access time increases accordingly. Access time also varies to some extent due to disk size.

Floppy disks are designed to rotate at a speed of 360 rpm and, therefore, have a greater access time than hard disks. Floppies use moving heads and may or may not use both surfaces of the diskette.

Another factor of importance in disk drives that relates to speed is the method of access. Disks use a combination of random and sequential access to read or write data on the disk. The disk randomly accesses the data storage area specified by the track and sector address. Once there, data is read or written sequentially at that location. Using this type of access makes the disk much faster than magnetic tape units. Drums use the same type of access as disks but have a faster access time due to their higher speed of operation. Unless access time is critical, disks are the preferred magnetic storage device due to speed and cost.

Moving or fixed head. The magnetic record/playback heads in a disk drive consist of one or more moving heads to cover all the tracks of data *or* have one head for each track (fixed heads). As you can imagine, the fixed head disk drive is considerably more expensive than the moving head machine. The advantage of a fixed head disk is that there is no time required for moving the heads and, consequently, the disk drive mechanism is more precise in its operation. A fixed head assembly is illustrated in figure 2-23,B. Most hard and floppy disk drives are of the moving head variety, primarily due to cost.

A moving head hard-disk drive will generally have two heads for each disk. One head is used for the top surface and the second head for the bottom surface. Machines using a disk pack or multiple disks will have a moving head assembly similar to that of figure 2-23,A. The head assembly will move in or out of the disk pack, depending on the specific track to be addressed.

Floppy disk machines may or may not use both sides of the disk for data storage. Of course, if only one side of the disk is used, our data storage capability is cut in half. The heads in a floppy make physical contact with disk surface, whereas in the hard disk they do not. Because the heads in a floppy are in contact with the disk during read and write operations, it is imperative that the diskette be kept clean. Do not touch any exposed disk surfaces. Oils from the fingers can destroy any recorded area.

The heads in a hard disk ride on an *air bearing* that is created by the rotation of the disk at high speeds. This air bearing exists for approximately 50 to 100 microinches above the disk surface. If you consider

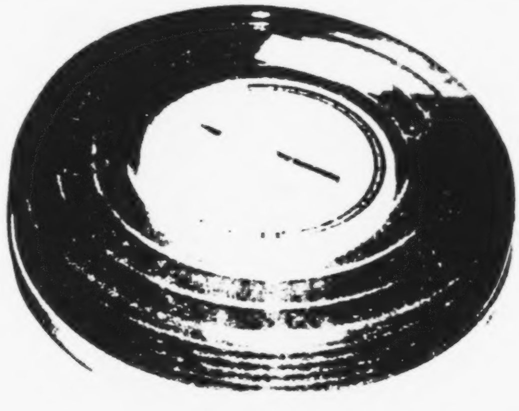


Figure 2-22. Disk pack.

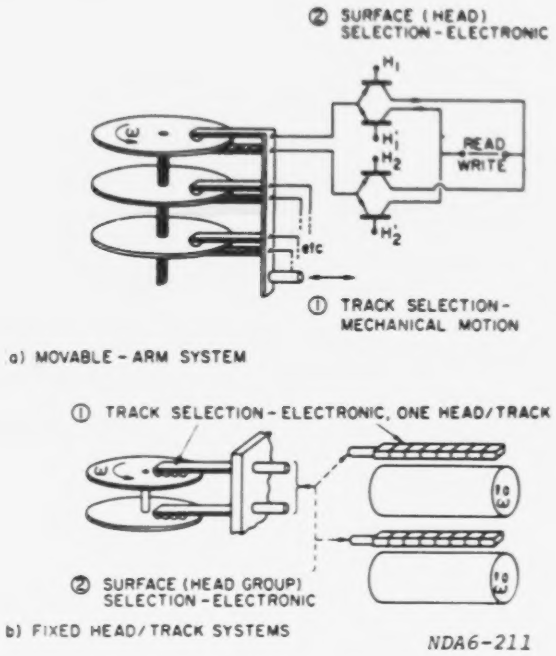

② SURFACE (HEAD) SELECTION - ELECTRONIC
H_1
H_1'
H_2
H_2'
READ
WRITE
etc
① TRACK SELECTION - MECHANICAL MOTION
a) MOVABLE - ARM SYSTEM
① TRACK SELECTION - ELECTRONIC, ONE HEAD/TRACK
② SURFACE (HEAD GROUP) SELECTION - ELECTRONIC
b) FIXED HEAD/TRACK SYSTEMS
NDA6-211

Figure 2-23. Characteristics and parameters: movable head and fixed head systems.

that dust or smoke particles can be 100 to 300 microinches in size, and if the head were to contact one of these particles, a "head crash" would result. A head crash means that the magnetic head has hit the surface of the disk and the disk and/or head will be damaged. Cleanliness in and around a disk drive unit is a necessity.

Disk material, size, and number. The point to be made here is that some characteristics of the disk itself will affect the storage capability of a disk drive.

Floppy disks are made of plastic, small in size, but they are easy to handle and inexpensive. Storage capability is limited per disk, but a great number of interchangeable disks can be used. The floppy disk device is ideal for the storage requirements of small mini/microcomputer systems. The relatively lower cost of these systems makes the floppy a cost-effective solution to storage requirements.

Hard disks are metallic, of large size, and can be stacked in one package to provide a large data bank. The high rotational speed used provides extremely fast access to data. Sophisticated electronics, high-density coding techniques, and multiple disks permit a very large amount of data storage. Due to the precise tolerances of the hard disk unit, the reliability of data is greater. These hard disk characteristics are valuable in large computer systems where an operating program requires fast access and minimal operator intervention.

Recording techniques. The recording technique used by a disk drive is another characteristic that determines the amount of storage we get from a single disk. A recording technique is also a factor in the cost of electronics used in a disk drive. The recording techniques in common use today are these:

- Return to zero (RZ).
- Nonreturn to zero (NRZ).
- Double frequency (DF) or frequency modulation (FM).
- Modified frequency modulation (MFM).

The analysis of these recording (coding) techniques is not appropriate here. Suffice it to say that MFM is becoming a more often-used technique than the other three. MFM is also known as "double density" recording, because twice as much data can be recorded in the same space than with the other coding methods listed. This advantage of MFM is offset to some extent by the fact that the electronics required for its use is more complex and expensive.

Exercises (014):

1. Given a fixed-head disk with a disk speed of 3600 rpm, what is the access time?

2. Is access time increased or decreased when using fixed heads instead of moving heads?

3. What are the characteristics which help determine a disk drive's data storage ability?

4. How is data accessed on all disk drives?

5. What characteristic of a disk drive is being used if there is a head per track?

6. What kind of coding technique is used to double the amount of data recorded in a storage location on the disk surface?

7. Why would the number of disks used be a disadvantage when using a floppy disk drive with a major operating system requiring large amounts of data?

015. Specify the characteristics of keyboards.

Keyboards. A keyboard is basically a typewriter. However, there is a difference in the primary function of the two. As you know, a typewriter's primary function is to produce a hard copy of the keys depressed by an operator; whereas a keyboard's primary function is to input information to a computer.

Many computer systems use a keyboard with a digital encoder as an input device. When a key is depressed, the encoder converts the action of depressing that particular key into a digital code. By this means it is possible to insert data into a digital computer in the computer's machine language. The keyboard and its encoder serve as an interpreter between man and machine.

Many keyboards in use today use a read-only memory (ROM) for this encoder function. The ROM is permanently programmed with the ASCII, 7-bit codes which will represent each letter and number on the keyboad. When a key is depressed, switch action occurs and selects a particular address in the ROM which contains the 7-bit ASCII code for that key. This code is then output to the I/O interface in the CPU. Also stored in the ROM will be several control codes. These control codes will be selected by specific keys on the keyboard and will cause certain control functions to be implemented. Control codes will let the computer know when you have finished a line of information or tell the CPU when you are finished with your keyboard input. There may be a few or many control codes used, depending on system design.

Some of the older keyboards are an integral part of a typewriter, so you can see what keys have been depressed and provide a permanent record on paper of your input. Newer keyboards are interfaced with a video display which also serves as an output device for the CPU.

The keyboard is a very useful input device. It is usually the main interface between man and machine. It can be used to select other I/O devices for reading or writing, and it can cause the actual reading or writing of that device to occur. This is a very useful feature in that it is a simple matter to initialize a computer system for its primary mission through the use of the keyboard.

Mechanical keyboards, such as used in a typewriter, will probably give you the most problems as a maintenance specialist. For this reason, we will present a discussion of the typing principles associated with a typical keyboard.

Typewriter Principles. Since we have compared the keyboard to a typewriter, let us discuss how the keyboard causes the actual typing of characters to take place. The way it types is a clue to how it generates digital codes for input and types these codes for a teletypewriter or flexowriter.

The typewriter portion of our *typical keyboard* is not a conventional typewriter. Insted of a hammer (with a character on it) flying up and striking a ribbon, a ball (with many characters on it) rotates, tilts, and then strikes the ribbon when a key is depressed. Our typewriter, then, has the characters imprinted on a typehead ball, as illustrated in figure 2-24. This is the action that we want to discuss then: What causes the ball to rotate and tilt to a desired character, move forward, and strike the ribbon when a keyboard key is depressed? Now look at figure 2-25; it shows the typehead character arrangement of the typehead ball illustrated in figure 2-24.

Note that the typehead ball in figure 2-24 is divided into two character hemispheres: shift-up and shift-down. Now look at figure 2-25. It shows the character arrangement for the shift-down hemisphere of the typehead ball. In order to simplify this discussion, we'll use only characters in the shift-down hemisphere.

Character selection. From the typehead character arrangement in figure 2-25, it should be apparent that selection of a character is done by two different movements of the typehead: rotate and tilt. For example, to select the letter M, the typehead must be tilted one row and rotated two columns in the positive direction. This is expressed as tilt 1, rotate +2. All movements are with respect to the tilt 0, rotate 0 (home) position of the typehead. The typehead returns to this position after typing each character. For example, typing the word "ARE" causes the following actions to take place:

- Depress key A—Typehead tilts 1, rotates -5, moves forward to strike ribbon, moves back, and returns to home position.
- Depress key R—Typehead tilts 0, rotates -3, moves forward to strike ribbon, moves back, and returns to home position.
- Depress key E—Typehead tilts 1, rotates +1, moves forward to stike ribbon, moves back, and returns to home position.

Tilt and rotate mechanism. The typehead is tilted and rotated by gears, tapes, and pulleys. First, let us examine the tilt mechanism which is shown in figure

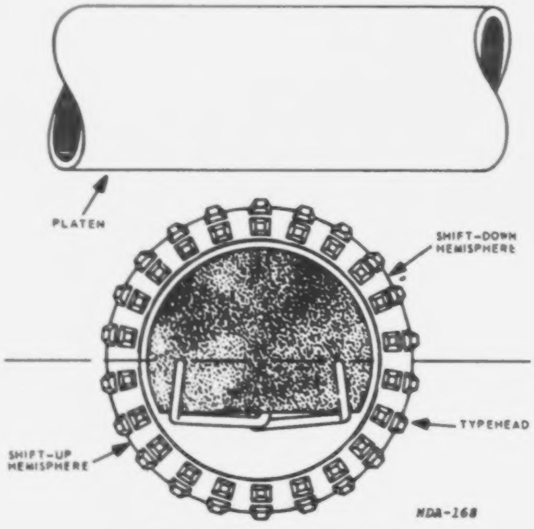
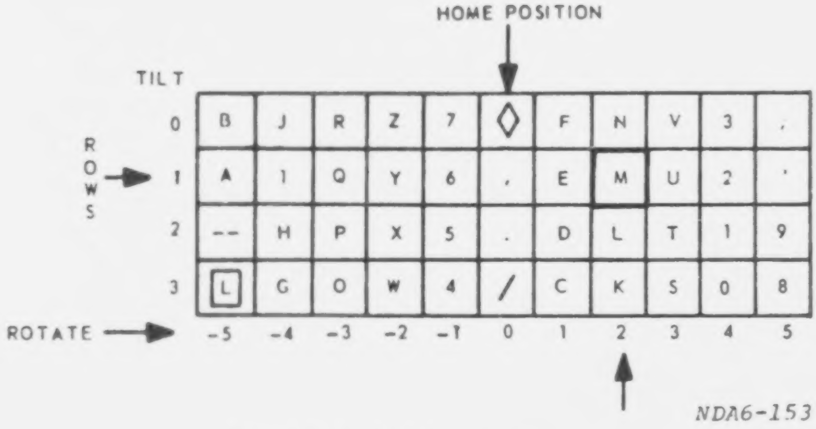


Figure 2-24. Typehead and platen.



TILT	-5	-4	-3	-2	-1	0	1	2	3	4	5
0	B	J	R	Z	7	◊	F	N	V	3	.
1	A	1	Q	Y	6	,	E	M	U	2	'
2	--	H	P	X	5	.	D	L	T	1	9
3	L	G	O	W	4	/	C	K	S	0	8

Figure 2-25. Typehead character arrangement.

2-26. The typehead fits over the upper ball socket. The typehead has been removed in the illustration in order to show the tilt mechanism. Rotating the tilt sector pulley rotates the bottom tilt sector gear. This rotating motion is translated into a tilting motion by the gears and causes the tilt ring and upper ball socket to tilt. Notice the arrows on the figure. Pulling the tape in the direction of the arrow causes the tilt ring to tilt up. Since the typehead is fastened to the ball sockets, the typehead tilts in the same direction as the tilt ring. When the tape is released, the spring pulls the pulley back to its original position, setting the typehead back to the 0-tilt position.

Now let us see how the typehead is rotated. Look at figure 2-27; it shows the upper ball socket connected to a rotate shaft. The two ball joints between the shaft and the upper ball socket allow the typehead to be moved in both the rotate and tilt directions. Notice that the rotate pulley is also moved by pulling on a tape attached to the pulley. Now that you understand that pulling on a tilt tape tilts the typehead and pulling on a rotate tape rotates the typehead, the next step is to take a look at the mechanical linkages that pull the tapes. We are progressing from the motion of the typehead to the motion of the typekey. This may seem like going backward, but it is the easiest way to see this action.

Tilt tape system. This system is shown in figure 2-28. One end of the tilt tape is fastened to the tilt sector pulley. The other end passes over a pulley on the tilt arm, over a fixed pulley, and then to a fastener. The tilt arm pivots at the bottom, and in doing so, it pulls the tape, rotating the tilt sector pulley. How much pull and how much the typehead tilts is controlled by two latches: tilt latch 1 and tilt latch 2. These tilt latches are, in effect, mechanical adders that have four positions: tilt position 0 through tilt position 3. The important thing to note here is that these four tilt positions correspond to the four rows of characters illustrated in figure 2-25.

Rotate tape system. This system is illustrated in figure 2-29. Again, a rotate arm is tilted by a mechanical linkage to position the rotate pulley. For our explanation, consider the right-hand pulley as fixed, since we stated earlier that for simplicity we would not discuss the shift-up. The rotate differential that tilts the left-hand pulley is shown in figure 2-30.

Because the rotate differential must position the typehead in 10 different positions other than 0 rotate (these positions correspond to the 11 columns shown in fig. 2-25), it has a more complicated linkage. Note that the latches are all at rest in figure 2-30. The latch labeled +1 is called the R1 latch, because it is selected by the R1 interposer selector lug illustrated in figure 2-31. When pushed down, it rotates the typehead to the +1 column. The latch labled +2 is the R2 latch; it causes the typehead to rotate to the +2 column. When both R1 and R2 are pushed down, the typehead rotates to the +3 column. Latch R2A (labeled +2A) is never used alone; it adds with R2 to provide +4 rotation. R2A, R2, and R1 add to provide +5 rotation.

The latch labeled -5 is called the R5 latch; it functions in conjunction with the R5 lug of the interposer. This latch only functions during negative rotate operation; that is, columns -5, -4, -3, -2, and -1 in figure 2-25. Combining the action of the -5 latch (fig. 2-30) with the

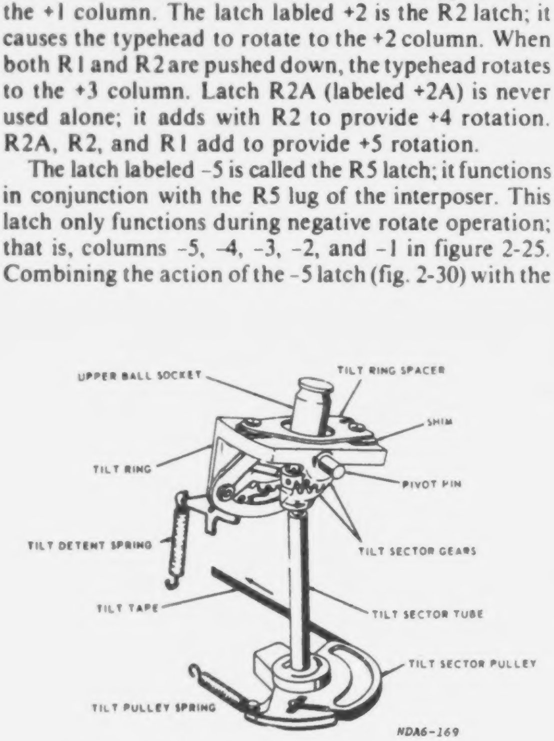


Figure 2-26. Rocker portion of tilt mechanism.

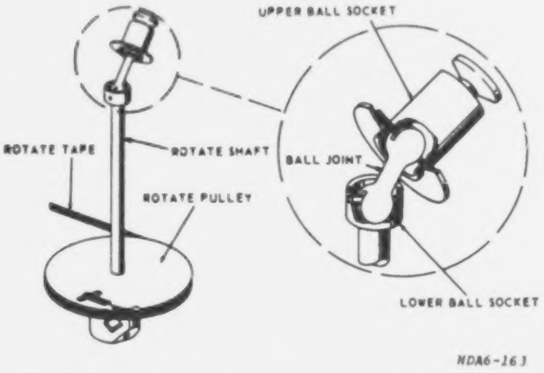


Figure 2-27. Rocker portion of rotate mechanism.

positive latches results in a negative rotate operation of the typeball. For example (refer to figs. 2-30 and 2-31):

Interposer Lug (Selector Latch)	=	*Typeball Rotation*
R5(-5)+R2(+2)+R2A(+2)	=	-1
R5(-5)+R2(+2)+R1(+1)	=	-2
R5(-5)+R2(+2)	=	-3
R5(-5)+R1(+1)	=	-4
R5(-5)	=	-5

Latch selection. Now we'll see how depressing a key selects the latches to be operated and at the same time generates a digital code. Figure 2-32 shows a key attached to its key lever pawl and its selective interposer mechanism. When the key is depressed, they key lever pawl strikes the selective interposer. This action causes the interposer to move down in front of the filter shaft. The large-cycle clutch-release lug of the interposer (fig. 2-30) releases a clutch that allows the filter shaft (fig. 2-31), which is geared to an electric motor, to rotate 180° and forces the interposer forward.

Note in figure 2-31 that there are seven lug positions on each interposer in addition to the clutch-release lug. A combination of these lugs determines the character to be printed and a particular code to be transmitted. Each key has its own selective interposer. When a key is depressed, the key lever pushes its selective interposer down so that each selector lug rests immediately behind the selector bail, as shown in figure 2-33. The cycle clutch is released, the filter shaft rotates, and the selector bails that are contacted are forced forward to engage the latch interposers. The latch interposers move forward, pulling the selector latches back.

Look at figure 2-34 and note the latch bail. The same mechanism (cycle clutch bail) that allows the filter shaft to rotate causes a drowned movement of this latch bail. If a selector latch is *selected*, it is pulled back; and, as the latch bail moves down, it *doesn't* make contact with the contact actuator. Therefore, the normally closed (NC) contact points associated with that particular selector latch remain closed. If a selector latch is *not selected*, it is not pulled back; and, as a result, the following actions occur:

- The latch bail pulls down on the selector latch.
- The selector latch extension moves down.
- The contact actuator arm moves down.
- The contact actuator crossbars open the NC contacts.
- When the selector latch bail restores, the contact actuator rises under the spring tension of the opened contacts.

The above action is true for all the selector lugs on each interposer (fig. 2-31) except lug R5 (-5 rotate). Its point contacts are normally opened (NO) and

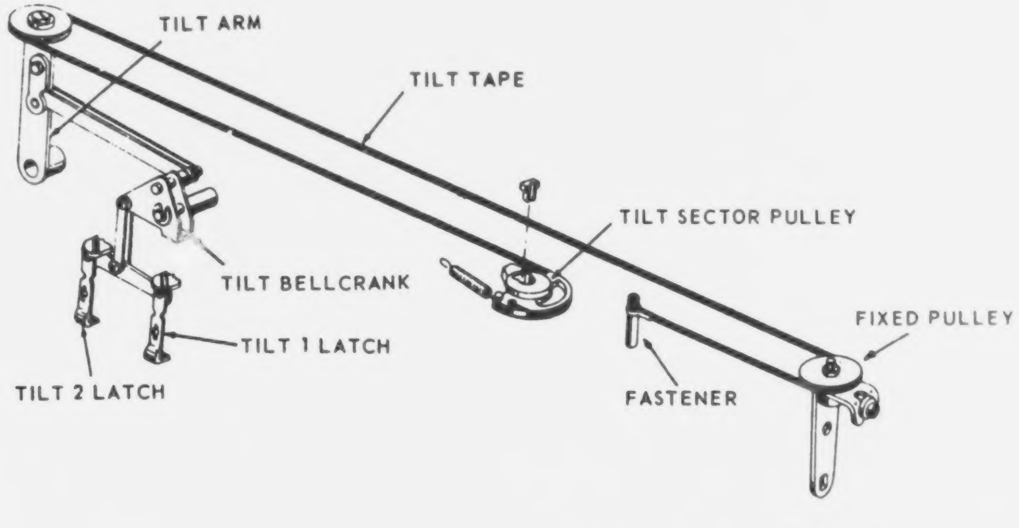


Figure 2-28. Tilt tape system.

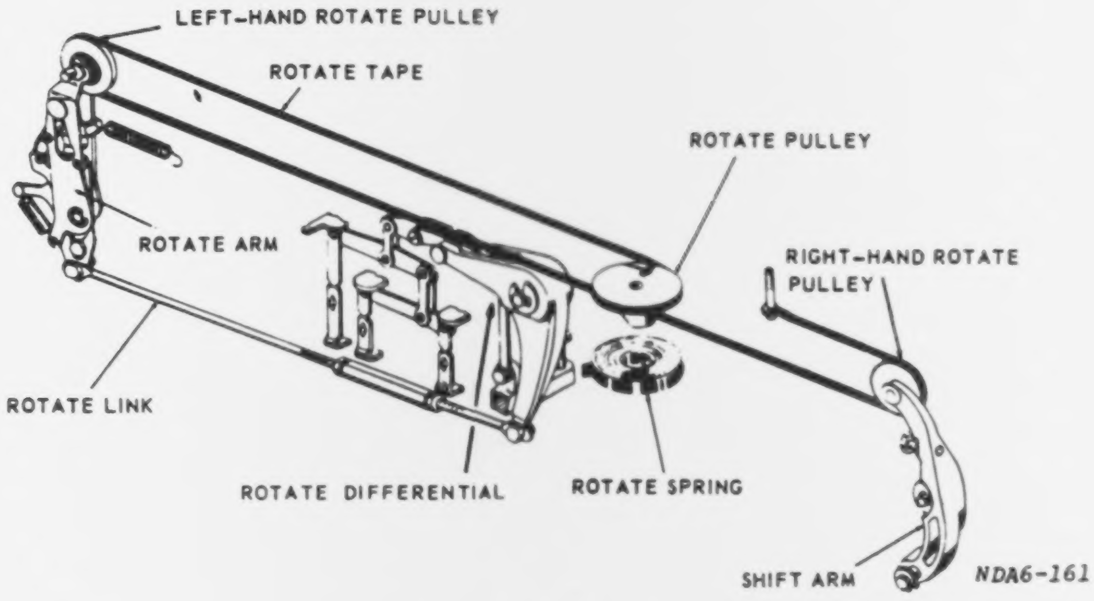


Figure 2-29. Rotate tape system.

remain opened for all positive (including 0) column rotate positions. These were illustrated in figure 2-25. When a negative column rotate position is required, the R5 contacts are closed.

Let us tie together the mechanical rotate-tilt mechanism, the latch selection, and the binary field data code associated with our typical keyboard. Figure 2-35 is a simplified schematic of switches associated with the field data code. These switches are arranged in the order of the field data code excluding the control bit (D6) and the parity bit (D7). Negative logic levels of -12V (logic 1) and 0V (logic 0) are used for our explanation. Notice that each data bit (D0 through D5) is controlled by the operation of interposer lugs T1, T2, R5, R1, R2, and R2A. Recall that these lugs control the operation of corresponding selector latches as explained above. Now refer to figure 2-25 and locate the letter A; it is selected by rotating the typehead -5 units and tilting it 1 unit. To obtain this mechanical movement, the following latches must be selected:

Rotate latches:				
	R2A	R2	R1	R5
Rotation	0	0	0	-5

Tilt latches:		
Tilt	T2	T1
	0	1

Notice in figure 2-35 that the following contacts are transferred by its associated latch.

Contacts:	D5	D4	D3	D2	D1	D0
Transferred:	yes	yes	yes	yes	yes	no
Voltage:	0V	0V	0V	-12V	-12V	0V
Binary:	0	0	0	1	1	0

The resultant field code for character A is $000110_{(2)}$, which is equal to $06_{(8)}$.

Exercises (015):

1. What type of device (input or output) is a keyboard?

2. How is a character selected for typing on a typehead ball?

3. Refer to figure 2-25. Describe the different positions of the typehead ball when the word "AND" is typed.

4. Describe the difference between the D6 bit and D7 bit used in the field data code.

5. What code is used in the ROM of many keyboards?

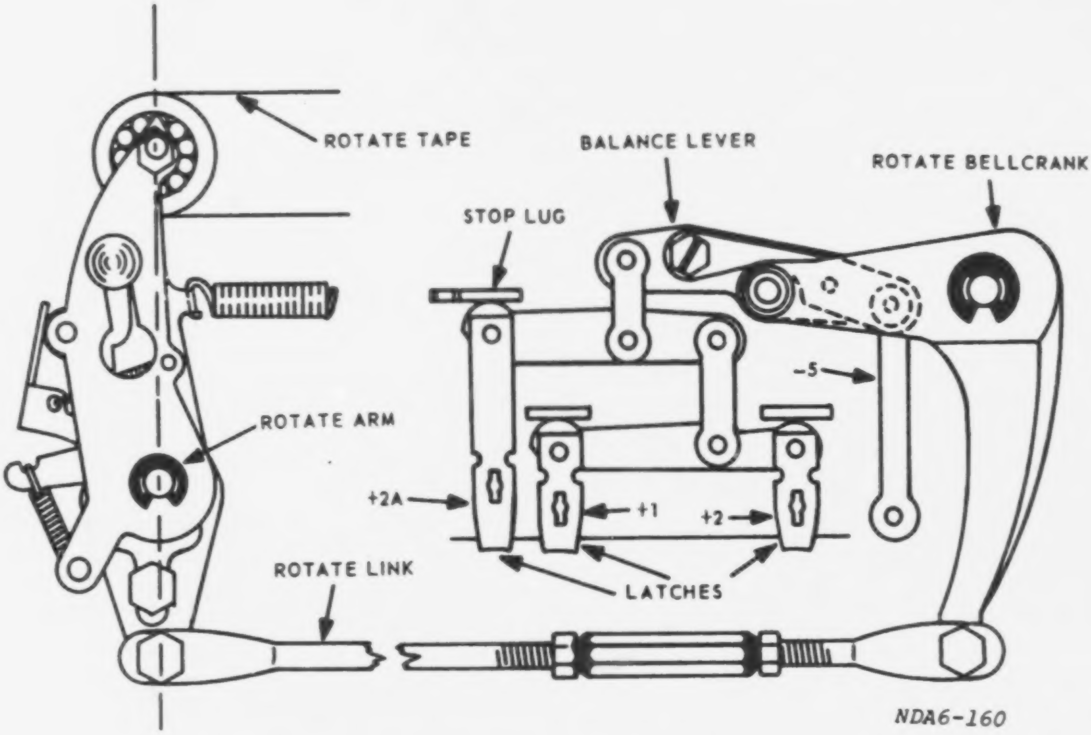


Figure 2-30. Rotate differential at rest.

6. How many character hemispheres are there on the printer typehead ball?

7. What is all character selection with reference to on the typehead ball?

016. Specify the characteristics of the impact and electrographic printers.

Printers. Printers provide another means of outputting data from a computer. Data from the computer system is provided in permanent visual records, at rates ranging from a few characters to several hundred characters per second. As output units, printing devices receive data from the computer system in symbolized electronic form. Once these electronic signals enter the appropriate circuits and actuate the printing elements, printing takes place. The two types of printers discussed here include the impact and electrographic printer.

Impact Printer. The impact printer (sometimes referred to as a line printer) is an outgrowth of the typewriter. The term "line" designates that the printer is capable of printing a line of characters at a time. Impact printers vary in speed of printout from about 100 lines per minute to over 1000 lines per minute. The number of characters per line also varies from one type of impact printer to another.

Mechanical description. The mechanical parts that do the work of printing in a typical line printer are shown in figure 2-36. The printing operation is accomplished by the print hammer striking the paper-and-ink ribbon against a raised character on the print wheel, thereby impressing the character on paper in the same manner as on a typewriter. An advantage of this type of printing is that multiple carbon copies may be produced.

The hammers are mounted in modules. A typical impact printer has four hammers per module. There is a print hammer for each vertical column of print; or, to put it another way, there is a hammer for each possible character in a line of print. Each hammer has its own driving electromagnet which is activated with an electrical pulse.

The print roll consists of a number of individual wheels (as many as 120) mounted on a common shaft. Each of these print wheels has raised chraracters around its outer edge, as shown on the insert of figure 2-36. When these print wheels are mounted to form the full print roll, all like characters are aligned with a selected notch on a timing disk. These notches cause

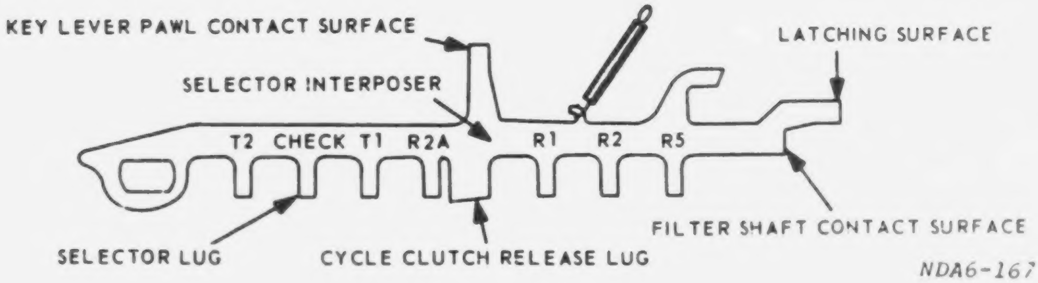


Figure 2-31. Interposer.

electrical pulses to be generated as they pass the pole pieces of a magnet. Since each pulse represents a certain character, this disk is called the *character pulse generator*. Its function is to identify the row of a character. A second disk with a single notch is provided to identify the first character on the roll.

The print roll is driven directly by a motor. Speeds up to 2000 rpm have been attained; however, 1000 rpm is a more common operating speed. It is not always possible to print a line per revolution of the print wheel due to delays in feeding paper, but speeds of 1800 lines per minute have been attained.

Electrical circuits. The electrical circuits of major importance in the printing cycle are listed and discussed below. These circuits are shown in block form in figure 2-36.

- Synchronizing pulse generator.
- Character generator.
- Electronic distributor.
- Storage matrix.
- Hammer drivers.

The function of the *synchronizing pulse generator* is to produce pulses that are synchonized to the rows of characters on the print roll and identify these characters. The index pulse identifies the No. 1 character on the print roll by resetting a counter in the electronic distributor to 0.

The *character generator* simply produces a pulse stream at the rate of one pulse per character row on the print roll. When the No. 1 (first) character row on the print roll passes under the print hammers, the first character pulse after the index pulse is generated; the No. 2 is under the print hammer at the generation of character pulse 2; row 3 matches pulse 3, etc., through pulse 165. This series of character pulses is called the *character pulse stream*. The character pulse sequence is repeated as the print roll makes each revolution.

The *electronic distributor* accomplishes several functions. Its primary function during the print cycle is to channel each individual pulse of the pulse stream into separate lines that connect to the storage matrix in accordance with the number of the pulse (with reference to the index pulse). Also, it is the circuit that recognizes the index pulse and is reset by it.

Upon identifying the first pulse, the distributor does two things: (1) it selects a line to the storage matrix that corresponds to row 1 on the print roll, and (2) it sends an electric pulse through this line to the storage matrix. When the second pulse is detected, the distributor selects a second line and pulses it—the No. 3 pulse is channeled through a third line. Thus, each character pulse is sent to the storage matrix on a separate line, and each of the lines is pulsed as a corresponding character row passes under the print hammers. Each line, therefore, represents a separate character.

After all characters in a line are printed (end of print cycle), the paper must be moved up one space for the next line of print. It is then ready to begin another

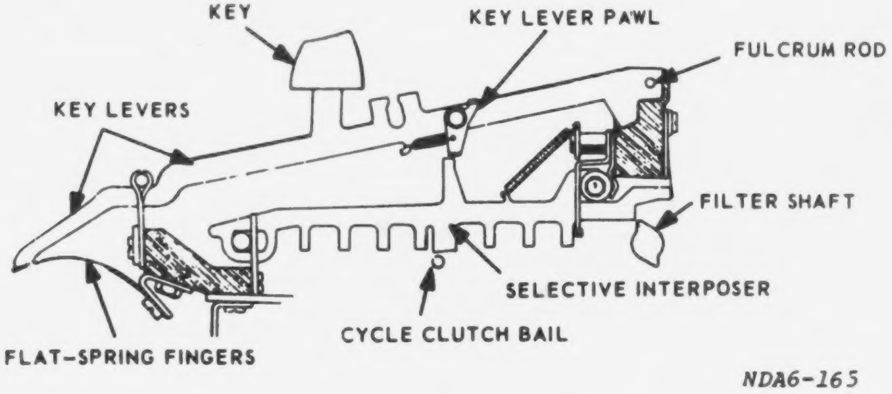


Figure 2-32. Key and interposer mechanism.

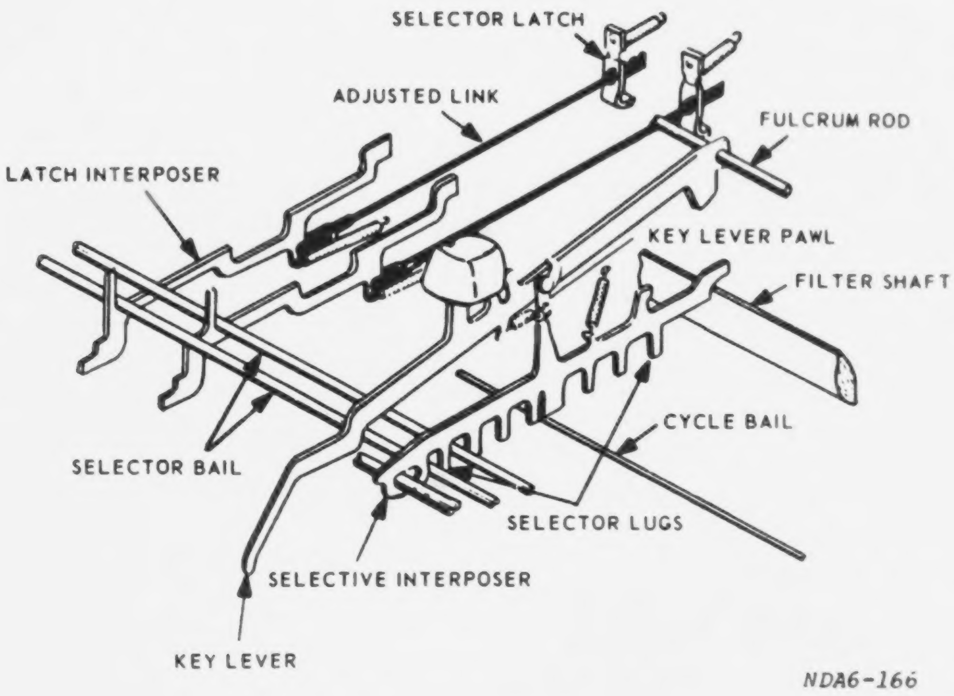

SELECTOR LATCH
ADJUSTED LINK
FULCRUM ROD
LATCH INTERPOSER
KEY LEVER PAWL
FILTER SHAFT
CYCLE BAIL
SELECTOR BAIL
SELECTOR LUGS
SELECTIVE INTERPOSER
KEY LEVER
NDA6-166

Figure 2-33. Selection.

print cycle. An additional function of the electronic distributor is to produce the pulse that initiates the paper-feed mechanism.

It is important for you to remember the following: The electronic distributor receives the character pulse stream; it uses these pulses to enerize specific lines in accordance with the character row count; then, at the end of the print cycle, produces a pulse that triggers the paper-feed mechanism.

The *storage matrix* serves as a data storage buffer and hammer trigger pulse generator. Data from an external register is stored in this matrix at desired locations. For example, let us assume that AN is the first word in the line to be printed; also, that row 1 on the print roll is all N's and row 2 is all A's. We use this example to point out that the characters need not be in alphabetical and/or numerical order.

For the letter A, the computer would write a binary 1 in the storage matrix at the intersection of the column 1 line and row 2. For the letter N, it would write a binary 1 at the intersection of the column 2 line and row 1. Nothing would be written in any of the rows for column 3 since it is to be a space. All of the other words would be written in the storage matrix in this manner.

The matrix enters into the printing process as follows: When the No. 1 row of characters (N's) is about to pass under the print hammers, the first pulse of the print cycle (T1) is received from the signal distributor on line 1. The T1 pulse simultaneously reads all N characters for all words of the line being printed. It is the function of the storage matrix during T1 pulse time to produce an output hammer trigger pulse for all columns that have a binary 1 written into the N's row. In our example, the N (column 2) of the word "AN," therefore, would be written during the T1 pulse. The A (column 1) will be printed during the second pulse (T2), along with all other A's that appear in the line. Column 3 has no data written in it, since it is to be a space; therefore, no print hammer trigger pulse is generated from the storage matrix for this column. As the print cycle progresses, all characters

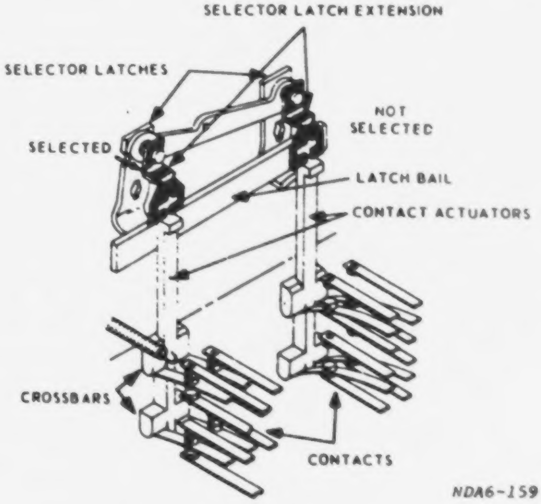

SELECTOR LATCH EXTENSION
SELECTOR LATCHES
NOT SELECTED
SELECTED
LATCH BAIL
CONTACT ACTUATORS
CROSSBARS
CONTACTS
NDA6-159

Figure 2-34. Control actuator.

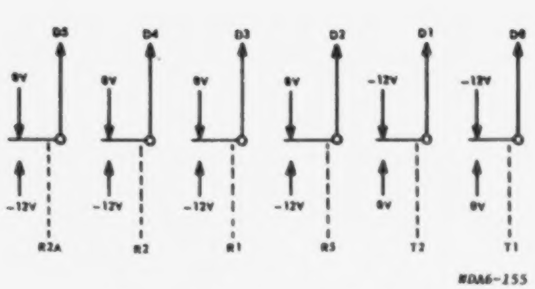

D5
D4
D3
D2
D1
D0
0V
-12V
R2A
R2
R1
R5
T2
T1
#DA6-155

Figure 2-35. Digital coding switches.

and spaces are printed in this manner until the print cycle is completed.

The pulses from the storage matrix are not of the proper power and shape to drive the hammers; therefore, they are shaped and amplified in the print *hammer driver circuits.* A power driver and shaper is provided for each hammer.

Mechanical action of printing. The method of printing discussed here is referred to in some textbooks as printing "on-the-fly," because the print roll does not stop as the print hammer strikes. The hammer must strike quickly (with a short dwell time) so that the character is not smudged by the raised character on the print wheel as it passes.

Adjustments are built into each hammer circuit for individual adjustment of the darkness of the printed character. All hammers are adjusted for the same force of print. Also, there is a line adjustment for setting the darkness of the print for the full line.

A high-speed line printer with the cabinet doors removed is shown in figure 2-37. The paper is stored in the bin below the print roll. During printing, the paper passes through the printer and onto a shelf behind the machine. The modules that make up part of the electrical circuits, including the matrix, are shown at the right of the figure.

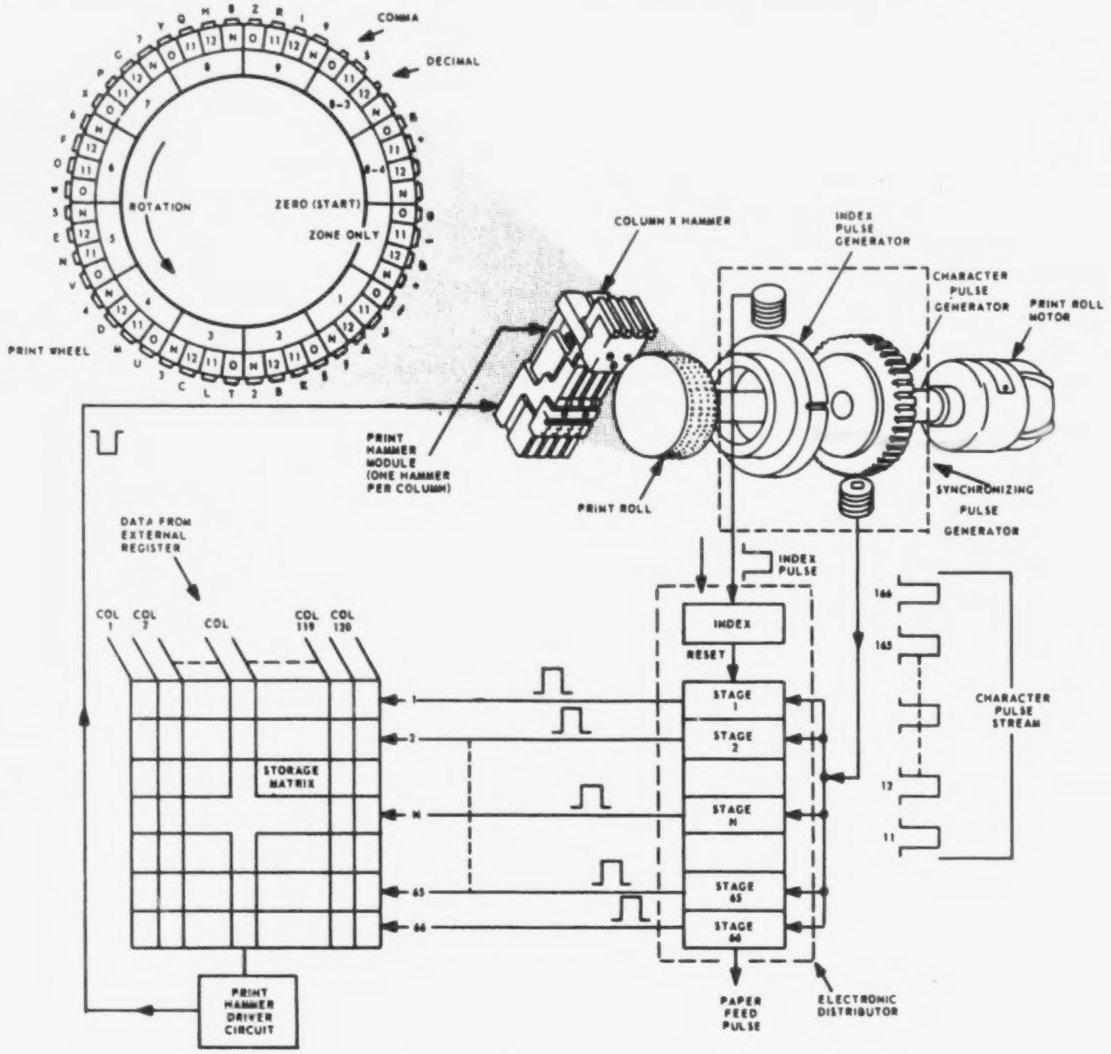

COMMA
DECIMAL
ROTATION
ZERO (START)
ZONE ONLY
PRINT WHEEL
COLUMN X HAMMER
INDEX PULSE GENERATOR
CHARACTER PULSE GENERATOR
PRINT ROLL MOTOR
PRINT HAMMER MODULE (ONE HAMMER PER COLUMN)
PRINT ROLL
SYNCHRONIZING PULSE GENERATOR
INDEX PULSE
DATA FROM EXTERNAL REGISTER
COL 1
COL 2
COL
COL 119
COL 120
STORAGE MATRIX
INDEX
RESET
STAGE 1
STAGE 2
STAGE N
STAGE 65
STAGE 66
1
2
N
65
66
166
165
12
11
CHARACTER PULSE STREAM
PAPER FEED PULSE
ELECTRONIC DISTRIBUTOR
PRINT HAMMER DRIVER CIRCUIT

Figure 2-36. Impact printer diagram.

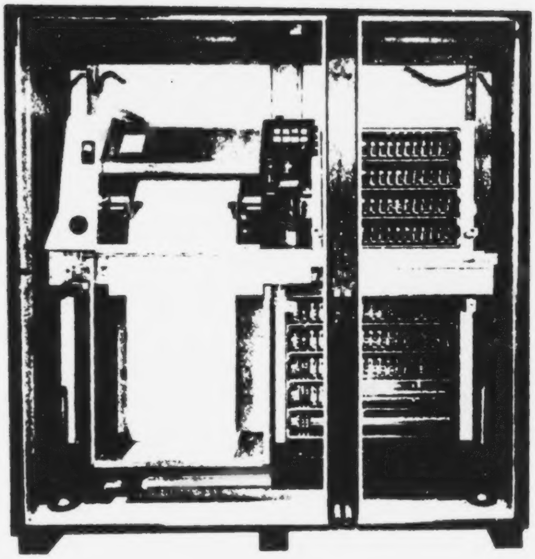


Figure 2-37. Impact printer.

Electrographic Printer. In some ways the electrographic printer is similar to the usual typewriter or printer, but in other respects it is quite different. Its description here emphasizes how it differs.

Character format. The electrographic printer is sometimes referred to as the wire matrix burn printer, because it burns the imprint of a wire matrix character onto a specially prepared paper. Upon close inspection, the printed character looks like a group of dots. Figure 2-38,A, shows an example of two such characters, an E and an M. Of course, the actual print is smaller than shown in the figure. If every dot of the print code were printed, it would appear as shown in figure 2-38,B. Looking at figure 2-38,B, observe that the dots are arranged in five columns and seven rows to form a 5 by 7 matrix. By proper selection of dots in this matrix, any desired character can be printed.

Print heads. Messages are printed a character at a time on continuously moving electrosensitive paper by three continuously moving print heads, shown in figure 2-39. The print heads are transported on a belt which is skewed (slanted) at an angle so that the print head rises as it travels across the page. The rate of rise of the print head is the same as that of the paper. These actions result in parallel, horizontal lines of print. As one print head completes a line, the following head on the belt is drawn into position to start the next line. Since there are three print heads on the belt, a given head prints every third line.

Each print head, as shown in figure 2-40, contains seven styluses arranged vertically. These styluses make electrical contact to the print amplifiers through "fingers" which slide along a commutator. The dots which make up a character are formed by burning away a thin white coating on the surface of the electrosensitive paper, exposing a black underlayer. The styluses print the selected dots a column at a time. As the print head moves across the page, additional columns are printed until a total of five columns has been used to complete a character. A one-column letterspace is left between characters (see insert on fig. 2-39).

Exercises (016):

1. Sometimes the impact printer is referred to as a line printer. What does the term "line" mean?

2. Describe the function of the synchronizing pulse generator that is used in the impact printer.

3. What is another name for the electrographic printer, and why was it given this name?

4. What is the primary function of the electronic distributor during the print cycle?

5. How often is the entire print cycle accomplished with the impact printer?

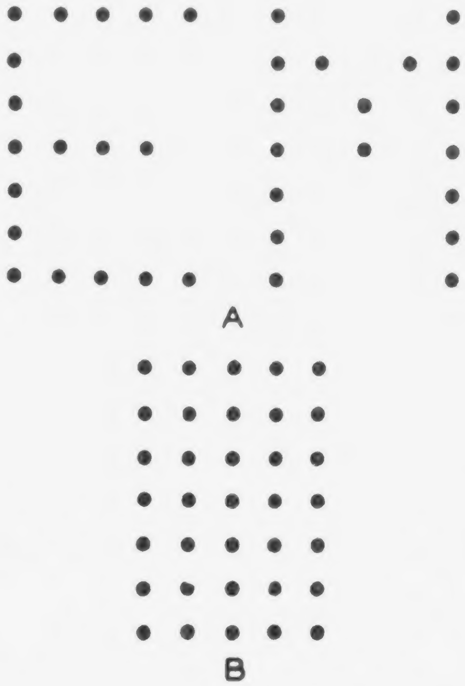


Figure 2-38. Dot matrix character format.

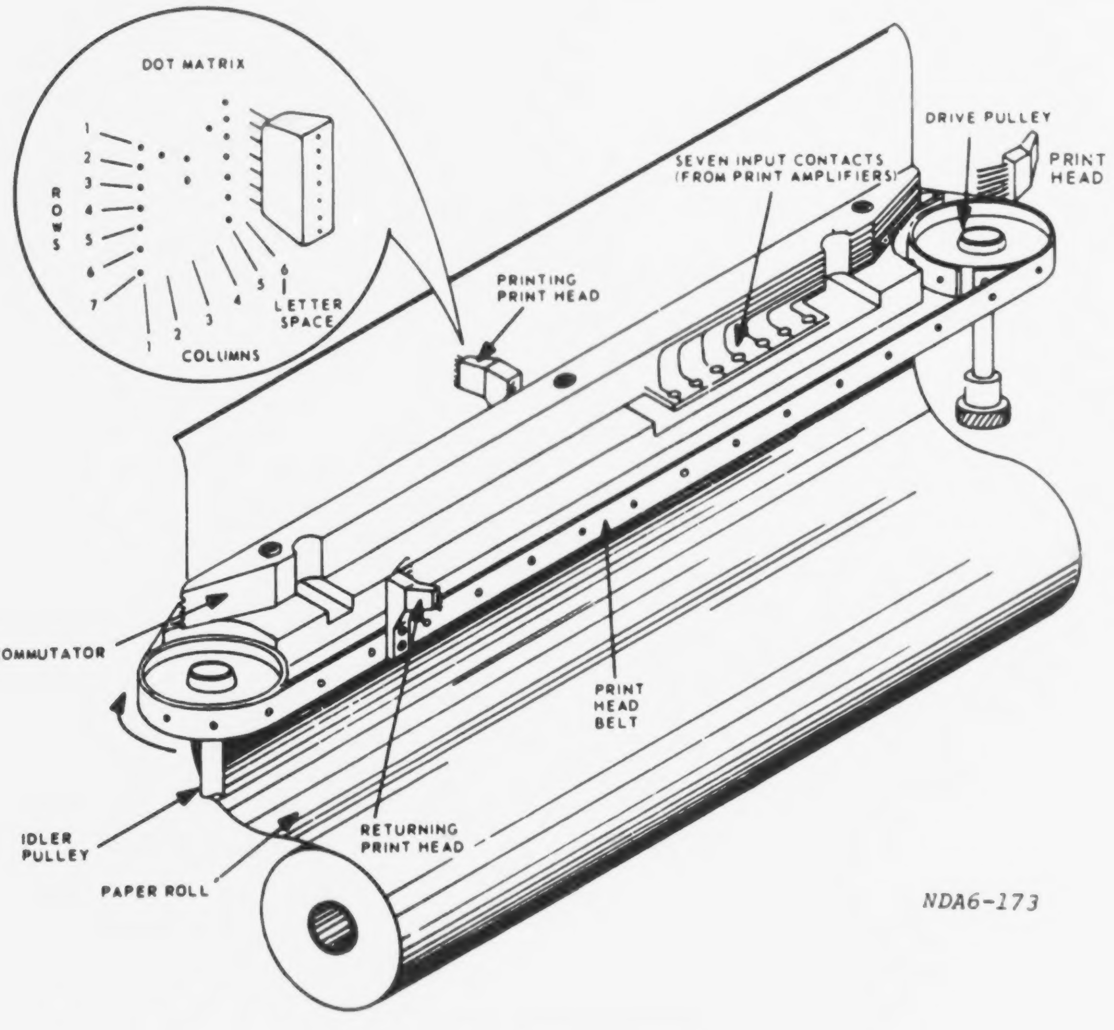

DOT MATRIX
1
2
3
4
5
6
7
ROWS
1
2
3
4
5
6
COLUMNS
LETTER SPACE
PRINTING PRINT HEAD
SEVEN INPUT CONTACTS (FROM PRINT AMPLIFIERS)
DRIVE PULLEY
PRINT HEAD
COMMUTATOR
PRINT HEAD BELT
IDLER PULLEY
RETURNING PRINT HEAD
PAPER ROLL
NDA6-173

Figure 2-39. Electrographic printer.

6. On the impact printer, what produces the pulse that initiates paper feed?

017. Specify characteristics that define the use and operation of visual displays, modems, plotters, and other peripheral devices.

Visual Displays. A visual display in its simplest form may be nothing more than a series of lamp or light emitter diode (LED) indicators. More often than not, the most common visual displays use the cathode ray tube (CRT) as the display element. The display and its electronics are usually referred to as a CRT terminal. A keyboard is, in many cases, used in conjunction with the terminal or is an integral part of it. The keyboard is used to direct the operations of the terminal.

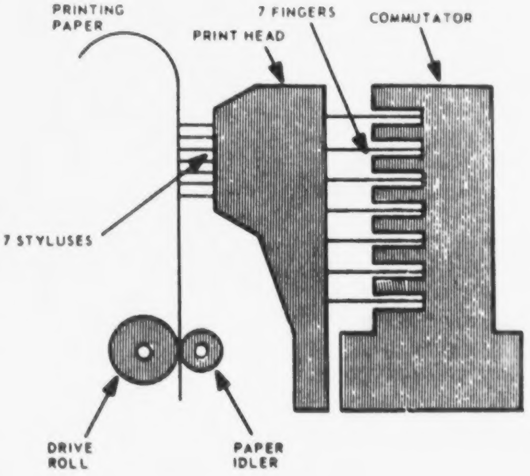

PRINTING PAPER
7 FINGERS
COMMUTATOR
PRINT HEAD
7 STYLUSES
DRIVE ROLL
PAPER IDLER

Figure 2-40. Print head.

Another type of visual display device is the *plasma display* terminal. It is similar in operation to the CRT terminal but uses a unique display element. The actual indicating element is called a *plasma panel.* The panel consists of two plates of glass separated and parallel to each other with the intervening space filled with a neon and argon gas mixture. There are 512 fine wire electrodes etched on the inside of each glass plate. The glass plates are then oriented so that the 512 electrodes on each are at right angles to each other. This creates a 512 by 512 matrix which provides a total of 262,144 addressable locations in the panel. By addressing one of these locations and applying a voltage pulse, the gas at that location is ignited and that *one* point glows. By using a constant sustaining voltage on all the electrodes, once a location on the matrix has been fired, it will remain lit. To extinguish a particular location or locations, address the location(s) and pulse the sustaining voltage to 0.

The plasma display is very bright and readable. It can display a wide variety of graphics and alphanumerics. Because the panel is transparent, maps or graphics can be projected from the rear of the panel. Therefore, the panel can serve two purposes at the same time. The color of the display is orange or green. The plasma terminal requires only 300 volts DC or less to operate the panel. This makes the terminal ideal for airborne environments.

CRT Terminals. A typical CRT terminal is depicted in figure 2-41. The CRTs used in a terminal can be one of two types. These are the standard television-type CRT and the *storage* CRT. The display on the standard CRT must be refreshed periodically because unless you continually send information to be displayed, the display fades. A storage tube eliminates this problem, using a secondary electron emission technique in the tube. Displays on the storage tube will remain for hours without information continuously being sent to the CRT. The only time you need send new data is if you want to change information on the display or you want completely new information to be displayed.

Some cathode ray tubes are special-purpose tubes with provisions for writing alphabetic characters. Figure 2-42 shows a simplified diagram of a sample display tube. Writing on the viewing screen is done by forming a character and positioning the character on the tube face. Characters may be generated by a stenciling process; that is, the electron beam is directed through a selected aperture in a character-forming matrix and directed by electrostatic deflection plates to a selected position on the tube face. The face of CRTs is phosphor coated. The phosphor emits light when struck by the electron beam coming from the cathode. The light generated by the coating persists long enough for human perception. The length of time the phosphor remains lit is dependent on the type of phosphor used.

Information in binary-coded pulse form is transmitted from the storage element of the computer or from the input system to the display equipment. There it is converted to analog deflection voltages which generate the desired visual display. Since the information on the tube face does not persist for a long period of time, it is sometimes desirable to record this information in a more permanent form. Camera systems are available which automatically photograph the display tube face and process the film to provide a positive transparency.

Categories of Terminals. Terminals are usually classified as *dumb, smart* or *intelligent*, depending upon their capability. Newer terminals are controlled by microprocessors and contain memory elements. Keyboards are usually a part of all terminals and, depending on how the terminal is classified, can be used for a number of functions.

A dumb terminal has little capability except to display data coming from the computer. It may be referred to as a monitor, and the keyboard used with it does nothing more than act as source of input data for the computer. This type of terminal is the least expensive.

The smart terminal usually has some form of internal memory. It also has a cursor, which is a line or mark of some kind which is used to change selected information on the display. With the cursor we can add, change, or delete information from the screen of the display. The keyboard of this type of terminal can interact with both the computer and the CRT terminal.

The intelligent terminal can be programmed and has most of the capabilities of a microcomputer. Many data handling functions can be done by this terminal which were formerly done by the host computer. A disk or tape may also be part of this terminal for additional data storage. The keyboard is used for programming the terminal, data input for the terminal and computer, and for editing display information.

Modems. The term "modem" is a contraction of *modulator-demodulator*. In a modem, the modulator-demodulator circuits are both on the same chassis using some common circuitry. A modem converts the signals coming from a CRT terminal or other peripheral, and/or the computer, into a form suitable for transmission over phone lines. The modem also changes data coming from a phone line into a form usable by the computer.

The modem is essentially an analog-to-digital converter. Because of the high bandwidth requirements of a digital signal, serious deterioration of this signal occurs in a transmission line. By converting the digital signal to an analog form and converting it back to digital for the computer, the reliability of the data is preserved.

The term "data set" is often used instead of modem. However, data sets do additional operations such as dialing, control, automatic calling, automatic answering, and answer back. The line speed rate of modems is currently 1200 bauds. This indicates that the modem transfers data at the rate of 1200 bits per second (b/s).

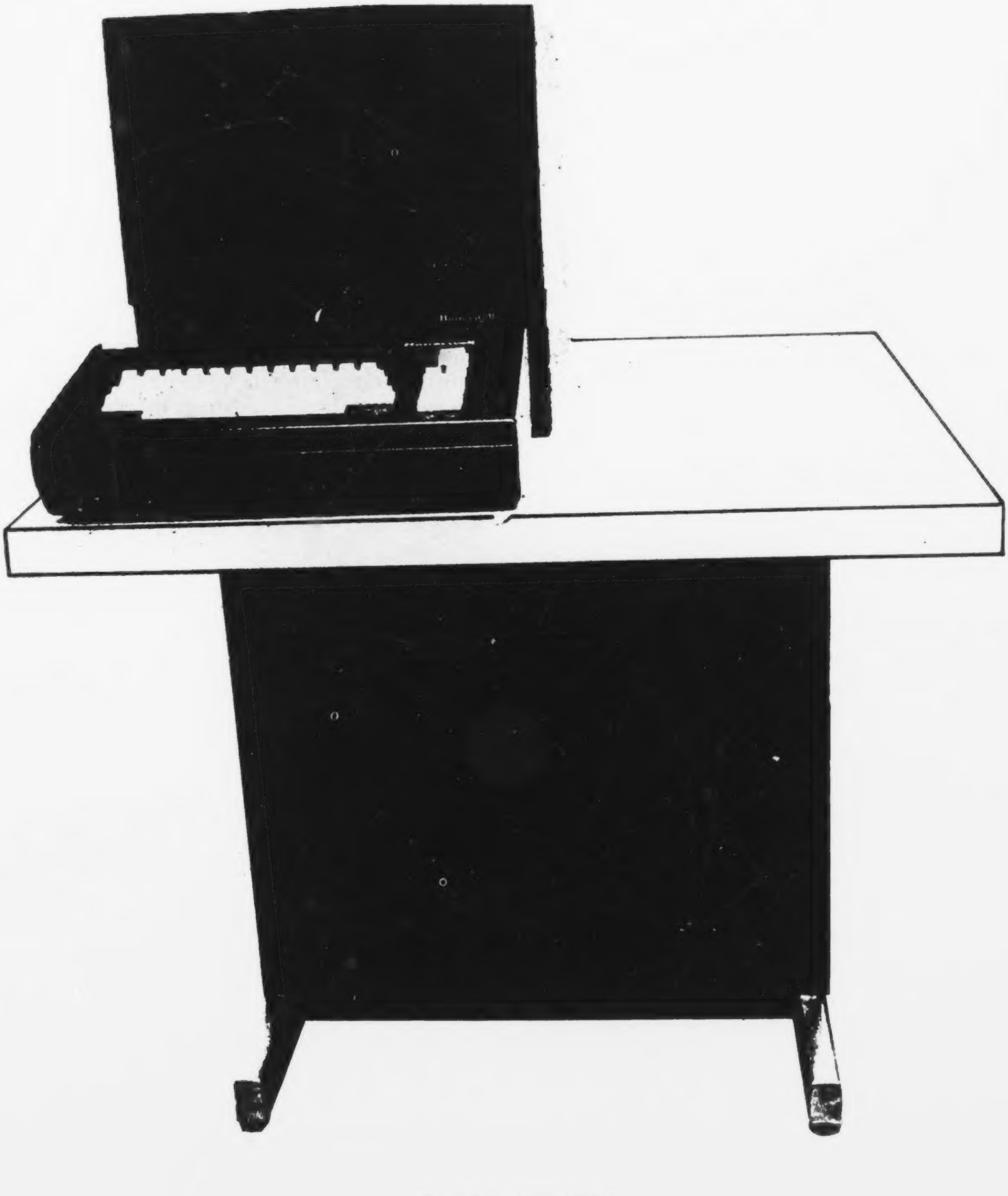


Figure 2-41. Visual display.

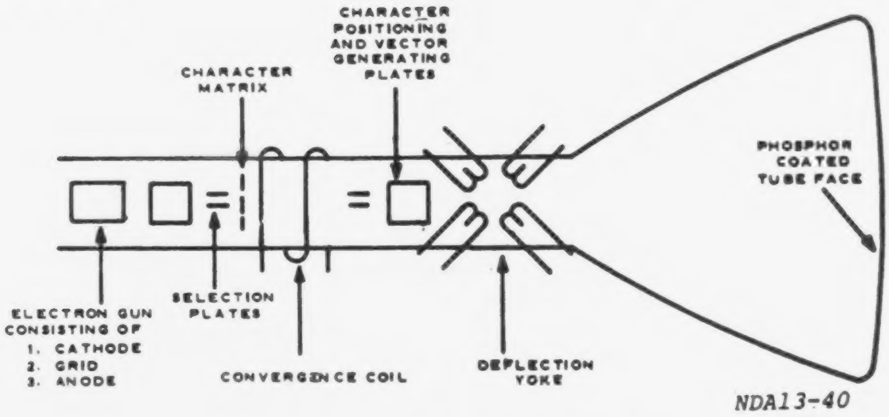

CHARACTER POSITIONING AND VECTOR GENERATING PLATES
CHARACTER MATRIX
PHOSPHOR COATED TUBE FACE
ELECTRON GUN CONSISTING OF
1. CATHODE
2. GRID
3. ANODE
SELECTION PLATES
CONVERGENCE COIL
DEFLECTION YOKE
NDA13-40

Figure 2-42. Simplified display tube.

Plotters. A plotter is another hard-copy peripheral, similar to the printer, but the plotter produces *graphic* data on paper. A plotter can be used to graphically show information such as radar, target, or map data. As the paper moves through a plotter, fixed or movable pens (styluses) draw a picture using the data received from the computer.

Plotters may use moving pens, in which case the speed of the pens will determine how fast the device will plot. In the fixed styluses' plotter, the speed of the paper moving past the styluses will determine how fast the plotting operation will be. Of course, using many fixed styluses, spaced closely, the accuracy of the plotter is better. After all, you can only have so many moving pens covering the plotting paper before they start running into each other.

Because of the similarity in function and operation, newer plotters have a printer as well. These plotter-printers are peripheral devices which can produce printed and graphical data—all in one unit!

Projection Displays. Whenever large visual displays are needed, projection systems are used. One such system photographs a special CRT on movie film. The film is rapidly processed, and then it is projected on a screen of any desired size. Another system uses a photo process involving plates and projectors; either of these systems can be made to give color as well as black and white. They do cause some delay, which is less than 1 minute in some types. Indications are that projection systems can be produced which exceed the recognition speed of the human eye.

Other Input/Output Devices. The input/output devices we have discussed so far are commonly identified with general-purpose digital computers. Possible types of I/O devices associated with special-purpose computers are limited only by the capability of any device to transmit and to receive information in a form that can be converted for use in a digital computer.

The choice of an I/O device to be used with a special-purpose computer will depend on the sources of information needed to solve specific problems. These sources are sometimes called data links. The digital computer is not restricted to accepting information only from tapes, cards, or keyboards. Any data from any source can be used as long as the data is changed into the binary code of pulse-no-pulse.

Information can be transmitted and received from teletype machines, telemetering devices, analog computers, the human voice, telephone lines, and radio. These devices may be linked directly to the computer.

Exercises (017):

1. How do we erase a particular location on the plasma panel matrix?

2. What two purposes can a plasma display terminal satisfy?

3. Name the two types of CRTs used most often in CRT displays.

4. How does one type of CRT eliminate the refresh requirement?

5. How is the electron beam positioned on the CRT face?

6. What type of visual display terminal is nothing more then a television monitor?

7. What type of visual display technique can be used when we need a very large display?

8. Name the categories of CRT terminals.

9. What is a modem, and what is another name for it?

10. What is a plotter?

11. What determines the choice of I/O device to be used in a special-purpose computer system?

CHAPTER 3

Storage Media

THE STORAGE MEDIA used in a computer system can be divided into two categories. First is the *internal* storage media used by a digital computer for storing data and instructions which must be processed. Second, a large storage area is needed *external* to the computer to serve as an auxiliary storage. With the tremendous amounts of information that a computer needs for its many functions, it becomes too expensive to store all the data required in a random access fast main memory.

The primary internal storage medium, used at present for main memory, is the magnetic core. Magnetic cores are expensive, and therefore semiconductor/solid-state memories are used in addition to cores in many newer computers. Another memory type in use in some computers is the thin film memory. On the horizon, and already in use in some applications, is a new technology, bubble memories.

Mass storage of data in external media is performed primarily by magnetic drums, tapes, and disks. Some external storage may also be done by solid-state memories located in a peripheral device such as an intelligent terminal.

3-1. Storage System Theory

This chapter explores the various types of internal and external storage media used in modern-day computer systems. In order to do this, we must first ask what makes up a storage system and what requirements must be met by a system in order to store digital data.

018. Specify the characteristics and requirements of a storage system.

Storage Systems. The block diagram of a typical storage system is shown in figure 3-1. This diagram represents either an internal or external storage system. The *storage* unit may be magnetic core, a disk, or some other storage medium. The *storage control unit*, also called a device *controller* for a peripheral, may be a separate unit from the medium; or it could be an integral part of the storage unit. Newer device controllers are microprocessor controlled, while others use discrete logic or integrated circuits.

The alternate data path represents a function such as direct memory access (DMA) used in some computer systems. DMA permits a very fast direct transfer of data and instructions between a storage medium such as a disk and main CPU memory. If the data from the storage unit must be processed by the CPU before it is stored, then a transfer through the controller occurs.

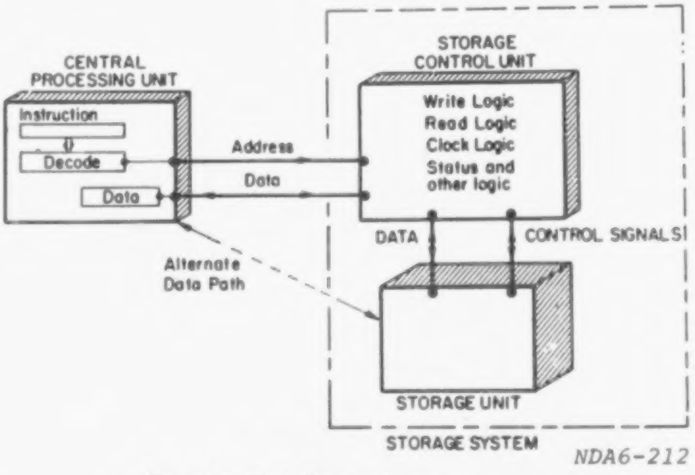


Figure 3-1. Block diagram of a storage system.

Several requirements must be met in order for a storage system to perform as such. The following information on storage system requirements is taken from the book, *Computer Storage Systems and Technology,* by Richard Matick.

> . . . all memory systems must be able to store information and, subsequently, find and retrieve it, all on command from the CPU. To achieve this, a storage system must have the following basic requirements:
>
> 1. Medium for storing energy.
> 2. Energy source for writing the information - that is, "write" transducers (word and bit).
> 3. Energy sources and sensors to read - that is, read and sense transducers.
> 4. Information addressing capability - that is, address selection mechanism for reading and writing.

All storage systems are alike in their need for a medium. The use of magnetic cores, a magnetic disk or tape, or an electronic circuit such as a flip-flop, all serve as a form of storage medium. The last three requirements will be met differently, depending on whether a system uses random or nonrandom access.

A transducer is defined as some device which will translate a signal from one system or medium into a form required by another system or medium. One form of transducer familiar to everybody is the loudspeaker. It transforms electrical energy into its acoustical equivalent. In a computer system, a magnetic tape unit uses a magnetic read/write head as its transducer. The read and write transducers may be separate units, as are the ones in a magnetic core memory, or in one device such as the tape head.

Addressing for a storage unit is determined by its type of access. Each memory location in a magnetic core storage unit has an address selection circuit. In a sequential access unit such as magnetic tape, addressing must be done through a controller using some form of media/transducer interaction. It takes longer to address this way, but the cost per bit to retrieve data is much lower than with a direct-wired or random access memory.

Exercises (018):

1. What are the two components of a storage system?

2. How can we get a faster transfer of data from or to a storage system and the computer?

3. What are the four requirements that must be met by all storage systems?

4. Why is a magnetic disk storage unit cheaper for storing digital data than a random access memory unit?

5. What is one form of a storage medium which requires an address selection path for each bit of data stored?

019. Identify basic components of a memory section.

Parts of Memory. The memory section (fig. 3-2) consists of five basic components: storage medium, memory address register, memory exchange register, storage selection circuits, and storage control. At the start of the program, the data and instruction words are written into the storage medium and, when needed, are read out of the storage medium for use in the arithmetic, control, input, or output section.

The address of the word to be read or written is sent to the memory address register from the control section. If the word is to be written, the word itself

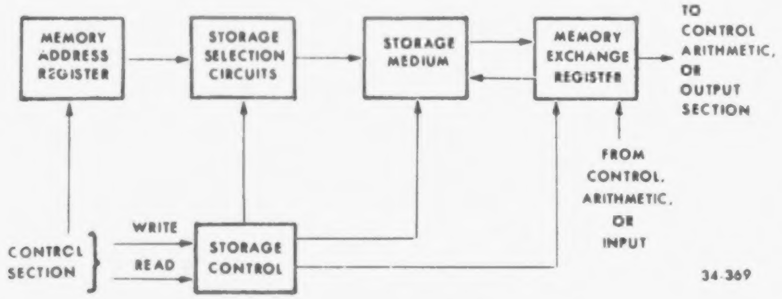


Figure 3-2. Memory section.

is sent to the memory exchange register. The storage selection circuits decode the address and select the proper storage location in the storage medium. The control section also sends a write or read signal to the storage control to begin the selected process. When a write signal is received, the storage control gates the memory exchange register, the storage selection circuits, and the storage medium, thereby allowing the data in the memory exchange register to be transferred to the storage medium location selected by the storage selection circuits.

When a read signal is received, the storage selection circuits (using address information received from the memory register) select the storage medium location from which information is to be read out; and the information is transferred to the memory exchange register. The memory exchange register, in turn, sends the information to either the control section, arithmetic section, or output section, depending upon the function code designator.

Exercises (019):

1. Name the five basic components of the memory section.

2. The address of the word to be read or written is sent to the memory address from the ______________ ______________.

3. Which circuits decode the address and select the proper storage location in the storage medium?

4. Where are the outputs of the memory exchange register applied?

020. Define terms that apply to the operation of the memory section.

Special Memory Terminology. In discussing the operation of the memory section, certain terminology is used which is peculiar to memory. These terms are defined briefly in the following paragraphs.

Storage capacity is generally measured by the number of bits, or of words and digits, of a stated base that can be stored in a medium. For example, a given medium may store 4,096 32-bit words, or 131,072 bits.

The access time is the time interval between the instant at which information is called from storage and the instant at which delivery is completed. The minimum time from the beginning of one access to the beginning of the next is often important and is called the cycle time. The cycle time is generally longer than the access time.

A random access storage unit is one in which the time required to read or write a word is independent of the location. An example of a random access unit is the magnetic core storage unit (discussed later).

A sequential access storage unit is one in which the access time depends on the location of the desired word in the storage medium. Maximum, minimum, and average access times are often stated as well as the minimum time from the beginning of one access time to the beginning of the next. Magnetic tapes and card decks are examples of storage media that use sequential access. Two types of sequential access are in use: the sequential cyclic (as used with drums or disks) and the sequential progressive (as used with magnetic tape or punched cards).

Periodic access is used for reading and recording on magnetic drums or disks. With these storage devices, information is available under a reading or recording head only for a specified period of each revolution.

Speed measurements of a particular storage unit are least ambiguous when accompanied by a statement of the type of access used. Two classes of access are recognized: random and sequential.

Data read from storage systems such as magnetic cores and electrostatic devices is extracted (removed) from the device in the process. Because the data is lost, the process is referred to as *destructive readout*. To restore the same data at the same storage location, the word must be rewritten after reading.

If data is not destroyed in a storage system in the reading process — if it can be read over and over again without rewriting — the system has *nondestructive readout*. An example of this type of storage is a flip-flop. Sensing the output voltage (reading) from a given side of a flip-flop generally does not change the state of the flip-flop, and the stored data is retained.

Volatility expresses the inability of a storage device to retain stored data when power is removed from the equipment containing the storage device. Storage devices such as flip-flops, acoustic lines, and electrostatic tubes lose the stored data when power is removed and are, therefore, classified as volatile storage devices.

Factors Determining the Choice of Memory Form. The choice of the storage medium to be used in a computer depends on several factors. Among these are (1) the intended computer use or purpose, (2) physical size, (3) cost, (4) power consumption of the equipment, (5) access time, and (6) reliability. (Reliability is a measure of the ability of the computer to function without failure over a long period.)

The type of storage device determines the size and amount of data the computer can handle and also affects the timing of the control section. The speed of operation of the storage medium determines (to a great extent) the instruction execution time and, thus, the overall time required for the computer to execute a given program.

Exercises (020):

1. The number of bits, or words and digits, of a stated base that can be stored in a medium is referred to as the ______________ ____________________ .

2. Define the term "access time."

3. Name the three types of access.

4. What are the two types of sequential access?

5. The choice of the storage medium to be used in a computer depends upon several factors. Name five.

6. What determines the size and amount of data the computer can handle, and also affects the control section timing?

3.2 Major Internal Storage Media

The major storage media used for main memory in current computers are the magnetic core, thin film, and semiconductor devices. Thin film and magnetic core memory technologies have just about reached their limits as far as future reductions in size, cost, and speed are concerned. Semiconductor memory technology, however, is still improving in regard to these same device characteristics.

021. Name two types of magnetic cores, and state how they are constructed.

Magnetic Core Memory. One of the most advanced methods for storing internal data in a computer is to use magnetic cores. Cores, which have certain advantages over drums, are generally constructed in two ways. The first type of core, called a tape-wound core, is made by wrapping a tape of magnetic material around a nonmagnetic toroidal form. (A "toroid" is a doughnut-shaped solid object.) The second type of core is called a ferrite core, and it is made by molding finely ground ferrite into a toroidal form. The ferrite used is a ceramic iron oxide with magnetic properties. The ferrite particles are then heat fused or "sintered" by applying heat and pressure. In both types, the rectangular *B–H* curves (shown later) of the cores indicate the characteristic that makes them ideally suited for digital applications.

In magnetic core memories, each data bit is stored in the magnetic field of a small, ring-shaped magnetic core (fig. 3-3). Magnetic cores generally have four wires running through them. Two wires are used for read selection. (These same two wires are used for write by reversing the direction of current flow.) An inhibit wire prevents writing a 1 when a 0 is to be written, and the sense wire picks up the signal voltage generated by shifting a core from 1 to 0 in a read cycle.

Since a single core stores only 1 bit of a word, many cores are required to handle all the bits in every word to be stored. These cores are arranged in "arrays," similar to the tracks and slots used in magnetic drum storage, in order to assign memory address locations and write and locate data quickly for readout purposes. The technique used most frequently for writing and reading data in magnetic core arrays is known as the coincident-current technique. This technique is explained in subsequent paragraphs.

In computer memory applications, the ferrite core is magnetized by a flux field produced when a current flows in a wire (drive line) that is threaded through the core. It retains a large amount of this flux when the current is removed. Flux lines can be established clockwise or counterclockwise around the core, depending upon the direction of the magnetizing current. Reversing the direction of the current flow reverses the direction of the flux field and the core magnetization. These two unique states represent 0 and 1 respectively.

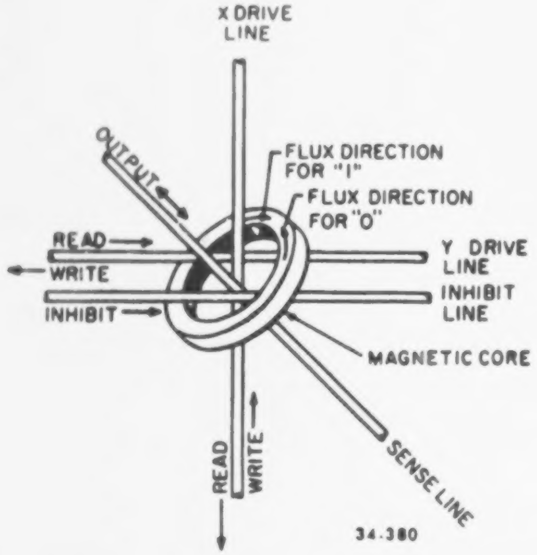


Figure 3-3. Magnetic core showing X, Y, inhibit, and sense lines.

Exercises (021):

1. Name two types of cores.

2. How is a tape-wound core made?

3. What is a toroid?

4. How is a ferrite core made?

5. How many wires are generally running through a magnetic core? For what are they used?

6. How many bits are stored in a single core?

7. Cores are arranged in ________________________ .

8. What technique is used most frequently for writing and reading data in magnetic core?

9. What two unique states, representing a 0 and 1, are used with ferrite cores?

022. Specify the operations for core magnetization.

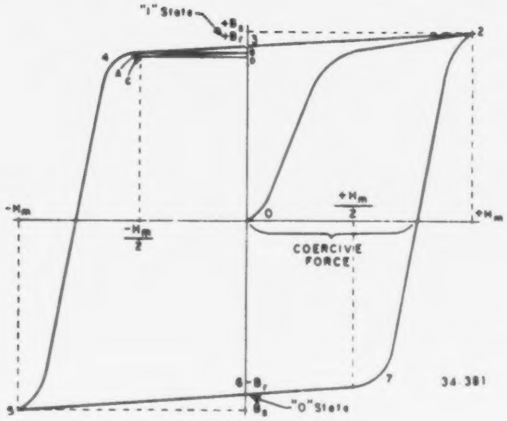


Figure 3-4. Hysteresis loop.

Magnetization Process. The state of magnetism of a core is explained using a hysteresis loop shown in figure 3-4. The points defined on the loop illustrate the magnetic flux density in gauss (B) as a function of the field (induced by the current) in oersteds (H). In this diagram it is assumed that all magnetism has been removed from the core. This condition is assumed merely to show how a magnetizing force is established in the core and how the core magnetism enters into its hysteresis loop. Actually, this core and all magnetic material exist in nature in some state of magnetization as a result of the influence of the earth's magnetic field. The 0 point in figure 3-4 represents a condition of 0-ampere turns in oersteds (H) and 0 core magnetization in gauss (B). If a current pulse is conducted through the drive line (fig. 3-3) with an intensity that produces a magnetomotive force of a magnitude $+H_m$ (fig. 3-4), the core magnetization will change (saturate) as shown along the magnetization curve defined by the numbers 0, 1, and 2. This action establishes a flux density in gauss (B) in the core of a magnitude indicated here as $+B_s$.

If the current is returned to 0, the core magnetism does not return to 0, but drops along the loop to a point $+B_r$(3). This amount of magnetism (which is referred to as residual magnetism) is only slightly less than that produced when the driving current was present. Thus, the core stores almost the entire amount of the induced magnetism.

Another pulse of magnitude $+H_m$ would now merely shift the core to $+B_s$ again (from 3 to 2) and, after the pulse has been removed, the core magnetism would return to $+B_r$ (2 to 3).

Now, if a current pulse of the same magnitude, but in the opposite direction, is conducted through the drive line so that a magnetomotive force of an intensity $-H_m$ is produced, the core flux shifts along the curve outlined by the numbers 3, 4, and 5. At 5 the core is again saturated, but because of the current reversal the magnetism is in a direction opposite to that first considered. Thus, the core saturates in the opposite direction when $-H_m$ is applied. When the $-H_m$ magnetizing force is removed, the core magnetism drops along the loop from 5 to 6 (to $-B_r$) level with negligible losses for long periods of time.

The path of the curve from 3 to A shows the results of applying a force $\frac{H_m}{2}$ to a core which was in the $+B_r$ state. When this force is removed, the core returns to a point B on the curve. Subsequent applications of the force $\frac{H_m}{2}$ cause a similar transversal (B to C to D) with the important exception that the first transversal causes the major reduction of residual flux.

The use of magnetic cores as storage devices should be obvious. If the $+B_r$ state of the core is arbitrarily called the 1 state, then the $-B_r$ state represents the 0 state. In computer memory applications, several (up to

60 or more) of these cores are arranged so that each is magnetized to store either the 0 or 1 state. The magnetic state of the combined cores represents a computer word. To apply more than one drive current and to sense or inhibit changes in the core condition, we must use several core windings (drive lines). These windings are illustrated in figure 3-3.

Any change in the flux of a core induces a voltage in all wires passing through the core. Hence, the induced voltage on the sense line (winding) is sampled to see if the core switches from $+B_r$ (fig. 3-4) to $-B_r$ when $-H_m$ is applied. If a large induced voltage is sensed (over, say, 50 millivolts), the core was in the 1 state and has been switched from $+B_r$ to $-B_r$ (the 0 state). Because the contents of the core are determined in this manner, the current pulse corresponding to magnetomotive force (MMF) $-H_m$ is called a "read pulse." (The read pulse, when applied to a selected core, drives the core from the 1 to the 0 condition.) Because the core condition stored before sensing is destroyed during readout, a memory utilizing this type of magnetic core storage element is referred to as a destructive-readout memory. If the data that was stored is to be used again, a restore (or rewrite) function is initiated to return the core to its original state.

Exercises (022):

Refer to figure 3-4 for questions 1 through 4.

1. Assume the core represented is in the 1 state and a current flow sufficient to produce an MMF of $+H_m$ is applied to the drive line. What is the flux density of the core after the current is removed?

2. Another pulse of magnitude $+H_m$ is applied. What is the flux density of the core now?

3. Assume now a current pulse of the same magnitude, but in the opposite direction, is conducted through the drive line so that a magnetomotive force of $-H_m$ is created. What is the flux density of the core when this current is removed?

4. If the core were in the $+B_r$ state and a force of $\frac{H_m}{2}$ were applied and removed, at what point on the curve would the core be?

5. What is the current pulse corresponding to MMF $-H_m$ called?

6. The read pulse, when applied to a selected core, drives the core from the ________ to the ________ state.

023. State how cores are magnetized by vector sums of current.

Magnetizing Cores By Vector Sums of Currents. The use of windings to magnetize the core and to sense the signal resulting from the application of read pulse is one method by which data can be read out or written into the internal storage facilities of a computer. Straight current-carrying wires are used when space is critical and the cores are small, because it is very difficult to wind coils on a very small toroidal form. As we have said, small cores help to increase the storage capacity per given area and decrease the core switching time.

The magnetic intensity and the flux around a current-carrying wire form patterns of concentric circles around the conductor. Because the core and the wire are concentric, some of the flux created by the wire passes through the core, as shown in figure 3-5.

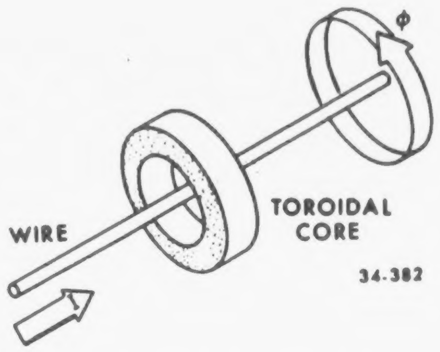


Figure 3-5. Core magnetization using a single wire.

If two current-carrying wires passing through a selected core are placed at right angles to each other, the effect is as though there were a single wire carrying the vector sum of the current (see fig. 3-6). Switching the core involves the use of vector addition. The vector sum, or resultant, of the two wires' magnetic intensities is a third magnetic intensity located midway between the two original magnetic intensities. If each wire carries 0.707 of the current required to switch a core and if a core is oriented in the direction of the resultant magnetic intensity, the core will switch. If only one wire carries current, the core will not switch. This method is called the "coincident current" method of core switching.

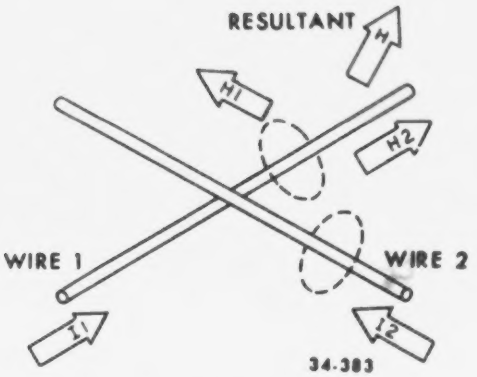


Figure 3-6. Derivation of vector sum results.

Exercises (023):

1. What method is used to read out or write data into the internal storage facilities of a computer when space is critical?

2. Why is it desirable to use small cores?

3. What is the effect of two current-carrying wires that pass through a core at right angles to each other?

4. What is the "coincident current" method of core switching?

024. Specify the operations of a core plane array.

Coincident Current in Core Plane Array. Coincident current core switching is used with an arrangement of wires and cores called a core plane array, similar to that shown in figure 3-7. This 4 × 4 array is made by crossing long lengths of insulated wires so that they form a squared-grid arrangement with 16 cores in a square pattern of 4 cores on each side of the array. The cores are placed at the junctions of the grid wires so that they encicle the resultant magnetic-intensity vector. These junctions can be thought of in terms of Cartesian coordinates; the horizontal locations assigned an "X" designator and the vertical a "Y" designator.

If a current equal to one-half of the current value required to switch a core (half-write current) is applied through both X3 and Y2 in the direction to produce a 1 condition, the only core that will be switched is the core located at the junction of the X3 and Y2 wires. The other cores along wires X3 and Y2 will not be switched, because the intensity of the magnetic flux produced by only one-half current is insufficient. These cores are said to be "half-selected." Core X3-Y2 is switched (if it is not already in the 1 state) because of the resultant magnetic intensity created by the combined one-half currents in a binary 1 direction at the X3-Y2 junction. Any of the 16 cores in this core plane may be switched to store a 1 by applying half-write currents through the associated X and Y wires. The core at the junction of any two driving wires (one X and one Y) can be set to a 1 or 0 condition, depending on the direction of current flow through the driving wires.

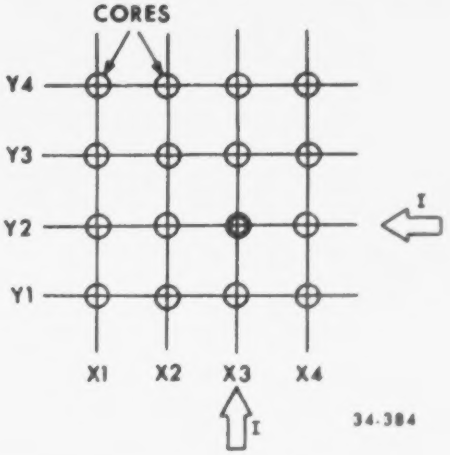


Figure 3-7. Core plane array.

To read the data (1 or 0) that has been stored in a core requires a sense winding. This winding passes through the center of each core, as shown in figure 3-8. Only one core in an array may be switched at a time. Therefore, when a read-current pulse is applied to wires X3 and Y2 (that is, opposite to the write currents), the magnetic flux or core X3-Y2 changes direction (if the core is storing a 1), thereby inducing a voltage in the sense winding. Any core may be read the same way by applying a read pulse to the associated X and Y winding of the core.

If a core has not been switched by half-write currents, as explained, it contains a 0. On application of the read pulse to the X and Y windings of that core, the direction of the magnetic intensity in the core does not switch; therefore, a pulse is not induced in the sense winding.

Consider now that all of the cores on line Y2 (fig. 3-8) are storing a 1 and that the core at the junction of Y2 and X3 is being read. When read-currents (half-currents) are applied on lines X3 and Y2, all of the cores on line Y2 are disturbed. This disturbance causes

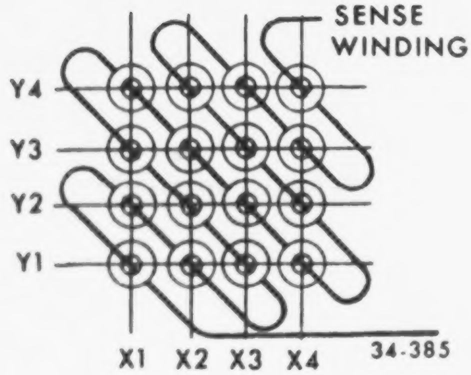


Figure 3-8. Sense winding of a core array.

low-amplitude (noise) inputs to be induced in the sense line along with the full-amplitude sense line input from the core at the X3–Y2 junction.

Two types of pulses minimize the effects of noise from adjacent cores during readout: disturb and strobe pulses. The disturb pulse (equivalent to a half-read) is a drive signal of an amplitude (coercive force) $\frac{-H_m}{2}$, which is applied to a core immediately after a 1 state is written in the core. The disturb pulse (fig. 3-4) drives the core magnetism from $+B_r$ (the state at which the magnetism is established in the core at the time the 1 is stored) to a point A on the hysteresis loop. When the $\frac{-H_m}{2}$ pulse is removed, the core magnetism returns to point B. A subsequent half-read pulse drives the core to point C and, when removed, permits the magnetism to be established at D. (This could represent the induced noise from a half-selected core where a selected core is being read.) Note that the change in core magnetism from point B to point D is less than the amount of change when the first half-read pulse is applied. Consequently, less noise will be induced in the sense winding from adjacent cores in figure 3-8 if a disturb pulse is applied on the line before reading the core at the Y2–X3 junction.

Noise pickup during reading is further minimized by strobing. This technique involves selecting the mid-amplitude portion of the amplified sense pulse. Selection is done by ANDing the amplified sense pulse with an accurately timed pulse referred to as the "strobe pulse."

Because the magnetic intensity around a core storing a 1 is switched to a 0 direction on receipt of a read pulse, the datum stored in that core is destroyed (destructive readout). The ideal readout method is, of course, one in which the data stored is not erased but remains stored for subsequent readout (nondestructive readout). With magnetic cores, however, if you want a core that has been read to retain the stored data (a 1), a subsequent write pulse must be applied to the core each time this 1 is sensed.

It may be desired to write each bit of a word into the internal storage of the computer, 1 bit per core array. Usually, the number of core arrays used for this purpose is the same as the number of bits per word. The arrays are stacked on top of each other with the first bit stored in the top array, the second bit in the next to the top array, and so on.

To permit storing the bits of a word in the same relative core position of the stacked arrays, the same X and Y driver wires of each array are connected in series or parallel. Thus, when the coordinate wires of one core in an array are energized, every corresponding core in the other arrays also is energized.

This method of driving each X and Y winding of an array in series or parallel with every corresponding X and Y winding on the other arrays of the assembly introduces a problem. In storing a word, some 1's and some binary 0's are normally written in one vertically stacked column of cores. When the X and Y driving wires are energized to write a 1 in the selected cores, every core will switch and contain a binary 1. A method must, therefore, be incorporated to prevent or inhibit the writing of a 1 in those cores which must store a 0. The magnetic field that would switch these cores is cancelled out by running an inhibit wire parallel to one of the driving wires (X or Y) as shown in figure 3-9.

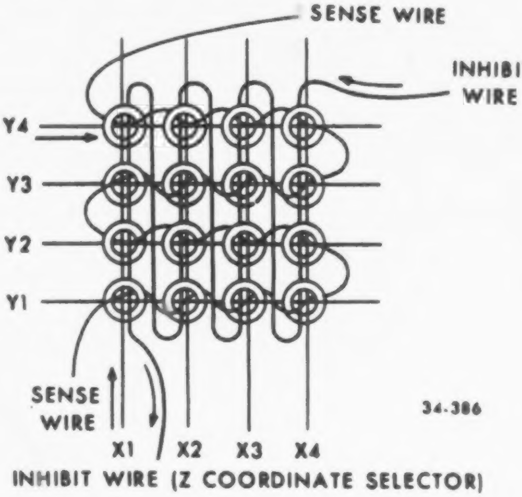


Figure 3-9. Inhibit wire of a core array.

When, for example, current flows through a particular X driving wire, the same amount of current is made to flow in the opposite direction through the inhibit wire. Since the magnetic fields created by these parallel and closely spaced wires are equal and opposite to each other, the effective magnetic field is 0. The flux of the Y driving wire (one-half write current) is insufficient to switch the core, so the core is not switched (retaining a 0).

Representative Core Matrix. Figure 3-10 is a simplified diagram of a memory board that contains four memory matrices arranged in quadrants. The X and Y

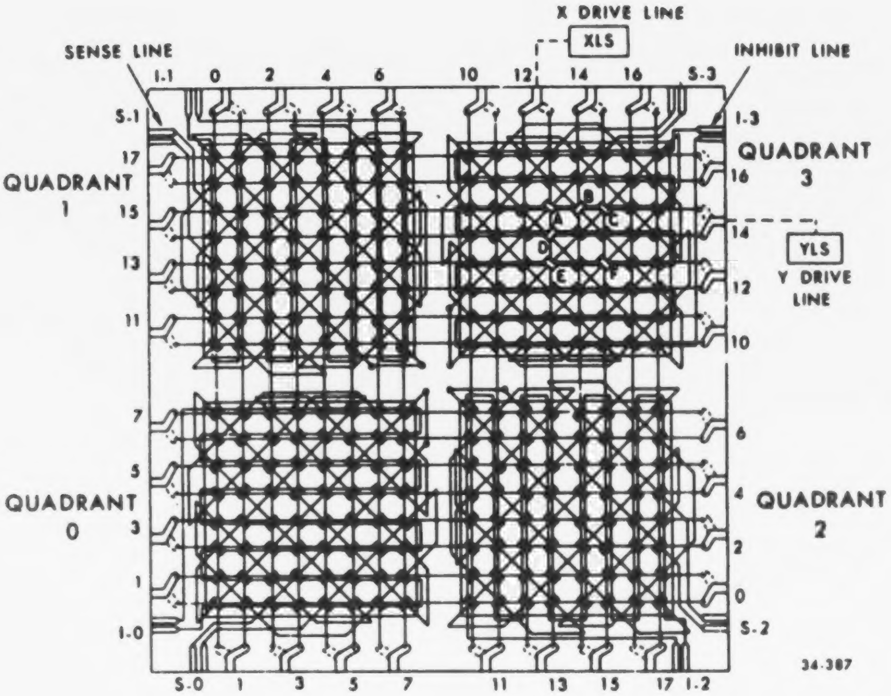

X DRIVE LINE
XLS
SENSE LINE
INHIBIT LINE
I-1
0
2
4
6
10
12
14
16
S-3
S-1
17
QUADRANT 1
15
13
11
I-3
QUADRANT 3
16
14
YLS
Y DRIVE LINE
12
10
A
B
C
D
E
F
7
5
QUADRANT 0
3
1
I-0
6
4
QUADRANT 2
2
0
S-2
S-0
1
3
5
7
11
13
15
17
I-2
34-387

Figure 3-10. A simplified magnetic core board, 16 by 16 array.

drive lines, the sense line, and the inhibit lines are shown for each quadrant. As we said, any one of the magnetic cores in the matrix can be selected. A coincident half-amplitude current pulse is generated in a selected column of a selected quadrant. The core at the intersection of the row and column receives a net full-amplitude current pulse and is, therefore, selected.

For example, assume that core A in quadrant 3 is to be selected. Drive lines 13X and 15Y are each driven with half-amplitude current pulses. Core A, at the intersection of lines 13X and 15Y, receives a net full-amplitude current pulse. All other cores in 13X and 15Y lines receive half-amplitude current pulses (cores B, C, D, E, etc.), which is an insufficient current amplitude to switch or alter data stored in these cores. The cores which receive only half-amplitude current are half-selected. The remaining cores, which are neither half-selected nor fully selected, are referred to as unselected cores (for example, core F). Core A is "selected."

Exercises (024):

1. With what is coincident current core switching used?

2. Refer to text figure 3-7. What is required to produce a 1 in the core at the intersection of Y3 and X2?

3. What is required to read the data (1 or 0) which has been stored in a core?

4. How many cores in an array may be switched at a time?

5. Summarize the two ways to eliminate the effects of noise from adjacent cores during readout?

6. Because of the magnetic intensity around a core storing, a 1 is switched to a 0 direction on receipt of a read pulse. What happens to the datum stored in that core?

7. How are magnetic fields cancelled out to inhibit the writing of a 1 in the cores containing a 0 when the X and Y drive lines are connected in series or parallel?

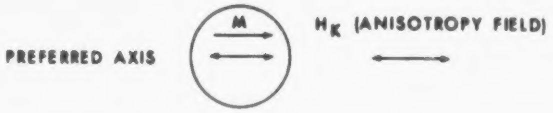
025. State how a thin film memory operates.

Thin Film Memory. Thin film memory consists of a ferromagnetic material, permalloy, deposited (under controlled conditions in a vacuum chamber) on a substrate of thin glass. After all air has been removed from the chamber, a shutter arrangement is opened and vapors from molten permalloy pass through a mask and are deposited on the substrate. The pattern thus formed is determined by the shape of the mask. The thickness of each spot (magnetized area) is controlled by the amount of time the shutter is open.

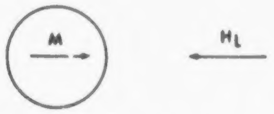
A magnetic field is applied parallel to the surface of the substrate during deposition. The film spots thus become easier to magnetize in a direction parallel to that in which the magnetic field was applied during the deposition process. This direction is known as the preferred direction; likewise, the axis of this magnetism is referred to as the preferred axis.

Storage. Thin film materials are well suited for storing binary data, since they have a stable state of magnetization in each direction parallel to the preferred axis. The double-headed arrow in the circle shown in figure 3-11 *indicates the preferred axis.* When the direction of magnetization is caused to rotate through 180° (starting from the preferred axis), there is first a torque which tries to retain the magnetism along the preferred axis. If the magnetizing force is sufficiently strong, the magnetism will be shifted to a point perpendicular to the preferred axis. Beyond this point, there is a forward torque which causes the magnetism to be aligned in the material exactly 180° from the preferred axis. The torque is caused by the field H_k, which is produced during the deposition process. This field is called the anisotropic field. (The word "anisotropic" refers to the ability of the magnetic material to assume different positions in response to external stimuli.)

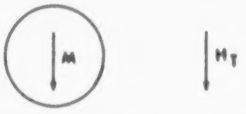
If the magnetic stimulus is removed after the anisotropic field is formed, this field (H_k) causes the magnetic vector to be aligned parallel to the preferred axis. Applying a coercive force, H_c, which is less than that required to switch the magnetization but produces a



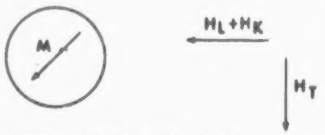
A. POSITION OF MAGNETIC VECTOR WITH NO FIELDS APPLIED



B. POSITION OF MAGNETIC VECTOR WITH ONLY HL LONGITUDINAL FIELD (BIT CURRENT APPLIED)



C. POSITION OF MAGNETIC VECTOR WITH ONLY HT TRAVERSE FIELD (WORD CURRENT APPLIED).



D. POSITION OF MAGNETIC VECTOR WITH BOTH H_L (LONGITUDINAL FIELD FOR BIT "0") AND HT (TRAVERSE FIELD WORD CURRENT) APPLIED.

Figure 3-11. Rotation of the magnetic vector of a film spot.

field parallel to the preferred axis, causes no significant change in the state of the magnetized material.

Applying only a traverse field, H_T (fig. 3-11,C); i.e., a magnetic field perpendicular to the preferred axis and which is stronger than H_K, causes the magnetic state of the spot to be rotated 90°, as shown in figure 3-11,C. If fields are applied so that the vector sums of $H_L + H_K$ are active forces on the spot, the position of the resultant magnetic vector will be as illustrated in figure 3-11,D. If H_T is then removed from the spot, the direction of the magnetization becomes the same as that for H_L. When H_L is removed, the spot remains in the state until H_T is again applied. Thus, the direction of H_L determines the direction of the stable state of magnetization of the film spot.

Switching. Because a concentric magnetic field is produced around a flow of current, it is possible to switch a film spot by passing current through drive lines in close proximity with the spot. The drive and sense lines (1-line array) are sometimes etched on Mylar sheets that are carefully aligned and attached to epoxy boards to give the required strength to the line array.

Figure 3-12,A, shows a film spot and the line array on one side of the spot. An identical set of these lines is placed on top of the film spot. The connectors for the line array are wired so that the word lines produce two turns. (Bit lines are effective in selecting a particular bit of a word. Word lines provide for word selection from memory.)

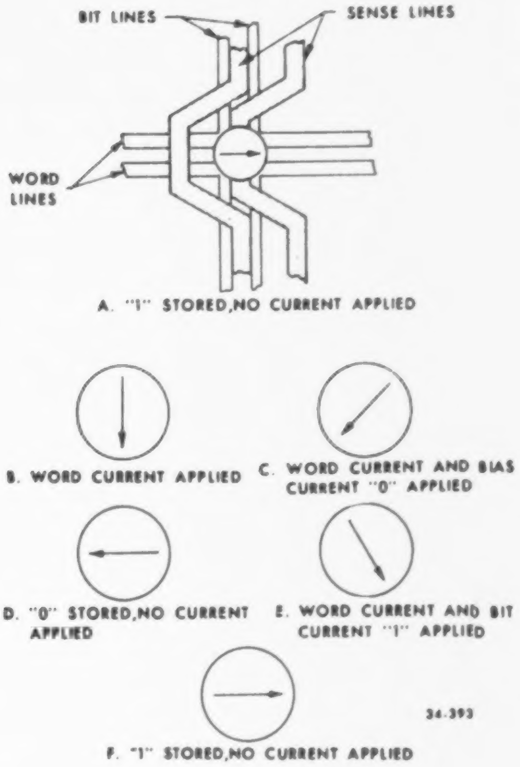

BIT LINES
SENSE LINES
WORD LINES
A. "1" STORED, NO CURRENT APPLIED
B. WORD CURRENT APPLIED
C. WORD CURRENT AND BIAS CURRENT "0" APPLIED
D. "0" STORED, NO CURRENT APPLIED
E. WORD CURRENT AND BIT CURRENT "1" APPLIED
F. "1" STORED, NO CURRENT APPLIED
34-393

Figure 3-12. Switching a film spot.

The arrow of the film in figure 3-12,A, shows the stable-state magnetic vector with a 1 stored. If word current flows down the word lines, the magnetic vector rotates 90°, as shown in figure 3-12,B. If bias current is applied to the bit lines, the magnetic vector rotates toward the 0 stable state, as shown in figure 3-12,C. After the word current is removed, the vector completes the 180° rotation from the 1 state. Thus, a 0 is stored, as shown in figure 3-12,D.

If a 1 is to be stored in the spot (see figs. 3-12,E, and 3-12,F), current applied to the bit lines is reversed. Thus, the magnetic vector is rotated toward the 1 state. If the word current and then the bit current are removed, the stable state of magnetization will represent a 1.

Sensing. The thin-film memory is a destructive readout memory; i.e., reading a spot (location) clears the contents of that address. During a readout, all of the addressed spots are switched toward the 0 state. The sharp change in the magnetic field around any spot causes a voltage to be induced in the sense lines. The magnitude of this voltage depends upon the change in the magnetic flux resulting from the switching process.

The output is read from the memory by ANDing a strobe pulse with the output from a sense amplifier (not shown) whenever a 1 is stored in the location being read. No output from the AND circuit indicates a 0 has been read.

Exercises (025):

1. Of what does thin film memory consist?

2. How is thin film constructed?

3. How is the thickness of each magnetized area controlled?

4. What is the meaning of the term "preferred direction"?

5. The torque that aligns the magnetism in a film spot parallel to its preferred axis in the absence of external stimuli is produced by the ______________ ______________.

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6. What happens to the magnetic spot when only a transverse field, H_T, stronger than H_K is applied? (Refer to fig. 3-11).

7. Again referring to figure 3-11, what does the direction of H_L determine?

8. Why is it possible to switch a film spot by passing current through drive lines in close proximity with the spot?

9. Refer to text figure 3-12. What conditions in the word and bit lines initiate the writing of a 1 in a film spot?

10. In a thin-film memory, what happens to all of the addressed spots during a readout?

026. Specify the characteristics of the RAM type of semiconductor memory, and state the advantages and disadvantages.

Solid-State Memories. A few years ago, the computer was a large vacuum-tube unit using many different types of storage devices. The ferrite core memory reduced the size and access time of the storage unit. Transistors replaced the vacuum tube, reducing the size, cost, and power required by the computer. Then came the integrated circuits (ICs) replacing the transistors, and now we have large scale integration (LSI) replacing small scale ICs. LSI reduced the size, cost, and power requirements drastically. With the arrival of LSI, new solid-state memories have been developed that are small and cheap, and require power in the milliwatt range. A common item in wide use today, and a good example of the size and cost of the LSI circuits and memory, is the battery-powered hand-held calculator with memory storage. Let us discuss the solid-state memories that evolved from IC technology.

Semiconductor Random Access Memory (RAM). The solid-state RAM and the ferrite core memory are very similar in operation. The ferrite core and RAM use X and Y lines to select one location. In the ferrite core memory, only one core per plane is selected at a time with a given address. In the RAM, one memory *cell* per chip is selected at a time with a given address. An 8X256-bit RAM stores 256 bytes for a total of 2048 bits. The same would be true of a core memory which had 8 planes of 256 bits each. Well, we know that the magnetic cores store 1-bit in each core—the individual cores are the storage medium. What is the storage element in RAMs?

There are two technologies that are primarily used to implement a RAM on an IC chip. These are the *bipolar* and *MOS* RAMs. Bipolar IC RAMs use the standard transistor in flip-flop circuits to store data. MOS RAMs use the MOSFET as the storage element. There are two types of MOS RAMs used in semiconductor memories. These are the *static* and *dynamic types. A static MOS RAM uses MOSFETs interconnected as flip-flop* circuits to store bits of data. The dynamic RAM uses the capacitance that exists between the gate and channel of a MOSFET to store bits of data. An added requirement for the dynamic RAM is that it must be refreshed. If a 1 is stored in the gate capacitance of a MOSFET, the charge will eventually leak off. Refreshing the dynamic RAM with critically timed clock signals maintains the data in the MOSFET. Although the dynamic RAM requires additional driving circuitry for refresh, it requires less power for operation than the static RAM. On the other hand, static RAMs are easier to drive but are most costly than the dynamic type.

Solid-state memories give us a significant reduction in size, power requirements, and cost. If this is so, why not change all memories to the RAM instead of core? What are the advantages and disadvantages of using solid-state RAMs in comparison to magnetic cores?

Advantages and Disadvantages of RAM. First, let us discuss the advantages of the solid-state RAM over the ferrite core RAM. The core memory has current drivers for the X, Y, and inhibit lines. Also, the core memory must have sense amplifiers because of the low-level signal on the sense line. This all requires power supplies that supply the memory with the high current needed for its operation. The RAM also uses X and Y lines for addressing; however, no current drivers are required for their operation. No sense amplifiers are required because the "cells" in some solid-state memories have the ability to feed up to 10 circuits without additional buffers. The RAM's access time is about 50 nanoseconds with power dissipation of about 0.5 watt. From this, you can see that a much smaller power supply will do the job for the RAM. Its relatively small size is also an advantage for the solid-state RAM. An example is a 1024-bit RAM on a chip 91 mils by 125 mils. You might ask, "With all this going for it, why not use the RAM in all computers?" The answer to this question brings us to the one main disadvantage of the RAM: It is volatile!

Recall the statement, "The core memory is the best overall storage device for use as computer main memory." The reason for this statement is the ability of the core memory to retain stored data indefinitely with or without power applied. The solid-state RAM must have power to retain data. If the RAM solid-state memory loses power, data is lost. This is a big disadvantage when critical data must be stored. A solid-state memory that overcomes this disadvantage is the read-only memory (ROM).

Exercises (026):

1. How many cells per chip can be read with a given address, using a solid-state RAM?

2. What are some of the advantages of the RAM over a ferrite core?

3. What is the main disadvantage of the RAM?

4. What would happen if a solid-state RAM lost power?

5. Explain the differences between the bipolar and static MOS RAMs.

6. Explain the differences between the static and dynamic MOS RAMs.

027. Specify the characteristics of a solid-state ROM, and identify the different types of ROM available.

The Read-Only Memory (ROM). The ROM is a random-access memory device just like the magnetic core and solid-state RAM memories. The major difference is that the ROM has its data permanently programmed in, at the time of manufacture. Therefore, you can only read data from the ROM. In order to change the ROM program, you must change the ROM. ROMs are used in microcomputers to store the permanent program for the microprocessor. The ROM is either part of the microprocessor IC or it may be a separate chip.

Early ROMs used a diode matrix to store data. The presence of a diode in the matrix represented a 1, the absence of a diode equaled a 0. In a similar fashion, newer ROMs use bipolar transistors and MOSFETs to do the same thing. As we mentioned earlier, if you want to change the data in the ROM, you have to change the ROM itself. To remedy this, the programmable read-only memory (PROM) has been developed. Several methods are used to program or reprogram a PROM.

The PROM. The PROM is a memory device that can be programmed by the user, rather than at the factory. There are two major categories of PROMs. One type can be programmed once by the user but cannot be reprogrammed. The second, more versatile type, is the PROM that can be programmed once, erased, and then reprogrammed. PROMs use either bipolar or MOS transistors as memory cell elements.

In the nonreprogrammable PROM, *fuse links* are connected between each memory cell and the matrix. To program the device, selected fuse links are burned open by a specified external voltage used for the purpose of programming the chip. Once the fuse links are destroyed, in a pattern representing the stored data, the data is permanently stored. Now for the reprogrammable PROMs. What methods are used for erasing data in this type of PROM?

Erasable PROMs. This type of PROM can have the data stored within erased by ultraviolet light or through electrical means. Storage of data in an EPROM is done using the gate storage charge of a MOSFET. Unlike the solid-state MOSFET RAM, the gate of a MOSFET in the EPROM is isolated from the electrical circuit. Once a charge is stored in the MOSFET gate structure, it will remain until erased.

Ultraviolet EPROM. This type of EPROM can be recognized by the opaque material on top of the EPROM chip. This window is used when ultraviolet light is injected to erase the gate storage charges in the memory. Programming is done with specialized equipment which charges the gate of selected memory cells.

Electrically erasable PROMs (EEPROMs). This type of EPROM can be electrically written and erased. Higher than normal voltages are used when writing or erasing data in this memory chip.

Electrically alterable PROMs (EAPROMs). The major difference between this device and the EEPROM is that this PROM is capable of being programmed or erased in the circuit. Previous ROMs and PROMs mentioned must all be removed from the circuit for programming.

Exercises (027):

1. How is the diode ROM programmed?

2. When programming a PROM which can't be programmed again, what is used to program the device?

3. What are the two main types of PROMs?

4. What two methods are used for erasing EPROMs?

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5. What is the storage element in an EEPROM?

3-3. Mass Storage/External Media

This category of storage system(s) includes primarily the drum, tape, and disk. These forms of magnetic storage media can store tremendous amounts of data for a computer system. The magnetic disk unit has become the more versatile and most popular storage system in use with modern computer systems. All three will be discussed in this section. First, let's look at some of the characteristics of recording heads and the different recording techniques used with magnetic storage media.

028. Specify the characteristics of read-write heads.

Read-Write Heads. Surface magnetic writing is performed by means of a coil of wire (called the write coil) wrapped around a specially shaped core (fig. 3-13). The core consists of low-retentivity magnetic material, such as Mumetal, and is provided with an airgap. The entire device is called a write head.

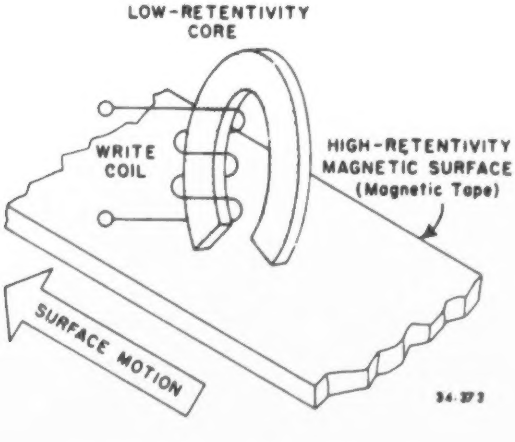


Figure 3-13. Surface magnetic wiring arrangement.

Applying a signal voltage across the write coil produces a flow of current; this creates a magnetomotive force that causes flux to pass through the series combination of core and airgap and through that portion of the magnetic surface close to the airgap. Since the reluctance of the magnetic surface is very much less than that of the parallel airpath, most of the magnetic flux passes through the magnetic surface. This resembles the manner in which current flows through a circuit containing two parallel resistors of unequal values. The magnetic surface is moved past the airgap at a constant speed so that each element of the high-retentivity magnetic surface retains a portion of the magnetic flux that existed at the moment when that portion of the surface was near the airgap of the write head.

The pole pieces, or ends of the core that forms the airgap, are designed so that the lines of flux passing between their tips will lie parallel to the surface of the tape. In this manner, as shown in figure 3-14, the main magnetic field retained by the magnetic surface is parallel to the surface. This produces a strong retained field. The core may consist of solid metal, or it may be laminated to reduce eddy currents.

The method of magnetizing the moving surface, as shown in figures 3-13 and 3-14, is called "longitudinal recording." This term is applied to magnetic tapes, since the direction of flux is along the long axis of the tape.

In computer applications, the speed may be several hundred inches per second. Consequently, abrasive wear of the pole tips and the magnetic surface could become a problem if contact were permitted. Thus, in order to improve overall reliability, the pole tips of most computer magnetic heads are separated from the moving magnetic surface by a distance of a few thousandths of an inch. Although the increased path reluctance produced by this arrangement requires greater driving currents, the absence of abrasive wear justifies its use.

During a reading operation, the magnetized magnetic surface moves past the airgap of a device that is very similar to the write head. In the course of the reading operation, some of the flux from the moving magnetic surface passes through the read core which has a much lower reluctance than the surrounding air. As a result, voltages are induced across the coil mounted on this core. In some instances, both the write and read coils are wrapped around the same core; and

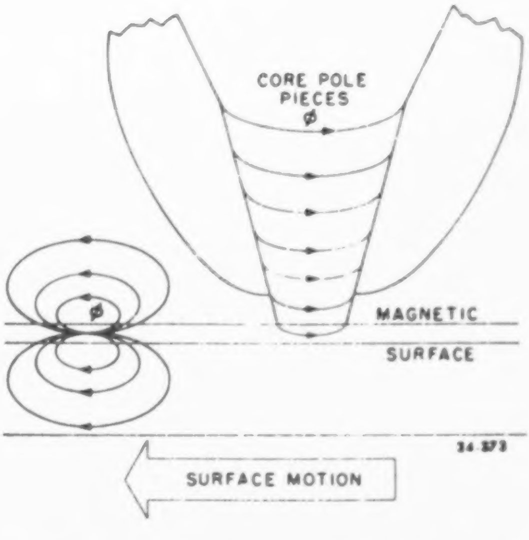


Figure 3-14. Magnetizing a memory surface by the longitudinal recording method.

the device is then called a read-write head. When a read-write head is used, suitable external circuitry must be used so that the voltages induced in the read coil during a reading operation (and in the write coil during a writing operation) do not produce interference in the associated electronic driving and reproducing circuits. The waveform of the voltages induced in the read coil are similar to the waveforms of the signal originally used to magnetize the surface of the tape.

The space between the magnetic head pole tips is usually referred to as the gap width or the gap, and its dimensions are extremely important. The gap width determines the number of pulses that can be written on a given portion of the magnetic surface. Since each pulse magnetizes the entire portion of the surface across the airgap at a particular instant, the surface area on which each pulse is written is determined by gap width, gap length, pulse duration, and tape speed.

It is desirable from both a frequency-response and a pulse-writing point of view to use the smallest possible airgap. However, if the airgap width is too small, its reduced reluctance permits the loss of some flux that would otherwise have passed through the magnetic surface. Furthermore, the difficulties of manufacturing small, uniform gaps must be considered. To meet these criteria, the gap width is usually in the order of 0.001 inch.

A very important characteristic of a magnetic surface writing device is the number of pulses or bits of information (binary digits) that can be written upon a given length of magnetic surface. This is called the packing factor or bit density. When information is to be stored, it is desirable to store as many bits as possible on a given length of surface. This decreases the amount of required storage space and also reduces the time required later to gain access to the information. Two main factors affect the maximum bit density: the previously discussed gap width of the read-write head and the interaction of the magnetic fields of the storage surface.

Interaction of magnetic fields occurs between adjacent magnetized areas of the tape surface. If these areas, which possess the characteristics of tiny bar magnets, are too close together, their magnetic fields will combine. When the magnetic surface is read, only two pulses will be produced—one at the beginning of the series of combined flux pulse and the other at the end of the series. The interaction is reduced when increased spacing is used between the magnetized areas. However, this increased spacing reduces the bit density. Spacing between magnetized areas can be made large either by increasing the surface speed or by recording the data at a lower pulse-repetition frequency.

The actual areas of the magnetic surface that are separately and distinctly magnetized are sometimes called storage cells. A pulse is said to be "written in a storage cell." One storage cell is required to record each bit of any binary word written on a magnetic surface.

Besides writing, we must also be able to erase data that are no longer needed. Two methods of surface erasing are commonly employed. The first method, DC erasing, magnetically saturates the surface, thereby masking all previously written data. The second method, AC erasing, actually returns the surface to a state of 0 flux or demagnetizes it.

Exercises (028):

1. Briefly describe the write coil for surface magnetic writing.

2. How are the pole pieces designed?

3. Why would a laminated core be used?

4. What is longitudinal recording?

5. What is the reason for positioning the pole tips a few thousandths of an inch away from the magnetic surface?

6. When a combination read-write head is used, why must external circuitry be used?

7. The space between the magnetic head pole tips is usually referred to as the ____________ ____________ ____________ ____________ ____________.

8. Why are the gap width dimensions important?

9. What happens if the gap width is too small?

10. Gap width is usually in the order of ____________ ____________.

11. Define the term "packing factor" or "bit density."

12. What is another factor that affects the maximum bit density?

13. How can the space between magnetized areas be made larger?

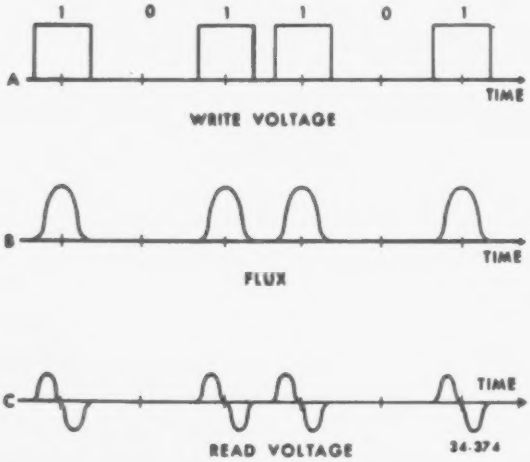
14. How many storage cells are required to record each bit of any binary word written on a magnetic surface?

15. Name the two methods of surface erasing, and state how they are done.

029. Name the different types of recording systems, and state their functions.

Recording Systems. Now consider some recording systems. Several types are used. In the simplest, a pulse indicates a binary 1, while no pulse (the absence of a pulse) indicates a binary 0.

In the *positive-pulse return-to-zero system,* the waveforms of the binary word 101101 appear, as shown in figure 3-15,A, or 3-15,B. This method is abbreviated RZ. The flux slope is positive at the leading edge of the pulse, zero at the top of the pulse, and negative on its trailing edge. During the reading process (fig. 3-15,C), a positive pulse and a negative pulse are induced in the read head each time the flux pulse stored on the magnetic surface passes the airgap. This occurs because the induced voltage is proportional to the rate of change of the flux.



ure 3-15. Waveform of positive-pulse return-to-zero (RZ) system.

In the *positive- and negative-pulse return-to-zero method,* both positive and negative current pulses can be used to write a binary word. In this instance, a positive pulse can be used to represent a binary 1, and a negative pulse can be used to represent a 0 (fig. 3-16). The output for binary 1 (fig. 3-17) will consist of a small positive pulse, followed by a large negative pulse and then a small positive pulse. The opposite will occur for a binary 0 read pulse; that is, a negative pulse followed by a large positive pulse and then a small negative pulse. The larger pulse is generated when there is a maximum rate of change of flux. This occurs when the current changes from a maximum in one direction (either positive or negative) to a maximum in the other direction ($d\phi/dt = \max$).

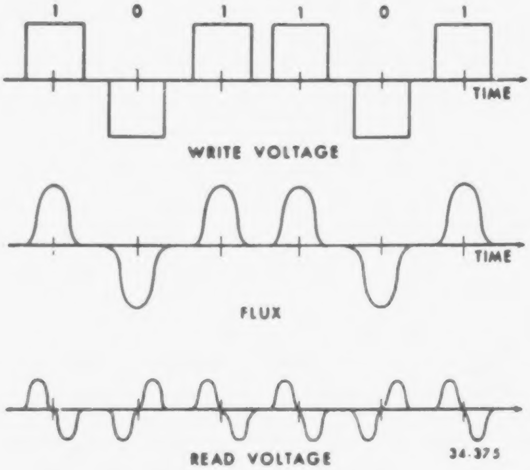


Figure 3-16. Waveform of positive and negative pulse return-to-zero system.

The *nonreturn-to-zero system* (NRZ) uses a slightly different principle. In an NRZ system, changing flux can be used to indicate a 1, while a constant flux is used to represent a 0. Thus, the magnetic flux is never returned to zero. This concept can be illustrated by writing 101101 in the NRZ system of recording, as shown in figure 3-18.

To further clarify this point, consider the action for *serial readout* of the data represented in figure 3-19, using the AND circuit and the clock pulses (B_1). The operation of the AND circuit to produce the output ($F_1 = A_1B_1$) is understood. Each bit of data using this method (return-to-zero method) rises from the zero level to maximum voltage and remains at that level long enough to permit the clock pulse to be ANDed with each bit of data in coincidence. It then returns from the maximum level to zero. The time between clock pulses is necessarily long, and the overall time to read a single bit is long in relation to the actual AND operation. This, in itself, is the read process.

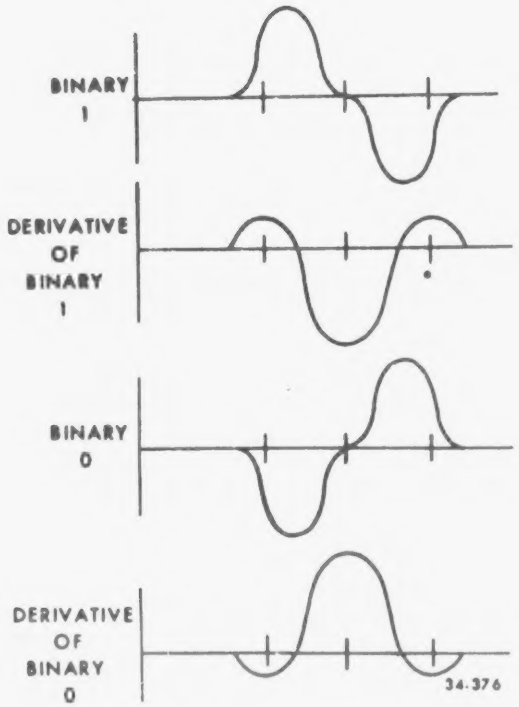


Figure 3-17. Comparison of the waveform of binary 1 and 0 and their derivatives.

The unique way in which the nonreturn-to-zero method lends itself to faster reading is seen by studying the waveforms in figure 3-20 and their actions to produce the output ($F_2 = A_2B_2$) from the AND circuit. Note that the output produced in the 5μs read period for return-to-zero method is still 110111 (6 bits), whereas the nonreturn-to-zero output produced in the same period is 111100000011 (12 bits). Thus, serial data can be read in a shorter period using the nonreturn-to-zero method, since the clock pulses can be applied at a higher clock rate.

Exercises (029):

1. During the reading process, figure 3-15,C, a positive pulse and a negative pulse are induced in the read head each time the flux pulse stored on the magnetic surface passes the airgap. Why?

2. In which recording system can both positive and negative current pulses be used to write a binary word?

3. In the positive and negative pulse return-to-zero method, when is the larger pulse generated?

4. In the nonreturn-to-zero recording method, how are binary 1 and 0 indicated?

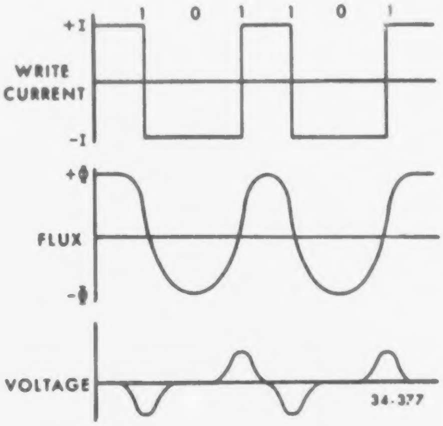


Figure 3-18. Waveforms of the nonreturn-to-zero (NRZ) system.

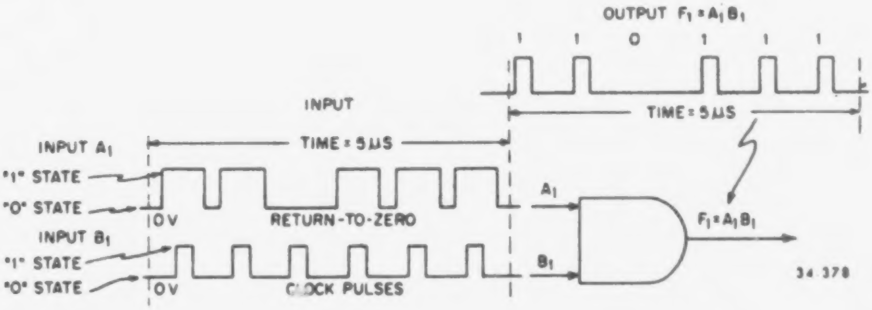

OUTPUT F₁ = A₁B₁
1 1 0 1 1 1
INPUT
TIME = 5μS
INPUT A₁
TIME = 5μS
"1" STATE
"0" STATE
0V
RETURN-TO-ZERO
INPUT B₁
"1" STATE
"0" STATE
0V
CLOCK PULSES
A₁
B₁
F₁ = A₁B₁
34.378

Figure 3-19. Serial readout (return-to-zero).

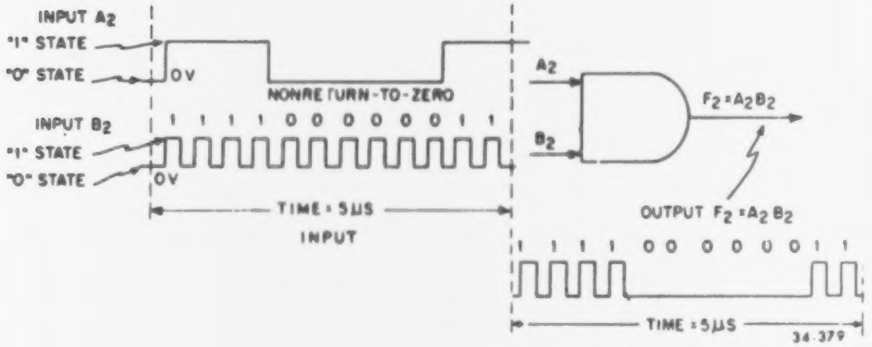


Figure 3-20. Serial readouts (nonreturn-to-zero).

5. In serial readout using an AND-gate and the return-to-zero method, when is there a binary 1 output?

6. Which method affords far faster reading of serial data? Why?

030. Identify specific design and operational factors and functions related to magnetic drum memories.

Magnetic Drums. The magnetic drum storage system is a common type of endless track memory. Its most important components are a rotating drum and a set of stationary heads. The magnetic drum consists of a nonmagnetic base cylinder, usually manufactured of aluminum because of its paramagnetic characteristics and good heat dissipation. The cylinder is precision milled to exact specified dimensions. The diameter of drums vary from 1/4 inch to 4 feet, and their lengths vary from 1/4 inch to 3 feet. A magnetic coating is applied to the base in one of three ways. One method is to dip or spray the aluminum surface with red or black oxide of iron. Red oxide is preferred because of its lower resistivity. The second method is to closely wrap the drum surface with ferromagnetic wire and then mill the surface flat. This method obtains certain properties not present in the iron oxides. The third method of magnetic surface preparation is to electroplate the surface with a ferromagnetic alloy. This method has wide use because of the slightly better magnetic properties produced by electroplating.

The drum is usually formed directly on a shaft, and the shaft is turned to produce drum rotation. The shaft can be directly connected to the rotor of a drive motor, or it can be belt-driven by an adjacent motor. The bit density around the circumference ranges from 50 to 120 bits to the inch per channel. A channel is a path around the drum controlled by at least one read-write head and used for storing 1's and 0's. The number of channels that a drum is capable of handling depends upon the several factors referred to next. Some compromise must be achieved between the factors of memory capacity, signal amplitude, and reliability of the system to determine the channel spacing. This spacing normally runs between 15 and 30 channels to an inch.

Figure 3-21 illustrates the construction of a magnetic drum. The channels are 30 mils wide and spaces 15 mils apart. The distance between the channels prevents "crosstalk," which is interference caused by magnetic flux from adjacent channels.

Construction of Read and Write Heads. There are several methods of constructing magnetic heads. Figure 3-22 illustrates three of these methods. In figure 3-22,A, there are two separate heads, one for writing and one for reading. The erase bar magnetizes the drum surface in one direction, the direction for a 0. When the surface passes under the write head, the head will be pulsed to reverse the flux on the drum surface, thereby writing a binary 1. If a binary 0 is to be written, the write head is not pulsed; and the magnetic flux remains in the direction for a 0. With this system, reading usually takes place within 270° after writing has occurred, or the information will be erased.

To obtain an output (readout), the flux passing the read head induces an EMF that represents a binary 0 or a binary 1. Output circuits then clip and shape the pulses to the desired shape. In some instances, paramagnetic shims are placed between the pole pieces of the write head, and this increases the induced flux density on the surface of the drum when writing is taking place.

In figure 3-22,B, and figure 3-22,C, the same heads are used for writing and reading. The erase bar is eliminated because the head can magnetize in two directions. In figure 3-22,B, the head also has an airgap. This airgap breaks up the core to reduce hysteresis loss.

Magnetic Head Identification. The symbols for indicating the magnetic heads which read, write, read and write, and erase information on a drum, tape, or disk surface are pictured in figure 3-23. These symbols are almost self-explanatory. An arrow pointed toward

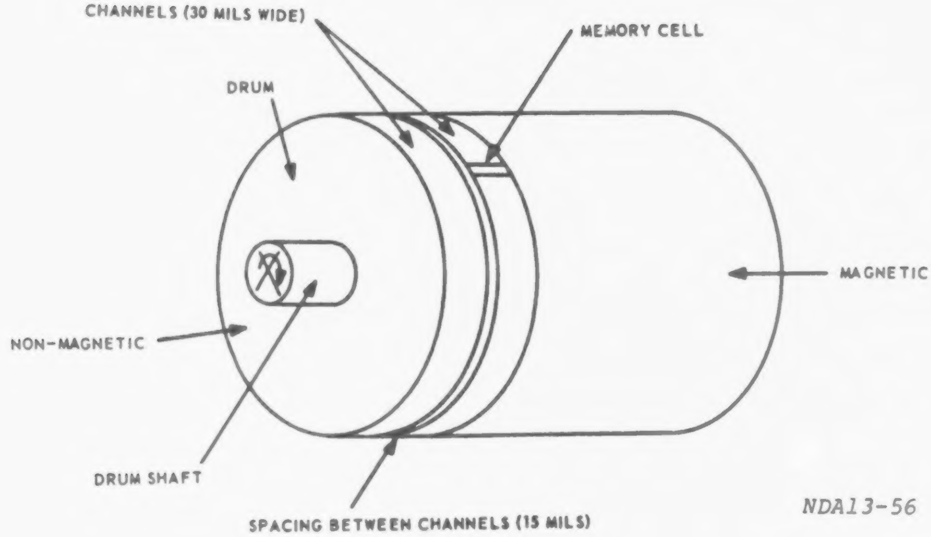

CHANNELS (30 MILS WIDE)
MEMORY CELL
DRUM
MAGNETIC
NON-MAGNETIC
DRUM SHAFT
SPACING BETWEEN CHANNELS (15 MILS)
NDA13-56

Figure 3-21. Drum construction.

the drum surface indicates a write head. When the arrow points away from the drum surface, it indicates that the head is taking information from the drum surface or reading. A head that performs both the read and write function contains arrows pointed toward the drum and away from the drum. The drum head symbol with an X inside is an erase head. The degrees labeled in the figure show the angular position with respect to the zero timing channel on the drum. For example, the head on the extreme left is at 0°. The second head is 10° away from the first head, and the third head is 20° away from the first head, etc.

Methods of Recording on Drum Surface. There are several methods of placing information on magnetic

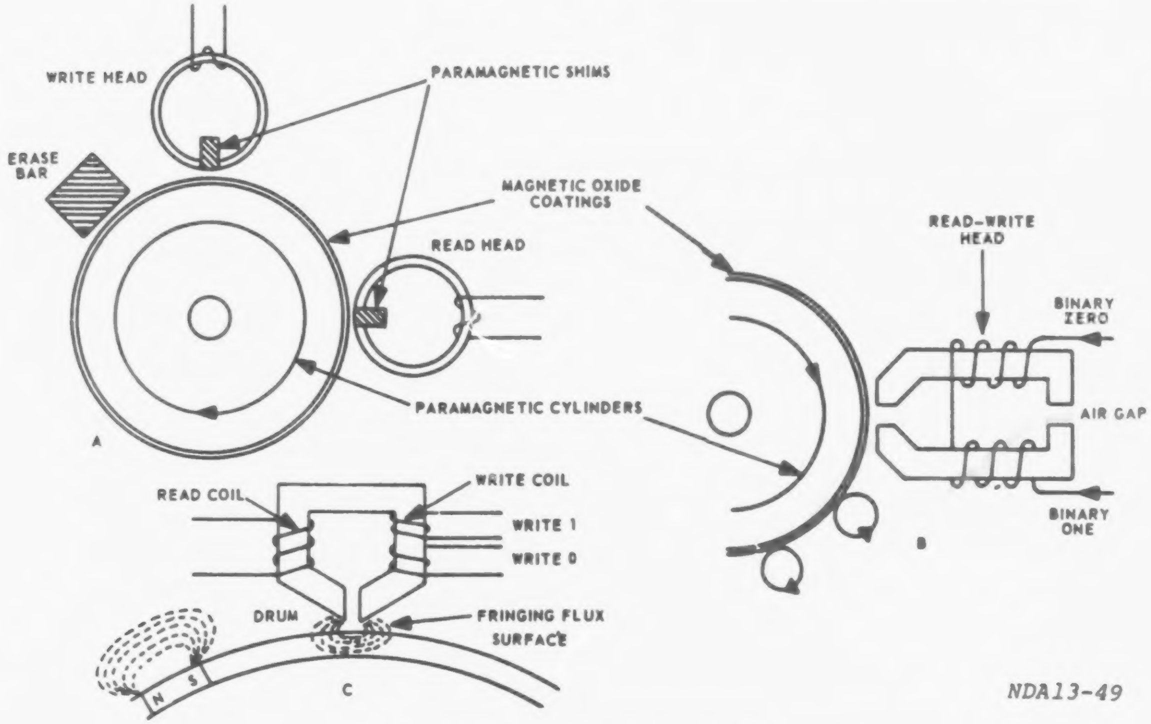

WRITE HEAD
PARAMAGNETIC SHIMS
ERASE BAR
MAGNETIC OXIDE COATINGS
READ HEAD
READ-WRITE HEAD
BINARY ZERO
AIR GAP
BINARY ONE
PARAMAGNETIC CYLINDERS
A
B
READ COIL
WRITE COIL
WRITE 1
WRITE 0
DRUM
FRINGING FLUX
SURFACE
N
S
C
NDA13-49

Figure 3-22. Types of read and write heads.

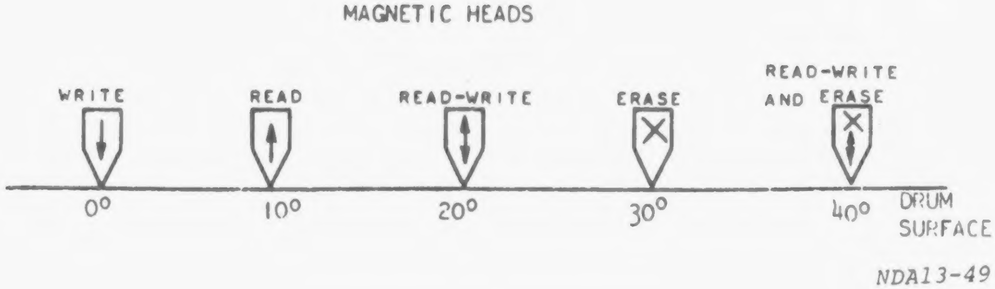

MAGNETIC HEADS
WRITE
READ
READ-WRITE
ERASE
READ-WRITE AND ERASE
0°
10°
20°
30°
40°
DRUM SURFACE
NDA13-49

Figure 3-23. Magnetic head logic symbols.

surfaces, some of which were derived for specific applications and some of which were meant for general systems. Figure 3-24 illustrates three main types of recording techniques that are commonly used.

Figure 3-24,A, illustrates the return-to-bias method. This technique uses a pulse for each binary 1 and no pulse for a binary 0. In this system the drum utilizes the erase bar which produces only binary 0's on the surface. Therefore, when recording (writing) of a binary one is to take place, a pulse is applied to reverse the flux at that particular spot.

Figure 3-24,B, illustrates the nonreturn-to-zero method. This technique utilizes reversal of flux for a 1 and a steady flux for a 0 or a group of 0's. It is a two-level system, and there is no distinct spacing between bits in any one channel. Therefore, timing and readouts become very important in keeping the proper synchronization in the memory.

Figure 3-24,C, illustrates the return-to-zero method. This technique utilizes a pulse for each digit being recorded. The drum surface is magnetized in one direction for a 1 and in the opposite direction for 0. The application of these pulses is controlled by a master timing unit within the computer. Therefore, spacing of information is achieved; and a no-flux area exists between bits in the drum channel.

The return-to-zero method is further illustrated in block diagram form in figure 3-25. The write flip-flop is controlled by a chain of information to be recorded on the drum. If a 1 is to be recorded, the flip-flop goes into the 1 state. If a 0 is to be recorded, the flip-flop goes to the 0 state. Whichever side is high will enable one of the AND-gates. The flip-flop output goes to AND-gates with write pulses causing an output from AND-gate A or B. The output of the AND-gates feeds the primary of a center-tapped transformer, inducing

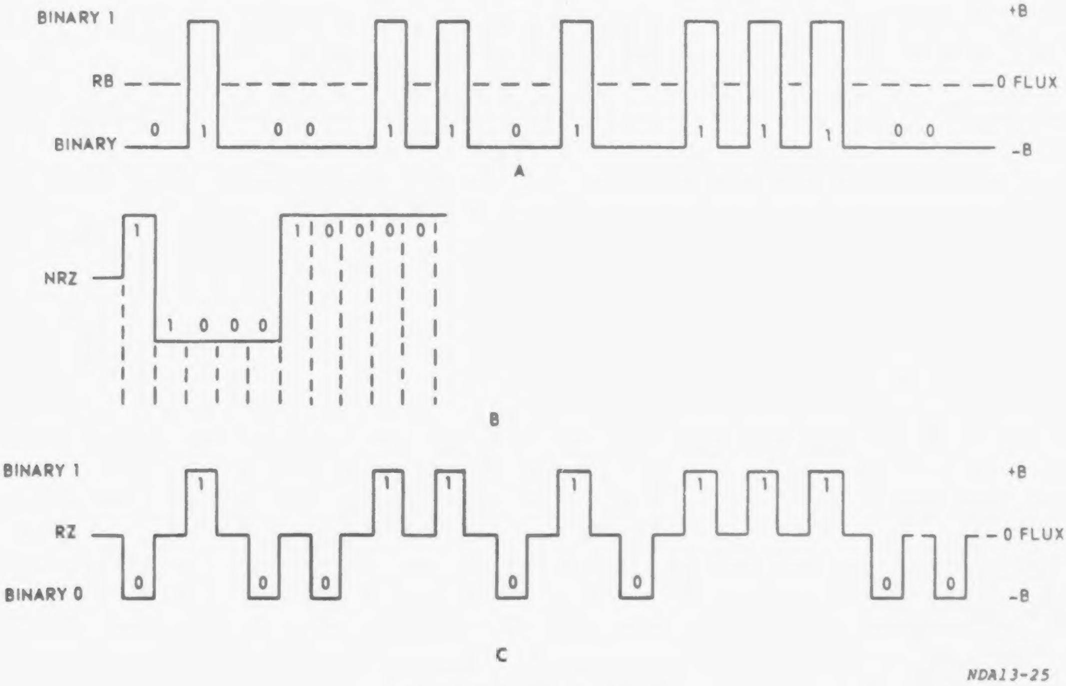
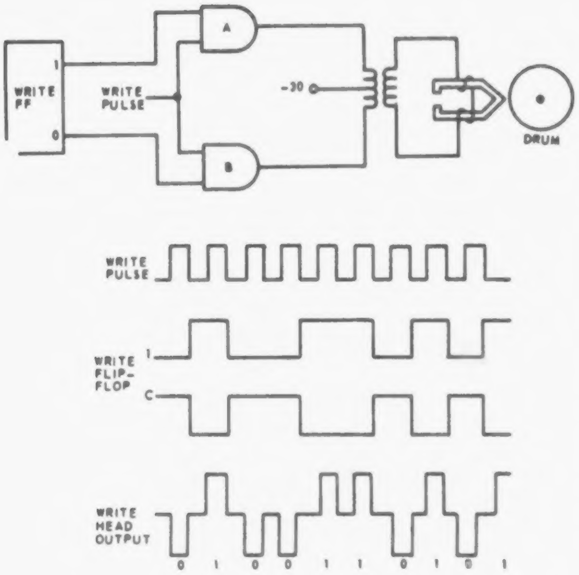

BINARY 1
RB
BINARY
+B
0 FLUX
-B
0 1 0 0 1 1 0 1 1 1 1 0 0
A
NRZ
1 1 0 0 0 1 1 0 0 0 0
B
BINARY 1
RZ
BINARY 0
+B
0 FLUX
-B
0 1 0 0 1 1 0 1 0 1 1 1 0 0
C
NDA13-25

Figure 3-24. Recording techniques.



NDA13-50

Figure 3-25. RTZ method.

currents of the opposite polarity in the secondary and setting up the polarity of the writing head itself. This produces the waveform designated "write head output," which is the same as the output previously shown for the return-to-zero method.

Parity Checks. A "parity-checking system" is a system that is used to check the validity of each computer word after it has left a storage medium or has been transmitted over transmission lines. This check is needed because noise may change the data contained in a word.

Here the parity check concerns the magnetic drum. One of two methods could be used. One method is to use an additional drum system and store identical data on both drums. Both drums are addressed at the same time and their output compared. If there is a difference, the computer sounds an alarm. This method, of course, is expensive. It is used only where a high degree of reliability is needed. The other method requires only an extra channel on the drum. The binary digits in a word are counted. If there is an odd number of 1's in the word, a binary 1 is inserted in the parity-check channel. If there is an even number of 1's in the word, a binary 0 is inserted in the parity-check channel. Then when the parity check is made, the number of 1's is counted and the count should always be even. This method is the one used most frequently.

Drum Storage Systems. There are several ways in which the computer word can be arranged on a drum. Figure 3-26 illustrates the parallel and interlaced parallel arrangements. These examples are based on an imaginary drum with four address tracks, eight storage tracks, and one parity-check track. There are 16 memory cells or segments per track. The tracks are represented by columns, and the memory cells available for a given angular position on the drum are represented by rows. In both cases, the word 01011001 and parity at address 1100 are underlined so that the student can understand the arrangement of the data on the drum. The term "track" means the same thing as "channel."

In the parallel arrangement, the bits of a word are all available at the same time. This requires more equipment than other arrangements, because all of the channels are in use at the same time. However, the parallel arrangement makes it possible to read and write information rapidly. The computer word could be arranged so that the addresses follow one another in their numerical sequence. An alternate scheme is to have the consecutive addresses separated from one another by a definite number of spaces. This is the interlaced parallel arrangement. It is used when the computer is incapable of the speed of the parallel arrangement and when other arrangements are, for some reason, not considered advantageous.

ADDRESS TRACKS	STORAGE TRACKS	PARITY CHECK
0 0 0 0	0 1 1 0 0 0 1 1	0
0 0 0 1	0 1 0 1 1 0 1 1	1
0 0 1 0	0 0 0 1 1 0 1 1	0
0 0 1 1	0 1 0 1 1 0 0 1	0
0 1 0 0	1 0 1 1 1 0 1 0	1
0 1 0 1	0 1 1 0 0 1 1 1	1
0 1 1 0	1 0 0 1 0 1 1 0	0
0 1 1 1	1 0 0 1 0 0 0 0	0
1 0 0 0	0 1 0 0 1 1 0 1	0
1 0 0 1	1 1 1 0 0 1 0 1	1
1 0 1 0	0 0 0 1 0 1 0 1	1
1 0 1 1	1 0 0 1 0 1 1 0	0
1 1 0 0	0 1 0 1 1 0 0 1	0
1 1 0 1	1 1 0 0 1 0 1 0	0
1 1 1 0	1 1 1 0 0 1 1 1	0
1 1 1 1	0 0 0 1 0 0 0 1	0

A. PARALLEL

ADDRESS TRACKS	STORAGE TRACKS	PARITY CHECK
0 0 0 0	0 1 1 0 0 0 1 1	0
0 0 1 0	0 0 0 1 1 0 1 1	0
0 1 0 0	1 0 1 1 1 0 1 0	0
0 1 1 0	1 0 0 1 0 1 1 0	0
1 0 0 0	0 1 0 0 1 1 0 1	0
1 0 1 0	0 0 0 1 0 1 0 1	1
1 1 0 0	0 1 0 1 1 0 0 1	0
1 1 1 0	1 1 1 0 0 1 1 1	0
0 0 0 1	0 1 0 1 1 0 1 1	1
0 0 1 1	0 1 0 1 1 0 0 1	0
0 1 0 1	0 1 1 0 0 1 1 1	1
0 1 1 1	1 0 0 1 0 0 0 0	0
1 0 0 1	1 1 1 0 0 1 0 1	1
1 0 1 1	1 0 0 1 0 1 1 0	1
1 1 0 1	1 1 0 0 1 0 1 0	0
1 1 1 1	0 0 0 1 0 0 0 1	0

B. PARALLEL INTERLACE

NDA13-51

Figure 3-26. Drum storage arrangements.

Addressing the Drum. Figure 3-27 is a block diagram of a parallel magnetic drum system. Words may be written on the drum surface by any one of the eight bands of read-write heads illustrated in figure 3-27. Each band of read-write heads is associated with 13 different channels. Thirteen bit words can be stored at 1024 different angular positions or slots making a drum capacity of 8192 words (8X1024). To address any location, 13 bits are needed in the address register, 3 bits for band selection, and 10 bits for angular position selection.

When words are to be written, they are stored in the storage register until the storage control unit is informed by a central control unit that writing is to occur. The three flip-flops of the address register then provide input signals to the band selection decoder which selects one of the eight bands (0-7). The 10 flip-flops of the address register are used for angular position selection 0-1023. Their output signals are compared in the coincidence detector with the write heads counter, which is triggered by the output pulses of a separate timing channel that has previously had binary 1's permanently recorded on it. When the output signals of the 10 flip-flops in the address register compare with the output signals of the angular position counter, a signal is applied to the storage control unit causing the word in the storage register to be recorded on the drum surface at the selected location. Any word previously recorded in that location is destroyed. After recording has taken place, the storage control unit informs the central control unit that the operation has been completed.

When words are to be read from the drum surface, the central control unit informs the storage control unit that reading is to occur. The three flip-flops in the address register provide proper input signals to the selection decoder to select one of the eight bands. The coincidence detector then compares the output of the angular position counter with the output of the 10 flip-flops in the address register. When the outputs compare, a signal is applied to the storage control unit, causing the selected word to be read from the drum surface. The word is stored in the storage register until it is either rewritten or destroyed.

Exercises (030):

1. The magnetic drum is a type of ______________ track memory.

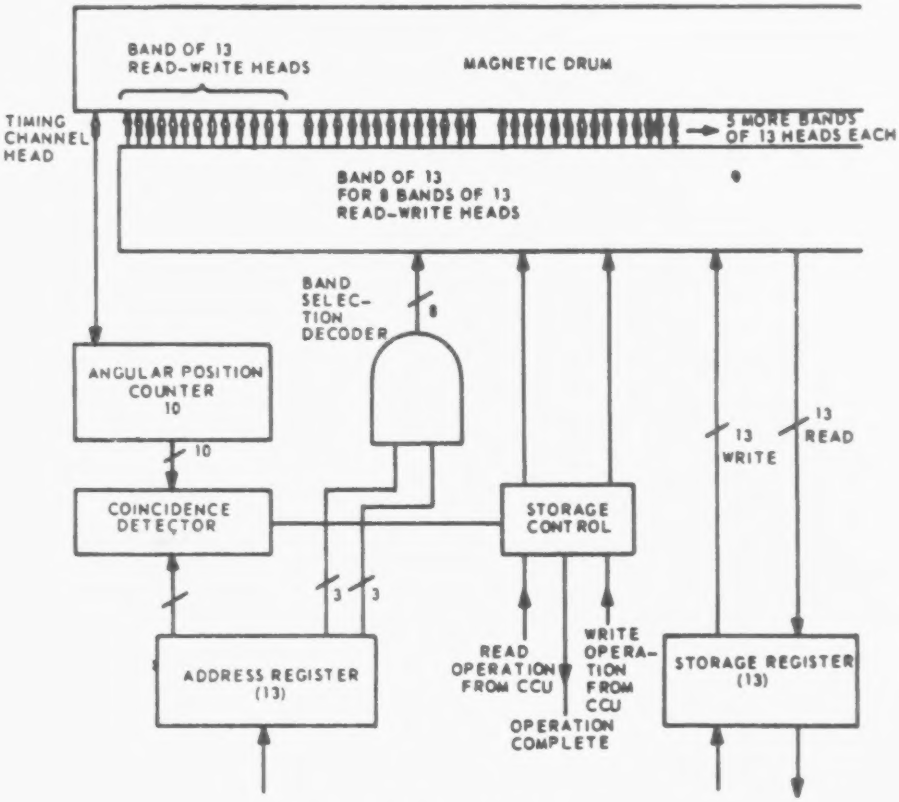

BAND OF 13
READ-WRITE HEADS
MAGNETIC DRUM
TIMING
CHANNEL
HEAD
5 MORE BANDS
OF 13 HEADS EACH
BAND OF 13
FOR 8 BANDS OF 13
READ-WRITE HEADS
BAND
SELEC-
TION
DECODER
8
ANGULAR POSITION
COUNTER
10
10
13
WRITE
13
READ
COINCIDENCE
DETECTOR
STORAGE
CONTROL
3
3
ADDRESS REGISTER
(13)
READ
OPERATION
FROM CCU
WRITE
OPERA-
TION
FROM
CCU
OPERATION
COMPLETE
STORAGE REGISTER
(13)

Figure 3-27. Drum addressing.

. A drawn channel is controlled by at least one ______ ______ ______.

3. A magnetic drum normally has up to ______ channels per inch.

4. The airgap in a read-write head reduces ______ loss.

5. What does figure 3-28 represent?

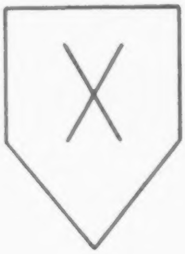


Figure 3-28. Figure for objective 030, exercise 5.

6. In the return-to-zero method of writing on a magnetic drum, if a binary 1 equals +6 volts, then a binary 0 equals ______ ______.

7. Why is timing most important in the NRZ method of recording?

8. The ______ drum method of parity is used when a high degree of reliability is needed.

9. Which type of parity is used most frequently?

10. When information is to be written on a magnetic drum, the band selection decoder receives input signals from the three flip-flops in the ______ register.

031. Specify design and operating characteristics of magnetic tape.

Magnetic Tape. Magnetic tape, fast and economical, is still a popular input/output medium used in a large proportion of computer processing systems. Being economical, it is often used when the processing does not justify the use of more expensive on-line random processing media such as magnetic disk.

Tape drives. Magnetic tape drives are available which use seven- and nine-channel tapes (refer to fig. 3-29). The seven-channel drives correspond to the expanded binary coded decimal (EBCD) coding form and the nine-channel drives correspond to the expanded binary coded decimal interchange code (EBCDIC). The seven-channel drives will be used on machines using EBCD and nine-channel drives on machines using EBCDIC. Most computers using EBCDIC with nine-channel tapes will have one seven-channel tape drive to allow input from other computer systems EBCD. Translation from EBCD to EBCDIC may be accomplished with either hardware or software.

Tape sensing. Magnetic tape used with different computer systems will have similar mechanics but may differ in minor details. All reels of magnetic tape must have some method provided to detect the beginning and ending of a reel of tape. For this purpose, reflective strips (photosensing markers) are placed on the nonrecording (shiny) side approximately 10 feet from the ends of the reel of tape (see fig. 3-30). These reflective strips enable the tape drive to sense the beginning and end of the usable portion of tape. Some systems also have a marker indicating the physical end of the tape. This may be a clear strip of plastic near the very end of the tape.

Loading. To load a tape, the operator mounts the reel of tape on the tape drive and positions the tape so that the beginning-of-tape reflective strip is beyond the beginning of tape photosensor (see fig. 3-30). The tape is then rewound until the beginning of tape photosensor senses the light reflected from the beginning of tape reflective strip. The tape drive pauses in this position and is now ready to read or write, awaiting the command from the computer. This is called load point.

If the tape is an output tape, writing will continue until the end-of-tape warning (ETW) photosensor senses the ETW reflective strip. If writing has not been completed when ETW is sensed, the rest of the block followed by the end-of-tape mark and trailer label will be written, even though the ETW has been passed.

On some systems, the sensing of the ETW will set a switch which may be interrogated programmatically. On these systems, it is the programmer's responsibility to check for the ETW. If the program is not written to check for the ETW, then if the ETW is reached during a write operation, writing will continue beyond the ETW and on to the clear end-of-tape marker. When sensing the end-of-tape marker, the tape drive will stop and the program will not be able to reactivate that tape drive without operator intervention.

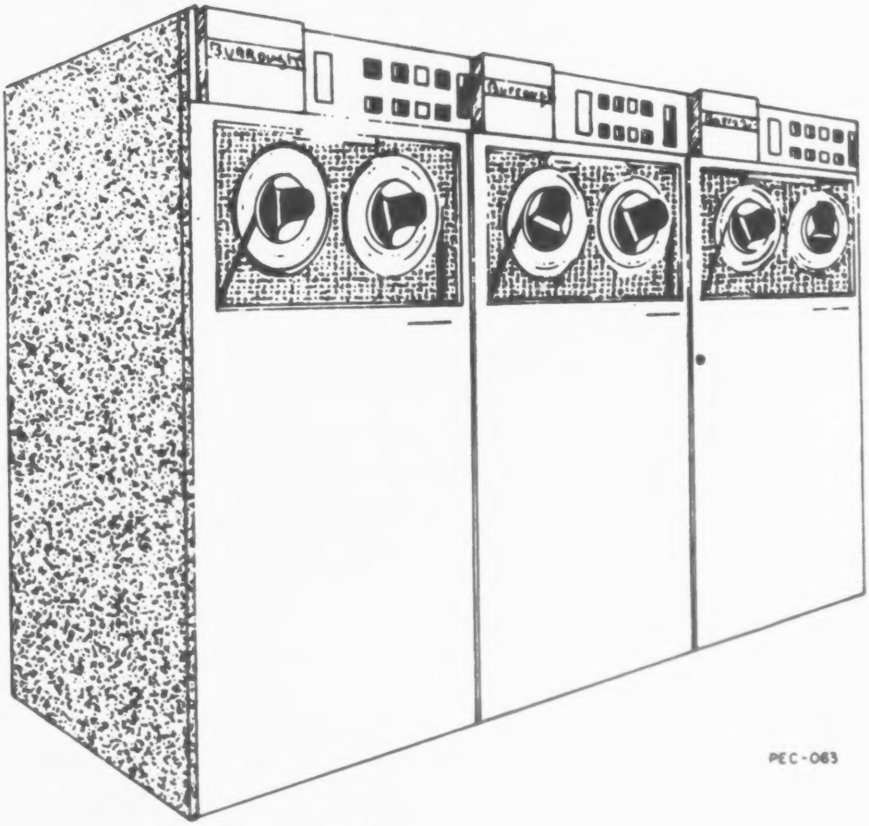


Figure 3-29. Magnetic tape units.

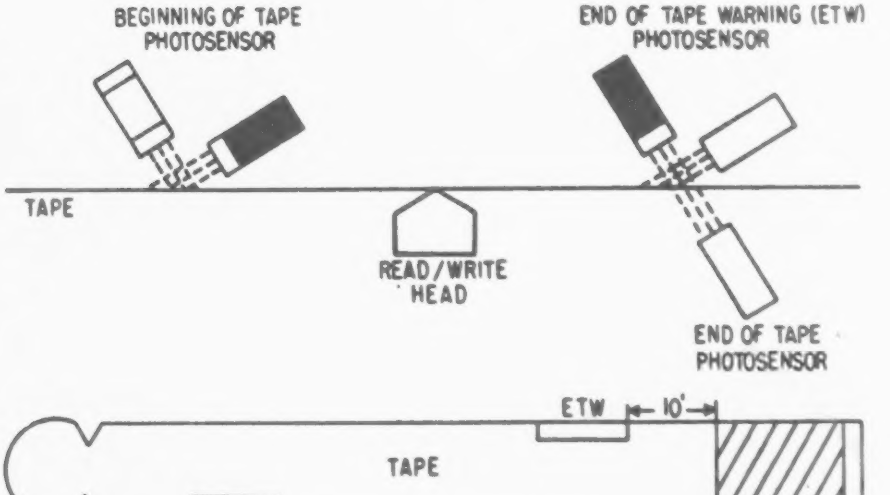

BEGINNING OF TAPE PHOTOSENSOR
END OF TAPE WARNING (ETW) PHOTOSENSOR
TAPE
READ/WRITE HEAD
END OF TAPE PHOTOSENSOR
ETW
10'
TAPE
10'
BEGINING OF TAPE REFLECTIVE STRIP
CLEAR STRIP OF PLASTIC INDICATING END OF TAPE

Figure 3-30. Beginning and end-of-tape markers.

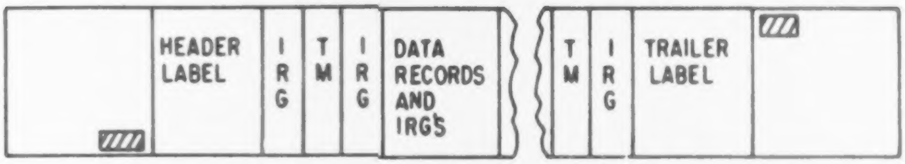


Figure 3-31. Tape labels.

Internal labels. Internal labels are simply identifying records written on magnetic tape (refer to fig. 3-31). Header (beginning of file or reel) and trailer (end of file or reel) label records are written on each reel of magnetic tape, followed by a tape mark. The tape mark is a one-character record indicating the end of a header label or the beginning of a trailer label. A header label is the first record on each reel of a magnetic tape file. The exact format for this label will vary from system to system, but it will contain essentially the same information: file name, reel number, creation date, and purge date. The trailer label will contain such information as file identification, reel number, block count, record count, and a sentinel for end of file or end of reel. The end-of-file sentinel indicates that the entire file has been read. The end-of-reel sentinel indicates the end of one reel in a multiple-reel file (see fig. 3-31).

External labels. External labels are those labels which are physically attached to the reel of tape. There are two types: reel identification and file identification labels. The reel identification label will be a permanent fixture on the magnetic tape reel and will contain the reel serial number used by the magnetic tape library, the date is was received from the manufacturer, and the current length of tape. The second type of external label is solely for file identification and will contain such information as file name, reel number (one of three, two of three, etc.), run date, purge date, and trunk number the file was created upon.

Tape file formats. There are three basic file formats available to the programmer. These are the single-reel file, the multiple-reel file, and the multiple-file reel (see fig. 3-32). The single-reel file, as the name implies, is an entire file contained on a single reel. The header and trailer labels will indicate that the reel number is one, and the trailer label will have the end-of-file sentinel set indicating the end of the file.

A multiple-reel is a file which contains two or more reels of data. The first and all but the very last reel will contain end-of-reel sentinels indicating that there is more data to follow on subsequent reels. The last reel of the file will have the end-of-file sentinel set to indicate the end of that reel and also that it is the end of the file.

The multiple-file reel is a reel of magnetic tape containing two or more files of data. The first file will have a header label and tape mark followed by data, and then the tape mark and trailer label. This is the same as in the single-reel file format. With this format, the trailer label of the first file is followed by an inter-record gap (IRG) (a blank space left on tape for the purpose of separating records) and the header label, tape mark, and data and trailer label for a second file. These two entirely separate files will be contained on one reel of tape. This method is useful as long as the two files are not needed simultaneously.

The simplest tape file organization format (easiest to program) is fixed length, unblocked records. With this type of format all records within the file are the same length and each record is separated from the next consecutive record by an IRG. (An IRG, or inter-record gap, was defined as a blank space left on tape for the purpose of separating records. It is usually 1/2 to 3/4 inch and allows the tape handler a space to slow down, stop, and regain speed between read instructions.) For example, in converting a card file to a tape file we could use this format. Each card would be considered an entire record; thus, the tape file would have an 80-character record followed by an IRG and the second 80-character record.

Assuming tape density of 800 bits per inch (bpi) (normal tape density), and an inter-record gap of 1/2 inch, the file would have 1/10 inch of data followed by 1/2 inch of IRG, or less than 20 percent of the tape being used for data (see fig. 3-33).

The second type of tape file organization format is variable-length unblocked records. This is the same as the first, except that the records may be of different lengths. This has the advantage of making each record as consolidated as possible. With fixed-length records, certain data fields within some of the records may not be used; but with variable-length records, each record has only the data fields that are being used. Thus, using the example above, some of the cards in the card file may have an excess of unused fields; and others may have two or more cards being used for the same record. This record format is shown in figure 3-34.

Although variable-length records have the advantage of not wasting any space within the record, they do offer some disadvantages to the programmer. Each record may have a different record format, so the programmer must be able to determine what length the record is and where each of the data fields within the record is located.

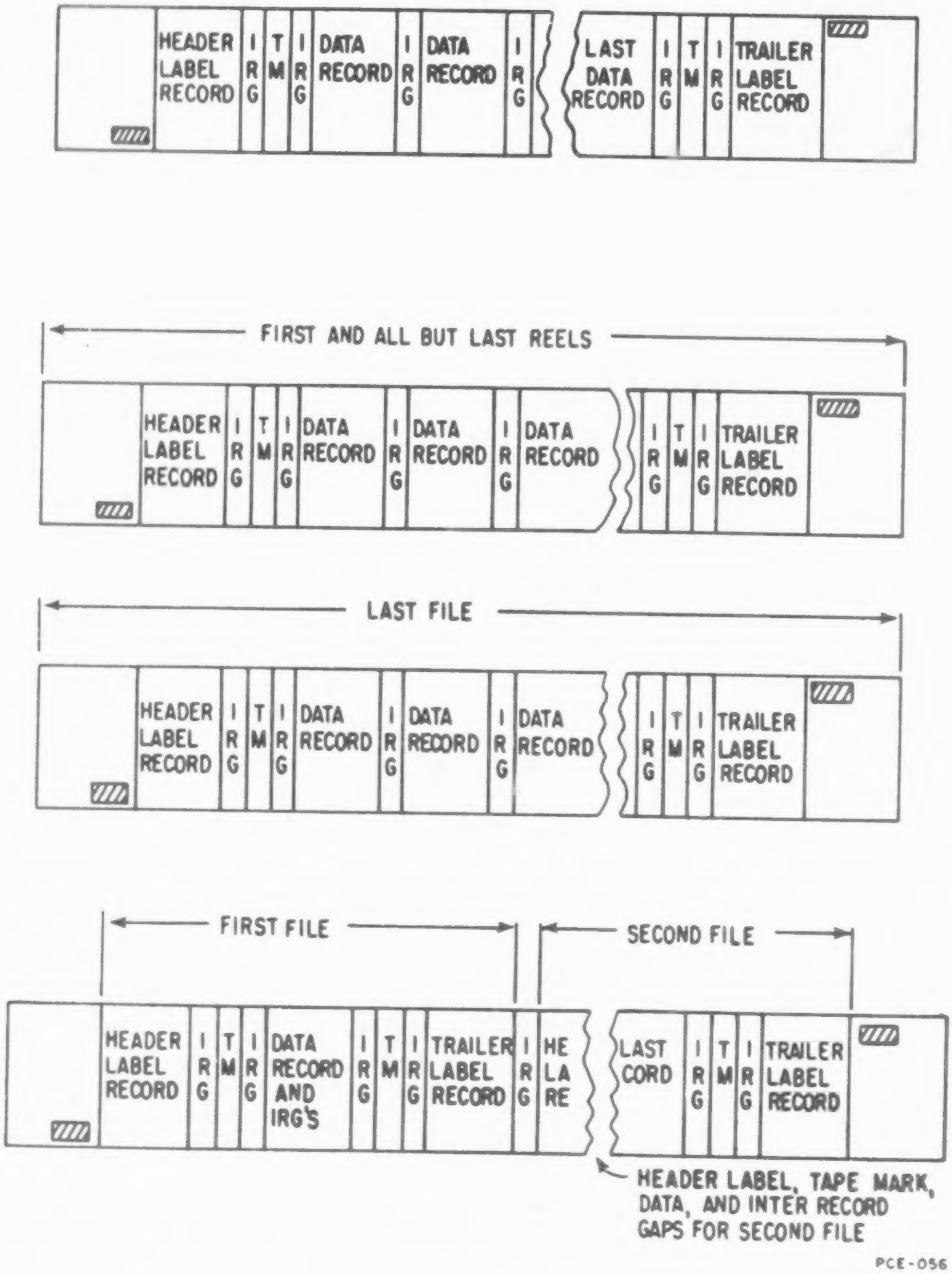

HEADER LABEL RECORD
IRG
TM
IRG
DATA RECORD
IRG
DATA RECORD
IRG
LAST DATA RECORD
IRG
TM
IRG
TRAILER LABEL RECORD
FIRST AND ALL BUT LAST REELS
HEADER LABEL RECORD
IRG
TM
IRG
DATA RECORD
IRG
DATA RECORD
IRG
DATA RECORD
IRG
TM
IRG
TRAILER LABEL RECORD
LAST FILE
HEADER LABEL RECORD
IRG
TM
IRG
DATA RECORD
IRG
DATA RECORD
IRG
DATA RECORD
IRG
TM
IRG
TRAILER LABEL RECORD
FIRST FILE
SECOND FILE
HEADER LABEL RECORD
IRG
TM
IRG
DATA RECORD AND IRG'S
IRG
TM
IRG
TRAILER LABEL RECORD
IRG
HE LA RE
LAST CORD
IRG
TM
IRG
TRAILER LABEL RECORD
HEADER LABEL, TAPE MARK, DATA, AND INTER RECORD GAPS FOR SECOND FILE
PCE-056

Figure 3-32. Tape file formats.

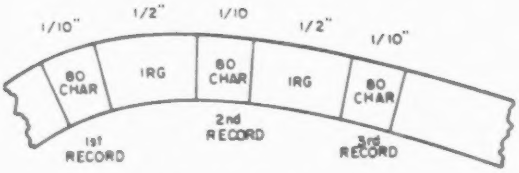

1/10"
1/2"
1/10
1/2"
1/10"
80 CHAR
IRG
80 CHAR
IRG
80 CHAR
1st RECORD
2nd RECORD
3rd RECORD

Figure 3-33. Fixed-length unblocked records.

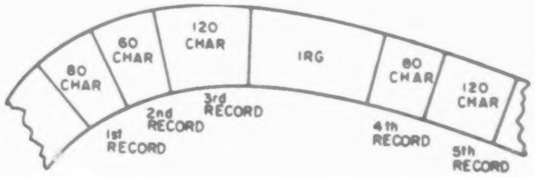

80 CHAR
60 CHAR
120 CHAR
IRG
80 CHAR
120 CHAR
1st RECORD
2nd RECORD
3rd RECORD
4th RECORD
5th RECORD

Figure 3-34. Variable-length unblocked records.

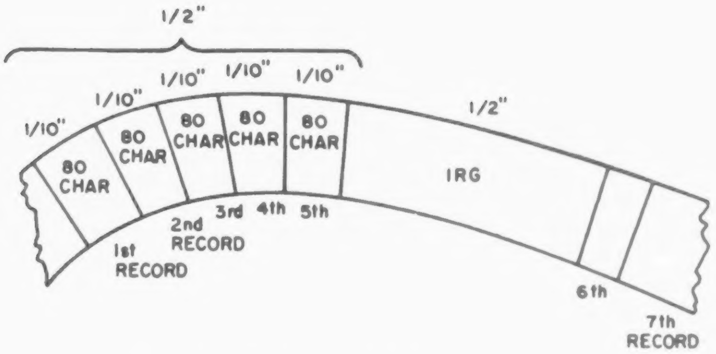


Figure 3-35. Fixed-length blocked records.

Another problem that is common to both fixed-length and variable-length unblocked records is that quite often an excess of tape is wasted on inter-record gaps because the record lengths are small. This problem is solved by the remaining two tape file organization formats: fixed-length and variable-length blocked records.

Blocking of records means that several records, whether fixed or variable length, are grouped between two IRGs. This has the obvious advantage of conserving tape because fewer IRGs are required for the same number of records. See figures 3-35 and 3-36.

Using the previous example and again assuming 800 bpi and 1/2 inch IRG, if we block five records per block (80 characters per record), we get 1/2 inch of data and 1/2 inch of IRG, or 50-percent tape utilization (fig. 3-35) as opposed to less than 20 percent before blocking (fig. 3-36). We can increase the tape utilization even more by blocking 10 records per block. With this we would get 1 inch of data for each 1/2 inch of IRG, or approximately 67-percent utilization.

Blocking of records also has certain disadvantages to the programmer. Since the tape reader reads from IRG to IRG, the entire block of records must be read at the same time. This will require a larger input area in your program, which could be a serious consideration if internal storage is critical. Also, since the entire block is read at one time, the programmer must be able to determine where one record ends and the next one starts. This is no problem for fixed-lengths records, but for variable-length records this could be a big problem.

There are several methods of determining the length of each variable-length record in a block. One method is with the use of a record mark. This is a special character in the record. Another method is to specify the length of the record in the first three or four positions of the record.

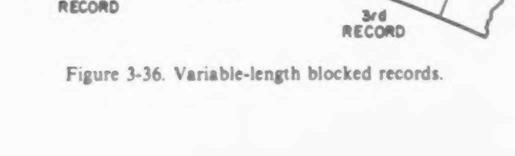


Figure 3-36. Variable-length blocked records.

The type of format selected for a particular file will depend primarily on two criteria: time and space available. For the discussion of these two criteria, we will be talking about the two extremes of the four formats: fixed-length, unblocked and variable-length, blocked records. The other two formats will be a compromise between these two extremes.

The criterion of time can be further broken down into two categories: programmer time and execution time. Fixed-length unblocked records require a less complicated program, and thus the programmer takes less time to achieve an operational program. However, the execution time will probably be greater because more read instructions will have to be executed to complete the program, such as one read instruction per record as opposed to one read instruction per 5 or 10 records (depending on how many records are in each block). For variable-length blocked records, a more complicated program is required; so the programmer time will be greater, although, as mentioned above, execution time will be less.

The second criterion, that of space, refers to the amount of internal storage available, as well as the amount of storage on magnetic tape. The space on tape was already mentioned; fixed-length unblocked records require more space on tape than do variable-length blocked records. However, variable-length blocked records require more internal storage than do the other types.

The programmer must then decide which file format is most advantageous for the particular situation with which he or she is involved. The decision must be based on computer time and space available, as well as overall production time (from initial problem to final solution) available. The proper format could mean the difference between one reel of magnetic tape as opposed to two or more reels of tape. The decision must be made for each problem. The correct decision will save time and money in the long run.

A sequential file was described as one whose records are arrayed in a logical sequence. This sequence is established by a key field or fields. For example, the file may be sequenced according to the key field Social Security number in ascending sequence. Thus, the key field is SSN and the logical sequence is from smallest to largest. The following illustration shows a file arranged alphabetically by name in ascending sequence within a descending sequence based on rank, an occurrence that is not at all uncommon.

COL AMMENS
COL WILLIAMS
MAJ CUMMINGS
MAJ JOHNS
MAJ SMITH
CAPT ADAMS
CAPT DIXON
CAPT FISHER
2LT ZIMMERMAN

Sequential files are normally associated with magnetic tape files, although sequential files can also be maintained on an immediate access storage device.

Two basic tape processing methods are available for use with magnetic tape. They are tape change and tape rewrite. Both of these methods are based on the batch processing concept. The transactions that are to be matched against a master file must be grouped onto one tape and sorted into the exact same sequence as the master tape.

Once the transactions are sorted, the method may be chosen to process the transactions against the master file. In the rewrite method, the transactions are matched against the master file. If there is no transaction for a master file record, that master file record is written without change to the updated master file. If there is a transaction for a master file record, the master record is updated with data from the transaction record and then written onto the updated master file (see fig. 3-37).

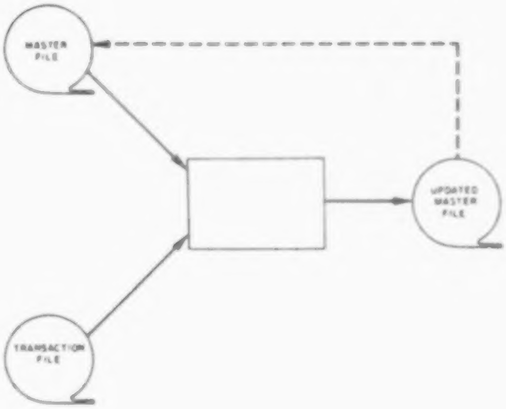


Figure 3-37. Tape rewrite.

The rewrite method is very inefficient and time-consuming when there are few transactions. For example, if the master file consists of nine reels of tape and the transaction tape contains only one record, then nine reels of tape will have to be written to process the one transaction. The rewrite method is appropriate when there is a high percentage of transactions to process against the master file. When a small number of transactions are expected to be processed against a large master file, it may be best to use the tape change method of processing.

The tape change method duplicates only those records being updated by a transaction (see fig. 3-38). On the first cycle, there will be no old active items file

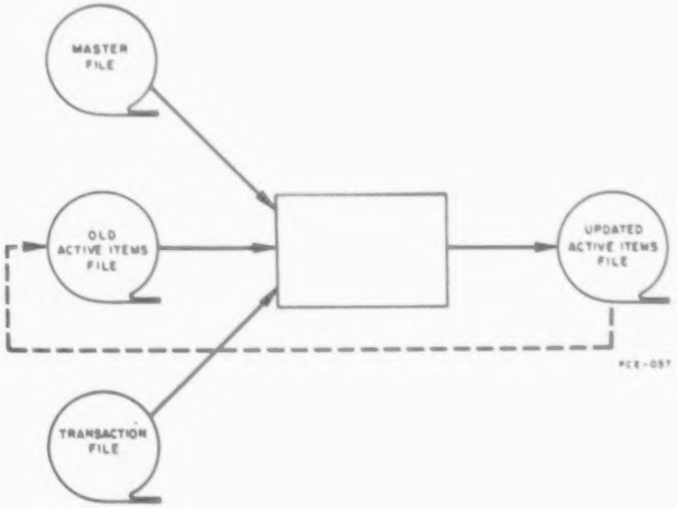


Figure 3-38. Tape change.

as input. The transaction file will be matched against the master file, and the updated items are written onto the updated active items file. On the second cycle, the updated active items file and the old active items file become input files. In this run, the transaction file is matched against the old active items file and the master file.

The transaction record is first compared with an old active items file record. If there is a match, the old active items record, being more current than the equivalent master file record, is updated and written to the updated active items file. If there is not a match between the transaction file record and an old active items file record, the record on the master file is then the most current and is updated and written onto the updated active items file.

Only those items of the master file having activity are involved in being written and rewritten. All of the other items in the master file will not be involved in the input/output process other than being read for comparison.

Application of the tape change method may be illustrated with an example of a wholesale grocery company. In this type of company, 10 percent of its inventory may do 90 percent of its business. If the company had a master inventory file consisting of 10 reels of tape which had to be updated daily, the 10 percent of items that do the most business could be grouped together on the first reel of tape. Then, for most of the items in the transaction file, only the first reel of the master tape would need to be read. Rarely would it be necessary to read all 10 reels.

With the tape change method, the updated active items file becomes larger and larger. When the point arrives where the updated items file becomes too bulky and awkward or the master file outdated, it will be necessary to perform a rewrite with the updated active items file matched against the master file.

Exercises (031):

Indicate whether the following statements are true or false by marking T or F.

_____ 1. Magnetic tape is used for on-line random processing.

_____ 2. Computer systems must have some method of detecting the end of a reel of tape.

_____ 3. On some systems, the end of tape may be determined by the program.

_____ 4. External labels are classified as header and trailer labels.

_____ 5. Internal labels are records written on tape.

_____ 6. The single-reel file is a single reel containing several files.

_____ 7. A multiple-reel file is a series of reels containing one file.

_____ 8. An inter-record gap separates records.

_____ 9. Variable length records are an advantage for the programmer.

_____ 10. Blocking of records means that there is more than one record between record gaps.

_____ 11. Blocked records require a larger input area in the program.

_____ 12. Execution time is less with fixed-length records.

_____ 13. Variable-length blocked records require more space on tape.

_____ 14. Files on magnetic tape are sequential.

_____ 15. The rewrite method of tape processing is very efficient whenever there are few transactions.

032. Specify design and operating characteristics and applications of a magnetic disk memory, and define basic terms associated with it.

Magnetic Disk Memory. Magnetic disks are a convenient medium for semipermanent storage of mass volumes of production programs. For many applications disks are superior to magnetic tape for rapid acquisition and storage of mass volumes of systems programs and data.

Magnetic disks resemble phonograph records which have been coated with iron oxide. The disks (or records) are arranged in stacks in much the same way as a record stack in a modern "jukebox." All of the disks are continuously revolving and spaced apart so that a record head, driven by an access mechanism, can be positioned between the disks.

The data is recorded at certain addresses on a specific disk. When readout of a particular bit of storage is desired, the recording head is automatically positioned and the data is read "serially" from the surface of the selected disk.

The basic unit of information on the disk is a character. By design each character contains a given number of bits (for fixed-word applications). One or more of these characters in a group form a record. A circular data track (fig. 3-39) consists of one or more records, associated record addresses, gaps, and data track identification. A track of information, as shown in this figure, is defined in more detail later. A number of data tracks aligned on vertically arranged disks (fig. 3-40) form a cylinder of information. A magnetic disk file system may contain one or more blanks (modules). Each module contains a specified number of disks with their associated cylinders and data tracks. The flow chart in figure 3-41 illustrates the steps necessary to retrieve or store information.

Refer to figure 3-39 as you study the characteristics of a typical circular data track

a. Track format. One basic operation principle must be understood. The data is read or stored serially, character by character and bit by bit on a data track. All data tracks have the maximum storage capacity.

b. Index points. Each data track (fig. 3-39) must contain a minimum number of control and addressing characters in a specific format. The index points are magnetic marks that indicate the beginning and end of a data track. They are used for timing purposes. In

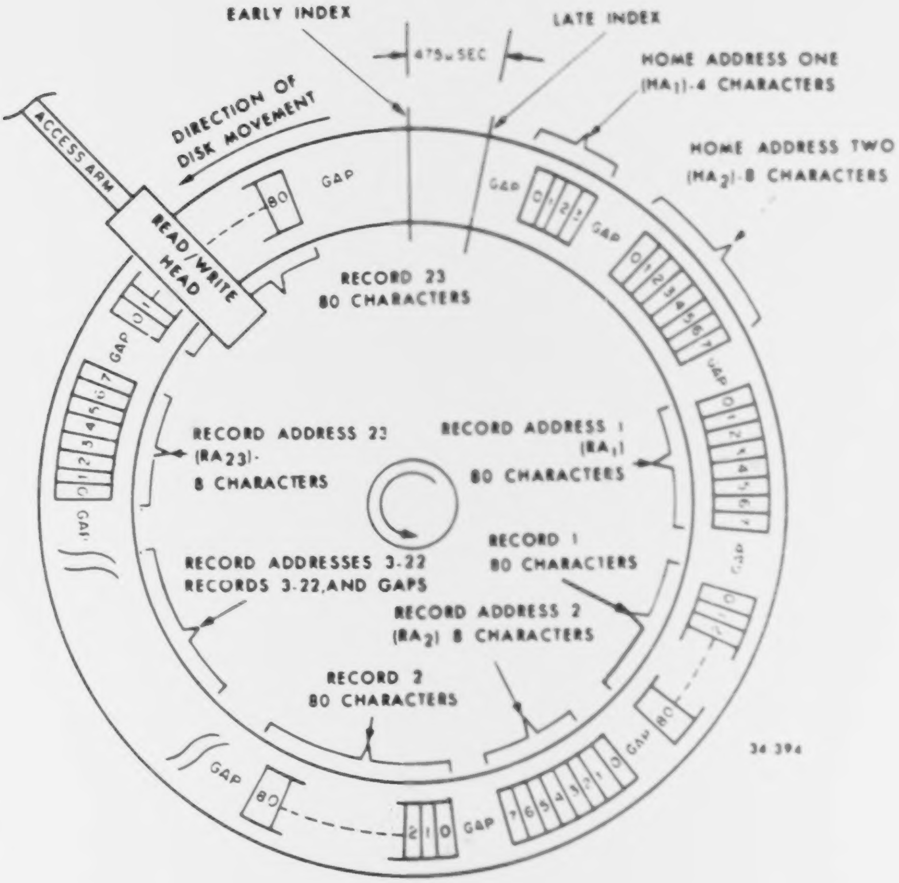

EARLY INDEX
LATE INDEX
475 μSEC
HOME ADDRESS ONE (HA1)-4 CHARACTERS
HOME ADDRESS TWO (HA2)-8 CHARACTERS
DIRECTION OF DISK MOVEMENT
ACCESS ARM
READ/WRITE HEAD
GAP
80
RECORD 23 80 CHARACTERS
RECORD ADDRESS 23 (RA23)- 8 CHARACTERS
RECORD ADDRESS 1 (RA1) 80 CHARACTERS
RECORD 1 80 CHARACTERS
RECORD ADDRESSES 3-22 RECORDS 3-22, AND GAPS
RECORD ADDRESS 2 (RA2) 8 CHARACTERS
RECORD 2 80 CHARACTERS
0 1 2 3 4 5 6 7
34 394

Figure 3-39. Circular data track.

this case, the late index follows the early index by approximately 475 microseconds.

c. Home address one. Home address one (HA_1) is a prerecorded number. It is represented in figure 3-39 as having four digits. This is the actual address of a data track and is, therefore, referred to as the track number. HA_1 is the first group of characters to follow the late index.

d. Home address two. Home address two (HA_2) is written by the programmer and serves as a programmer's aid. It can be used for category and file numbers as identifiers. It can also be used as a file protect code. For example, it could be used to signal to a second user that this track is normally not to be used.

e. Record address. The record address is also a programmer's aid. It can be used to identify individual records or for any other convenient purposes.

f. Gaps. Gaps are written between all addresses and record areas on a data track. They are used to distinguish specific data areas. Gaps usually contain check characters and internal synchronization information required for proper disk system operation.

Generally, one disk surface in a given module is used only for format tracks. A format track affects all data tracks of the cylinder that are vertically in line with it. The format track determines what is written on each track of its associated cylinder. The programmer can write or modify the format tracks as desired.

Track capacity is directly related to the configuration of the format tracks. The maximum number of characters that can be written on a data track must include home address two (HA_2), record addresses (RA), and gaps.

System Components. A minimum disk file system consists of a disk file controller (DFC), a file control unit, and a disk storage unit. The disk file controller controls the operation of the file control and disk storage units. Specifically, it provides the following functions necessary for the operation of the disk system:

- Data assembly and disassembly.
- Signal level conversion.
- Function translation.
- Parity check.

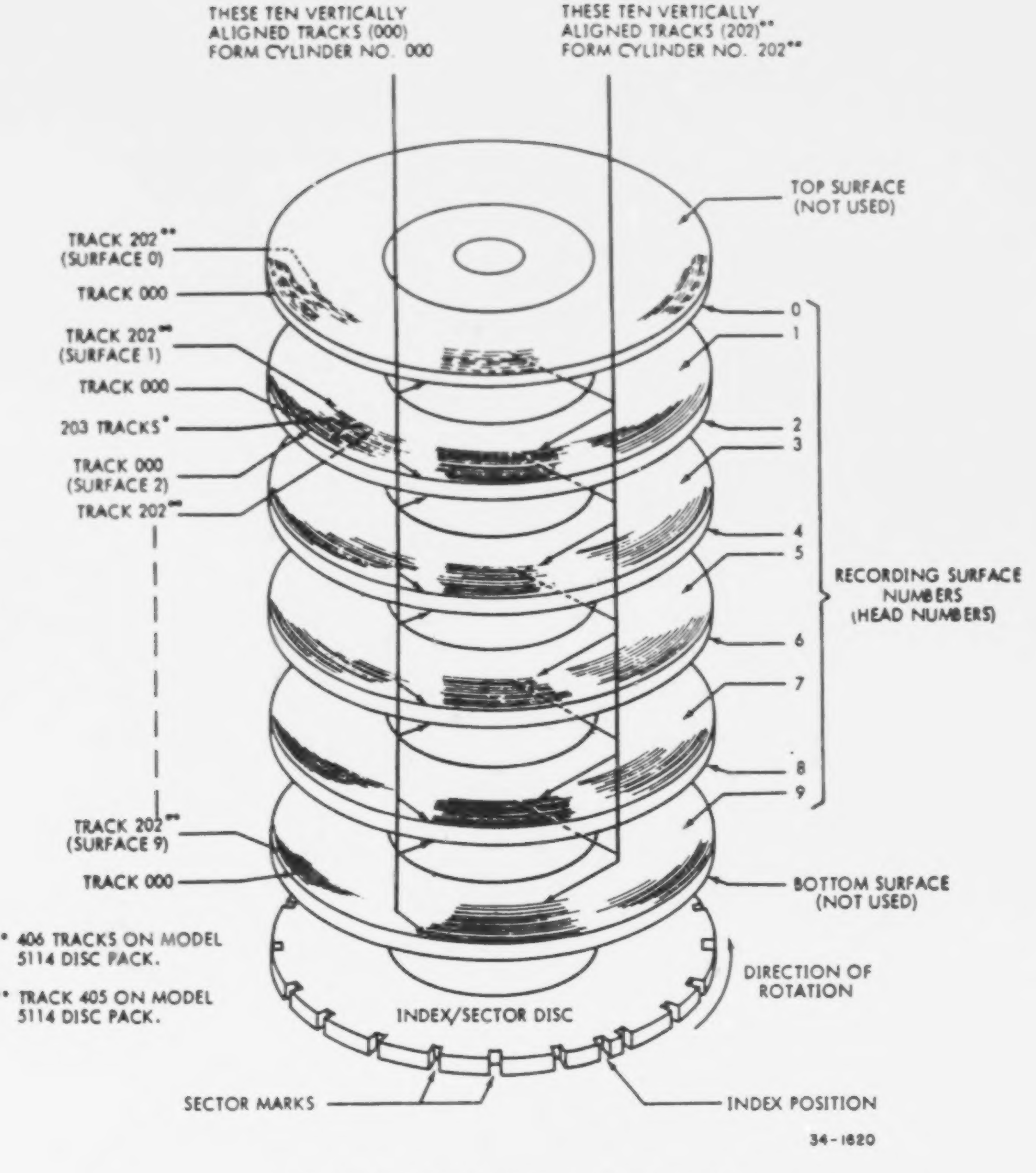

THESE TEN VERTICALLY ALIGNED TRACKS (000) FORM CYLINDER NO. 000
THESE TEN VERTICALLY ALIGNED TRACKS (202)** FORM CYLINDER NO. 202**
TOP SURFACE (NOT USED)
TRACK 202** (SURFACE 0)
TRACK 000
TRACK 202** (SURFACE 1)
TRACK 000
203 TRACKS*
TRACK 000 (SURFACE 2)
TRACK 202**
0
1
2
3
4
5
6
7
8
9
RECORDING SURFACE NUMBERS (HEAD NUMBERS)
TRACK 202** (SURFACE 9)
TRACK 000
BOTTOM SURFACE (NOT USED)
* 406 TRACKS ON MODEL 5114 DISC PACK.
** TRACK 405 ON MODEL 5114 DISC PACK.
DIRECTION OF ROTATION
INDEX/SECTOR DISC
SECTOR MARKS
INDEX POSITION
34-1620

Figure 3-40. Description of data storage disk pack assembly.

- Parity generation.
- Sense and status response.

The file control unit accepts instructions from the disk file controller, decodes them, and transmits the appropriate signals to the disk storage unit. In addition, the file control unit provides control timing, read, write and sense timing, parity and character generation, parity and character checking, format circuits, and data comparison circuitry. The disk storage unit contains magnetic disk modules. The disks in each module are mounted on a common shaft and rotate at a given speed.

Exercises (032):

1. For what type of storage are magnetic disks used?

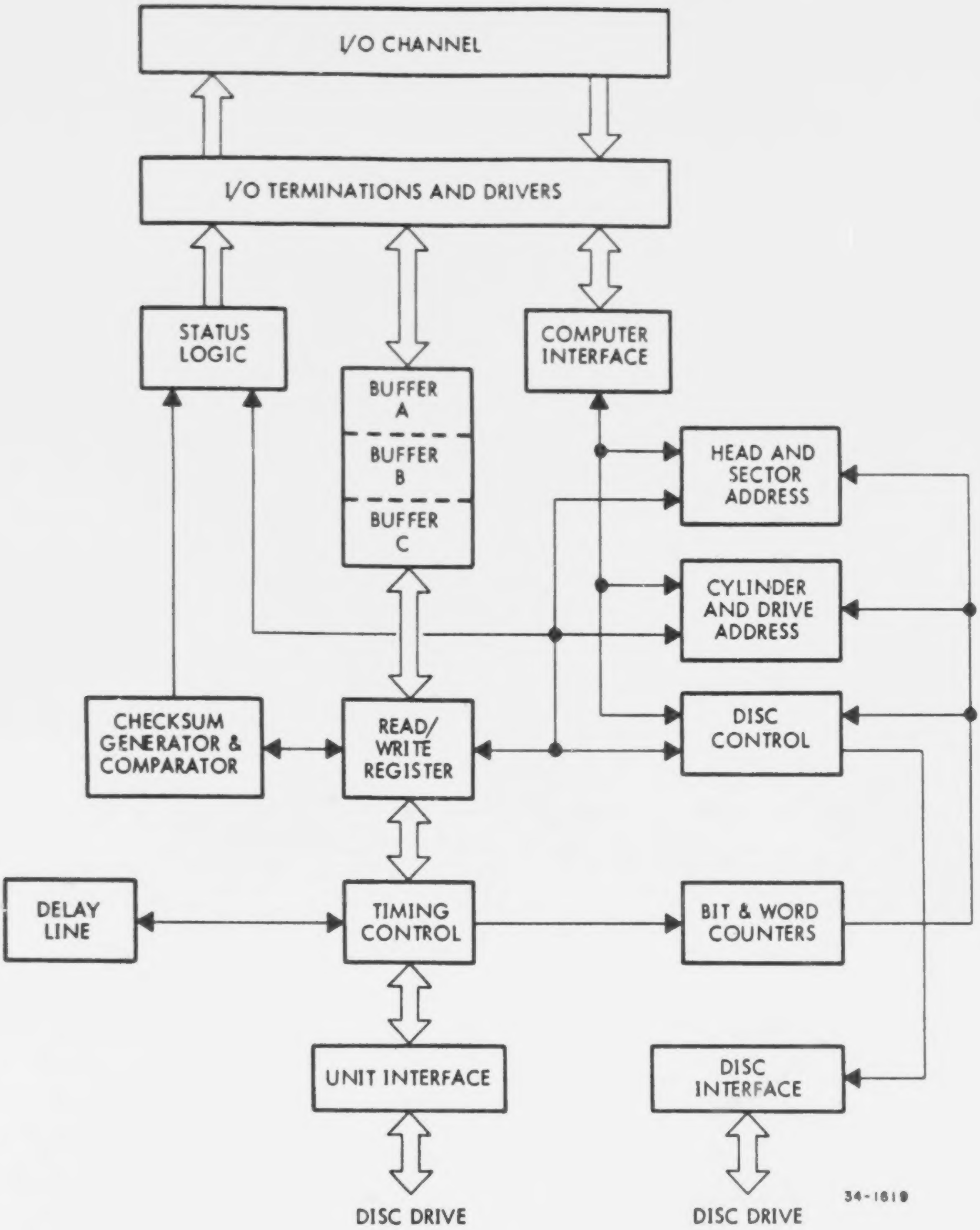

I/O CHANNEL
I/O TERMINATIONS AND DRIVERS
STATUS LOGIC
COMPUTER INTERFACE
BUFFER A
BUFFER B
BUFFER C
HEAD AND SECTOR ADDRESS
CYLINDER AND DRIVE ADDRESS
DISC CONTROL
CHECKSUM GENERATOR & COMPARATOR
READ/ WRITE REGISTER
DELAY LINE
TIMING CONTROL
BIT & WORD COUNTERS
UNIT INTERFACE
DISC INTERFACE
DISC DRIVE
DISC DRIVE
34-1619

Figure 3-41. Flow chart illustrating storage and retrieval of data from disks.

2. Describe a magnetic disk memory.

3. How is data from a magnetic disk read off?

4. What is the basic unit of information on the disk?

5. What is a cylinder of information?

6. What are index points and how are they used?

7. Which address is referred to as the track number and is prerecorded?

8. What is home address two (HA_2) used for?

9. Name another address that is also a programmer's aid.

10. Where would you expect to find a gap and what would it consist of?

11. What is determined by the format track?

12. Of what does a minimum disk file system consist?

13. Name six necessary functions of the disk file controller.

14. What is the purpose of the file control unit?

15. Where are the magnetic disk modules located?

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Glossary

Access Time—The time it takes to address a storage location in main memory or other storage media, and to receive the data or instruction that was stored there.

Accumulator—A register in the CPU which holds the operand for arithmetic and logical operations and receives the result from such operations.

Address—A computer word(s) which specifies a location in memory.

ALU—The *a*rithmetic *l*ogic *u*nit, the basic part of a computer which performs arithmetic and logical computations/operations.

Architecture—How a computer system is arranged internally; its organizational setup.

Asynchronous—Digital operations that occur without the use of a system clock. One circuit is activated by the output from a previous circuit (see Synchronous).

Baud—Commonly referred to as a bit rate; i.e., bits per second in serial data communication.

Bubble Memory—A memory device which stores bits using magnetic bubbles moving in thin film. A bubble represents 1, and the absence of a bubble represents a 0.

Bus—The communications lines in a computer system which carry data, instructions, and addresses to the various parts in a system. For example, an 8-bit word (byte) computer uses an eight-line data bus.

Byte—A series of 8 binary bits used as a unit.

CPU—The *c*entral *p*rocessing *u*nit of a computer which interprets and executes program instructions. It may also contain ROM/RAM, ALU special register groups, and timing circuits.

Cycle Time—A continuously repeating time period, set by system timing circuits, at which computer operations are performed. It may take one or more of these cycle times to execute one operation.

DMA—*D*irect *m*emory *a*ccess, a method of allowing an I/O device to have direct access to main memory. It permits a direct transfer of data and/or instructions between the I/O device and memory.

EAROM—An *e*lectrically *a*lterable *r*ead-*o*nly *m*emory. This ROM can be programmed and erased without removing it from the circuit.

EEPROM—An *e*lectrically *e*rasable, *p*rogrammable ROM.

EPROM—An *e*rasable, *p*rogrammable ROM. To erase this type of ROM usually requires an ultraviolet light source.

Execute—The computer process which interprets an instruction and then completes the requested action, such as add, subtract, or compare.

Fetch—A CPU operation in which the CPU goes to memory to get a word.

Firmware—A computer program or microprogram which is put in a ROM, usually by the computer maker.

Hardware—All of the equipment that makes up a computer system.

Index Register—A register in the CPU, used to alter a memory address.

I/O—The input/output part of a computer system is the circuits and equipment used to communicate with the CPU. I/O equipment consists of peripheral devices such as disks, tapes, and terminals. I/O circuits provide the lines of communication.

Instruction—A computer word which tells the CPU where to obtain operands, what operations to perform, what to do with results, and sometimes where to obtain the next instruction.

Interrupt—A signal, usually generated by an I/O device, which tells the CPU that the device wishes to send or receive data.

LSI—*L*arge-*s*cale *i*ntegration, integrated circuits made using this technique contain from 100 to 1000 gates per chip. Microprocessors are one form of LSI.

Machine Cycle—The time it takes to get a word from memory. The smallest period of time necessary for a complete process of computer action to repeat itself.

Memory—A basic part of the computer which is used to store data and instructions required by the CPU for its operations.

Microcomputer—A computer which uses a microprocessor as its CPU.

Microprocessor—A large scale integrated circuit which contains all the logic and, in some cases, a microprogram in ROM; used to perform the functions of a CPU.

Microprogram—A group of microinstructions stored in ROM which are used to implement the main program's instructions (macroinstructions).

MOSFET—*M*etal *O*xide *S*emiconductor *F*ield-*E*ffect *T*ransistor. The primary active element used in LSI chips for microprocessors and solid-state memories.

Nibble—A series of 4 binary bits worked on as a unit.

NMOS—Integrated circuits which use N channel MOSFETs to implement a function; i.e., microprocessors.

Peripherals—Equipment used with the computer for the input and output of data.

PROM—A *p*rogrammable *r*ead-*o*nly *m*emory. A solid-state memory which can be programmed by the user.

RAM—A *r*andom *a*ccess *m*emory in LSI form that can be read from or written to. This form of solid-state memory is volatile.

ROM—A *r*ead-*o*nly *m*emory in LSI form which can only be read from. Information in this device is stored there at time of manufacture, unless it is a PROM or EPROM.

Sequential Access—A storage technique in which the items of information stored become available only in a one after the other sequence, whether or not all the information or only some of it is desired; for example, magnetic tape storage.

Software—Computer programs used to direct the operations of a computer system.

SSI—*S*mall-*s*cale *i*ntegration. A technique used in integrated circuits to produce the equivalent of 10-12 logic gates on one chip.

Stack—A set of registers or memory locations used to store a specific number of computer words. They are stored in such a fashion that the last word stored is the first word retrieved. It is a temporary storage location which helps speed up CPU operations.

Stack Pointer—A register used to point to the location in stack where the next word is to be stored or retrieved.

Synchronous—Digital circuits using a common timing source (clock); all operations will occur in sync with this clock (compare with Asynchronous).

Terminal—A peripheral device used for the input and output of data in a computer system. Usually employs a visual display.

Tri-State Logic—Logic used to permit several different circuits to have access to the same communication lines (bus). The three states are HIGH, LOW, and the high-impedance or disconnect state.

Ultraviolet PROM—A programmable read-only memory which can be erased by the application of ultraviolet light. The PROM package has a translucent window on top used when erasing.

VLSI—*V*ery *l*arge-*s*cale *i*ntegration. An integrated circuit technique which provides the equivalent of 1000 or more gates on the chip.

Answers for Exercises

CHAPTER 1

Reference:

001 - 1. (1) d.
 (2) c.
 (3) a.
 (4) b.
 (5) d.
 (6) c.
 (7) b and c.

002 - 1. Microprocessor.
002 - 2. A desk-top computer using standard discrete and integrated circuit logic.
002 - 3. A small computer that uses a microprocessor as the CPU.

003 - 1. ROM.
003 - 2. The parallel peripheral interface adapter or PIA.
003 - 3. 12.
003 - 4. Calculated from data in the program and data in internal registers.
003 - 5. Software permanently stored in ROM.
003 - 6. No. The data is nonvolatile.
003 - 7. The RAM loses its data if power is removed.
003 - 8. The total set of addresses which the microprocessor can generate.

004 - 1. The n-channel MOSFET.
004 - 2. The control and register sections.
004 - 3. By decoding contents of instruction register and timing counter.
004 - 4. The process status register.
004 - 5. LIFO—the last word stored is the first word retrieved.
004 - 6. The high-impedance or disconnect state.

CHAPTER 2

005 - 1. They must be able to modify all data so that it is acceptable to the computer during the input phase of the operation and to present data in usable form during the output phase. Second, the devices must operate quickly and efficiently in conjunction with the computer.
005 - 2. Slowness of response.
005 - 3. Program I/O cycles to run concurrently with computation and simultaneously provide multiplexed inputs to the computer from several I/O devices.

006 - 1. They operate at high speeds and are connected directly to the computer.
006 - 2. Usually, when large amounts of data are being processed and when very little computation is required.
006 - 3. Equipment that prepares (and sometimes processes) data external to the computer.
006 - 4. Sorters, card punches, and tabulators.
006 - 5. They serve as intermediate storage devices to facilitate transfer of data between two media whose operating speeds are difficult or impossible to synchronize.
006 - 6. Reading data slowly from the input device and, at a later time, writing this data at electronic speeds into the main memory. It must also be capable of reading in data at electronic speeds from the main memory and writing this data slowly at the output device.

007 - 1. The IBM type.
007 - 2. Zones.
007 - 3. Alphabetical.
007 - 4. Pulse-no-pulse (digital).
007 - 5. Single; single.
007 - 6. As input/output medium.
007 - 7. The number of columns, the RRC has 90 columns and the IBM has 80.

008 - 1. In parallel form, longitudinally across the matrix.
008 - 2. 960.
008 - 3. Temporary storage of data en route to the computer.
008 - 4. It causes the 9's row to be read at the reading station.
008 - 5. The drive lines in the matrix are activated, and their selected cores are switched to the 1 state.
008 - 6. By one each time a 12-bit column is transferred.
008 - 7. The computer is available for other operations while the read-in is in progress.

009 - 1. Punched cards.
009 - 2. Sequentially.
009 - 3. 4.
009 - 4. Zone.
009 - 5. Mylar.

010 - 1. Storage.
010 - 2. Input.
010 - 3. Brushes.
010 - 4. Slower; less.

011 - 1. (1) d.
 (2) f.
 (3) g.
 (4) a.
 (5) b.
 (6) c.
 (7) c.
 (8) b.
 (9) c.
 (10) h.
 (11) i.

012 - 1. Storage.
012 - 2. False.
012 - 3. Code.
012 - 4. False.
012 - 5. Input; output.
012 - 6. Starts; stops.
012 - 7. False.
012 - 8. Tension.

013 - 1. The floppy disk unit.
013 - 2. The Winchester.
013 - 3. Hard disk units.
013 - 4. Track and/or sector address.
013 - 5. Index.
013 - 6. The disk drive controller.
013 - 7. Magnetically recorded on an oxide-coated disk in concentric circles called tracks.

014 - 1. Approximately 8.35 ms.
014 - 2. Decreased.
014 - 3. Speed of disk rotation, whether moving or fixed heads are used, the size, number, and the material of the disks, and the recording technique used.
014 - 4. A combination of random and sequential.
014 - 5. Fixed heads are being used for faster access but at higher cost.
014 - 6. MFM.
014 - 7. Every time you needed data from another disk the operator would have to physically change the disk.

015 - 1. Input.
015 - 2. The typehead ball is tilted and rotated.
015 - 3. A = tilt 1, rotate -5; N = tilt 0, rotate 2; D = tilt 2, rotate 1.
015 - 4. D6 is the control bit; D7 is the parity bit.
015 - 5. 7-bit ASCII code.
015 - 6. Two, shift-up and shift-down.
015 - 7. Tilt 0 and rotate 0, or home position.

016 - 1. When printing, the printer prints a line at a time.
016 - 2. To produce pulses that are synchronized to the rows of characters on the print row and identify these characters.
016 - 3. Wire matrix printer; it is given this name because it burns the imprint of a wire matrix character onto a specially prepared paper.
016 - 4. It channels individual pulses into separate lines that connect to the storage matrix.
016 - 5. One cycle for each line of print.
016 - 6. The electronic distributor.

017 - 1. We address that location in the 512 by 512 matrix and then pulse the sustainer voltage to 0.
017 - 2. It can be used as a self-generated visual display and as a projection display due to the transparency of the plasma panel.
017 - 3. The standard television CRT and the storage CRT.
017 - 4. The storage CRT uses a secondary emission technique inside the tube which eliminates the refresh requirement.
017 - 5. Through the use of deflection plates or coils.
017 - 6. The dumb terminal.
017 - 7. Projection displays.
017 - 8. The dumb, smart, and intelligent terminals.
017 - 9. A modulator-demodulator or data set. It is used as an interface between data transmission lines and a computer system.
017 - 10. A graphic display device.
017 - 11. Depends on sources of information needed to solve specific problems.

CHAPTER 3

018 - 1. The storage unit and the storage control unit.
018 - 2. By using DMA.
018 - 3. A storage medium, transducers for writing information into a storage medium, read and sense transducers, and an address selection mechanism.
018 - 4. Because you don't need a transducer for each storage location. Instead, common transducers are used for a number of storage locations (moving heads).
018 - 5. A magnetic core memory.

019 - 1. (1) Storage medium, (2) memory address register, (3) memory exchange register, (4) storage selection circuits, and (5) storage control.
019 - 2. Control section.
019 - 3. The storage selection circuits.
019 - 4. The control section, arithmetic section, or output section.

020 - 1. Storage capacity.
020 - 2. The time interval between the instant at which information is called from storage and the instant at which delivery is completed.
020 - 3. Random, sequential, and periodic.
020 - 4. Sequential cyclic and sequential progressive.
020 - 5. The intended computer use or purpose, physical size, cost, power consumption of the equipment, access time, and reliability.
020 - 6. The type of storage device used by the computer.

021 - 1. Tape-wound cores and ferrite cores.
021 - 2. By wrapping a tape of magnetic material around a nonmagnetic toroidal core.
021 - 3. A doughnut-shaped solid object.
021 - 4. By molding finely ground ferrite into a toroidal form and heat fusing, or sintering, the particles through heat and pressure. The ferrite used is a ceramic oxide with magnetic properties.
021 - 5. Four. Two are used for read and write selection (by reversing the direction of current flow). An inhibit wire prevents writing a 1 when a 0 is to be written, and the sense wire picks up the signal voltage generated by shifting a core from 1 to 0 in a read cycle.
021 - 6. One.
021 - 7. Arrays.
021 - 8. The coincident-current technique.
021 - 9. A current magnetizes the core in one direction, and reversing the direction of current flow reverses the direction of the flux field and the core magnetization.

022 - 1. The flux density of the core is $+B_r$.
022 - 2. 2. The flux density moves back up to $+B_s$.
022 - 3. The flux density is now $-B_r$.
022 - 4. The core would be at point $-B_s$.
022 - 5. It is called the "read pulse."
022 - 6. 1; 0.

023 - 1. Since the cores must be very small, straight current-carrying wires are used.
023 - 2. They increase the storage capacity per given area and decrease the core switching time.
023 - 3. The same as if there were a single wire carrying the vector sum of current.
023 - 4. If each wire carries 0.707 of the current required to switch a core and if a core is oriented in the direction of the resultant magnetic intensity, the core will switch. If only one wire carries current, the core will not switch.

024 - 1. With an arrangement of wires and cores called a core plane array.
024 - 2. The current must equal one-half of the current value required to switch a core (half-write current) through both Y3 and X2 in the proper direction.
024 - 3. A sense winding.
024 - 4. Only one core in an array may be switched at a time.
024 - 5. The two procedures used are: (1) a disturb pulse (equivalent to a half-read) which is a divide signal of an amplitude (coercive force) $\frac{-H_m}{2}$ applied to a core immediately after a 1 state is written in the core; and (2) strobe pulses, which involve selecting the midamplitude portion of the amplified sense pulse. Selection is done by ANDing the amplified sense pulse with an accurately timed pulse.
024 - 6. It is destroyed (destructive readout).
024 - 7. An inhibit wire is run parallel to one of the driving wires (X or Y).

025 - 1. Ferromagnetic material, permalloy, deposited (under controlled conditions in a vacuum chamber) on a substrate of thin glass.

025 - 2. After all air has been removed from the vacuum chamber, a shutter arrangement is opened and vapors from molten permalloy pass through a mask and are deposited on the substrate.
025 - 3. By the amount of time the shutter is open.
025 - 4. The direction in which the film spot is the easiest to magnetize. The direction of the magnetic field is parallel to that in which the magnetic field was applied during the deposition process.
025 - 5. Anisotropic field.
025 - 6. This transverse field causes the magnetic spot to rotate 90°.
025 - 7. The direction of the film spot's stable state of magnetization.
025 - 8. Because a concentric magnetic field is produced around a flow of current.
025 - 9. Current in the word lines and current in the bit lines.
025 - 10. They are switched toward the 0 state.

026 - 1. Only one.
026 - 2. Smaller size, reduced power requirements, and cost.
026 - 3. It is volatile. Data is lost when power is lost.
026 - 4. All data in the RAM is lost.
026 - 5. Bipolar RAMs use standard transistors connected as flip-flops, and the static MOS RAMs use MOSFETs interconnected as flip-flops. The flip-flops in each store the data.
026 - 6. Static MOS RAMs use MOSFETs connected as flip-flops to store data, and the static device does not require refreshing. The dynamic MOS RAMs use the gate capacitance of the MOSFET to store data, but this type of RAM requires refresh clocks in order to retain data in the gate capacitance.

027 - 1. The presence or absence of a diode in the ROM matrix determines if the data stored is a 1 or a 0.
027 - 2. Fuse links.
027 - 3. The reprogrammable and the nonreprogrammable.
027 - 4. Electrically or with ultraviolet light.
027 - 5. The isolated gate of a MOSFET.

028 - 1. A coil of wire is wrapped around a specially shaped core of low-retentivity magnetic material, such as Mumetal; the core is provided with an airgap.
028 - 2. So that the lines of flux passing between their tips will be parallel to the surface of the tape.
028 - 3. To reduce eddy currents.
028 - 4. It is the method of magnetizing used on magnetic tapes, indicating that the direction of flux is along the long axis of the tape.
028 - 5. To prevent abrasive wear of the pole tips or the magnetic surface.
028 - 6. So that the voltages induced in a read or write coil do not produce interference in the associated electronic driving and reproducing circuits.
028 - 7. Gap width or the gap.
028 - 8. The gap width determines the number of pulses that can be written on a given portion of the magnetic surface.
028 - 9. The reduced reluctance permits the loss of some flux that would otherwise have passed through the magnetic surface.
028 - 10. 0.001 inch.
028 - 11. Packing factor or bit density is the number of pulses or bits of information (binary digits) that can be written upon a given length of magnetic surface by a magnetic surface writing device.
028 - 12. The interaction of the magnetic fields of the storage surface.
028 - 13. By increasing the surface speed or by recording the data at a lower pulse repetition frequency.
028 - 14. One.
028 - 15. DC erasing magnetically saturates the surface, thereby masking all previously written data; AC erasing actually returns the surface to a state of 0 flux, or demagnetizes it.

029 - 1. Because the induced voltage is proportional to the rate of change of the flux.
029 - 2. In positive and negative pulse return-to-zero method.
029 - 3. When there is a maximum rate of flux change.
029 - 4. A changing flux indicates a binary 1, and a constant flux indicates a binary 0.
029 - 5. Only when the clock pulse is in coincidence with the data bit.
029 - 6. The nonreturn-to-zero method, because the clock pulses can be applied at a higher clock rate.

030 - 1. Endless.
030 - 2. Read-write head.
030 - 3. 30.
030 - 4. Hysteresis.
030 - 5. Erase head.
030 - 6. −6 volts.
030 - 7. Because there is no spacing of bits in any one channel.
030 - 8. Double.
030 - 9. Even.
030 - 10. Address.

031 - 1. F.
031 - 2. T.
031 - 3. T.
031 - 4. F.
031 - 5. T.
031 - 6. F.
031 - 7. T.
031 - 8. T.
031 - 9. F.
031 - 10. T.
031 - 11. T.
031 - 12. F.
031 - 13. F.
031 - 14. T.
031 - 15. F.

032 - 1. For semipermanent storage.
032 - 2. A magnetic disk storage unit is made up of many magnetic disks which have been coated with iron oxide. The disks are arranged in stacks as in a "jukebox." All the disks in this disk pack are continuously revolving and spaced apart so that a record head, driven by an access mechanism, can be positioned between the disks.
032 - 3. Serially.
032 - 4. The basic unit of information is a character.
032 - 5. A number of data tracks aligned vertically in a disk pack.
032 - 6. Magnetic marks that indicate the beginning and end of a data track. They are used for timing purposes.
032 - 7. The home address one (HA_1).
032 - 8. HA_2 serves as a programmer's aid. It can be used for category and file numbers and identifiers, as well as a file protect code.
032 - 9. The record address.
032 - 10. A gap is written between all address and record areas on a data track. It usually contains check characters and internal synchronization information required for proper disk system operation.
032 - 11. The way data will be read from or written on each track of its associated cylinder.
032 - 12. A disk file controller (DFC), a file control unit, and a disk storage unit.
032 - 13. Data assembly and disassembly, signal level conversion, function translation, parity check, parity generation, and sense and status response.
032 - 14. It accepts instructions from the file controller, decodes them, and transmits the appropriate signals to the disk storage unit. It also provides control timing, read, write, and sense timing, parity and character generation, parity and character checking, format circuits, and data comparison circuitry.
032 - 15. In the disk storage unit.

30554 02 S42 7811

10008 530 001 7811 SCDB

MODULE

SEMICONDUCTORS AND SEMICONDUCTOR DEVICES

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Preface

THIS TRAINING module, *Semiconductors* and *Semiconductor Devices*, is a refresher course in the electronic fundamentals of semiconductors. This module will apply to personnel in the 30XXX career ladders.

This module discusses semiconductors and their role in rectification, amplification, clamping, and the limiting of ac peak voltages by clipping.

If you have questions on the accuracy or currency of the subject matter of this text, or recommendations for its improvement, send them to the 3270th Technical Training Group/TTGCB, Lackland AFB TX 78236. NOTE: Do not use the suggestion program to submit corrections for typographical or other errors.

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This module is valued at 3 hours (1 point).

Material in this volume is technically accurate, adequate, and current as of August 1978.

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NOTE: In this module, the subject matter is developed by a series of Learning Objectives. Each of these carries a 3-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see if your answers match those in the back of this module. If your response to an exercise is incorrect, review the objective and its text.

Semiconductors and Semiconductor Devices

AS AN ELECTRONICS technician, you may have already acquired the knowledges taught in this module, but you probably need a review even though the information may not be fully applicable to the specific equipment for which you are now responsible. Although the content of this module is intended as a 3-level review, it is generally applicable to your job at all levels, and the importance of knowing it cannot be overemphasized. In this module, we discuss diodes and diode circuits, transistors, transistor amplifiers, clampers, and limiters.

1-1. Types of Diodes and Diode Circuits

N-type and P-type diode materials are formed by adding arsenic or indium to the basic crystal. When atoms of arsenic are added to silicon or germanium, the crystal gains one extra electron, forming N-type materials. P-type materials are formed when impurity atoms of indium are added to silicon or germanium crystals, causing a deficiency of electrons. Examples of solid state devices are PN junction diodes, zener diodes, silicon controlled rectifiers, and transistors.

001. State the operation of diode bias, resistance, and current flow, and list the SCR leads.

In this section, we will cover three types of solid state diodes: PN junction diodes, zener diodes, and silicon controlled rectifiers.

PN Junction Diodes. To form a junction diode, we join the two types of materials, the N-type material, with its excess of electrons and negative charge, and the P-type, with its deficiency of electrons and positive charge. The material that has negative charges is called a cathode, and the material with a positive charge is called an anode. The junction diode's block diagram and symbol are represented schematically in figure 1-1,A and B.

Forward bias. By applying a negative potential to the N-type material and a positive potential to the P-type material, we can *forward bias* the diode and cause current to flow. (See fig. 1-1,C.) Current flows through a junction diode because the forward bias reduces its resistance. What is the source of the diode's resistance and how does forward bias decrease it?

Resistance source. Where the two oppositely charged diode materials are placed together is called the *junction*. Since unlike charges attract, some of the negative and positive charges near the junction will move together and combine, depleting an area of all charges. This depleted area, called the depletion region, is electrically neutral and acts as a resistance to the remaining charges.

Decreasing resistance. Decreasing the resistance of the diode by applying forward bias allows current to flow. The negative potential of the power supply, by inserting additional electrons into the N-type material, forces electrons from the N-type material over into the P-type material. The P-type material now has more electrons than it can use, and the positive potential of the power supply will attract the electrons from the P-type material and return them to the power supply.

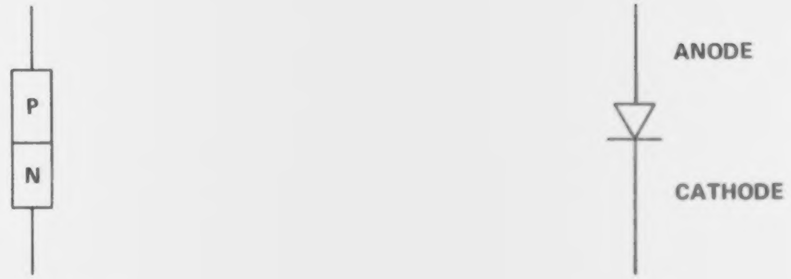
Reverse bias. The diode can be *reverse biased* by applying a positive potential to the N-type material and a negative potential to the P-type material. The positive potential on the N-type material attracts the negative charges. The negative potential at the P-type material attracts the positive charges. This causes the depletion region at the junction to widen, resistance to increase, and current to cut off. (See fig. 1-1,D.)

Zener Diodes. The zener diode, because of its construction, regulates input signals so that output will not exceed a predetermined voltage level. It is used primarily as a *voltage reference* device.

Depletion regions. The zener diode, like the junction diode, is made of N-type and P-type materials, but a few charges of opposite polarity have been added to each type of material. Each type of material now has two charges, minority charges and majority charges. The majority charges are the charges of the material itself. The minority charges are the added charges.

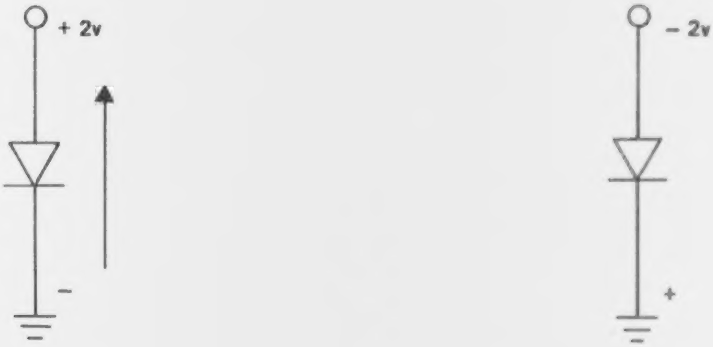
Where zener N-type and P-type materials are joined together, two depletion regions are formed, one by the majority charges and the other by the minority charges. When we apply a potential to the N-type and P-type materials, each depletion region behaves differently.

Forward bias. When the zener is *forward biased,* it acts as a PN junction diode. (See fig. 1-2,C.) The majority depletion region decreases in width,



A. BLOCK DIAGRAM

B. SYMBOL



C. FORWARD BIASED (Current Flow)

D. REVERSE BIASED (No Current Flow)

Figure 1-1. PN junction diode.

decreasing resistance, and provides a path for current flow. Even though the minority depletion region has increased in width, it has so few charges it does not offer much resistance to current flow. It only takes a small potential to cause current flow in the forward biased condition.

Reverse bias. When the zener is *reverse biased,* the minority depletion region decreases, creating a path for current flow. At the same time, however, the majority depletion region increases in width, offering high resistance to current flow. Further, because there are so many majority charges, no current will flow until the applied voltage becomes large enough to overcome the resistance of the majority charge depletion region.

The voltage required to overcome this resistance is called *breakdown voltage.* The breakdown voltage for the zener in figure 1-2 is 6 volts. No current will flow from anode to cathode until the applied voltage reaches 6 volts.

In a reverse biased configuration, the zener has very high resistance up to its breakdown voltage. (See fig. 1-2,D.) Once breakdown voltage is reached, the resistance of the zener begins to decrease. It acts just like a switch that will let current flow only at a certain voltage level. (See fig. 1-2,E.) Thus, the zener acts like an open component up to its breakdown voltage and then the resistance decreases in direct proportion to the increased voltage.

The schematic symbol for a zener closely resembles the symbol for a junction diode. The only difference is that the zener has two small lines protruding from the cathode, which gives the cathode the appearance of a Z, as shown in figure 1-2,B. The block diagram of the zener is shown in figure 1-2,A.

Silicon Controlled Rectifier. The silicon controlled rectifier (SCR), like the junction diode, rectifies an input signal. But, in the SCR, rectification is controlled by an external trigger pulse rather than by the input signal. Through the use of the external control, the rectified wave shape (voltage) can be varied. Consisting of four layers of N and P material, as shown in figure 1-3,A, the SCR has three leads—anode, gate, and cathode, as shown in figure 1-3,B.

Junctions 1 and 3. Junctions 1 and 3 are like junction diodes. They conduct when they are forward biased and cut off when they are reversed biased.

Junction 2. Specially treated to have minority charges like the zener, junction 2 is reverse biased and will conduct only when breakdown voltage is reached. No current will flow until a potential large enough to reach breakdown voltage is applied to the gate lead. Figure 1-3,C, shows the SCR with no trigger pulse applied to the gate lead. No current flows because junction 2 is reverse biased and the applied voltage has not reached breakdown level.

Figure 1-3,D, shows a trigger pulse applied to the gate. This pulse voltage causes the reverse bias of junction 2 to exceed the breakdown voltage, and current now flows from cathode to anode. The trigger pulse is of short duration. It needs to be applied only long enough to cause junction 2 to reach breakdown voltage. At breakdown voltage, current begins to flow.

The current flow through the resistance of junction 2 causes a voltage drop called *holding voltage*. The holding voltage takes over and keeps junction 2 in breakdown. Even though the trigger pulse is removed, current will continue to flow.

There are only two ways to stop current flow after the positive pulse has triggered the SCR. One way is to remove the potential from the anode and/or cathode. The other is to reverse bias junction 1 and junction 3 by changing the polarity of the potential applied to the cathode and anode.

Exercises (001):

1. To forward bias a junction diode, we must apply ______ potential to the N-type material and ______ potential to the P-type material.

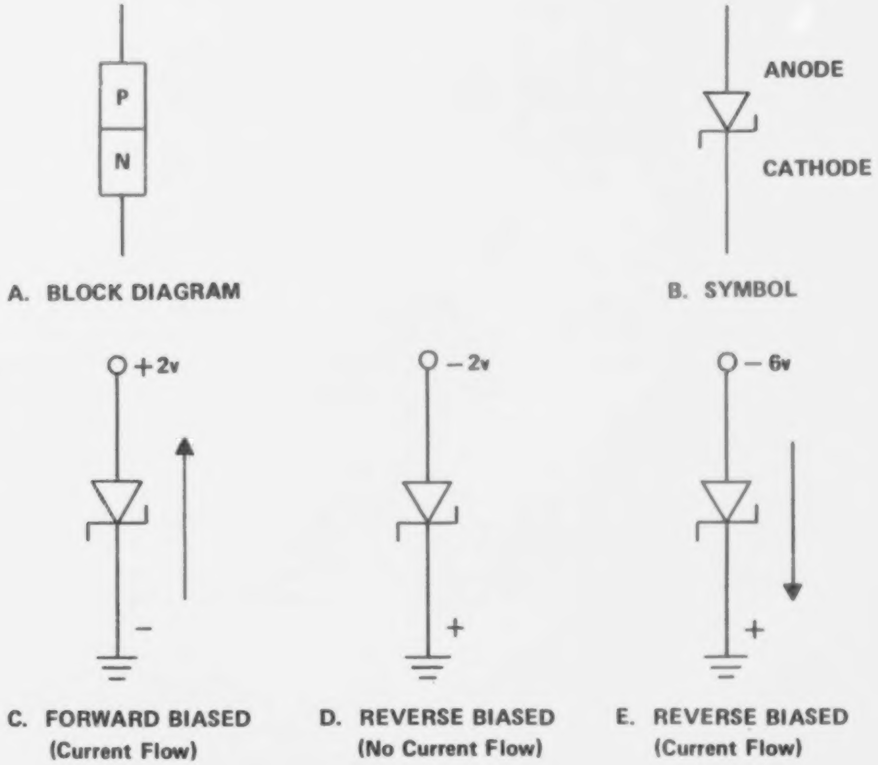
2. Current flows from the cathode to ______ in the junction diode.

3. Explain why, when a zener diode is forward biased. there is not much resistance to current flow.

4. Does the minority depletion region offer low or high resistance to current flow when the zener is forward biased?

5. In an SCR, no current will flow until a potential large enough to reach ______ ______ is applied to the gate lead.

6. Name the three leads of an SCR.



A. BLOCK DIAGRAM

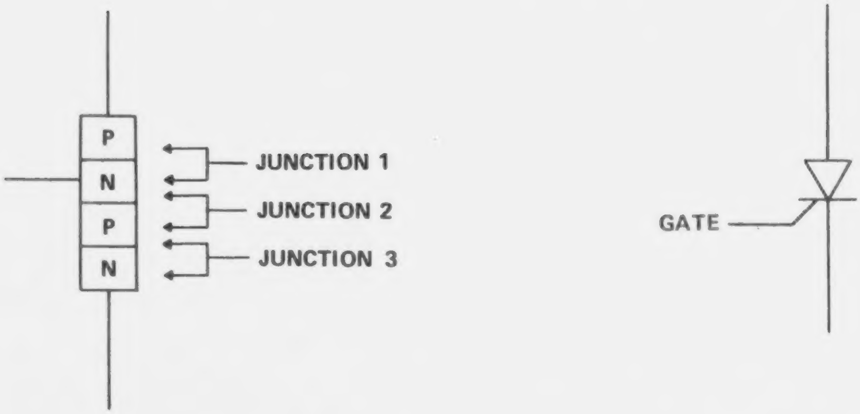
B. SYMBOL

C. FORWARD BIASED (Current Flow)

D. REVERSE BIASED (No Current Flow)

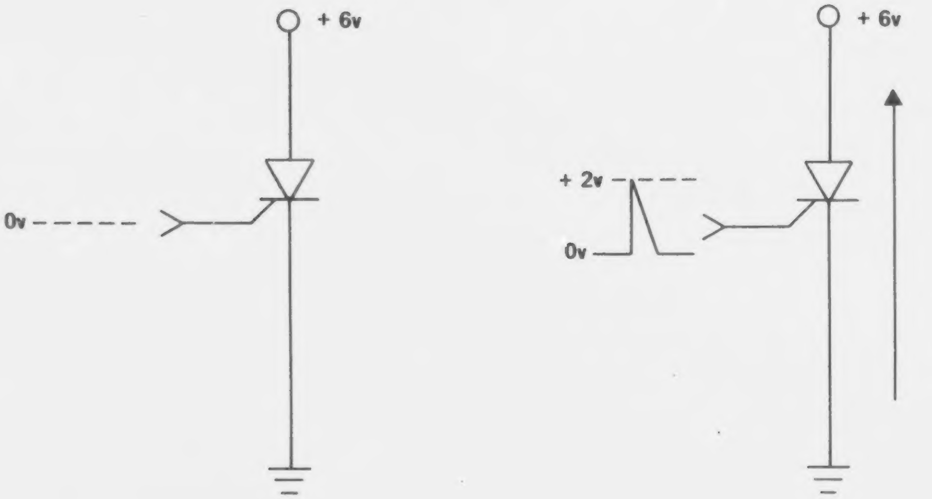
E. REVERSE BIASED (Current Flow)

Figure 1-2. Zener diode.


P
N
P
N
JUNCTION 1
JUNCTION 2
JUNCTION 3
GATE

A. BLOCK DIAGRAM

B. SYMBOL


+ 6v
0v
+ 6v
+ 2v
0v

C. NO BIAS
(No Current)

D. FORWARD BIAS
(Current Flow)

Figure 1-3. Silicon controlled rectifiers. 493

002. Compute voltage and frequency of a PN junction diode.

Like the diode tube, the junction diode rectifies ac input.

Positive Alternation. In figure 1-4,A, the positive alternation of a sine wave makes the anode positive, the diode conducts, and the current flows through R_1, causing R_1 to drop the positive applied voltage.

Negative Alternation. When the negative alternation of the input sine wave is felt at the anode, current flow stops. No current flowing through R_1 means no voltage. Thus, all the negative voltage is felt across the diode.

DC Output. The pulsating dc waveform seen across either the diode or the resistor is only half of the input waveform. Maximum output voltage will be one-half of the peak-to-peak input voltage. The frequency of the output signal will be the same as that of the input and is stated in terms of pulses per second (PPS). The output signal can be either positive or negative pulses, depending on which component the output is taken from. The four possible configurations of this basic half-wave rectifier and the resulting output of each are displayed in figure 1-4.

Exercises (002):

1. If an ac input signal is applied to a diode rectifier circuit and the output taken across the resistor is zero volts, is the diode conducting or cut off?

2. If the input to a half-wave rectifier is 20 volts peak to peak, 200 Hz, the output will be ______ volts dc at ______ pulses per second.

003. Answer questions about the output of a zener diode as an ac input changes direction of bias.

Positive Alternation. When a changing input signal is applied to a zener, as shown in figure 1-5,A, the positive alternation of the input reverse biases the zener. If breakdown voltage is 6 volts, the zener will act like an open between zero and 6 volts. No current will flow, so the applied voltage would be read as the zener output. At 6 volts, breakdown occurs and current begins to flow. As the input rises to 10 volts, current continues to increase, but voltage at the output remains 6 volts. Output remains at 6 volts because zener resistance decreases in direct proportion to any increase of input voltage above 6 volts.

Negative Alternation. During the negative alternation, the zener majority charges are forward biased and offer very little resistance to current flow. With this low resistance, R_1 drops the applied voltage, and voltage across the zener is zero volts. Thus, the output is rectified and held to a minimum of 6 volts.

Two Cycles of Input. Let us consider two cycles of input applied, as shown in figure 1-5,B. Keep in mind that the entire input signal (applied voltage) must be accounted for. At T_0 and T_2 the cathode (N material) is positive and the zener reverse biased. As the zener begins to conduct, R_2 has the largest resistance, so it drops the remaining part of the applied voltage.

Note that the zener limited the output to 3 volts, and R_2 dropped the remaining part of the positive alternations.

At T_1 or T_3 the zener, being forward biased, has very little resistance. R_2 now drops all the applied voltage and the zener output is zero volts.

Continuous Input. The circuit in figure 1-5,C, has a continuous input signal which varies in magnitude. The zener's breakdown voltage of 5 volts will not allow the output voltage to exceed 5 volts, regardless of input.

Note the second positive alternation of output on the schematic and chart. It is the exact reproduction of input. The reason for this is that breakdown voltage was not reached, the zener did not conduct, and the entire voltage was dropped across the zener.

Exercises (003):

1. Does current flow through the entire positive alternation of input in figure 1-5,A?

2. Is the resistance of the zener in figure 1-5,A, lowest at the positive 10-volt peak of the input or at zero volts?

3. What was the breakdown voltage for the zener in figure 1-5,B?

4. Does the combined voltage drop of R_2 and the zener equal applied voltage during the positive alternation of input in figure 1-5,B?

5. In figure 1-5,C, why is the output pulse from T_2 to T_3 an exact reproduction of input?

6. In figure 1-5,C, when the voltage level of input is less than breakdown voltage, is the output clipped?

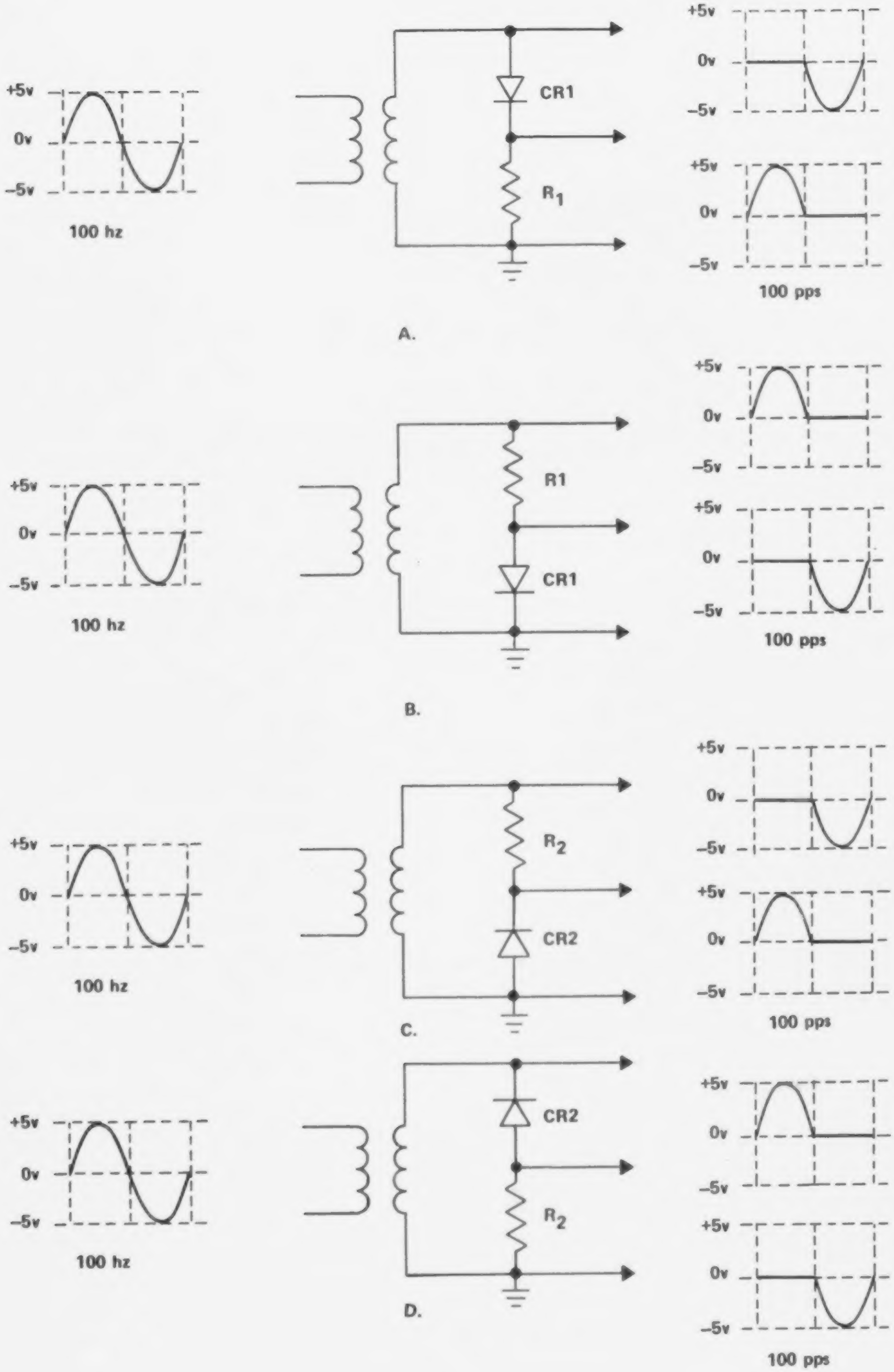
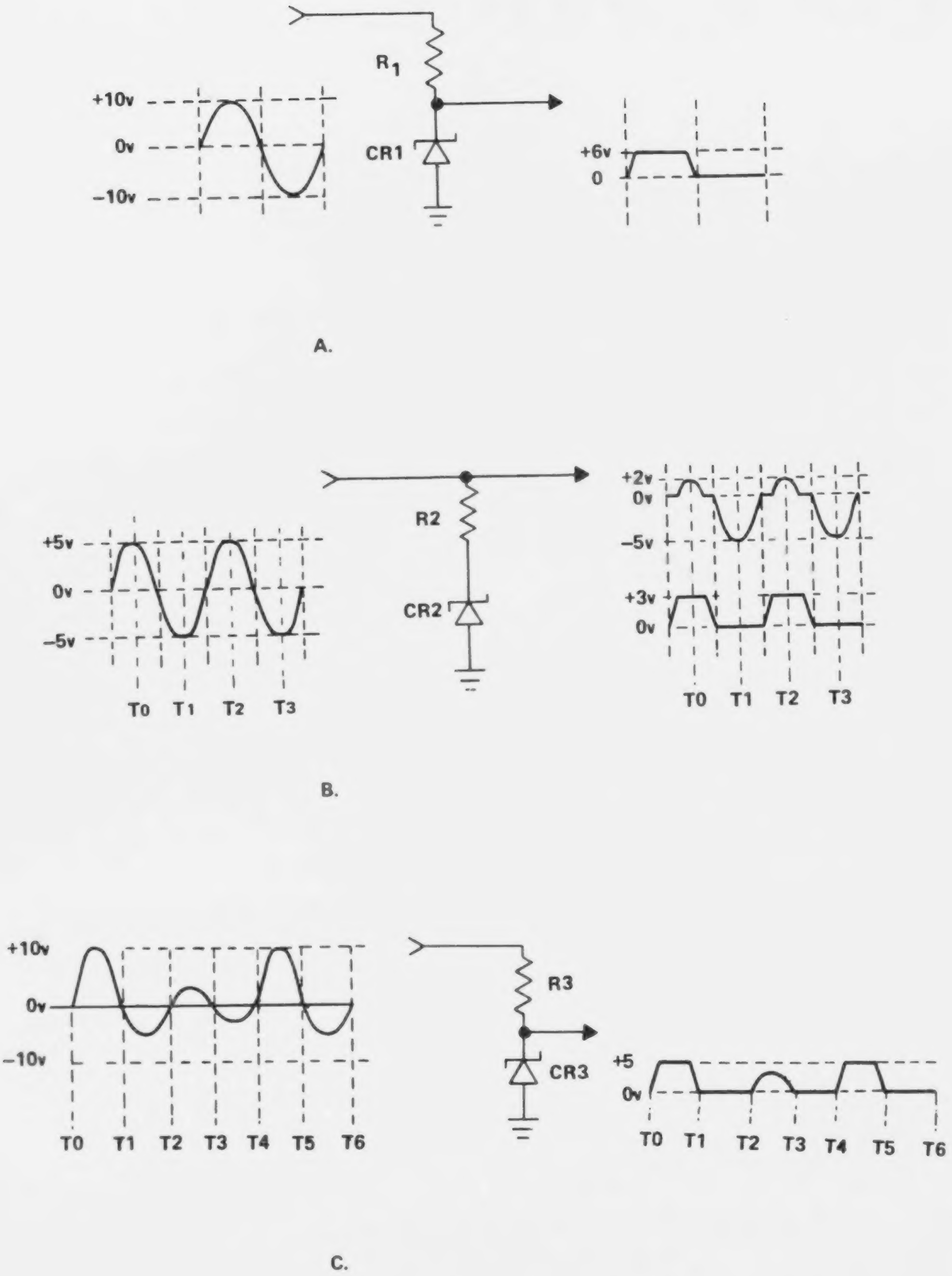

+5v
0v
−5v
100 hz
CR1
R_1
100 pps
A.
R1
CR1
B.
R_2
CR2
C.
CR2
R_2
D.

Figure 1 4. Half-wave rectifier circuits.



R1
+10v
0v
−10v
CR1
+6v
0
A.
+5v
0v
−5v
T0
T1
T2
T3
R2
CR2
+2v
0v
−5v
+3v
0v
T0
T1
T2
T3
B.
+10v
0v
−10v
T0
T1
T2
T3
T4
T5
T6
R3
CR3
+5
0v
T0
T1
T2
T3
T4
T5
T6
C.

Figure 1-5. Zener diode circuits.

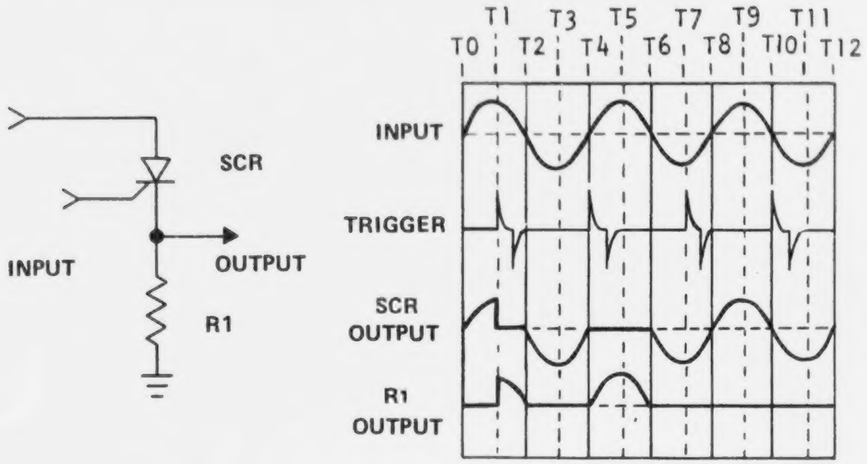


Figure 1-6. SCR circuit.

004. State the operational output of a positively triggered silicon controlled rectifier as ac input changes direction of bias.

Assume an ac input signal and a trigger. What kind of output would be given by the SCR in figure 1-6?

Anode Positive. From T_0 to T_2 the anode is positive, the cathode negative. The SCR is ready to conduct. But the trigger does not occur until T_1. So, between T_0 and T_1, the SCR is not conducting and the applied voltage is across the SCR.

At T_1 the positive trigger occurs. Current flows, R_1 now drops all the voltage, and zero volts is read across the SCR. Note how the SCR output drops to zero volts at T_1. Current continues to flow through the SCR from T_1 to T_2 because holding voltage has taken over and the negative trigger does not cut it off.

Reverse Bias. From T_2 to T_4 the negative input reverse biases the SCR, cutting it off. Despite a positive trigger, no current flows, and the negative input signal is dropped across the SCR.

The output across the resistor will be the opposite of the output across the SCR. Note that the output waveforms are dependent upon when the trigger is applied.

In the circuit shown, most of the input signal is read across the SCR from T_0 to T_1 because the trigger is not applied until late in the time period and the SCR is cut off for most of the input alternation. None of the input signal from T_4 to T_6 is produced across the SCR because the trigger is applied at the beginning of the cycle. The SCR conducts during the entire positive alternation of the input and R_1 drops all of the voltage.

Not all SCRs are triggered by positive pulses. Some may be triggered with a negative pulse. When the SCR is negatively triggered, the gate lead is connected to P-type material. All the operating characteristics of the SCR remain the same.

Exercises (004):

1. At any given time, the total voltage drop across both R_1 and the SCR will equal the ________ voltage.

2. That portion at the input waveform not reproduced across the SCR must be reproduced across ________ .

3. During which alternation is the SCR forward biased in figure 1-6?

4. When does the SCR conduct?

5. What is the output in the circuit illustrated in figure 1-6 when the SCR is forward biased and a negative trigger is applied?

005. Specify the characteristics of a variable capacitance diode.

Variable Capacitance Diode. The variable capacitance diode or varactor is a voltage controlled semiconductor capacitor. It is also called a varicap. To understand the operation, we must review the characteristics of the PN junction.

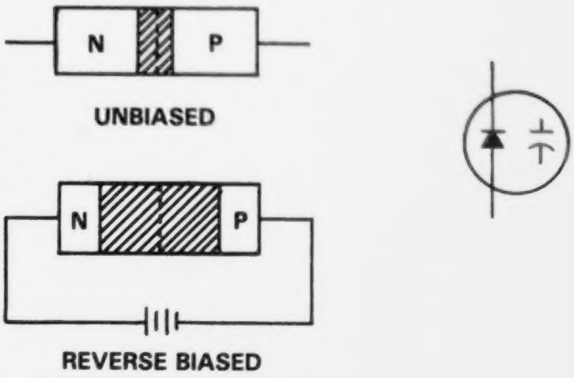


Figure 1–6A. PN junction and varactor schematic symbol.

When a PN junction is reverse biased, electrons in the N-type material are drawn toward the positive voltage source. Holes in the P-type material go toward the negative source. As a result of this action, carriers are pulled away from the junction; and very few, if any, holes or electrons will exist in this depleted or barrier region. Refer to figure 1-6A.

A semiconductor capacitor has now been formed. The N- and P-type materials act as the plates of the capacitor and the depletion region forms the dielectric. The formula for capacitance is

$$C = K \frac{(A)}{(D)}$$

where A is the area of the plates, K is the dielectric constant and D equals the distance between the plates of the capacitor formed. If the value of the reverse bias is increased, the depletion region widens, causing the capacitance to decrease as the distance between the plates (D) increases. If we decrease reverse bias, the depletion area narrows, bringing the plates (P and N materials) closer together and thereby increasing capacitance. By controlling the reverse bias, we control the varicap's value. Figure 1-6B is a generalized plot of the varactor's capacitance value at several values of reverse bias.

Varicap values generally range from about 10 to 300 picofarads (pf), although some are available at values up to 2,000 pf for low-frequency applications. The frequency at which a varactor operates also affects the value of its capacitance because of the frequency-sensitive characteristics of a PN junction.

Varactors are used as frequency determining elements in voltage controlled oscillators (VCOs) and the digital tuning circuits used in communications equipment and television sets. The same varactor principle is used within integrated circuits (ICs) to make capacitors out of diodes. Any circuit that needs a variable capacitance may be able to use the varactor.

Exercises (005):

1. Diodes, when reverse biased, become ________ ________ ________ .

2. When the depletion region widens, the capacitance of a varactor will (increase/decrease).

3. If the depletion region in a varactor narrows, the capacitance will (increase/decrease).

4. What part of a reverse biased PN junction forms the dielectric?

1-2. Transistors

By joining N-type and P-type materials in such a way that we have three elements, two N-type and one P-type or two P-type and one N-type, we can duplicate the functioning of diode tubes and junction diodes. To change the amount of current flow through a diode (tube or solid state), we had to change the value of the potential applied. By adding a third element to make a triode tube, we were able to control current flow without changing applied voltage. In the triode tube, the third element is called the control grid. The

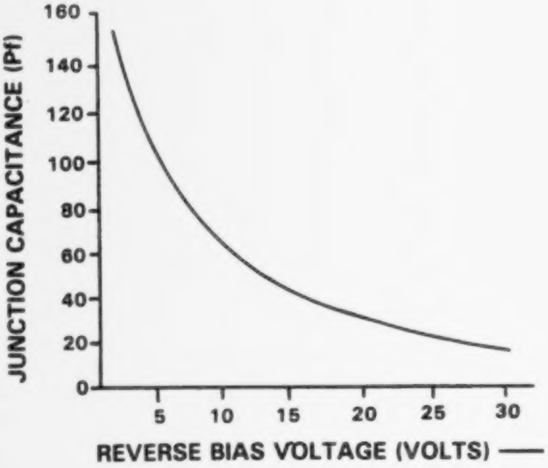


Figure 1–6B. Varactor reverse bias versus capacitance.

addition of a third and thinner layer, the *base*, brings to the semiconductor the property of *amplification*.

006. Describe NPN, PNP, and unijunction transistors.

The three types of transistors we will cover are NPN, PNP, and unijunction.

NPN Transistor. When two N-type materials are joined to one P-type material, an NPN transistor is formed. An NPN transistor is shown in figure 1-7,B. One junction is called the emitter-to-base (E-B) junction. The other is called the collector-to-base (C-B) junction. Figure 1-7,A, shows the block diagram of an NPN transistor. The NPN has a base, collector, and emitter leads.

PNP Transistor. When two P-type materials are joined to one N-type material, a PNP transistor is formed. A PNP transistor is shown in figure 1-8,B. Figure 1-8,A, shows the block diagram of a PNP transistor. The PNP has a base, collector, and emitter leads.

Unijunction Transistor. The unijunction transistor is a special-purpose transistor. Uni means one; therefore, the unijunction transistor has only one PN junction. The schematic symbol is shown in figure 1-9,B, and the block diagram is shown in figure 1-9,A. The unijunction has two base leads and one emitter lead.

Exercises (006):

1. Name the leads of a PNP transistor.

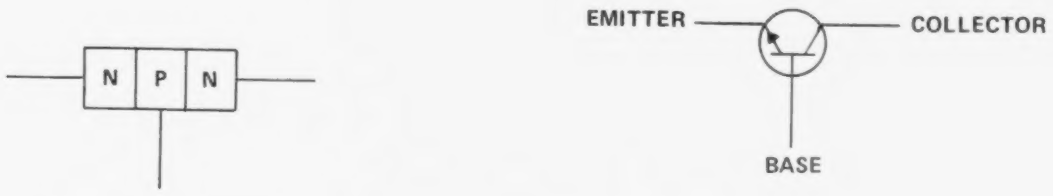
2. How many junctions does the NPN transistor have?

3. Name the leads and junctions of the unijunction transistor.

007. State relationships between polarity of inputs and direction in which junctions are biased.

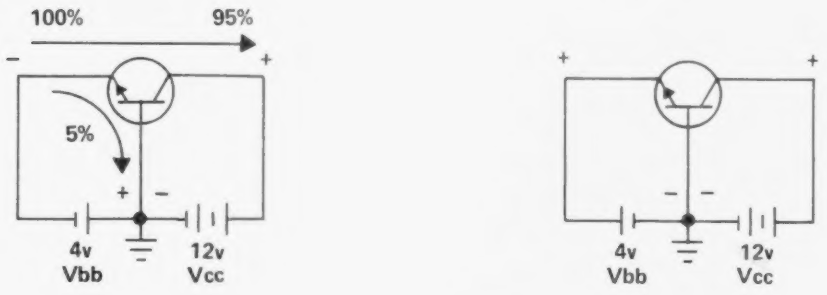
NPN Transistors. To have current flow through a transistor, the emitter-to-base junction *must be forward biased* and the collector-to-base *must be reverse biased.* (See fig. 1-7,C.)

The emitter-base (E-B) junction of a transistor controls the current flow. When the E-B junction is forward biased, electrons will flow from the negative terminal of the emitter battery (Vbb) to the emitter and through the base, which is very thin (.001 inch), to the collector. The positive potential on the collector battery (Vcc) then attracts them. Notice that there are



A. BLOCK DIAGRAM

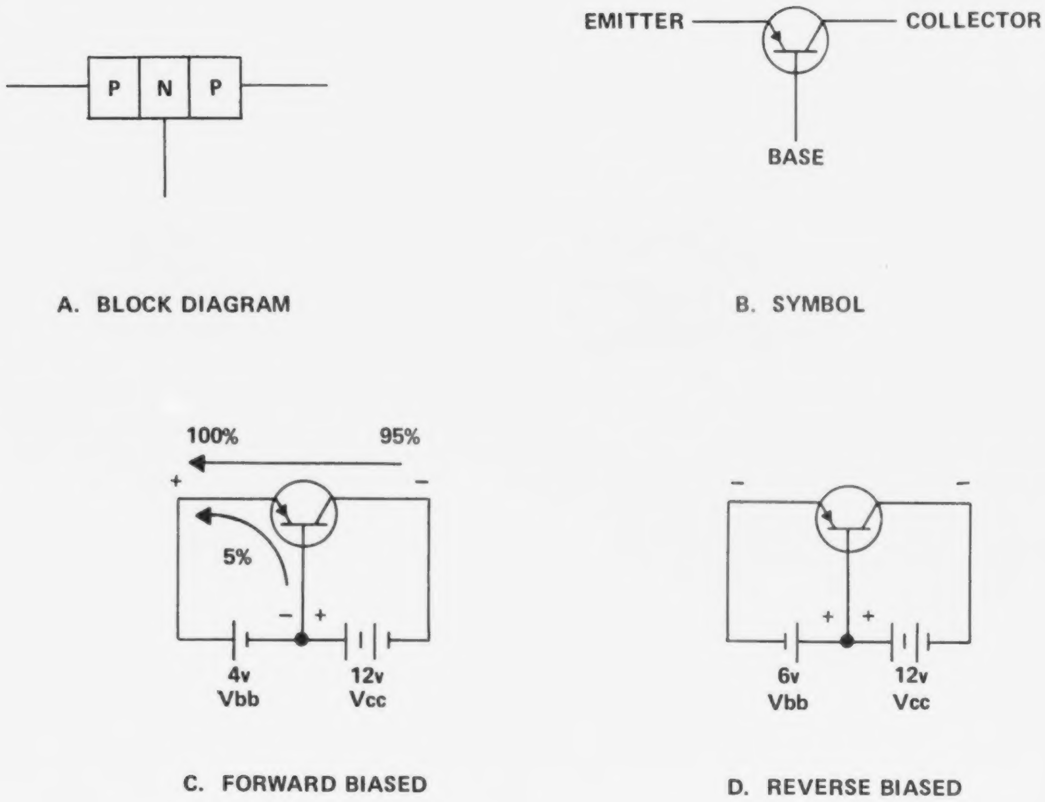
B. SYMBOL



C. FORWARD BIASED

D. REVERSE BIASED

Figure 1-7. NPN transistors.



A. BLOCK DIAGRAM

B. SYMBOL

C. FORWARD BIASED

D. REVERSE BIASED

Figure 1-8. PNP transistors.

two paths of current flow, from emitter to collector and from emitter to base lead.

Because the base is so thin, about 95 percent of the current flows from emitter to collector, and 5 percent flows in the base lead back to Vbb. Whenever the E-B junction is forward biased, current will flow and the *transistor* is considered forward biased.

In figure 1-7,D, the circuit shown is reverse biased. It differs from figure 1-7,C, by Vbb being reversed. Thus, a positive potential is applied to the emitter and a negative to the base, allowing for no current flow from either the E-B junction or from emitter to collector. In this state, the transistor is considered reverse biased.

PNP Transistors. The same rules for forward biasing hold true for a PNP transistor. (See fig. 1-8,C.) The E-B junction must be forward biased and the C-B junction reverse biased. But in the PNP, the emitter and collector materials have a positive charge. So, to forward bias the E-B junction, a positive potential must be applied to the emitter. A negative potential must be applied to the collector to reverse bias the C-B junction. With the collector negative and the emitter positive, the direction of current flow is reversed (current flows from collector to emitter), but the *transistor* is considered forward biased.

In fig. 1-8,D, the circuit shown is reverse biased. Vbb is reversed and applies a negative potential to the emitter and a positive to the base. No current flows from either the E-B junction or from emitter to collector. The transistor is considered reverse biased.

Unijunction Transistors. Figure 1-9,C, shows a reverse biased unijunction transistor. A battery is connected between base 1 and base 2 leads. Current flows through the base material as indicated by the arrows. The N-type base material acts as a resistor, and a definite positive voltage can be felt at various points throughout the base element. On the block diagram, +4 volts is felt on the base side of the PN junction. The emitter is connected to ground (zero volts), and the PN junction is reverse biased. No current flows in the emitter circuit.

Figure 1-9,D, shows a forward-biased unijunction transistor. In this circuit, a +5-volt battery is added to the emitter circuit. At the PN junction, a +4-volt potential is felt on the emitter. This forward biases the PN junction and current will flow in the emitter circuit as indicated by the arrows.

Exercises (007):

1. Which junction controls current flow in a PNP transistor?

2. How must the E–B junction be biased to get current flow in an NPN transistor?

3. A unijunction transistor is ________ ________ when the emitter is positive relative to the base and ________ ________ when the base is positive relative to the emitter.

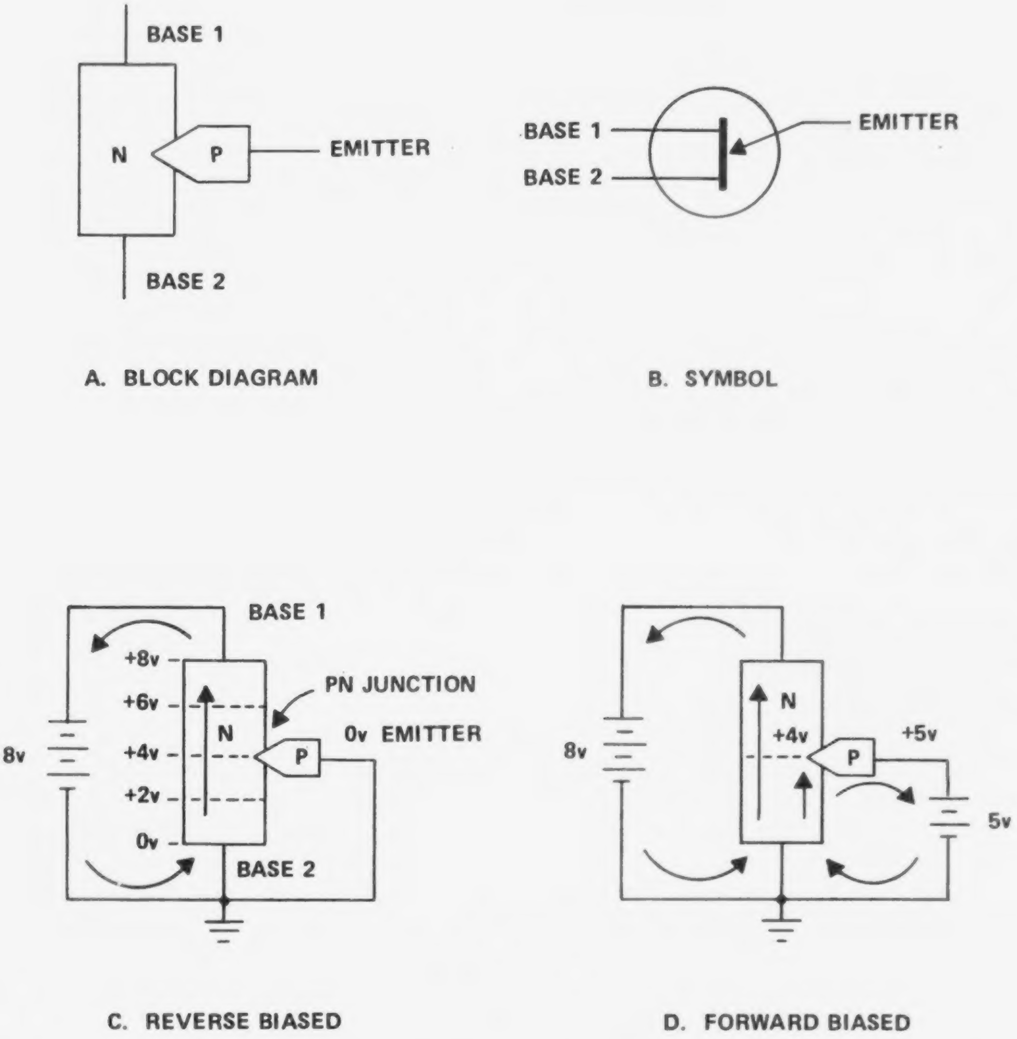
4. What potential must be applied to the emitter of a PNP to forward bias the E–B junction?

008. State the output-input functions of transistor amplifier base, collector, and emitter elements.

Common Elements. There are three basic transistor amplifier circuits. They are the common emitter, common collector, and common base. They are so named because one element is *common* to both the input and the output circuits. The element which does not have an input applied nor an output taken from it is the common element, and the name of this common element is the name used to identify the amplifiers. The three basic configurations for both the NPN and the PNP transistors are shown in figure 1-10.

Exercises (008):

1. The input is applied to the ________ and the output is taken from the ________ in a common base configuration.



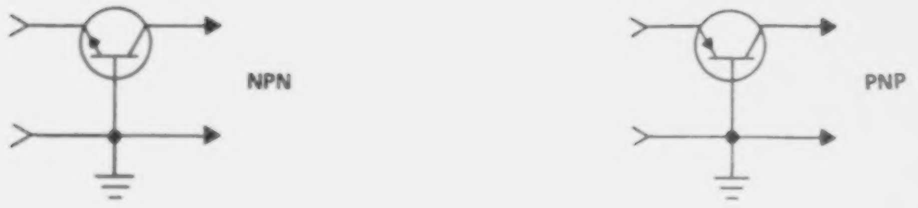
A. BLOCK DIAGRAM

B. SYMBOL

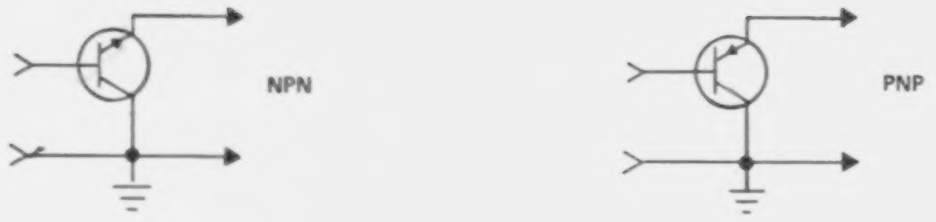
C. REVERSE BIASED

D. FORWARD BIASED

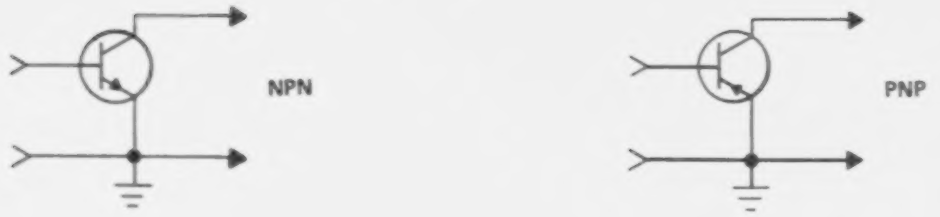
Figure 1-9. Unijunction transistors.



A. COMMON BASE



B. COMMON COLLECTOR



C. COMMON EMITTER

Figure 1-10. Transistor amplifier configurations.

2. The input is applied to the ________ and the output is taken from the ________ in a common collector configuration.
3. The input is applied to the ________ and the output is taken from the ________ in common emitter configuration.

009. State the effect on solid state amplifiers as ac input changes direction of bias and transistor resistance.

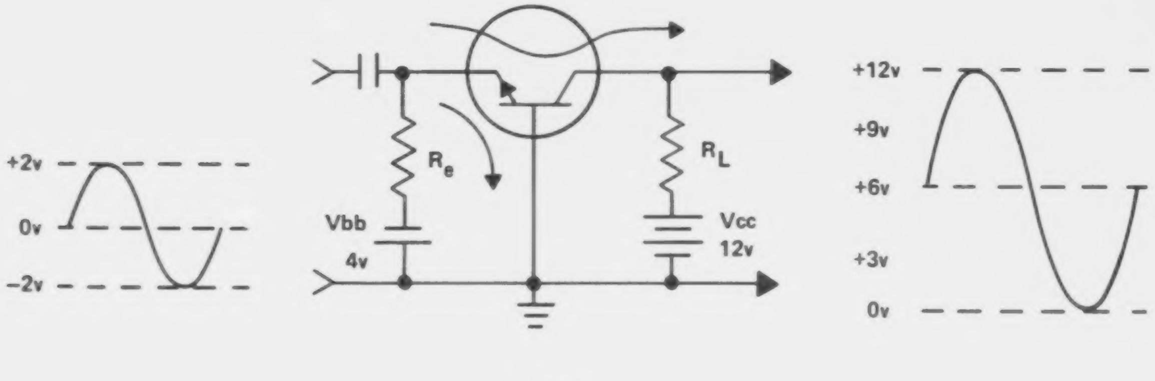
We varied current flow through the triode tubes by varying the bias between cathode and grid. In transistors, we vary the current flow by varying the bias in the E-B junction. In tubes, the B+ remained constant. In transistors, the collector potential (Vcc) applied to the C-B junction also remains constant. The changing potentials at the E-B junctions vary the width of the E-B depletion region, thereby varying the resistance and the amount of current flow. The potential on the C-B junction does not change.

Common Base Amplifiers. In the transistor circuit shown in figure 1-11,A, we have added an emitter resistor (Re) and a load resistor (RL). The emitter resistor drops part of Vbb (2 volts), leaving a negative 2 volts to be felt at the E-B junction. The C-B junction feels the positive voltage of Vcc and it is reverse biased.

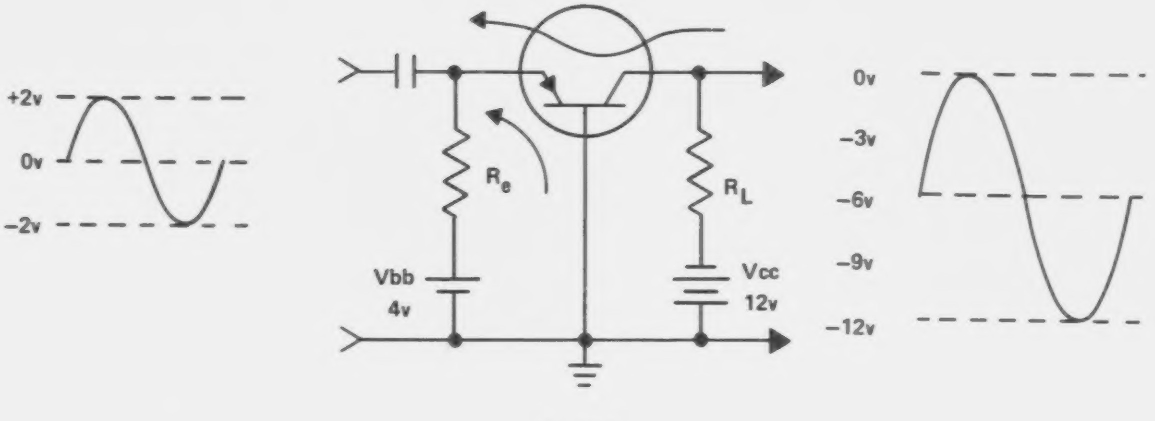
NPN. The NPN is forward biased and current flows in the circuit. The output of the circuit is developed by the transistor. Note that at quiescent, the transistor is developing a +6 volts output. The function of RL is to drop the remainder of Vcc. Since the transistor is developing +6 volts and Vcc is +12 volts, RL must be developing +6 volts.

When a 4-volt peak-to-peak signal is applied, the positive alternation of 2 volts decreases the E-B forward bias to zero volts. This causes the transistor resistance to *increase,* and the output increases from +6 volts to +12 volts (cutoff). During the negative alternation of 2 volts, E-B forward bias increases to −4 volts. This reduces transistor resistance, decreasing output from +6 to zero volts (saturation).

PNP. In figure 1-11,B, the positive alternation increases the E-B forward bias of the PNP transistor, decreases transistor resistance, and output decreases



A. NPN



B. PNP

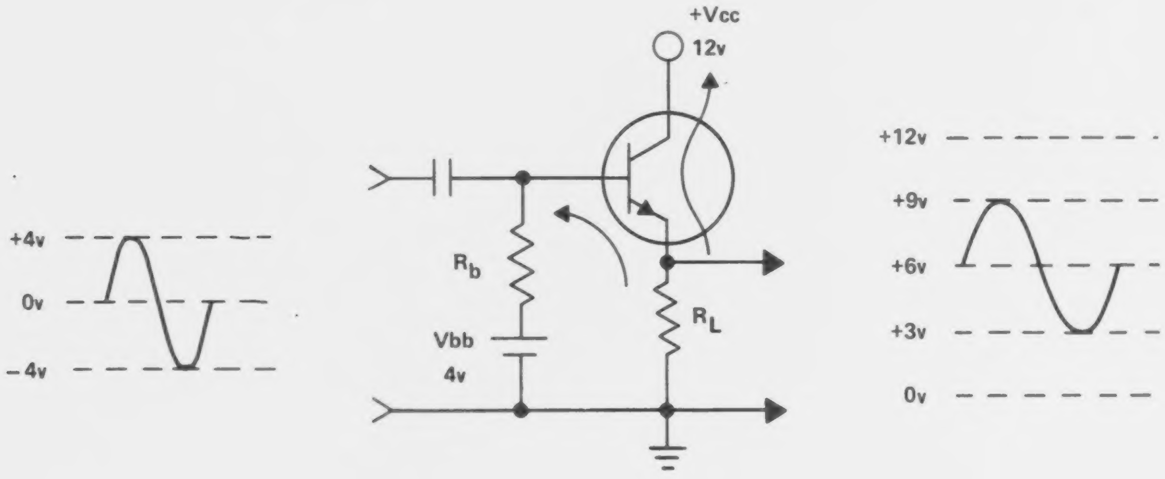
Figure 1-11. Common base amplifiers.

from −6 volts to zero volts. The negative alternation decreases E-B forward bias, increases transistor resistance, and output increases from −6 volts to −12 volts.

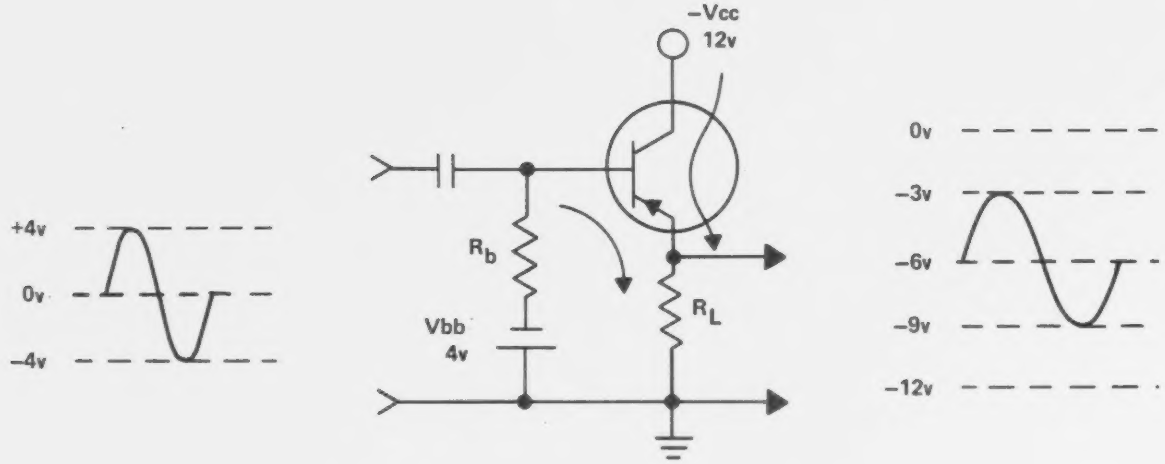
Common Collector Amplifiers. To this point, the common collector at quiescence seems to be similar to the common base and common emitter amplifiers. That is, a quiescent bias is established so as to forward bias the E-B junction. Quiescent output is either positive or negative, depending upon the type of transistor used.

However, the difference between the common collector and the other two amplifiers is that the output in the common collector is developed by the load resistor and *not* by the transistor. The function of the transistor in this configuration is to control the current flow through RL.

NPN. In figure 1-12,A, an NPN transistor at quiescence, the emitter potential (developed by RL) tends to reverse bias the E-B junction. To overcome this reverse bias, we have to make the base potential larger than the potential on the emitter.



A. NPN



B. PNP

Figure 1-12. Common collector amplifiers.

Now let us apply an input signal and see what happens. The positive alternation increases the positive potential on the base, which should cause forward bias to increase. But an increase in forward bias causes an increase in current through RL and the voltage developed by RL. As the voltage developed by RL increases, the positive potential felt on the emitter also increases. The positive alternation increases the positive potential on the base, but at the same time the emitter is becoming more positive. These two positive potentials are opposing each other. Thus, the input signal can never increase forward bias as it should and degeneration occurs.

During the negative alternation of input, the base becomes less positive. This tends to reverse bias the E–B junction. Current flow through RL and the voltage drop across RL decrease. The reduced voltage drop causes the emitter to become less positive (more negative) at the same time the base is becoming less positive. Once again bias will not change as much as it should, output will degenerate, and gain will be one or less.

PNP. In figure 1-12,B, using the PNP configuration, the positive input causes the output to increase toward the positive direction, and the negative input causes the output to decrease in the negative direction.

Common Emitter Amplifiers. The configurations shown in figure 1-13 are common emitter amplifiers. Forward bias on the E-B junction at quiescence is obtained by the bias battery (Vbb), which applies a positive or negative potential on the base. The potential on the base causes the emitter, which is at ground potential, to be either positive or negative with respect to the base.

In the transistor circuit, shown in figure 1-13,A, we have added a base resistor (Rb) and a load resistor (RL). The base resistor drops part of Vbb, leaving a positive 2 volts to be felt at the E–B junction. The C–B junction feels the positive voltage of Vcc and is reverse biased.

NPN. The NPN is forward biased and current flows in the circuit. The output is developed by the transistor. Thus, the quiescent output is +6 volts.

Now let's see how a 6-volt peak-to-peak signal will affect the output. The positive input to the NPN common emitter amplifier causes the output to decrease toward zero volts. The negative input causes the output to increase toward Vcc.

PNP. In figure 1-13,B, using the PNP configuration, the positive input causes the output to decrease toward −12 volts. The negative input causes the output to increase toward zero volts.

Exercises (009):

1. What is the effect of a positive input to an NPN common base amplifier?

2. What is the effect of a negative input on an NPN common base amplifier?

3. What is the effect of a positive input on a PNP common base amplifier? Negative input?

4. What is the effect of a positive input on an NPN common collector amplifier? Negative input?

5. What is the effect of an ac input to a PNP common collector amplifier?

6. Compare the effects of positive and negative inputs on PNP and NPN common emitter amplifiers.

1-3. Clamping

In this section, our purpose is to present a variety of circuits which use solid state devices to establish dc reference levels (clamping).

010. List the types of clampers, state their purpose, and compute amplitude of clamped dc signals.

Clampers. Often the positive or negative peaks of a signal must be clamped to a dc voltage level that will remain fixed despite signal variations. As in figure 1-14, a capacitor would block dc and the output signal would swing above ground reference, making average dc output zero. Thus, the output signal illustrated in figure 1-14 shows the shaded area of the positive alternation as equal to the shaded area of the negative alternation, although the amplitude of the positive peak exceeds the amplitude of the negative peak. If, however, the waveshape were a symmetrical square wave, the amplitude of the positive and negative peaks would be equal. You should therefore realize that the peak values of a signal, with respect to a dc reference, depend upon its waveshape. Moreover, we know peak values vary directly with signal strength. So we see that, although the capacitor establishes a dc voltage reference for the output signal, the output signal peaks are not clamped.

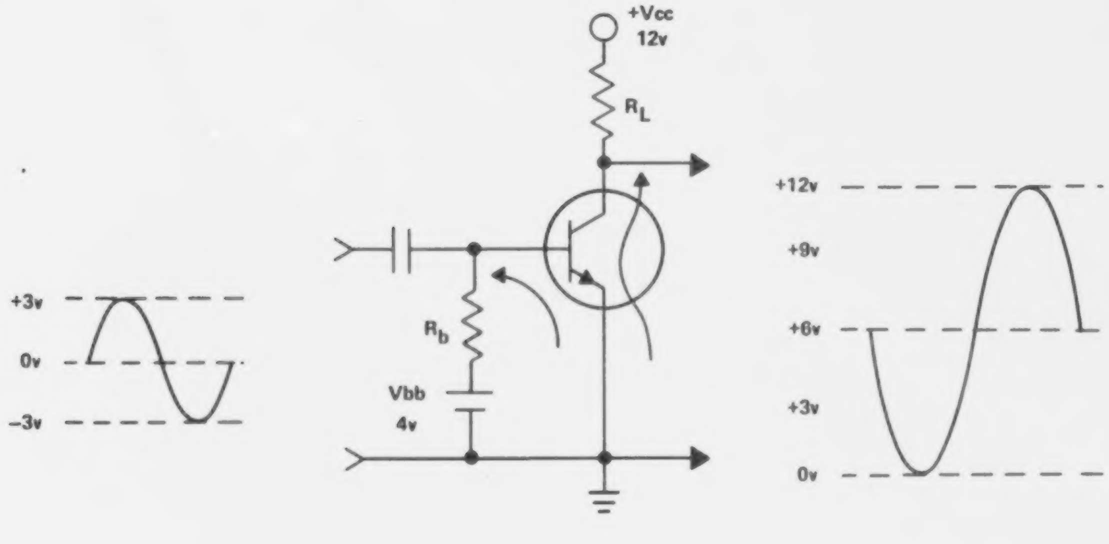
Here are some facts that pertain to clampers in general.

- A clamper does not alter the waveshape or amplitude. (This is true from a practical standpoint. A slight amount of distortion is inevitable, but can be made negligible by proper design.)
- The clamping reference is the same as the bias, which may be zero (unbiased), a positive dc voltage, or a negative dc voltage.

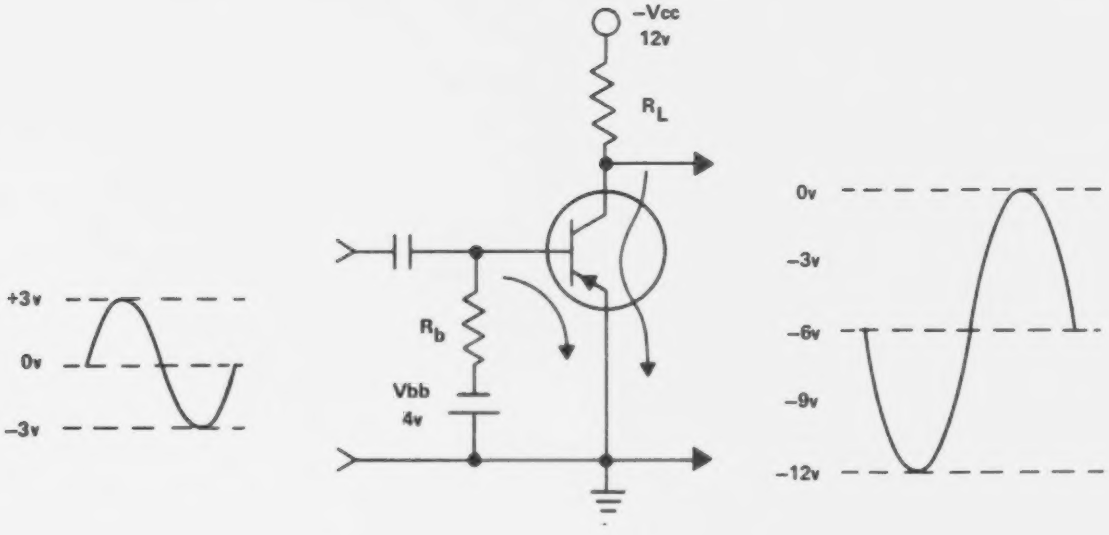
- A positive clamper clamps the output signal above the clamping reference.
- A negative clamper clamps the output signal below the clamping reference.

Diode Clamping Circuits. By employing a PN junction diode or transistor in conjunction with a capacitor and resistor, the signal peaks can be readily clamped to any dc reference level. The desired clamping reference can be obtained simply by biasing the circuit. Let us consider some specific unbiased and biased clamping circuits that are commonly used. These circuits are called clampers, and sometimes dc restorers (dcR).

Positive diode clampers. Figure 1-15 shows three positive diode clampers. Observe how the output signal from each circuit is clamped to a dc voltage level (clamping reference). The output signal is always



A. NPN



B. PNP

Figure 1-13. Common emitter amplifiers.

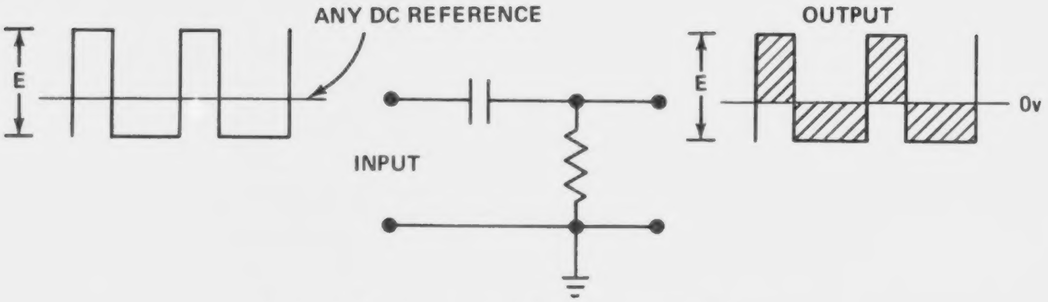

ANY DC REFERENCE
E
INPUT
OUTPUT
E
0v

Figure 1-14. Input and output of an ordinary coupling circuit.

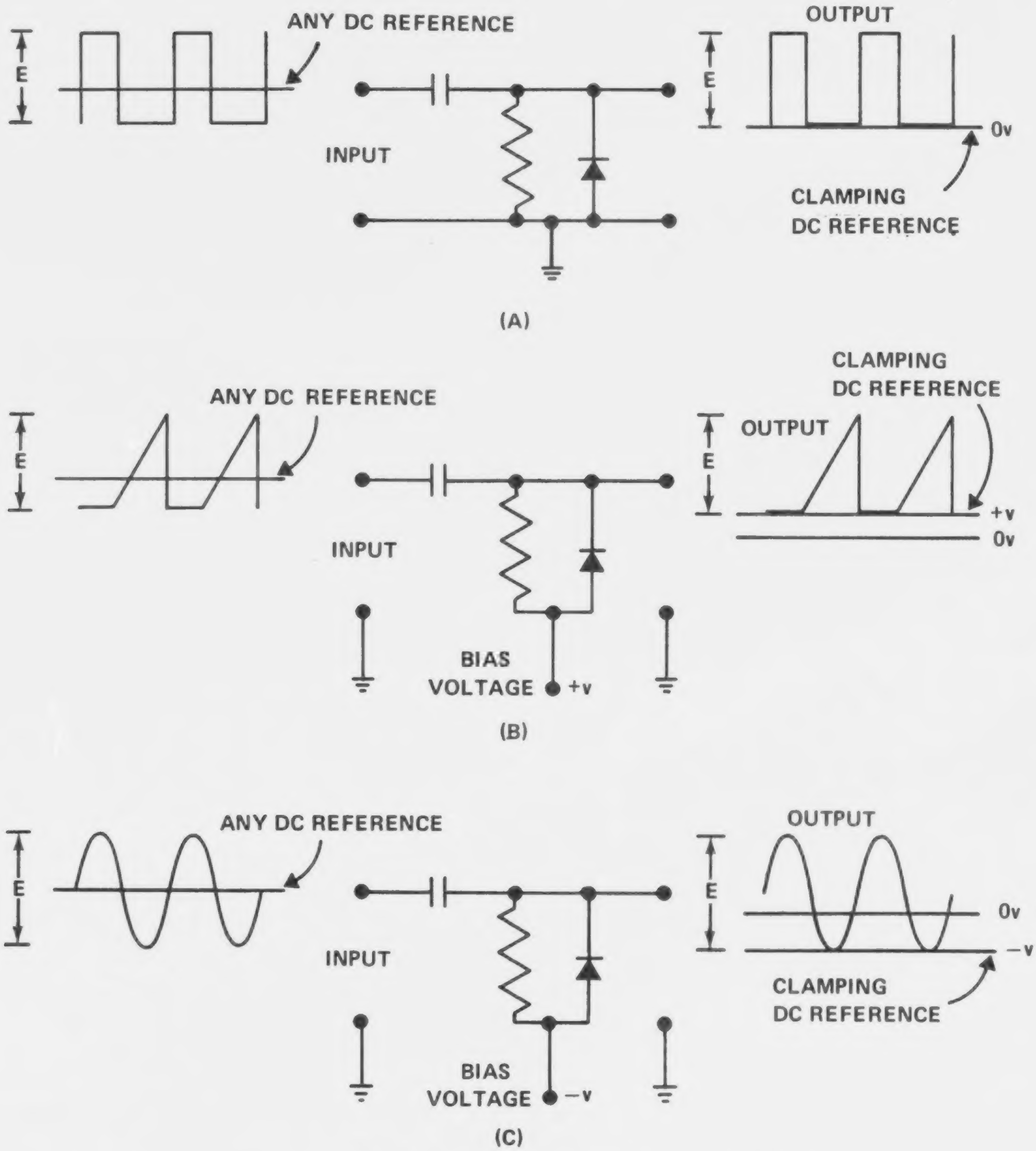

ANY DC REFERENCE
E
INPUT
OUTPUT
E
0v
CLAMPING
DC REFERENCE
(A)
ANY DC REFERENCE
E
INPUT
BIAS
VOLTAGE
+v
CLAMPING
DC REFERENCE
OUTPUT
E
+v
0v
(B)
ANY DC REFERENCE
E
INPUT
BIAS
VOLTAGE
−v
OUTPUT
E
0v
−v
CLAMPING
DC REFERENCE
(C)

Figure 1-15. Positive diode clampers.

above the clamping reference for *positive* clampers. These clampers may be unbiased or biased (positively or negatively), as shown in figure 1-15,A, B, and C, respectively.

Because of the rectifying action of the PN junction diode, the output side of the capacitor is kept charged above the clamping reference by an amount virtually equal to the peak voltage of the signal. Consequently, the output signal "rides" the clamping reference.

Study figure 1-15,A, B, and C carefully. Observe that, for all *positive* clampers, the anode (P electrode of the PN junction diode) is connected to the clamping reference. If unbiased, the clamping reference is ground. If biased, the clamping reference is the bias voltage (+V or −V). Since the output signal has the same waveshape and amplitude of swing as the input signal, the pertinent voltage values for any signal can be quickly ascertained.

By way of example, let us apply a sine wave signal to the input terminals of the biased positive clamper shown in figure 1-15,C. On the input side, we will assume that this sine wave varies in amplitude from −6 to +6 volts (12 volts peak to peak). If the bias on the clamper is −4 volts, the clamping reference is −4 volts. Therefore, the output is a sine wave (same as input) that varies from −4 volts to +8 volts (12 volts peak to peak, same as input).

Negative diode clampers. Figure 1-16 illustrates negative diode clampers. In these circuits, the cathode (N electrode of the PN junction diode) is connected to the clamping reference (ground, +V, or −V). Connected in this way, the rectifying action of the diode keeps the capacitor charged *below* the clamping reference by an amount equal to the peak voltage of the signal. Thus, the output signal "rides" *below* the clamping reference for *negative* clampers, as illustrated.

Notice that the output signal and input signal differ only in their dc reference. So, again, it is a simple matter to determine the voltage values of the output signal for a given input and clamping reference. For example, let us put a sine wave into a negative diode clamper biased at +10 volts. If the input swings from −2 volts to −5 volts, the output sine wave signal will swing from +10 volts (the clamping reference) to +7 volts.

Common Emitter Clamping. The input circuit to a transistor may function as a clamper. This can be easily realized from figure 1-17.

NPN. In figure 1-17,A, we see an NPN transistor connected in the common emitter configuration. The base emitter junction rectifies like a PN junction diode. This input circuit corresponds to the negative diode clamper circuit of 1-16,A, since the emitter (N electrode) is connected to the clamping reference (ground). Thus, the incoming signal will always "ride" *below* ground, as shown.

PNP. If a PNP transistor is used (see fig. 1-17,B), the incoming signal will always "ride" *above* ground. The input circuit is a positive clamper and corresponds to the positive diode clamper in figure 1-15,A, since the emitter (P electrode) is connected to the clamping reference (ground).

Common Base Clamping. It is interesting to point out that a common base configuration clamps oppositely to the common emitter configuration; that is, the NPN transistor causes positive clamping and a PNP causes negative clamping. Just like diode clamping circuits, base-emitter clamping can be biased to obtain dc references other than ground.

Clamper Polarity. A quick way to identify a solid state clamper as positive or negative is to note the arrow direction of the diode or transistor symbols. If the arrow points *away* from the bias or ground terminal (upward in all our illustrations), the circuit is a positive clamper. The arrow direction for a negative clamper points *toward* the bias or ground terminal (downward in all our illustrations).

Exercises (010):

1. State the reason clamping is required.

2. List the types of solid state clamping.

3. Clampers are also called ________ .

4. A negative clamper clamps the output signal ________ the clamping reference.

5. If the arrow of the diode points away from the bias terminal, the circuit is a ________ clamper.

6. If the arrow of the diode points toward the bias terminal, the circuit is a ________ clamper.

7. A positive diode clamper is supplied with an 8-volt peak-to-peak ac input and a bias of −10 volts. What is the peak voltage of the most positive alternation?

8. A negative diode clamper is supplied with a 10-volt peak-to-peak ac input and a bias of zero volts. What is the peak voltage of the most negative alternation?

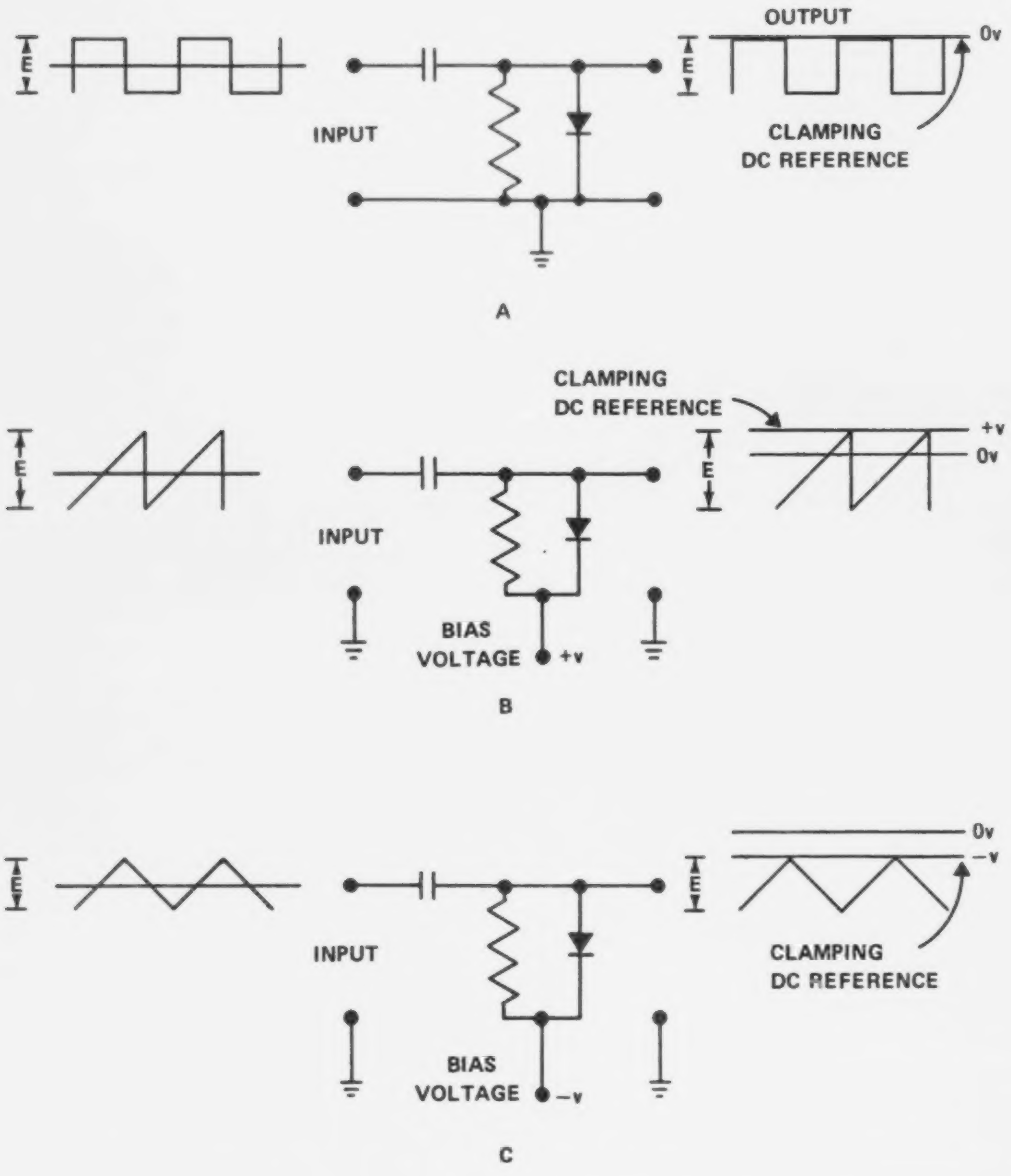

E
OUTPUT
0v
E
INPUT
CLAMPING
DC REFERENCE
A
CLAMPING
DC REFERENCE
E
+v
0v
E
INPUT
BIAS
VOLTAGE
+v
B
E
0v
−v
E
INPUT
CLAMPING
DC REFERENCE
BIAS
VOLTAGE
−v
C

Figure 1-16. Negative diode clampers.

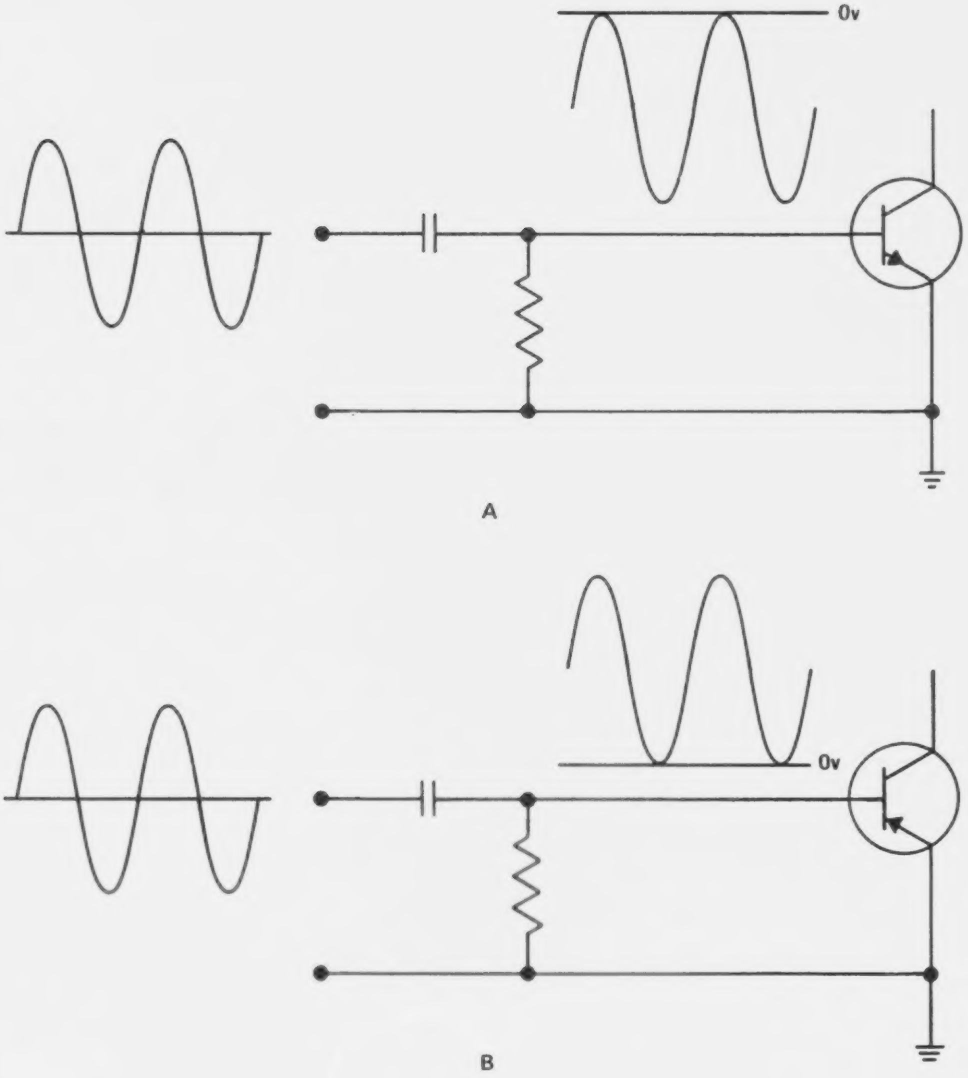


Figure 1-17. Base emitter clamping.

9. A 10-volt peak-to-peak ac input is supplied to both an NPN and a PNP common emitter clamper. What is the peak voltage value of the most positive alternation of the input to each?

10. A 6-volt peak-to-peak ac input is supplied to both an NPN and a PNP common base clamper. What is the peak voltage of the most negative alternation of the input to each?

1-4. Limiting

A circuit that limits the amplitude of either the positive or the negative alternation of a signal, or both, is appropriately called a limiter. It is sometimes referred to as a clipper, since the positive peak, negative peak, or both peaks are clipped by the circuit. The signal is therefore flattened on the top, the bottom, or both top and bottom.

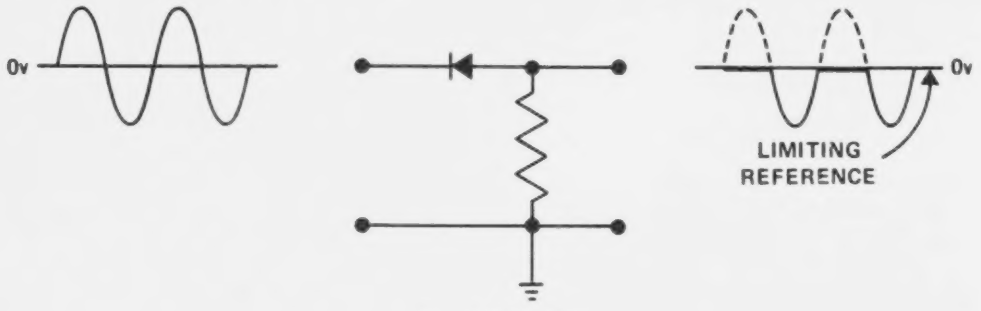
011. Given statements concerning peak-to-peak ac input and volt bias, state the output of series limiters.

Limiters are used extensively for waveshaping. A sine wave can be clipped to virtually a square waveform. The output waveshapes from signal generators can be greatly improved. Rounded or peaked leading and trailing edges of signals from multivibrators can be squared up, and triggers from pulse generators can be shaped or restricted in amplitude. Moreover, changes in signal strength—caused by instability, noise, and loading—will not be evident if the signal is properly clipped. So in addition to waveshaping, a limiter can prevent unwanted amplitude variations and eliminate noise.

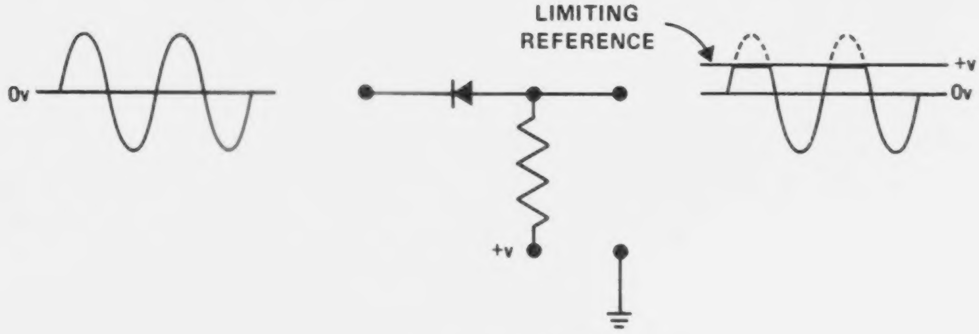
Series Limiter. Signals can be limited by placing a rectifying device in series with the load. Thus, an ordinary PN junction diode in series with a resistor constitutes a *series-limiter* circuit.

For this arrangement, limiting occurs when the PN junction diode is reverse biased by the input signal. Since there is some reverse current flow, the limiting action is not as perfect as with an electron tube limiter, which has no reverse current flow. To obtain good limiting, it is therefore necessary that the resistor be quite small in value compared to the reverse resistance of the PN diode. This type of limiter is better suited for a low-resistance load.

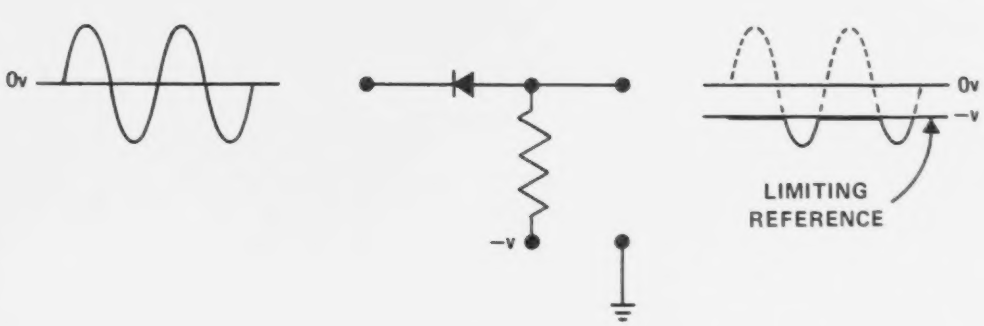
Positive series limiters. The circuits shown in figure 1-18 limit the upward swing of the signal (most positive or least negative level). For this reason, these circuits are known as *positive series limiters.* These circuits can



A. UNBIASED



B. POSITIVELY BIASED



C. NEGATIVELY BIASED

Figure 1-18. Positive series limiters.

be unbiased or biased to obtain the desired amount of positive limiting.

The unbiased circuit (see fig. 1-18,A), is simply a half-wave rectifier. Only the negative alternation is seen across the output terminals. Assuming the load resistance to be several orders of magnitude smaller than the reverse resistance of the PN diode, the positive alternation is clipped at the limiting ground reference, zero volts.

When biased positively (see fig. 1-18,B), only a portion of the positive alternation is clipped. The limiting reference is +V, since the PN diode is conductive until this voltage is reached by the input signal. During the time that the input signal is above (more positive than) +V, the diode is reverse biased (virtually open), and +V, is seen at the output.

By applying a negative bias (see fig. 1-18,C) to the positive series limiter, a greater amount of clipping occurs. Only that portion of the input signal which is more negative than −V appears at the output.

So we conclude that a smaller amount of positive limiting results from an increase in positive bias, whereas a greater amount of positive limiting results from an increase in negative bias.

Negative series limiters. Reverse the diode connections in the circuits just discussed, and we have the limiters shown in figure 1-19. Reversing the diode in a limiter circuit gives the opposite type of limiting. This is easily understandable, since the rectification is exactly opposite in direction. Note that the circuits in figure 1-19 limit the downward movement of the signal. Thus, they are *negative* series limiters. When unbiased (see fig. 1-19,A), only the positive alternation appears at the output.

Figure 1-19,B, shows how positive bias increases the amount of limiting. If less than a full alternation is to be limited, a negative bias is applied (see fig. 1-19,C) so that only a part of the negative alternation is clipped. Thus, the effect of bias on negative limiters is the opposite of that on positive limiters.

Varying Outputs. Our illustrations show sine wave signals, but you should realize that any signal waveform is limited by these circuits. To determine the output waveshapes of a given signal input, do the following:

(1) Redraw the input waveshape at the output.

(2) Draw a line at the bias level (0 V, if unbiased) to establish the limiting reference.

(3) If the anode is connected to the output terminal (positive series limiter), erase the signal above the limiting reference.

What remains is the output signal. Apply this procedure to figures 1-18 and 1-19 to become convinced of its validity.

Exercises (011):

1. What is the output of an unbiased positive series limiter?

2. What is the output of a positive series limiter biased at +6 volts and supplied with a 12-volt peak-to-peak ac input?

3. What is the output of a positive series limiter biased at −6 volts and supplied with a 12-volt peak-to-peak ac input?

4. What is the output of an unbiased negative series limiter?

5. What is the output of a negative series limiter which is supplied with an 8-volt peak-to-peak ac signal and 3-volt positive bias?

6. What is the output of a negative series limiter which is supplied with a 9-volt peak-to-peak ac signal and a bias of −4 volts.

012. Give answers to statements about shunt and series limiters and compare their functions.

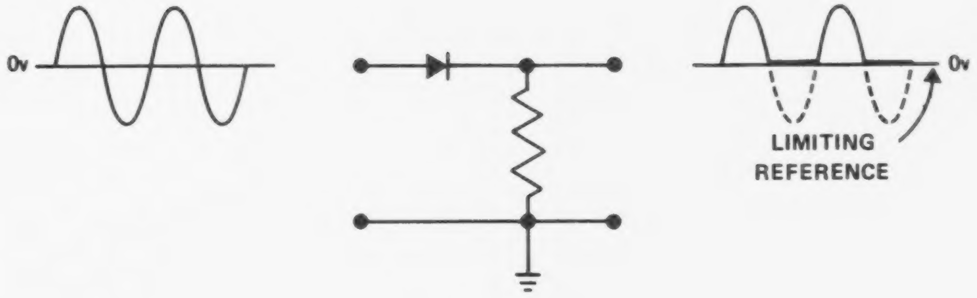
Shunt Limiter Circuits. Another simple way to limit a signal is to place a resistor in series with a rectifying device that is in shunt with the output load (see fig. 1-20,A). This arrangement comprises a shunt limiter circuit, which limits the signal when the rectifying device is in its highly conductive state.

Positive shunt limiter. Using a PN diode, limiting results whenever the diode is forward biased.

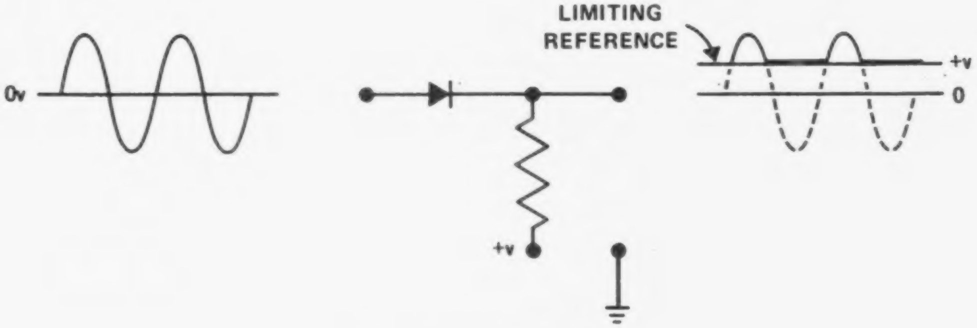
In the design of this circuit, consideration must be given to the ohmic value of the series resistor. Its resistance should be very small compared to the load resistance. If it isn't, the signal output will be attenuated by the voltage drop across the series resistor, since the series resistor and load resistance form a voltage divider. Therefore, this type operates best with a high-resistance load.

Study the circuit diagram in figure 1-20. You should recognize these circuits as positive limiters. The output waveforms are obtained in the manner previously described for the positive series limiter. Like the positive series type, observe that the anode of the diode is connected to the output terminal.

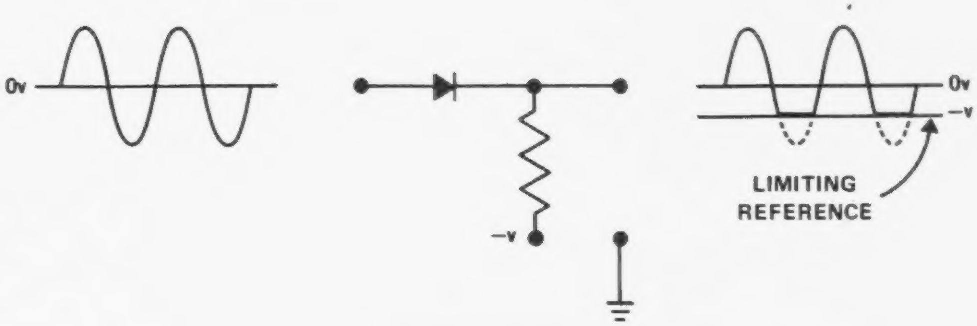
Negative shunt limiters. A reversal of the diode's direction changes the circuit of figure 1-20 to those of figure 1-21. Now we have negative shunt limiters. The cathode of the diode is connected to the output terminal just as it is for the negative series type. The same procedure is used for determining the output waveform.


0v
0v
LIMITING
REFERENCE

A. UNBIASED

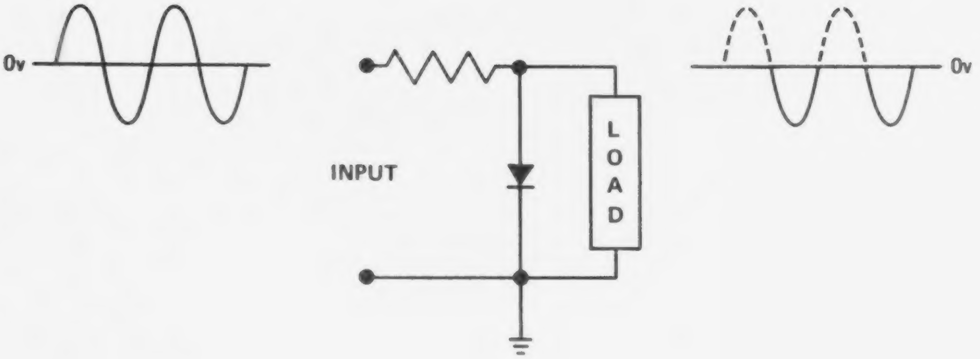

0v
LIMITING
REFERENCE
+v
0
+v

B. POSITIVELY BIASED

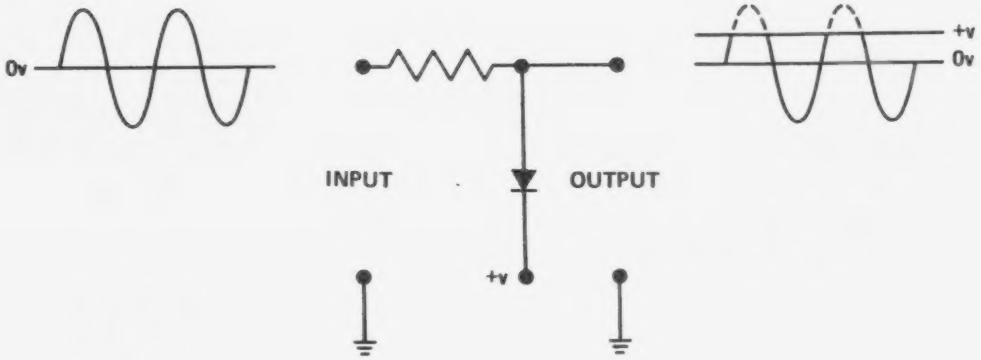

0v
0v
−v
LIMITING
REFERENCE
−v

C. NEGATIVELY BIASED

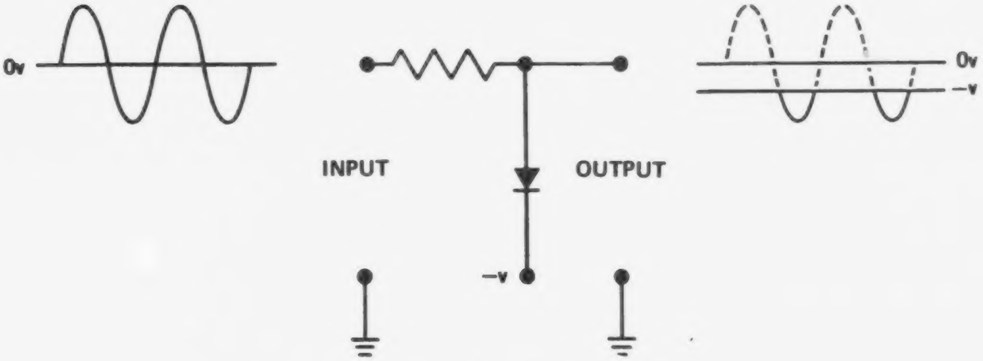
Figure 1-19. Negative series limiters.


0v
INPUT
L O A D
0v

A. UNBIASED

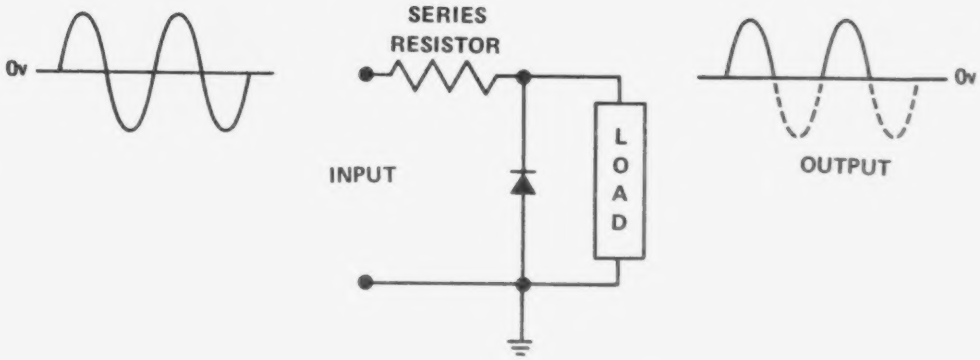

0v
INPUT
OUTPUT
+v
+v
0v

B. POSITIVELY BIASED


0v
INPUT
OUTPUT
–v
0v
–v

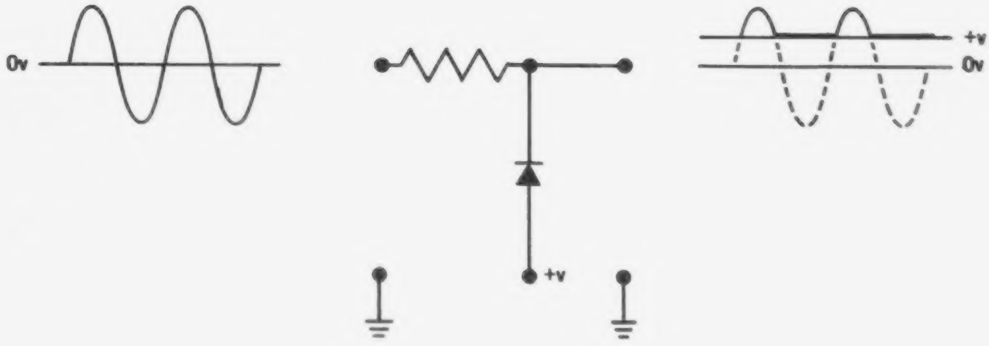
C. NEGATIVELY BIASED

Figure 1-20. Positive shunt limiters.

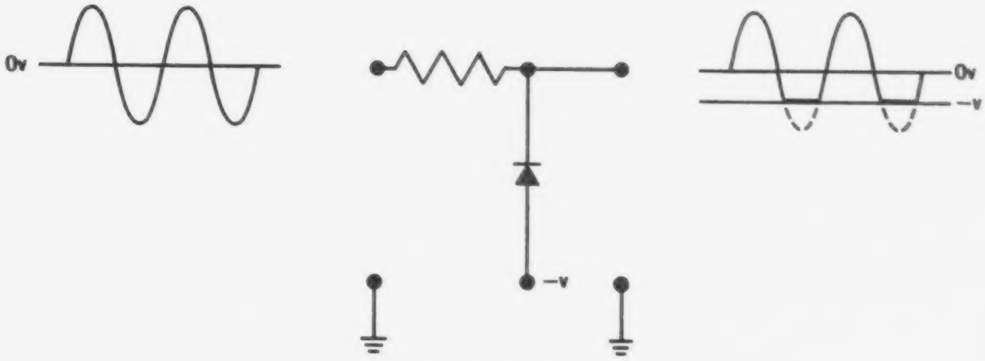


0v
SERIES
RESISTOR
INPUT
L O A D
OUTPUT
0v

A. UNBIASED



B. POSITIVELY BIASED



C. NEGATIVELY BIASED

Figure 1-21. Negative shunt limiters.

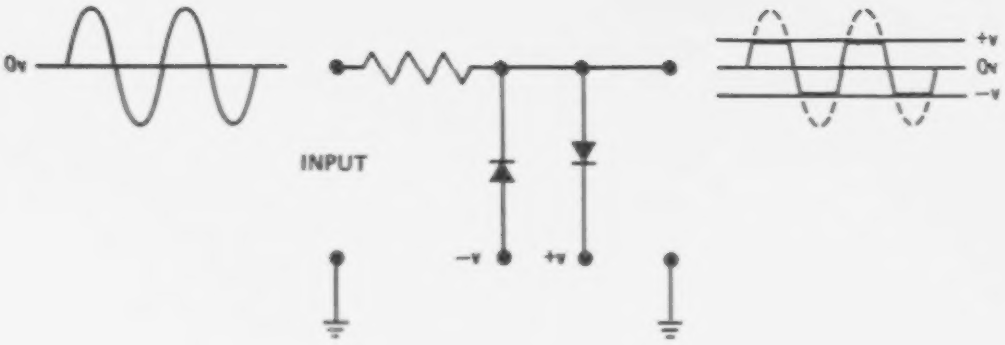


Figure 1-22. Positive and negative shunt limiters.

Adjustable polarity. An advantage offered by the shunt arrangement is shown in figure 1-22. With this circuit, both positive and negative limiting are accomplished. The bias can be adjusted to give the amount of limiting desired. Thus, a sine wave can be clipped to obtain nearly a square-wave output. A perfect square wave is approached by increasing the clipping and by increasing the amplitude of the sine wave input.

Exercises (012):

Indicate whether the following statements are true or false.

___ 1. In both a shunt and series limiter, the limiting component is in parallel with the load.

___ 2. In both a shunt and series limiter, the limiting component is conducting when the circuit is limiting.

___ 3. The outputs of positive series and shunt limiters are the same, given like inputs.

___ 4. Outputs of negative series and shunt limiters are the same, given like inputs.

Bibliography

Department of the Air Force Publications:

TO 31-1-141-3, *Basic Electronic Circuit Theory*.
TO 31-1-141-4, *Semiconductor Circuit Theory*.

NOTE: None of the items listed in the bibliography above are available through ECI. If you cannot borrow them from local sources, such as your base library or local library, you may request one item at a time on a loan basis from the AU Library, Maxwell AFB AL 36112, ATTN: ECI Bibliographic Assistant. However, the AU Library generally lends only *books* and a limited number of *AFMs*. TOs, classified publications, and other types of publications are not available. Refer to current indexes for latest revisions of and changes to the official publications listed in the bibliography.

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ANSWERS FOR EXERCISES

Reference:

001 – 1. Negative; positive.
001 – 2. Anode.
001 – 3. The minority depletion region has increased in width but has so few charges that it does not offer much resistance to the majority current carries.
001 – 4. Low.
001 – 5. Breakdown voltage.
001 – 6. Anode, cathode, and gate.

002 – 1. Cut off.
002 – 2. 10; 200.

003 – 1. No.
003 – 2. At +10 volts.
003 – 3. 3 volts.
003 – 4. Yes.
003 – 5. The input signal did not exceed breakdown voltage.
003 – 6. No.

004 – 1. Applied.
004 – 2. R1.
004 – 3. During the positive alternation.
004 – 4. When it is forward biased and a trigger of correct polarity occurs.
004 – 5. 0 V.

005 – 1. Varactors or varicaps.
005 – 2. Decrease.
005 – 3. Increase.
005 – 4. The depletion region or barrier region.

006 – 1. Base, collector, and emitter.
006 – 2. 2.
006 – 3. Base 1, base 2, and emitter. The PN junction.

007 – 1. The E–B junction.
007 – 2. Forward biased.
007 – 3. Forward biased; reverse biased.

007 – 4. Positive.

008 – 1. Emitter; collector.
008 – 2. Base; emitter.
008 – 3. Base; collector.

009 – 1. Forward bias of the emitter-to-base junction decreases; transistor resistance and output increase.
009 – 2. Emitter-to-base forward bias increases; transistor resistance and output decreases.
009 – 3. In each case, the effect is the opposite of that upon a PNP common base amplifier.
009 – 4. Both a negative and positive input have essentially the same effect on an NPN common collector amplifier. In both cases, base-emitter bias changes in the same direction as the input. As a consequence, degeneration decreases the voltage value of the input as well as the degree of amplification.
009 – 5. The output amplitudes of both the negative and positive alternations are decreased from that of the input.
009 – 6. Positive input causes both the PNP and NPN C–E amplifier output to decrease in voltage. Negative inputs cause increases in voltage.

010 – 1. For many applications a dc voltage level must remain fixed.
010 – 2. Positive diode clampers, negative diode clampers, and base-emitter clamping.
010 – 3. DC restorers (dcR).
010 – 4. Below.
010 – 5. Positive.
010 – 6. Negative.
010 – 7. −2 volts.
010 – 8. Negative 10 volts.
010 – 9. For the NPN, it is ground, zero volts. For the PNP, it is 10 volts above ground, or 10 volts.
010 – 10. For the NPN, it is 0 volts. For the PNP, it is −6 volts.

011 – 1. The output will be limited to the negative alternation if the ac input.
011 – 2. Output will be identical to input because only that portion of input above bias voltage is flattened.
011 – 3. No output because no portion of the input is more negative than the −6 volt bias.
011 – 4. The output is the positive alternation of the input.
011 – 5. Three volts of the positive alternation is clipped because of the positive 3 volt bias, leaving an output of +3 to +4 volts.
011 – 6. A half volt is clipped, resulting in a negative alternation of 4 volts maximum amplitude.

012 – 1. False.
012 – 2. False.
012 – 3. True.
012 – 4. True.

STOP- 1. MATCH ANSWER SHEET TO THIS EXERCISE NUMBER.
2. USE NUMBER 2 PENCIL ONLY.

EXTENSION COURSE INSTITUTE
VOLUME REVIEW EXERCISE

30554 02 23

ELECTRONIC PRINCIPLES AND DIGITAL TECHNIQUES

Carefully read the following:

DO's:

1. Check the "course," "volume," and "form" numbers from the answer sheet address tab against the "VRE answer sheet identification number" in the righthand column of the shipping list. If numbers do not match, return the answer sheet and the shipping list to ECI immediately with a note of explanation.
2. Note that item numbers on answer sheet are sequential in each column.
3. Use a medium sharp #2 black lead pencil for marking answer sheet.
4. Write the correct answer in the margin at the left of the item. (When you review for the course examination, you can cover *your* answers with a strip of paper and then check your review answers against your original choices.) After you are sure of your answers, transfer them to the answer sheet. If you *have* to change an answer on the answer sheet, be sure that the erasure is complete. Use a clean eraser. But try to avoid any erasure on the answer sheet if at all possible.
5. Take action to return entire answer sheet to ECI.
6. Keep Volume Review Exercise booklet for review and reference.
7. If *mandatorily* enrolled student, process questions or comments through your unit trainer or OJT supervisor. If *voluntarily* enrolled student, send questions or comments to ECI on ECI Form 17.

DON'Ts:

1. Don't use answer sheets other than one furnished specifically for each review exercise.
2. Don't mark on the answer sheet except to fill in marking blocks. Double marks or excessive markings which overflow marking blocks will register as errors.
3. Don't fold, spindle, staple, tape, or mutilate the answer sheet.
4. Don't use ink or any marking other than a #2 black lead pencil.

NOTE: **NUMBERED LEARNING OBJECTIVE REFERENCES ARE USED ON THE VOLUME REVIEW EXERCISE.** In parenthesis after each item number on the VRE is the *Learning Objective Number* where the answer to that item can be located. When answering the items on the VRE, refer to the *Learning Objectives* indicated by these *Numbers*. The VRE results will be sent to you on a postcard which will list the *actual* VRE *items you missed*. Go to the VRE booklet and locate the *Learning Objective Numbers* for the items missed. Go to the text and carefully review the areas covered by these references. Review the entire VRE again before you take the closed-book Course Examination.

MULTIPLE CHOICE

Note to Student: Consider all choices carefully and select the *best* answer to each question.

1. (200) As applied to semiconductors, "forward bias" means a positive voltage is applied to

   a. the N-type area while a negative voltage is applied to the P-type area.
   b. both areas of the semiconductor.
   c. the P-type area while a negative voltage is applied to the N-type area.
   d. reduce the flow of current through the conductor.

2. (201) When the input to a half-wave rectifier is 40 volts peak-to-peak, the output voltage is

   a. 80 volts.
   b. 40 volts.
   c. 20 volts.
   d. 10 volts.

3. (203) When a silicon controlled rectifier is reverse biased, a positive trigger will cause it to

   a. reach breakdown voltage.
   b. start conducting.
   c. stop conducting.
   d. remain unchanged.

4. (205) Which of the following semiconductor devices has two base leads?

   a. Zener diode.
   b. PNP transistor.
   c. PN junction diode.
   d. Unijunction transistor.

5. (206) For current to flow through a transistor, the

   a. E-B and C-B junctions are reverse biased.
   b. E-B junction must be reverse biased.
   c. E-B junction must be forward biased.
   d. C-B junction must be forward biased.

6. (207) In figure 1-10 of Module 10008, the amplifier configuration that has the input applied to the emitter-base junction and takes the output from the collector-base junction is known as a

   a. common base.
   b. common collector.
   c. common emitter.
   d. emitter follower.

7. (208) Refer to figure 1-13 of Module 10008. How many degrees of phase shift occur between the input and output of a common emitter amplifier?

   a. 0.
   b. 90.
   c. 180.
   d. 270.

8. (209) When clamping occurs in a negative diode clamper, the output signal will

   a. always be zero.
   b. appear rectified.
   c. ride above ground reference.
   d. ride below the clamping reference.

9. (210) An unbiased positive series limiter is also a

   a. clamper.
   b. pulse shaper.
   c. full-wave rectifier.
   d. half-wave rectifier.

10. (211) When comparing the FET to the bipolar transistor, the gate is to the base as the drain is to the

a. collector.	c. source.
b. emitter.	d. grid.

11. (212) What type of FET consumes the least amount of power and can be used to store binary data?

a. JFET	c. Depletion MOSFET
b. MOSFET	d. Enhancement MOSFET

12. (213) If the inputs to an operational amplifier, connected in the differential or common mode configuration, are equal in amplitude and phase, what is the output?

a. The sum of the input signals.	c. Same as input.
b. Twice the input.	d. Zero.

13. (214) Linear integrated circuits are those circuits which perform

a. switching functions.	c. regulation or amplification.
b. high-frequency switching.	d. low-frequency arithmetic functions.

14. (215) What logic and package type are most common for digital ICs?

a. TTL in a DIP.	c. ECL in a DIP.
b. TTL in a flat pack.	d. CMOS in a flat pack.

15. (216) Some of the advantages integrated circuitry has over transistorized circuitry are emphasized in

a. weight and space savings.
b. high power and signal capabilities.
c. inexpensive to produce unique items.
d. higher amplification and power handling capacity.

16. (217) A zero in any decimal number performs the function of

a. a multiplier.	c. a divider.
b. a place holder.	d. an expander.

17. (219) Add the following binary numbers:

$$\begin{array}{r} 1011101010 \\ +1000111001 \\ \hline \end{array}$$

a. 10100100011.	c. 11100100011.
b. 10110100011.	d. 10100101011.

18. (221) What is the binary equivalent of $634_{(10)}$?

a. 1110001011.	c. 1100111011.
b. 1000111010.	d. 1001111010.

19. (222) What is the binary equivalent of $193.53125_{(10)}$?

a. 11000000.01111.
b. 11000001.10001.
c. 10010000.11001.
d. 10110001.10001.

20. (223) The decimal equivalent of $10110111_{(2)}$ is

a. 173.
b. 179.
c. 183.
d. 197.

21. (224) What is the decimal equivalent of $.11011_{(2)}$?

a. .84375.
b. .84374.
c. .83275.
d. .84365.

22. (226) Add $54_{(8)}$ and $45_{(8)}$.

a. $87_{(8)}$.
b. $88_{(8)}$.
c. $112_{(8)}$.
d. $121_{(8)}$.

23. (227) Convert $2371_{(8)}$ to its equivalent decimal number.

a. 1017.
b. 1267.
c. 1273.
d. 1274.

24. (228) What is an advantage of the hexadecimal number system over the binary system?

a. The binary system use fewer digits to represent numbers.
b. The hexadecimal number system generally requires fewer digits to represent numbers.
c. The hexadecimal system uses the same radix as the binary system.
d. The hexadecimal system uses more bits to represent a numerical value; therefore, there is less chance of error.

25. (229) Convert the decimal number $934_{(10)}$ to its hexadecimal equivalent.

a. 3A5.
b. 3A6.
c. 3B5.
d. 3B6.

26. (230) Convert $11011101011001101 1_{(2)}$ to its hexadecimal number equivalent.

a. X'2759B'.
b. X'3759B'.
c. X'3759C'.
d. X'3795A'.

27. (231) Perform the following addition of hexadecimal numbers.

X'1F2B'
X'3CEF'
+X'2594'

a. 80AF.
b. 81AE.
c. 2839.
d. 6237.

28. (232) Convert the decimal number 1590 to BCD.

a. 1010110010000.
b. 10010110010000.
c. 100010001000.
d. 110010001000.

29. (233) How is the decimal number 431 represented in the excess-three code form?

a. 010000011001.
b. 010000110001.
c. 011101100100.
d. 101010010111.

30. (234) Convert the binary number 1001001 to the Gray code.

a. 1100110.
b. 1101100.
c. 1101101.
d. 1110011.

31. (235) In a positive logic circuit using OV and -6V, a binary ZERO would be represented by

a. +6V.
b. +3V.
c. OV.
d. -6V.

32. (236) The logic function where the function is true with one input high, but *not* with both inputs high, is known as the

a. NOR function.
b. OR function.
c. AND function.
d. EXCLUSIVE OR function.

33. (237) Select an advantage of resistor transistor logic (RTL) over resistor diode logic (RDL).

a. Electrical inversion is possible.
b. Greater shunting effects of parallel inputs.
c. Greater shunting effects of parallel outputs.
d. Offers better performance at a reduced speed.

34. (238) Which of the following expressions used in Boolean math means that A and B are ANDed together?

a. A + B.
b. A / B.
c. AB.
d. A - B.

35. (239) Refer to figure 1-40 of Module 10005, Unit 2. Under what conditions are both Q1 and Q2 conducting?

a. A = 0; B = 0.
b. A = 0; B = 1.
c. A = 1; B = 0.
d. A = 1; B = 1.

36. (240) In NOT-circuit operations using RTL, logic inversion is accomplished by which transistor configuration?

a. Common base.
b. Common emitter.
c. Common collector.
d. Emitter follower.

37. (241) In figure 1-42 of Module 10005, Unit 2, with the transistor conducting,

a. R4 drops most of the applied Vcc.
b. R4 does not provide a voltage drop.
c. the voltage at the collector equals Vcc.
d. the voltage at the collector equals -3 volts.

38. (242) Refer to figures 1-42 and 1-43 of Module 10005, Unit 2. The difference between a typical PNP-transistor NAND-gate and a PNP-transistor NOR-gate is that the

a. NAND-gate has positive bias on the base of the transistor.
b. NOR-gate has negative bias on the base of the transistor.
c. NAND-gate has negative bias on the base of the transistor.
d. NAND-gate emitter junction of the transistor is reverse biased.

39. (244) Refer to figure 1-45,A, of Module 10005, Unit 2. With zero volt on the inputs, the

a. diodes are reverse biased.
b. transistor is cut off.
c. diodes are conducting.
d. output is +6 volts.

40. (247) Refer to figure 1-48 in Module 10005, Unit 2. If input A is HIGH and input B is LOW, the output will be

a. Vcc + IR3.
b. Vcc - IR3.
c. Vcc.
d. OV.

41. (248) Of the four possible binary subtractions, how many can be performed by the quarter subtractor?

a. One.
b. Two.
c. Three.
d. Four.

42. (250) Refer to figure 1-51,A, of Module 10005, Unit 2. If input A is LOW and input B is HIGH, what is the condition of Q1 and Q2?

a. Cutoff.
b. Saturated.
c. Q1 is on and Q2 is off.
d. Q2 is off and Q1 is saturated.

43. (251) Refer to the two NOR-gates shown in figure 1-52 of Module 10005, Unit 2. With a positive-going signal (+6 volts) applied to both inputs of either gate and with Vcc = 6 volts, what is the voltage on the collector of Q1?

a. +6V.
b. +3V.
c. OV.
d. -6V.

44. (252) Of the following functions, which one is performed by and EXCLUSIVE OR circuit?

a. $\bar{A}B + AB$.
b. $A\bar{B} + \bar{A}B$.
c. $A\bar{B} + A\bar{B}$.
d. $AB + \bar{A} + B$.

45. (253) Of the following IC logic families, which is in most common use today?

a. CML.
b. DTL.
c. TTL.
d. RTL.

46. (254) How many outputs are available from an ECL gate?

a. One.
b. Two.
c. Three.
d. Four.

47. (255) Which IC family uses multiemitter input transistors?

a. HTL.
b. ECL.
c. TTL.
d. DTL.

48. (256) In Boolean logic functions, the vinculum is used for

a. negation and complementing.
b. negation and inhibiting.
c. grouping and negation.
d. inhibiting operations.

49. (257) The Boolean expression $XYZ + LMN = P$ is descriptive of

a. a circuit where an OR-gate feeds two AND-gates.
b. a circuit where two AND-gates feed one OR-gate.
c. the EXCLUSIVE OR operation.
d. a six-input OR-gate.

50. (258) What are the logic levels used within the TTL IC family?

a. 0 and 5 volts.
b. 0 and 6 volts.
c. 0 and -5 volts.
d. -5 and +5 volts.

51. (259) In order to trigger a flip-flop, a differentiating circuit produces an output signal that is

a. a sharp spike.
b. a pulse with slow rise time.
c. a positive-going square wave.
d. a negative-going square wave.

52. (261) Refer to figure 1-12 of Module 10005, Unit 3. What is the purpose of C1?

a. To integrate the input to Q2.
b. To differentiate the output of Q1.
c. To set the threshold voltage of Q2.
d. To speed the transition from one state to another.

53. (262) Which of the following is *not* a basic requirement for sustained oscillations?

a. Amplification.
b. A regenerative feedback.
c. A frequency-determining device.
d. A frequency-compensating network.

54. (263) What is an identifying features of the Armstrong oscillator?

a. A tickler coil.
b. A tapped coil.
c. A split capacitor.
d. A resonant circuit.

55. (264) What is the identifying features of a Hartley oscillator?

a. A tapped coil.
b. A tickler coil.
c. A split capacitor.
d. A resonant circuit.

56. (265) What is the identifying feature of a Colpitts oscillator?

a. A tapped coil.
b. A tickler coil.
c. Split capacitors.
d. A resonant circuit.

57. (267) In a crystal, which type of cut increase stability by reducing its temperature drift?

a. X.
b. Y.
c. Z.
d. AT.

58. (268) What are the identifying features of a Butler oscillator?

a. A transistor and a tapped transformer.
b. A transistor and split capacitors.
c. Two transistors and a crystal.
d. Two transistors and three RC networks.

59. (269) What additional function does a frequency multiplier perform when connected to the output of an oscillator?

a. Acts as a buffer amplifier.
b. Acts as an emitter-follower.
c. Acts as a unilateralization for the oscillator.
d. Acts as a neutralization for the oscillator.

60. (270) What component of a blocking oscillator circuit primarily determines the duration and the shape of the output pulse?

a. The output transistor.
b. The transformer.
c. The circuit resistance.
d. The circuit capacitance.

61. (271) Pulse width (PW) indicates the length of a pulse measured in time and is often expressed as the time between

a. the top of the pulse and the average-power point.
b. the bottom of the pulse and the half-power point.
c. the half-power points (.707 times the peak pulse amplitude).
d. the average-power points (.636 times the peak pulse amplitude).

62. (272) Which multivibrator is used for pulse stretching in digital circuits?

a. Astable.
b. One-shot.
c. Free running.
d. Retriggerable bistable.

63. (273) Which multivibrator, if any, is a free-running square or rectangular-wave generator?

a. Astable.
b. Bistable.
c. Monostable.
d. No multivibrators are free-running.

64. (275) Refer to figure 4-3 of Module 10005, Unit 3. What is the relationship of input pulses to T pulses?

a. One T pulse out for every one input pulse.
b. One T pulse out for every eight input pulses.
c. Eight T pulses out for every one input pulse.
d. Eight T pulses out for every three input pulses.

65. (276) How often must the highest frequency in the voice band signal be sampled to provide quality reproduction?

a. 6 times per cycle.
b. 4 times per cycle.
c. 3 times per cycle.
d. 1 time per cycle.

66. (277) Which factor determines the number of pulses that may be placed within the 80 microsecond sampling period?

a. The DC level.
b. The pulse width.
c. The pulse amplitude.
d. The relative amplitude.

67. (278) If you use 2 microseconds as the base width of the intelligence pulses with the minimum samples repetition rate, how many units of time can you allow for pulse transmission?

a. 10.
b. 20.
c. 30.
d. 60.

68. (280) Where is the feedback or error voltage in a PLL circuit applied?

a. To the phase detector.
b. To the output of the voltage-controlled oscillator.
c. At the output of the phase-lock loop circuit.
d. To the VCO circuit.

69. (281) When an inherent data shift occur resulting in a frequency difference between data clocking rates on and off the media, a PLL is used for

a. frequency synthesizer.
b. data synchronization.
c. frequency synchronizer.
d. data synthesizer.

70. (282) A bistable multivibrator will stay in one state until the

a. cross-connected capacitor is discharged.
b. other state is triggered.
c. cross-connected capacitor is charged.
d. input pulse ends.

71. (283) Which type of flip-flop may have outputs that are *not* necessarily of opposite states?

a. D-type.
b. Set-reset.
c. R-S latch.
d. JK master-slave.

72. (285) The J-K flip-flop can only

a. operate in a synchronous mode.
b. operate in an asynchronous mode.
c. change output state each time the input state changes.
d. change state when both inputs are logical 1 simultaneously.

73. (286) What is the first step in the TTL JK master-slave flip-flop sequence of operation?

a. Disable the AND-gate inputs.
b. Isolate the slave from the master.
c. Enter information from AND-gate inputs to the master.
d. Transfer the information from the master to the slave.

74. (288) What identifies a counter as a down-counter?

a. The ONE-side output of each flip-flop is used.
b. The ZERO-side output of each flip-flop is used.
c. Both the ONE- and ZERO-side outputs of each flip-flop are used.
d. The output is taken from the ONE-side of the final flip-flop.

75. (289) In a 6-stage parallel down-counter preset to the count of 15, how many clock pulses are required to reach a count of 12?

a. 44.
b. 29.
c. 4.
d. 3.

76. (290) The purpose of the control flip-flop used with a counter is to determine the

a. direction of count.
b. maximum count.
c. number to be skipped.
d. number to be preset.

77. (292) Refer to figure 1-27 of Module 10005, Unit 4. The purpose of blocking FF-C after count 8 is to

a. remove four counts.
b. add four counts.
c. remove two counts.
d. add two counts.

78. (293) Refer to figure 1-30 of Module 10005, Unit 4. The Mod-10 adding counter advances the count by

a. operating FF-B and FF-C together.
b. setting FF-B and FF-C after FF-D sets.
c. allowing the count to jump from 9 to 16.
d. inhibiting FF-B and FF-C before FF-D sets.

79. (294) One difference between a gray counter and a parallel counter is that a

a. gray counter is controlled by a control flip-flop.
b. gray counter does not count pulses.
c. parallel counter can count higher.
d. parallel counter is controlled by a control flip-flop.

80. (295) Synchronous operation of counters is provided by having all flip-flops

a. cleared sequentially.
b. reset simultaneously.
c. clocked sequentially.
d. clocked simultaneously.

81. (296) If a storage register does *not* clear before new information is input, the result is

a. garbled data.
b. loss of data.
c. inverted data.
d. normal data.

82. (297) A shift register that inputs a word for each read-in pulse and outputs a bit for each transfer out is a

a. serial-in/parallel-out register.
b. parallel-in/serial-out register.
c. parallel-in/parallel-out register.
d. serial-in/serial-out register.

83. (298) Double-line transfer does *not* require which type of pulse?

a. Control.
b. Shift.
c. Transfer.
d. Clear.

84. (299) What type of electronic circuit translates a combination of inputs to one of a group of outputs?

a. Counter.
b. Decoder.
c. Encoder.
d. Register.

85. (300) Circuits that require more current at the output than can be developed by diodes often use

a. relay decoders.
b. OR-gate decoders.
c. transistor decoders.
d. pyramid AND-gate decoders.

86. (301) An encoder would most likely be used to convert

a. decimal to binary.
b. binary to decimal.
c. decimal to alpha.
d. alpha to decimal.

87. (302) When addition results in a sum too *large* for the *sum register* to hold, what occurs?

a. Reset.
b. Carry.
c. Machine stop.
d. An arithmetic fault.

88. (304) In an adder using parallel carry, a carry generated in one stage is

a. dropped at the stage when generated.
b. presented to the next higher stage only.
c. sequentially presented to all other stages.
d. simultaneously presented to all other stages.

89. (305) A circuit that will produce the correct result for each of three possible subtractions is the

a. OR-gate.
b. AND-gate.
c. inverter.
d. inhibitor.

90. (306) In figure 1-28 of Module 10005, Unit 5, assume the inputs are $A = 11001_2$, and $B = 11011_2$; with the values given, which AGs will be enabled by the register flip-flops?

a. AG-10.
b. AG-20.
c. AG-10 and AG-30.
d. AF-20 and AG-40.

91. (307) In figure 1-23 of Module 10005, Unit 5, to what stages is signal 3 applied?

a. 2^0 and 2^1.
b. 2^0 and 2^2.
c. 2^2 and 2^1.
d. 2^2 and 2^1 and 2^0.

92. (308) A bit is a binary digit that is expressed as a

a. half word.
b. character.
c. parity bit.
d. ONE or ZERO.

93. (309) What are the two types of parity-checking circuits?

a. Even and odd.
b. Decimal and binary.
c. Parallel and serial.
d. Detecting and generating.

94. (312) The storage error detection circuit is primarily what type of circuit?

a. Scanner.
b. Comparator.
c. Multiplier.
d. Inclusive OR.

95. (313) In a D/A converter, the step voltage amplitude depends upon the maximum count and the

a. ripple voltage.
b. static voltage.
c. stored voltage.
d. applied voltage.

96. (314) Shaped as numbers, the nixie tube has ten

a. anodes.
b. cathodes.
c. grids.
d. screens.

97. (315) The sine X generator output feeds an instrument with

a. an LED display.
b. a nixie display.
c. indicator needles.
d. a digital display.

98. (316) Refer to figure 1-48 of Module 10005, Unit 5. Which integrated circuit may be used for excess-three-to-decimal decoding?

a. SN74L42.
b. SN7442A.
c. SN74L43.
d. SN74L44.

99. (317) A microprogram is usually

a. only microinstructions in RAM.
b. a bipolar read-only memory (ROM) containing a set of microinstructions.
c. a program counter for the main program.
d. a substitute for the program in main memory.

100. (319) Which of the following in a microcomputer provides an interface between the microprocessor and peripheral devices such as a cassette or magnetic tape?

a. PIA.
b. ROM.
c. ALU.
d. RAM.

101. (320) A tristate (three-state) logic gate is capable of

a. low impedance state used with a bidirectional bus.
b. high impedance state used with a unidirectional bus.
c. disconnect state used with a bidirectional bus.
d. low impedance state used with an address bus.

102. (321) A disadvantage common to nearly all peripheral devices is

a. high-speed response.
b. high data exchange rates.
c. incompatible with phone lines.
d. slowness of response.

103. (322) Which of the following are devices classified strictly as off-line rather than auxiliary equipment?

a. Typewriters, line printers, and sorters.
b. Tabulators, line printers, and card punches.
c. Tabulators, card punches, and sorters.
d. Paper tape punches, card punches, and typewriters.

104. (323) The major difference between the two most widely used punched cards is the number of

a. rows of each.
b. columns of each.
c. zones.
d. spaces.

105. (324) What is the *main disadvantage* of reading data from IBM cards directly into the main computer memory?

a. The card-reading equipment is expensive.
b. The card-reading equipment requires too much space.
c. The process is inaccurate.
d. The method is slow and does not afford best use of computer time.

106. (325) Data on punched paper tape is similar to magnetic tape in that it *must* be read

a. on a random basis.
b. sequentially.
c. by pseudorandom selection.
d. on a random-sequential selection basis.

107. (326) What are two means of converting the punched paper tape code into an electrical code?

a. Brushes and punches.
b. Punches and electric cells.
c. Photoelectric system and brushes.
d. Mechanical punches and electric cells.

108. (328) Magnetic tape used as a storage medium is usually

a. a slow, random-access tape coated with oxide.
b. any tape coated with oxide.
c. a fast, sequential-access plastic tape coated with ferric oxide.
d. a coated plastic tape designed for large capacity memory storage.

109. (329) What are the concentric circle data paths on a disk called?

a. Tracks.
b. Sectors.
c. Margin paths.
d. Sector indexes.

110. (330) What recording technique is used on magnetic disks for maximum bit density?

a. FM.
b. AM.
c. NRZ.
d. MFM.

111. (331) What device in a keyboard can permanently store the codes for each key?

a. Typing ball.
b. The key switches.
c. A read-only memory.
d. The typewriter part of the keyboard.

112. (333) What visual display uses a secondary electron emission technique?

a. Standard CRT.
b. Storage CRT.
c. Plasma Panel.
d. LED.

113. (334) In a computer system, a magnetic tape unit uses which of the following as its transducer?

a. A storing energy output.
b. A read transducer.
c. A magnetic read/write head.
d. Multiple address selection mechanisms.

114. (335) In a write operation, what basic component of the memory section *first* receives the word to be written?

a. Storage control.
b. Memory address register.
c. Memory exchange register.
d. Storage selection circuits.

115. (336) All of the following are classified as volatile storage devices *except*

a. electrostatic tubes.
b. acoustic lines.
c. flip-flops.
d. cores.

116. (337) Name two types of magnetic cores used for storing internal data in a computer.

a. Ferrite and copper cores.
b. Tape-wound and toroid cores.
c. Copper and toroid cores.
d. Ferrite and tape-wound cores.

117. (339) What is the effect if two current-carrying wires are passed through a core at right angles to each other?

a. The result is a third magnetic intensity double that which is in each wire.
b. The result is as if a single wire carried the sum of the current.
c. The result is as if a single wire carried the vector sum of the current.
d. The result is a magnetic intensity equal to three times that of a single wire.

118. (340) What type of pulse will minimize the effects of noise from adjacent cores during readout?

a. Strobe.
b. Read.
c. Inhibit.
d. Half-write.

119. (342) What type of semiconductor RAM requires refreshing?

a. Bipolar.
b. Unipolar.
c. Static.
d. Dynamic.

120. (344) In *most* computer applications the write head is separated from the moving magnetic surface by a few thousandths of an inch in order to reduce

a. abrasive wear.
b. eddy current.
c. magnetic reluctance.
d. required driving current.

121. (345) A comparison of the RZ and NRZ systems shows that serial data can be read

a. in a shorter period using the non-return-to-zero method.
b. at the same rate.
c. twice as fast by the RZ system.
d. four times faster using the NRZ system.

122. (346) What is the purpose of providing a space between channels on a magnetic drum?

a. Increases data storage capability.
b. Permits faster access to data.
c. Prevents crosstalk.
d. Reduces noise.

123. (347) Which of the following labels is classified as an external magnetic tape label?

a. Header.
b. Trailer.
c. Reel identification.
d. End-of-file label.

124. (348) What is used to indicate the beginning and end of a data track on a magnetic disk?

a. A record.
b. Index points.
c. A gap.
d. A character.

END OF EXERCISE

MAIL TO: ECI, GUNTER AFS AL 36118-5643

STUDENT REQUEST FOR ASSISTANCE

PRIVACY ACT STATEMENT

AUTHORITY: 10 USC 8012. PRINCIPAL PURPOSE: To provide student assistance as requested by individual students. ROUTINE USES: This form is shipped with ECI course package. and used by the student, as needed, to place an inquiry with ECI. DISCLOSURE: Voluntary. The information requested on this form is needed for expeditious handling of the student's inquiry. Failure to provide all information would result in slower action or inability to provide assistance to the student.

I. CORRECTED OR LATEST ENROLLMENT DATA

1. THIS REQUEST CONCERNS COURSE (1-6)
2. TODAY'S DATE
3. ENROLLMENT DATE
4. AUTOVON NUMBER
5. SOCIAL SECURITY NUMBER (7-15) ☐☐☐ - ☐☐ - ☐☐☐☐
6. GRADE/RANK
7. NAME (*First initial, second initial, last name*) (17) – (18) – (19-32)
8. ADDRESS (33-53) (54-75)

OJT ENROLLEES--Address of unit training office with zip code.

ALL OTHERS--Current mailing address with zip code.

9. NAME OF BASE OR INSTALLATION IF NOT SHOWN ABOVE
10. TEST CONTROL OFFICE ZIP CODE/SHRED (33-39)

II. REQUEST FOR MATERIALS, RECORDS, OR SERVICE

X	*Place an 'X' through number in box to left of service requested.*
1	Request address change as indicated in Section I, Block 8.
2	Request Test Control Office change as indicated in Section I, Block 10.
3	Request name change/correction. *(Provide Old or Incorrect data here)*
4	Request Grade/Rank change/correction.
5	Correct SSAN. *(List incorrect SSAN here.)* *(Correct SSAN should be shown in Section I.)*
6	Extend course completion date. *(Justify in "Remarks")*
7	Request enrollment cancellation. *(Justify in "Remarks")*
8	Send VRE answer sheets for Vol(s): 1 2 3 4 5 6 7 8 9 10 Originals were: [ ] Not received [ ] Lost [ ] Misused
9	Send course materials. *(Specify in "Remarks")* [ ] Not received [ ] Lost [ ] Damaged
10	Course exam not yet received. Final VRE submitted for grading on ____________ (date).
11	Results for VRE Vol(s) 1 2 3 4 5 6 7 8 9 10 not yet received. Answer sheet(s) submitted ______________ (date).
12	Results for CE not yet received. Answer sheet submitted to ECI on ____________ (date).
13	Previous inquiry ([ ] ECI Fm 17, [ ] ltr, [ ] msg) sent to ECI on ____________ (date).
14	Give instructional assistance as requested on reverse.
15	Other *(Explain fully in "Remarks")*

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K	VOL 33-35	GR 36-38
M	33-34	35-40
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	TC 36-37	38
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	MC 39-42	

REMARKS *(Continue on reverse)*

OJT STUDENTS must have their OJT Administrator certify this record.

ALL OTHER STUDENTS may certify their own requests.

I certify that the information on this form is accurate and that this request cannot be answered at this station.

SIGNATURE

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ELECTRONIC COMPUTER AND SWITCHING SYSTEMS SPECIALIST

(AFSC 30554)

Volume 3

Systems Maintenance

AIR UNIVERSITY

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Preface

THIS THIRD and last volume of CDC 30554, *Electronic Computer and Switching Systems Specialist,* covers the principles of systems maintenance. Chapter 1 covers maintenance programming, the fundamentals of programming, instructions, and flow charting. Chapter 2, System Operation and Preventive Maintenance, takes up systems monitoring methods and procedures, operational/performance checks, and adjustment/alignments. Chapter 3, General Maintenance Techniques, provides equipment identification, test equipment, and an introduction to computer and switching systems. For Chapter 4 you are referred to Module 10001, *Corrosion Control* (which is included in your course package) for objectives 444-454. Chapter 5, Corrective Maintenance, includes troubleshooting methods and procedures, soldering, wire wrapping, repair and replacement of components, and circuit card repair. Chapter 6, Power Supplies, informs you about rectifiers, filters, regulators, and the typical solid-state power supply. The subject of Chapter 7 is the same as that of Module 10012, *Basic Techniques of Waveform Measurement Using an Oscilloscope* (which is included in your course package), and covers objectives 486 through 496.

Modules 10001 and 10012, referenced in the text, are included as separate inclosures.

Foldouts 1, 2, and 3 are printed and bound in the back of the volume.

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This volume is valued at 51 hours (17 points). These hours and points include those assigned to the modules that you will study as Chapters 4 and 7.

Material in this volume is technically accurate, adequate, and current as of July 1981.

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NOTE: In this volume, the subject matter is developed by a series of student-centered objectives. Each of these carries a three-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see whether your answers match those in the back of this volume. If your response to an exercise is incorrect, review the objective and its text.

Maintenance Programming

THE AIR FORCE'S NEED and use of electronic computers has increased since we entered the space age. These computers are required to perform specific operations rapidly, accurately, and most importantly, reliably. It is for this reason that attempts are made to simplify troubleshooting and reduce downtime. This is the role of maintenance programs and the reason for their development.

The first maintenance programs for the early large-scale computers printed out large amounts of information. Much of the information was of no use to maintenance personnel. After considerable refinement, these programs and their printouts became very useful as maintenance tools.

Computer systems have come a long way. They have advanced through vacuum tubes, transistors, and microelectronics into modular systems. Improvements in the quality, effectiveness, and instruction components (less instruction needed to perform the same functions) of the software have resulted in greater reliability and maintainability of computer systems. In other words, your job as an electronic computer and switching systems specialist continues to be simplified as the computer industry continues to make state-of-the-art improvements. Even with all these improvements, you will find that many of the basic theories used with the first computers can be related to many of today's newer systems.

In this chapter we are primarily concerned with programming, but we do not intend to try and make a programmer out of you. The programming we will study here is maintenance programming. You do not need the depth of programming knowledge that a computer programmer needs, but you do need enough knowledge of maintenance programs to:

- Analyze computer maintenance programs.
- Interpret computer maintenance program printouts.

1-1. Maintenance Programs

Maintenance programs are divided into three main classes: reliability, diagnostic, and utility programs. The programs use the same type tape, memory, computing, and drum circuits as operational programs.

400. Name the main types of maintenance programs and state the purpose of each.

This segment will cover, in order, the main classes of maintenance programming just referred to. The several subareas of diagnostic programs are examined in especial detail.

Reliability Programs. We use reliability programs in both preventive and corrective maintenance tests to detect circuit failures rapidly and to discover failures that may occur only under particular operating conditions. Examples of troubles that are not evident at all times are failures that appear at specific repetition rates or for certain combinations of bits. To detect such failures, reliability programs check logical operation, paths of information flow, timing, and the computer's ability to perform all functions, executions of instructions, etc.

Reliability programs check the logical functioning of either an entire computer section or of individual circuit groups in a section. Both methods assume that associated circuits, which are not directly checked by the program, are in satisfactory operating condition. These programs can be considered to fall into two categories, *first order* and *second order*. First-order reliability programs check the operation of assemblies or circuit groups, such as registers and counters. Second-order programs are designed to check basic circuits and components. In most cases, first-order programs are merely a combination of several second-order programs.

A reliability program provides a good or bad indication of the tested computer section or circuit's ability to perform its operating functions. For example, consider a reliability program that checks the switching time for relays within a specific section of a computer. As long as the switching time of the relays is within normal limits, the reliability program will indicate satisfactory operation. When the switching time is excessive, however, there is an indication that maintenance is required. If the program runs successfully, there are no failures within the checked area. In the event of a failure indication, the failure may be in the area being checked or in another area that has been assumed free of trouble. Diagnostic maintenance programs should then be used to locate the source of trouble.

Diagnostic Programs. To be efficient, diagnostic maintenance programs must enable you to narrow the area of a failure down to the smallest possible number of circuits. This can be done through increasing area, decreasing area, overlapping area, and large area checks. The most effective method will depend upon the particular type of computer being tested.

Increasing area check. The increasing area check initially tests a small number of circuits. If a check indicates that all tested circuits are operating properly, successive checks add progressively greater numbers of circuits. Circuits we know to be operating correctly are used to check other circuits. This process is continued until all circuits that can be checked by a maintenance program have been tested.

Decreasing area check. This method initially checks a large number of circuits. If trouble is detected in a large area, we check successively smaller portions of the equipment until the stages affected by the failure are not included in the test area. You should then be able to determine which stages are defective. If the check of a large area reveals no error, the remaining large areas of the equipment are checked until the trouble is detected. In many cases, trouble can be located more rapidly this way than by the increasing area method.

Overlapping area check. Another efficient method of isolating trouble to a small section of the equipment is the overlapping area check. The routines of this type of maintenance program overlap each other. Thus, a failure can be located at the overlapping portions of routines that indicate the presence of trouble.

Large-scale check. You may not be able to program an effective maintenance test for a small section of a computer. In such cases, a maintenance program can be used only to determine the general area in which the malfunction occurs. When the general area is located, conventional troubleshooting will be necessary to find the circuit in which a failure has occurred.

Confidence diagnostic program. This type of maintenance program is normally cycled in conjunction with the operational program, and in some instances, it is part of the operational program. Basically, confidence diagnostic programs provide the particular computer system with the ability to monitor the operation of on-line and backup (sometimes called standby) hardware. Confidence diagnostic programs are capable of detecting and isolating failures in the on-line and backup hardware as well as of monitoring hardware status.

Utility Programs. Utility programs are used as aids for both operation and maintenance programming. This type of program is used to print out information from magnetic cores or other storage devices within the computer memory section. It is also used to transfer maintenance programs from punched cards or magnetic tape into the computer memory section. Utility-tracing programs provide a printed record of the contents of various computer registers to let you follow maintenance program operations.

Exercises (400):

1. What are reliability programs?

2. Name the two categories of reliability programs and their purpose.

3. Which types of checks are used to narrow the area of a failure down to the smallest possible number of circuits?

4. What is an increasing area check?

5. If a check of a large area indicates a trouble, what check should then be made?

6. When routines intermingle, an ________ ________ check can be used.

7. What do utility-tracing programs provide?

1-2. Programming Fundamentals

Your instructions to a computer must be in a language that the equipment understands. Therefore, you must communicate by using a code of numbers or digits—the language of computers. Since the information you need to convey to the computer must be presented as a combination of digits, it is desirable for you to have some convenient method of describing these binary digits or bits.

401. Describe computer words and the functions they perform.

Computer Words. Normally, a specified number of bits within a computer representing an instruction, operation, or other data are considered to be one *word.* The number of bits in any particular word is called the *word length.* Both fixed and variable-word-length computers are in use today. Word length may vary from one system to another. However, the more common word lengths are 16 and 32 bits or digits long.

Operand words. The information used by a computer is in the form of instruction words and operand words. Operand words contain the data which is used in computations. The operand word may be a simple number or some form of alphabetic information. The computer operates on the operand, performing arithmetic steps, defining conditions, making decisions, and producing resulting information.

Instruction words. An instruction word is a binary-coded order to a computer. When the order is decoded, it permits the computer to perform a specific operation. One group of bits within an instruction word is called the *address portion* and identifies a specific location in the memory section of the computer. The other portion of the instruction word is referred to as the *command portion.* The command portion specifies the operation the computer is to perform. The bits which make up the command portion of the word may be further divided into groups, each having its own significance.

Addresses. Instruction words and operand words are stored in the memory section of a computer. In a *simple address computer,* a program instruction may specify only one location in the memory. Some computers are of the multiple-address type. Each instruction of a *multiple address computer* may specify two or more locations in the memory.

The number of digits required for the address portion of an instruction word is determined by the capacity of the computer memory. For example, if a memory section can store 4096 words, the memory locations can be designated by numbers 0 through 4095. Since the number of addresses can vary from one computer to another, and we have already stated that word length may be different, it is easy to see that the format of computer words will vary also. You will need to check the technical data for your computer to obtain specific word bit assignment information.

Exercises (401):

1. What is a computer word?

2. What is the function of the operand word?

3. What are the two component parts of the instruction word?

4. What determines the number of bits to be used for a memory address?

402. Define "mnemonic code instruction" and explain the function performed by selected instruction classes.

Here we will look, first, at mnemonic code instructions, after which, second, we will take up instruction classes. Five subareas of instruction classes are gone into further.

Mnemonic Code Instructions. You have considered the computer instruction word in the terms of its size and structure. The binary instruction code is very efficient for use with the computer, but it is not convenient for you or the programmer. Therefore, decimal mnemonic instruction codes are developed and used by the programmer to represent the binary instructions that are accepted by the computer.

These mnemonic codes may vary from one system to another or from one manufacturer to another. However, you will often find similarities in the assigned codes.

Writing programs for the computer is like writing a step-by-step procedure for someone to perform a task. The written mnemonic code doesn't look like the binary computer code, but it is a lot easier to read and write.

Instruction Classes. The mnemonic instructions are grouped into classes of computer operations. The following are examples of instruction classes for a hypothetical computer.

- Decision.
- Arithmetic.
- Transfer.
- Shift.
- Index register.
- Input/output.

Decision instructions. To enable the computer to make decisions, jump instructions are often provided. Depending upon the answer to a question, each jump instruction is followed by one of two possible courses of action. Either the normal sequence of executing instructions is maintained, or it is interrupted and a new sequence is begun. The following terms are associated with jump instructions.

a. Jump—the operation that causes the computer control section to select the next instruction to be executed from the memory location specified by the address part of the jump instruction. This interrupts the normal sequence of executing instructions.

b. Conditional jump—an instruction which causes a jump to occur if certain conditions are satisfied. If the conditions are not satisfied, the next sequential instruction is executed.

c. Unconditional jump—an instruction that causes a jump to occur independent of any conditions.

The jump mnemonic commands start with the letter "J." The letters that follow the "J" specify the type of jump or the conditions. Examples are:

- JHLT - Jump and halt.
- JMP - Unconditional jump.
- JOF - Jump on overflow.
- JAP - Jump if accumulator is positive.
- JAZ - Jump if accumulator is zero.

Arithmetic instructions. These are the instructions that perform arithmetic or logical operations on data stored in specific registers or accumulators of the computer. Examples are:

- CAM - Clear add memory.

- AM - Add memory.
- CSM - Clear subtract memory.
- SM - Subtract memory.
- MM - Multiply memory.
- DAQ - Divide.

Transfer instruction. The function of a transfer instruction in the computer is to duplicate a word in another section of the computer. The original word is unchanged by the transfer, and the contents of the receiving element are replaced. Examples are:

- TAM - Transfer accumulator to memory.
- TMQ - Transfer memory to Q register.
- TQM - Transfer Q register to memory.

Shift instructions. Shifting establishes the position of the binary point of a number before and after arithmetic operations. Since the value of a number is relative to the position of the binary point in a word, shifting is equivalent to multiplying or dividing by a power of two. Examples of mnemonic codes for shift operations are:

- SLA - Shift accumulator left.
- SRA - Shift accumulator right.
- SLAQ - Shift A and Q left.

Input/output instructions. These are the instructions that perform operations such as select - SEL, read - RD, write - WR, rewind - RWND, etc.

Exercises (402):

1. Define "mnemonic code instruction."

2. What is the advantage gained by using mnemonic instructions?

3. What are the three jump instructions?

4. What is the function of a transfer instruction?

5. What is the shift instruction used for within the computer?

403. Define terms and specify the process of scaling and floating point operation.

Scaling. Despite the arithmetic section's interpretation that all numbers are less than plus one or greater than or equal to minus one, you or the programmer are not restricted to this range. You may assume that the binary point is located anywhere within a word or outside of a word. Once you make this assumption, however, you must keep track of the assumed binary point throughout all arithmetic operations.

Fixed scaling. This process of representing any desired number by selecting an appropriate binary point is called *scaling,* and the number of positions between the computer's binary point and the assumed binary point is called the *scale factor.* The scale of a number is that power of two which, when multiplied by the computer number, produces the desired number.

For example, to represent the number 8 using the computer number 0.5, the scale factor must be 4. That is, with a scale factor of $4 = 0.1000 \ldots .0$, the computer number $0.5 - 0.1000 \ldots .0$, is equal to $0.5 \times 2^4 = 0.5 \times 16 = 8 = 1000$.

A positive scale factor indicates that the assumed binary point is to the right of bit position zero. A scale factor of zero indicates that the assumed point coincides with the arithmetic section's point. A negative scale factor indicates that the assumed point lies to the left of bit position zero. Note that a negative scale factor designates a fractional number, because it specifies that the binary point precedes the number. Similarly, except for minus one, a zero scale factor indicates a fractional number.

The manipulation of scaled numbers only requires that you keep track of the assumed binary point, which may move or have to be moved for arithmetic operation.

Floating point operation. When the number of operands required for a calculation is very large, or the range of the operands is not predictable, operation in the fixed point arithmetic mode becomes extremely difficult, because of the scaling requirement. When such situations are encountered, the floating point arithmetic mode is used.

In floating point operation, the binary points are automatically repositioned throughout the computation process, thus giving the correct results without any action by the programmer. This advantage of floating point arithmetic is offset by the disadvantage of having to use bits within the floating point word to indicate the position of the binary point, thereby reducing the precision that can be achieved with a given word size.

Almost everyone is familiar with the representation of very large or very small numbers by the convenient device of separating such numbers into three parts: the *mantissa,* the *base,* and the *exponent* of the base. For example, the very small decimal number 0.0000001234 can be compactly represented as follows: $0.1234 \times 10^{+6}$, whereby the mantissa is 0.1234, the base is 10, and the exponent is -6.

Note that this number was obtained from the decimal number by shifting the decimal point and giving the base 10 a negative exponent equal to the number of shifts. The name *floating point* arises from the fact that the decimal point "floats" in reference to the mantissa, its position being determined by the exponent. Note also that both the mantissa and the exponent of a floating point number can be either positive or negative and that the exponent is an integral power of 10.

Floating point values are often expressed in normalized form. A normalized decimal floating point number is one whose most significant digit immediately follows the decimal point. Thus, the number 0.1234×10^{-6} is in normalized form. Normalization allows for the maximum number of significant digits in a given number of digit positions.

Exercises (403):

1. Define the term "scaling."

2. What is a scale factor?

3. What does a scale factor of zero indicate?

4. What does a negative scale factor indicate?

5. When might floating point operation be required?

404. Tell what a "program loop" is and state the function of program loops and address modification.

Our two topics in this unit are, in sequence, loops and address modification and index registers. Material on four different subareas appears under loops and address modification.

Loops and Address Modification. Numerous computer operations are repetitive in nature. For example, consider the military payroll. Generally speaking, a certain basic pattern must be repeated over and over again in computing a payroll. The purpose of this objective is to acquaint you with some of the techniques used to insert an instruction in a program that will cause a particular section of that program to be repeated. The repeated section, together with the modifying elements, is usually referred to as a loop.

It is difficult to subdivide the loop into its component functions. However, the loop is normally considered to consist of the following four parts:

- Initializing.
- Computing.
- Modifying.
- Testing.

Initializing. The initializing part of a loop sets up the conditions to cause the loop to start in the correct manner. An important point for you to remember in connection with initializing is that the initial conditions are set up in the beginning of the loop and are not repeated. For example, the number 10 may initially be placed in a counter to indicate the number of times the loop is to be repeated. During the course of the routine, the contents of the counter will be systematically reduced. However, the loading of the computer happens only once, at the beginning of the routine.

Computing. An example of loop computing is the usual addition process involved in obtaining the sum of several numbers.

Modifying. Perhaps the most common example of loop modifying is the systematic change, or modification, of the address portion of a computer instruction.

Testing. The testing part of a loop functions to determine the number of times that the loop is to be repeated. You may remember the example of the counter that was initially loaded with the value of 10. The loop, of course, was to be repeated 10 times. The program must periodically check the contents of the counter, since this value is reduced by one each time the loop is performed. When the counter reaches zero, the proper number of loop repetitions has been performed.

Index Registers. Reducing programming, wasted computer storage space, and time are the primary values of the index registers. Specifically, index registers are used to perform many routine functions, such as sorting, tabulating, and table compilation. Such functions are performed by *iterative programs* or *loops* that repeat a certain number of instructions as often as necessary. For an iterative routine, your program data is usually stored in sequential locations. The computer is able to acquire this data through a single program instruction and an associated index register. Each time the computer causes the instruction to be executed, the amount in the index is either added to or subtracted from the address (memory location) of the current instruction. This modified address is known as the *effective address.* In other words, each time the computer executes a part of the basic instruction, that part, called the effective address, is the one used by the computer program. For example, if you wish to add 100 numbers that are stored in 100 sequential addresses, it is not necessary to use 100 instructions to add, but only one instruction that specifies the first address of the series to be added.

Exercises (404):

1. What is a "program loop" and what is its function?

2. How do index registers reduce programming?

3. What is an effective address?

1-3. Flow Charts

Before a program is actually written, it is usually necessary to show the required steps in block diagram form. This graphical description of a computer program is called a computer *flow chart.* The flow chart may be generalized or detailed, depending upon the requirements of the problem. Generally speaking, the larger and more complex the problem, the more detailed the flow chart will be.

405. Identify flow diagram symbols and their meanings, using figure 1-2 as necessary.

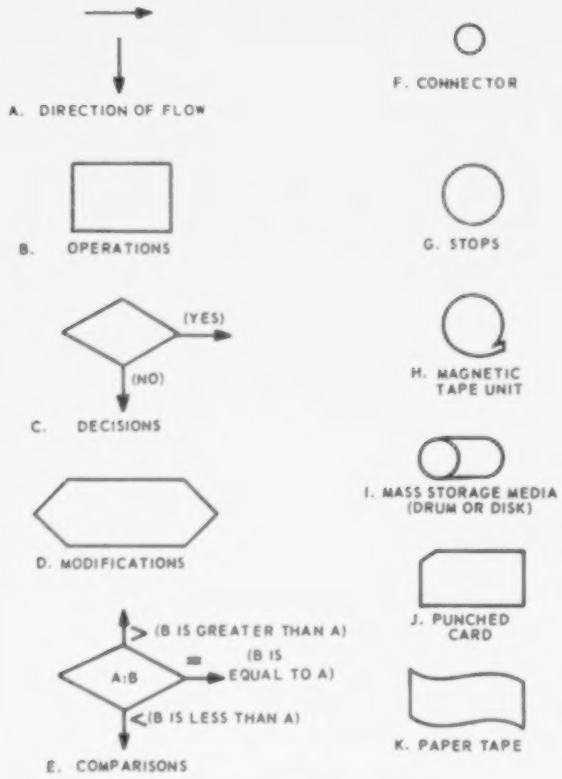

Figure 1-1. Typical flow chart symbols.

Flow Chart Symbols. Because flow charts contain many operations, it is desirable for each type of operation to be represented by a symbol of unique shape. It is advantageous to use a standardized set of these shapes or symbols, so that you may more easily interpret the different flow charts. Unfortunately, the symbology within the computer field has not yet reached a completely standardized state. Figure 1-1 illustrates the more frequently used flow chart symbols.

Flow lines. Refer to A of figure 1-1. The direction of flow line is used to connect all symbols and indicate the flow. If the direction of flow is in the normal direction (left to right or top to bottom), it is *not* necessary to use the arrowheads.

Operation symbols. Refer to figure 1-1, item B. This symbol is used for all program operations not involving reading, writing, decisions, or modifications. The operation symbol normally contains a description of a function. Several types of statements can be included within the operation symbol. For example, a combination of arithmetic formulas and statements indicating the movement of data may be included within a single box.

An operation box is connected to the rest of the flow chart by two flow lines—one entry and one exit. The operation box specifies the operation that must be executed before the program proceeds to the exit flow line.

Decision and comparison symbols. The symbols are illustrated in figure 1-1, C and E, respectively. These symbols indicate a place in the program where a test must be made in order to choose one of several courses. The symbol specifies the test to be made, and the flow lines leading from the box indicate the results of the test. The function of a decision symbol may be indicated by a simple question written within the symbol. Decision symbols never indicate a change in information in the computer, but only a possible change in the course of the program. For example, a simple type decision symbol may contain a question whose answer is yes or no. If the answer is yes, the program follows an exit flow line marked "Y"; if the answer is no, the program follows an exit flow line marked "N". Many notations are used with the decision and comparison symbols. Some of the more frequently used notations and their functions are these:

Notation	*Function*
= or EQ	On equal
≠	On not equal
> or HI	On greater than
< or LO	On less than
≥	On equal or greater than
≤	On equal or less than
+	On positive
−	On negative
= 0	On zero
≠ 0	On not zero
Y	On yes
N	On no
T	On true
F	On false

Modification symbol. Symbol D represents a modification. This symbol denotes an alteration in the address or operation part of an instruction. It may also be used to denote changes which are essentially counting in nature.

Connector symbol. The connector symbol is illustrated by item F. This symbol is used to connect remote portions of a flow chart with one another without the use of long or crossing lines. An *exit connector* terminates a flow line. It is normally labeled with a number or letter reference. The program will then continue at an *entry connector* symbol, which is labeled with the same number or letter reference.

Start, stop, or halt. The word "Halt," "Start," or "Stop" is usually placed within the symbol illustrated by item G. These symbols are used to clearly indicate the beginning, any temporary halts, and the end of a program. For example, a halt symbol may be used to show such conditions as input error or a wait for more data.

Input-output symbols. Symbols that represent input and output media are shown in items H, I, J, and K of figure 1-1. Input data can be obtained from punched cards, magnetic tapes, magnetic drums, and magnetic disks. Similarly, output data can be transferred to punched cards, paper tapes, magnetic drums, magnetic disks, and display devices.

Exercises (405):

Refer to figure 1-2 to answer questions 1, 2, and 3. Identify by the symbol, letter, or contents.

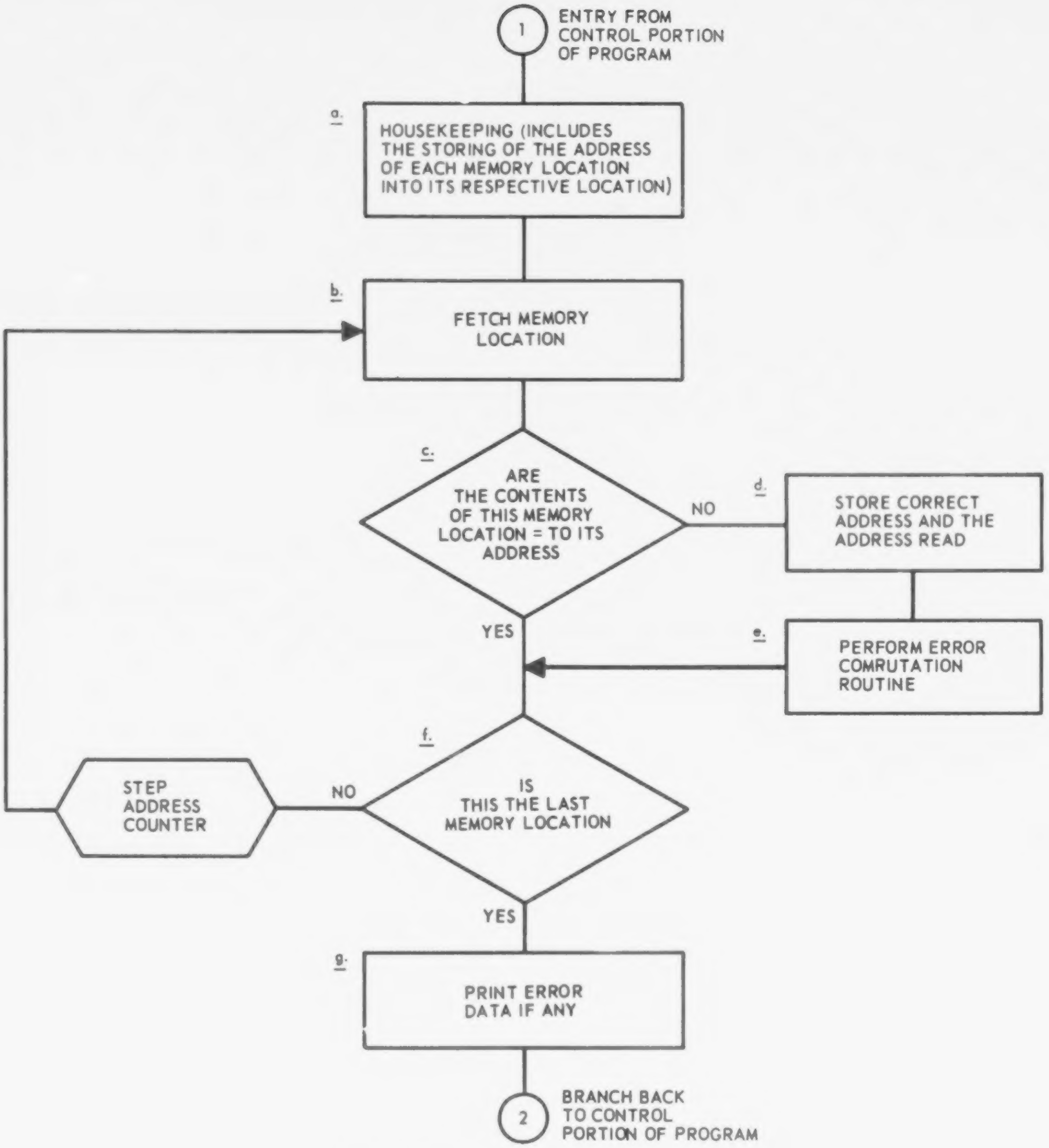
1
ENTRY FROM CONTROL PORTION OF PROGRAM
a.
HOUSEKEEPING (INCLUDES THE STORING OF THE ADDRESS OF EACH MEMORY LOCATION INTO ITS RESPECTIVE LOCATION)
b.
FETCH MEMORY LOCATION
c.
ARE THE CONTENTS OF THIS MEMORY LOCATION = TO ITS ADDRESS
NO
d.
STORE CORRECT ADDRESS AND THE ADDRESS READ
YES
e.
PERFORM ERROR COMRUTATION ROUTINE
f.
IS THIS THE LAST MEMORY LOCATION
NO
STEP ADDRESS COUNTER
YES
g.
PRINT ERROR DATA IF ANY
2
BRANCH BACK TO CONTROL PORTION OF PROGRAM

Figure 1-2. Flow chart for memory address test.

1. Identify the symbol representing a program modification.

2. Identify the decision symbols.

3. Identify the connector symbols.

4. What type of information is found within an operations symbol?

406. Specify the levels of flow charting and give an example of each.

Types of Flow Charts. A flow diagram or chart serves a multitude of very important functions. The chart illustrates the logical steps required, the decisions reached, and the path to be followed as a result of the decisions. Properly annotated, it calls attention to memory cell allocation, input/output requirements, data accuracy considerations, and register usage.

Flow charts can be conveniently classified according to the amount of detail that is included. There are *top-level flow charts* and *detailed flow charts.* The top-level flow chart normally defines the overall aspects of a problem, or at least the major functions. By comparison, the detailed flow chart is usually a detailed breakdown of one of the major functions of the top-level flow chart. The low-level flow chart may reach a one-to-one correspondence between symbols and instructions.

There will usually be several flow charts for a given program area. These may be compared to the prints found in a maintenance manual; for example, the block diagram to show the relationship of major units (top-level) or the schematics of the circuits (low-level). Flow charts should always be available at a level low enough to implement all the uses in that program.

Exercises (406):

1. What flow charts exist which can be classified by the amount of detail they include?

2. What are the two levels of flow charts?

3. A high-level flow chart is a very general overview, while a low-level flow chart may reach a one-to-one correspondence between what two things?

4. A schematic of a circuit would compare with which type of flow chart?

5. At what level should flow charts always be available?

1-4. Maintenance Programs

As stated earlier, many of the failure printouts generated by the older computer systems left much to be desired. However, as the software improved, so did the usability of the failure printouts. Your effectiveness as a maintenance specialist will depend greatly on your ability to interpret the failure printouts provided by the various programs in your particular computer system. It might be hard to believe, but work centers have often suffered excessive downtime because maintenance personnel misinterpreted a particular failure printout. Our Air Force has expended large sums of money to provide you with the best maintenance program publications available. Your on-the-job training will include many hours of studying these publications. This study will be rewarded by the respect you gain from your coworkers and supervisors every time you interpret a failure printout correctly and take the right corrective action. Normally, depending upon the system you are assigned to, maintenance program descriptions can be found in Chapter 4 of the TO or Section 4 of the appropriate manufacturer's service manual. As your training progresses and you become familiar with more of the maintenance programs in your system, one thing that should quickly become apparent to you is the standardization of these programs.

407. Cite certain significant programming aspects standardized within a computer system.

Examining, in order, the standardization of maintenance programs and the uniformity of maintenance program error printouts, below the first of these we will discuss the subareas of program organization and operator communication.

Standardization of Maintenance Programs. In each computer system, program standardization is essential in order to reduce the cost of the system and increase its usability. Within a given system, most programming aspects have been standardized—particularly program organization and operator communication.

Program organization. This kind of organization is the most important aspect of a successful programming system. Each program that is written must be organized in consideration of its functional relationship to the total system. Some maintenance programs are *executive control oriented;* that is, they are designed to be operated in conjunction with (or by) some type of control program. Other maintenance programs do not require external control and are designed to be *self-control oriented.* Other areas of program organization that you will see during your training are flow charts and tagging.

a. Flow charts. Recall that flow charts consist of a series of blocks, each containig a description of a computational function. As explained earilier, the particular flow chart symbols may change from system to system.

b. Tagging. Tagging makes a program easier to prepare and easier to understand by the original programmer, succeeding programmers, and those who use the program flow charts and descriptions. Many methods can be used in tagging instructions. In one method, a program listing is divided into blocks of logical functions. Each block has a header giving its name, function, and communication data. All data words, or constants, which are referenced in the block are grouped together and placed at the end of the block. Within the functional block itself, instructions and data can be tagged with a three-part tag to show block identification, type of reference, and a digit to distinguish several references of the same type. For example, the third part of a particular function tag, N4, might be any of the following:

- E - Entry.
- F - Exit or final.
- M - Instruction that is modified.
- C - Constant (unmodified).

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- T - Temporary constant.
- I - Input communication word.
- O - Output communication word.

The functional block N4 might have internal tags N4E, N4M1, N4M2, N4F, N4C1, N4C2, or N4T.

c. Control program. A maintenance control program is a package of control and helper routines that facilitates the loading and operation of the various maintenance program routines. The control program portion of a maintenance program provides special routines that fulfill common requirements of the program's test routines, thus preventing needless duplication of programming effort. For example, the same print, interrupt, or manual intervention routine is used by the various test routines in a maintenance program. A maintenance control program can be included as part of the on-line (active or operational) program as well as a backup (standby) program. In this environment, it is time shared with the on-line and backup program, and it provides confidence diagnostic checking of the system hardware. However, a maintenance control program can be strictly associated with an off-line environment (for example, scheduled maintenance period).

Operator communication. Depending on the particular system, operator communication can take on many forms. The more standardized types include interrupts, manual intervention, and printouts.

a. Interrupts. You are able to interrupt the processing of a maintenance program by initiating an external request from such devices as an external keyboard, a status maintenance console, a display console, or a test simulator. The method used by the control program to honor your requested interrupt is an interrupt processing routine. Once the control program recognizes the interrupt as a legal request, control is given to you, the requester. You can then enter additional data, initiate or change specific switch settings, or make ready and identify other hardware for testing.

b. Manual intervention. The manual intervention and interrupt are similar. In order to distinguish between the two, think of the manual intervention as being preprogrammed by the programmer. That is, at specified points in a given maintenance program, the program requests specific actions to be taken by the operator. These actions include setting specific switches, preparing card or tape inputs that will furnish needed information for the test, or making ready and identifying other hardware for testing.

c. Printouts. Standardization of maintenance programs is insured to some extent if a set of print routines (within the control program) is used by the various maintenance program test routines. The following items are considered essential to uniformity of program printouts, and the maintenance programs of the many systems normally adhere to them:

- Program heading.
- Results of program run.
- Error information—data failure, control failures, etc.
- Indicated repair statements.

Uniformity of Maintenance Program Error Printouts. Each computer system's maintenance program library insures uniformity of the format of its error printouts through the use of the four essentials indicated above. However, the experienced computer specialist and technician are the first to admit that their training on a new system would be much easier if all systems used the same data format on their printouts. Unfortunately, uniformity of the data format contained within each of the four essential items required on the error printout varies from system to system. The following example is provided to illustrate one format. Note the identification of the four essential elements that were presented in the previous paragraph. These elements are identified on the printout as follows: (1) program heading; (2) results of the program run; (3) error information; and (4) indicated repair statements.

```
    THE FOLLOWING PROGRAM WILL BE OPERATED
    UNDER CONTROL OF SMCP 3

    CDS 1L TAPES MC 1L 2606
    A COMPLETE DIAGNOSTIC AND MARGINAL CHECKING
    TEST OF THE TAPE DRIVES, TAPE ADAPTER UNIT AND
    ASSOCIATED CIRCUITRY.
(1) +-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-

    SS1-OFF SS2-OFF SS3-OFF SS4-OFF BSW 0.10100 1.00000

    NOW TESTING LOGICAL DRIVE 3 WHICH IS PHYSICAL
    DRIVE---.

(2) 4....E..2.... +150-040 FAILURE MC WORD 005 PRESCRIBED
    40 ROUTINE 2

(3) TAPE DRIVE NO. 3
    REWIND DIDNT GIVE DISCONNECT

    THESE PUS WERE MARGINED AND COULD CAUSE
    ERROR.
    13BJ
(4) THESE PUS WERE MARGINED BUT WOULD NORMALLY
    NOT CAUSE ERROR.
    13BS 13BL 13AP 13AJ 13AH 13BT 13BD 13BF 13BE

    THESE PUS NOT MARGINED BUT COULD CAUSE ERROR.
    13BH 13BG
```

Exercises (407):

1. What is an executive control oriented program?

2. What is a maintenance control program?

3. Operator communication with the computer can take what form?

4. What items are essential to uniformity of program printouts?

5. Why is it very difficult, in spite of the items named in exercise 4, for even an experienced computer specialist or technician when that person moves from system to system?

System Operation and Preventive Maintenance

THE ELECTRONIC COMPUTERS and switching systems being bought by the Air Force today are more complex, more reliable, and to some extent, easier to maintain than earlier systems. As these systems become more advanced, more state of the art, your role may become that of a system operator/maintainer. Your duties will include more monitoring of system operation along with your preventive maintenance inspections (PMIs). This is particularly true in the area of electronic switching. Once an electronic switching system has been placed into operation, it essentially operates itself, performing all required functions automatically. Your job then becomes that of an operator, monitoring for system failures, making programming changes from directives, or making required minor adjustments or alignments identified by equipment PMIs.

2-1. System Operations

The majority of the systems that you will maintain are automatic systems; that is, once they are installed, programmed, and operational, your task becomes limited to that of monitoring system operation. In this section, we will discuss some of the tasks you may be required to accomplish prior to and during system operations.

408. Provide general procedures required to place a system on-line or into operational status and indicate where you can find these procedures.

We cover in this unit initializing your system, system power ON/OFF procedures, and emergency operation of some systems—in that sequence.

Initialize System. The instructions you must follow to initialize your system are normally found in Chapter 2 of the appropriate service technical order. You might recall that this is also the chapter which provides the installation instructions for the system or particular equipment covered by the technical manual. The procedures followed to initialize a system are the preliminary procedures that are not normally repeated once they have been accomplished. These preliminary steps may only accomplish the arrangement of instructions and data in the computer memory. However, depending upon the system, much more may be involved. When you consider the initial installation and preparation of the equipment for normal operation, then many more tasks may also be included. Just a few examples are:

- Initial installation of equipment.
- Clearing of memory and registers of stray or erroneous data.
- Loading of program data.
- Initial cross-connects or terminal connections.
- Initial switch positioning or settings for equipment panels.

Once the system has been placed into operation, initializing will normally involve the preliminary steps of arranging instructions and data in the computer or switching system memories, thus restoring operation after a system failure.

System Power ON/OFF Procedures. The source of information regarding your system power ON/OFF procedures can be found in the appropriate system service manual or -2 technical order. Each computer or switching system has its own procedure; however, certain similarities can be found when the procedures of one system are compared to those of another.

First, some systems are portable, mobile, or transportable, and these systems require proper grounding before power is applied to the equipment. Of course, even the so-called fixed systems require grounding, which is taken care of by the station ground when the system is initially installed.

The second step is the checking of the input power. This can be as simple as plugging the equipment into an AC outlet or involve a more involved check of voltage, phase, and frequency of the power being applied. If the input power checks properly, the power is then applied. Often this involves the setting or turning on of the main circuit breaker and any number of lesser distribution switches or circuit breakers. It is very important that you follow the procedure for your specific equipment during this step. Some equipment can be seriously damaged if the proper sequence is not followed when applying power to equipment subassemblies.

The third step may be considered part of equipment operation, depending upon the system or equipment being turned on. This is the step where you clear all alarms caused by initial power being applied and initialize the system. At this point, you are ready to perform an operational check or already have full system operation.

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To power down or turn off your system is quite often the turn-on procedure in reverse. However, your system may have a slightly different procedure, so check your technical data.

Emergency Operation. Some systems provide for limited or emergency operation. This emergency operation may take many forms. Emergency operation in some systems refers to operation with backup or auxiliary power systems; i.e., batteries. Other systems have override or emergency procedures which disregard faults or system conditions that would normally place the system out of operation. Still others have emergency operating procedures for system restoration. These procedures may involve short or abbreviated programs, the termination of specific services, or power off of specific subsystems until the full system is restored to operation. Many systems have emergency shutdown or stop procedures. These procedures are designed to prevent serious damage to equipment during certain failures or conditions. An example of this might be the overheating of equipment within the system. If you are working on one of the newer systems, these emergency stops may be totally automatic.

Your knowledge of emergency operating, start, or stop procedures can be compared to the knowledge of first aid. You hope that you won't have to use it—but, when its use is required, your personal satisfaction will be great if you know the actions to take.

The specific procedures and emergency capabilities for your system are also found in the appropriate service manual or -2 technical order.

Exercises (408):

1. What is involved when you initialize an operating system?

2. Where can you find a step-by-step power-on procedure for your system?

3. What is the first action or precaution you should take before applying power to a system?

4. Where can you find emergency operating capabilities and procedures for a particular system?

2-2. System Monitoring

System monitoring is the listening and looking for any indication of a fault or equipment failure. This is usually accomplished by checking the fault and facility panels for the various equipment failures. These indications, whether audible or visual, can provide you with a definite starting point to correct a problem.

409. Specify the uses, types, and technical information associated with self-test indicators, and cite the effects of temperature and humidity on circuit components.

Taken up in this segment are indicator assemblies, power generating equipment, power storage equipment, and environmental control units. The first of these has three subareas involved.

Indicator Assemblies. An indicator may be installed anywhere that is convenient for visual observation. But in order for these indicators to convey any meaning to maintenance personnel, they must be labeled appropriately, and the labels or labeling must be kept in a readable condition at all times.

Since you are training on a computer or switching system, you should already be somewhat familiar with its fault indicator assemblies. Therefore, a study of selected fault indicator assemblies of different systems would be of little use to you here, especially when analysis proves they are all the same in principle. This text is used to present a study of these units in terms of their:

- Uses.
- Types.
- Associated technical order information.

Indicator assembly use. The two uses provided by indicator assemblies are the identification of a failing function or subfunction, and the identification of correct or incorrect data or data flow. Regardless of the extent of coverage that the indicator has on a panel, only one of these two uses is possible. For both uses to be present on a panel, at least two indicators must be used. Let's examine this thought more closely.

A fault indicator or data flow indicator lamp is frequently located on the panel or assembly containing the circuit it represents.

This arrangement is convenient for verification of that function or subfunction of the system. It does, however, have a distinct limitation; that is, each cabinet, rack, chassis, or drawer must be inspected in order to locate the inoperative function. This system is cumbersome, time-consuming, and inefficient. To overcome this limitation, additional indicators are installed at a centralized, convenient location within the system. Notice the words *additional indicators.* Primary indicators, those located at the function, are necessary in addition to those remoted to the more convenient location. Some of the most used locations for convenience are:

- Front doors of cabinets.
- Fault and facility panels.
- Fault indicator and confidence indicator consoles.

Thus far, we have established that each function or subfunction within a system will likely have an indication of operation or failure. Further, because of the volume of circuits and placement of units, a conveniently located fault indicator assembly is made. This assembly, called by various names, provides at a glance the status of all or most of the equipment within the system. We also identified the two general uses for this indicator assembly. Let's examine each use respectively.

The indicators are positioned in groups that are

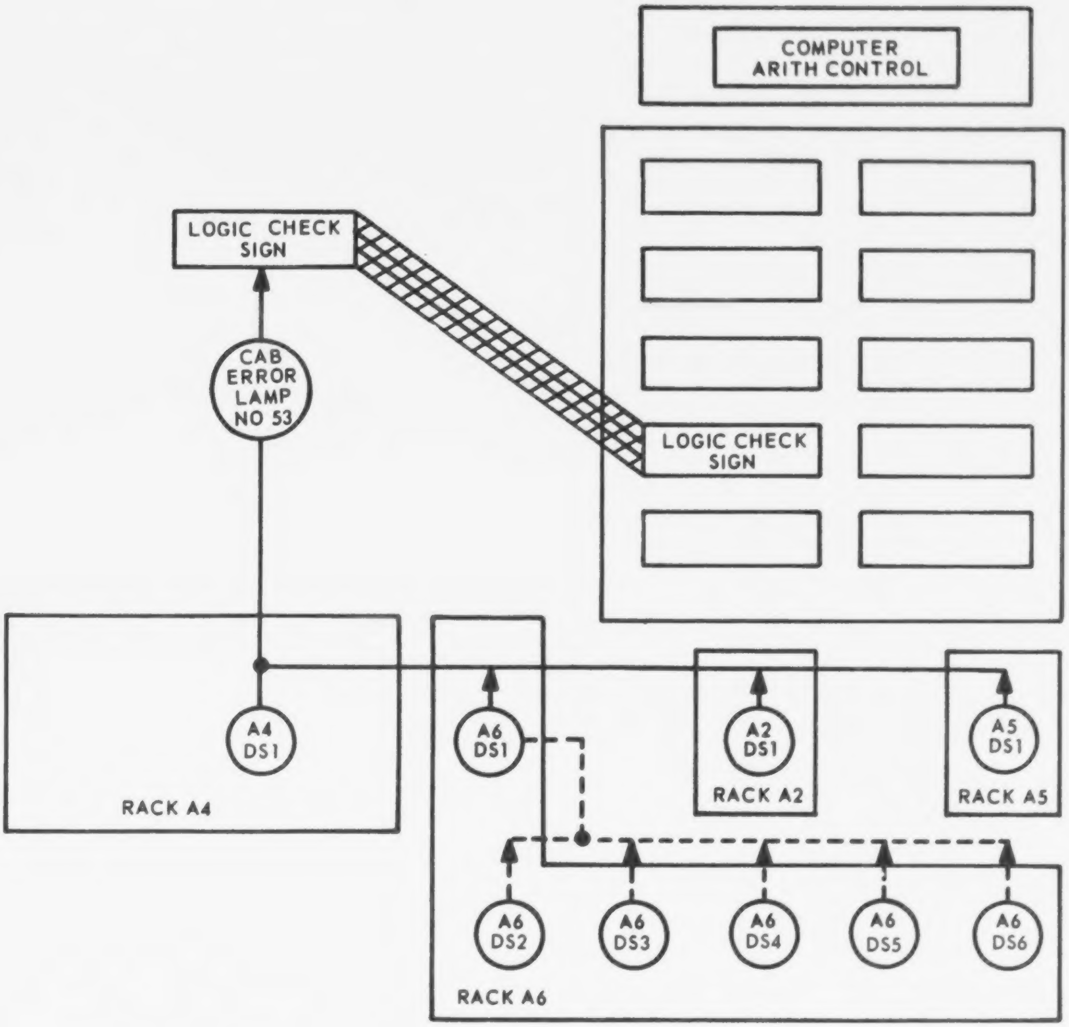

Figure 2-1. Typical fault facility panel.

associated with specific functions of the equipment. Figure 2-1 illustrates this arrangement. The block to the right represents a portion of the central fault panel. It has a functional title, *computer arith control,* and has 10 lamps, representing indications of subfunctions within the arithmetic control unit. For explanation and use in this study, only the *logic check sign* indicator is examined. Before identifying when the lamp would light, review the other elements of the figure. Only cabinet 53 is involved, but within the cabinet, racks A2, A4, A5, and A6 provide some control over the logic check sign fault indicator. The light will turn on when an incorrect *check sign* (parity) error occurs from a subfunction in rack:

- A2 when A2-DS1 lights.
- A5 when A5-DS1 lights.
- A4 when A4-DS1 lights.
- A6 when A6-DS1 lights.

Shown in the figure are five additional fault indicators for rack A6. They are DS2, 3, 4, 5, and 6. If one or more than one of these indicators turn on, the rack A6-DS1 lamp lights also. Lamps A2-DS1, A4-DS1, A5-DS1, and A6-DS1 are rack lights and receive their inputs from circuit indications. The breakout of racks A2, A4, and A5 is similar to that indicated for rack A6 in the figure. For this study, the detail in the figure is sufficient. If any rack light comes on, it provides the necessary input to the cabinet light, which, in turn, provides the input to the fault indicator—*logic check sign*—located in the *arith control* area of the fault facility panel. From this indication, we determine that a problem exists in the arithmetic control circuits and, as a troubleshooting aid, the fault indicator has directed attention to a local area. But, what about data flow?

Circuit lamps installed on panels are used in various methods to identify data flow. In figure 2-2, four lamps are used to display the status of a transmitter (XMT A or B) during transmission time. In this system only one lamp

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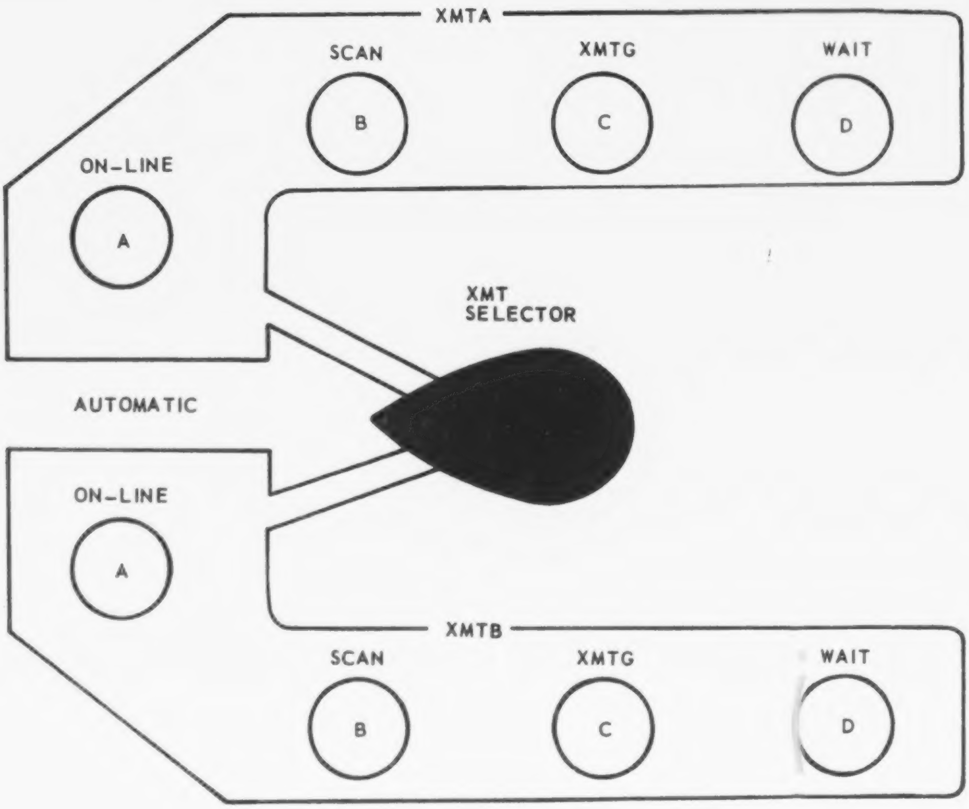


Figure 2-2. Transmit status panel.

is on at any given time. For example, when data is being transmitted by XMT A, a sequence occurs in which lamps B, C, and D are lit and go off. This sequence is repeated each time data is transmitted and, when the cycle is completed, lamp A returns to the on state.

Another example of data flow is that of lamps associated with a register or counter. In a register, grouping of its lamps provides a display that, when read, reveals the data stored. This is contrasted with counter operations where each lamp turns on and off at a predetermined rate, thus making count determination difficult. However, the experienced maintenance specialist can look at the lamps of a counter and determine whether it is stepping correctly by its stepping sequence and rate. All of these examples show the second use of indicators; i.e., data flow. To give you some idea of the more common equipment configurations of fault indicator panel assemblies, we will identify various types.

Types of indicator panels. Figure 2-3 illustrates many of the different arrangements of indicators used for the two purposes stated. You should also note that the indicator may be combined with a switch as a single unit. Thus, the activation of a busy switch may light a busy lamp in the face of the switch when it is depressed. This type of switch indicator is common on status panels.

For identification, correlate the indicator types listed below and their corresponding callout letter of the figure:

A—Counters and registers in operation.

B—Information registers displaying memory core data.

C—Confidence indicators detecting fault conditions.

D—Fault and facility panel showing fault status (upper portion) and data transfer (lower portion).

E—Status panel displaying status of the computer and associated equipment.

F—Confidence indicator console panel indicating status of the entire system.

Technical order information. Many portions of the technical orders describe or identify each of the indicators on the panel, board, drawer, assembly, or cabinet. The parts of technical orders and their series that provide data for interpretation and information on the use of indicators are listed below:

- Circuits and diagrams: -3 series.
- Operations chapter of the service manual: -2 series.
- Principles of operation chapter of the service manual: -2 series.
- Maintenance chapter of the service manual: -2 series.
- Fault location guides: part of the maintenance chapter.
- Control and indicator tables: within the operations chapter.

Figure 2-4 shows three examples of the various methods in which indicator lamps are shown in technical

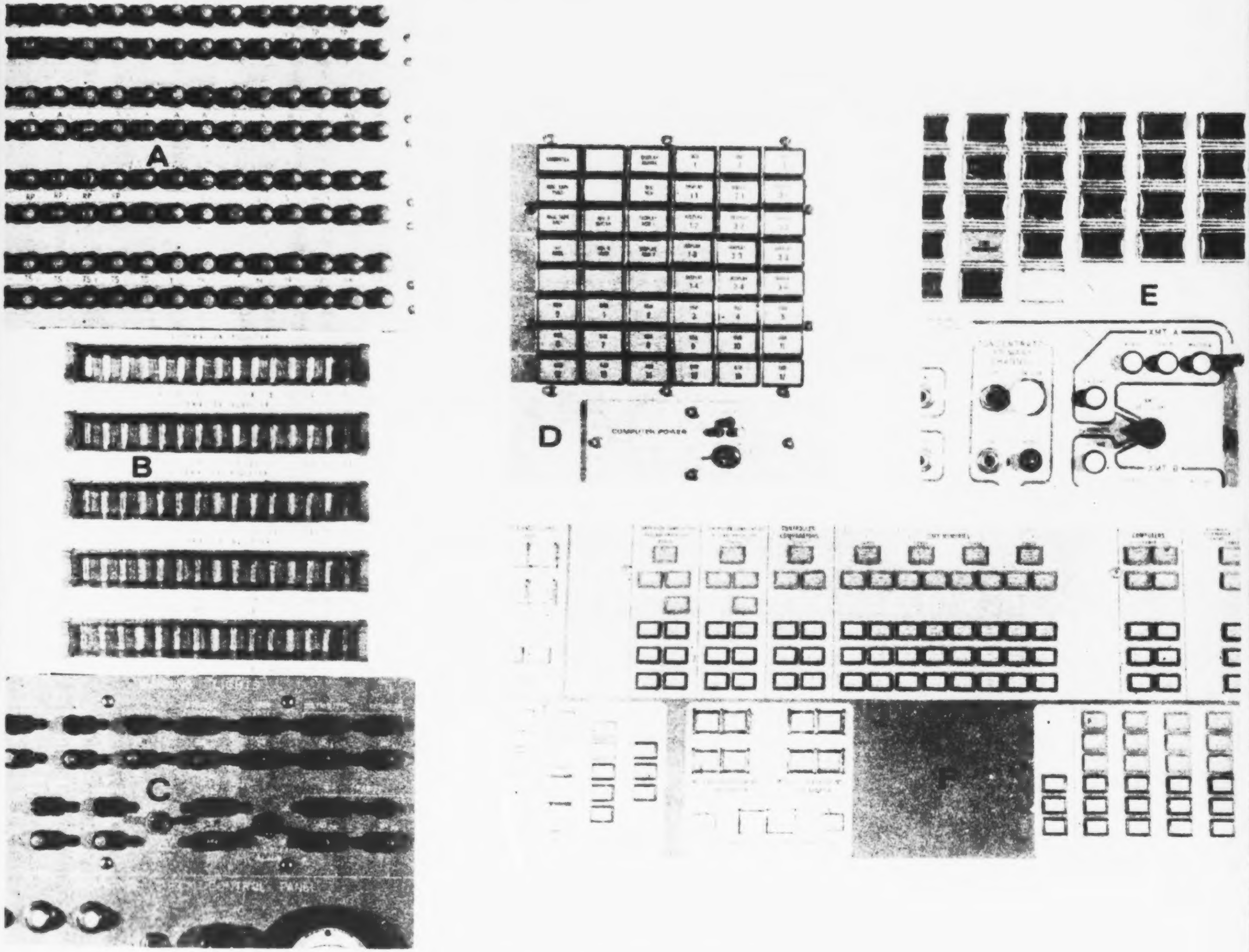
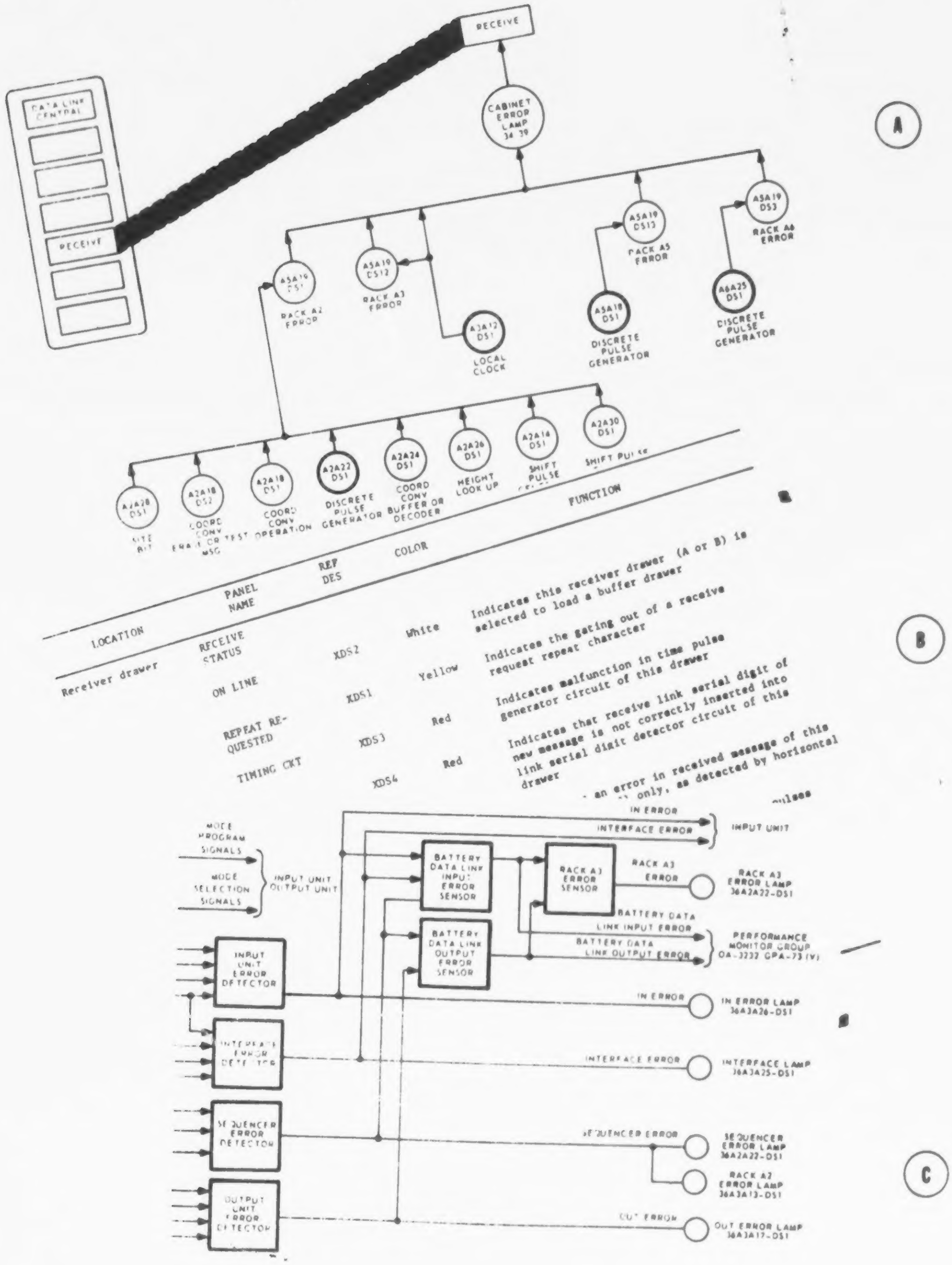

A
B
C
D
E
F
COMPUTER POWER
CONTROL PANEL
XMT A
XMT B

Figure 2-3. Types of indicator panels.


A
DATA LINK CENTRAL
RECEIVE
RECEIVE
CABINET ERROR LAMP 34 39
A5A19 DS1
RACK A2 ERROR
A5A19 DS12
RACK A3 ERROR
A3A12 DS1
LOCAL CLOCK
A5A19 DS13
RACK A5 ERROR
A5A18 DS1
DISCRETE PULSE GENERATOR
A5A19 DS3
RACK A6 ERROR
A6A25 DS1
DISCRETE PULSE GENERATOR
A2A28 DS1
SITE BIT
A2A18 DS2
COORD CONV ERROR OR TEST MSG
A2A18 DS1
COORD CONV OPERATION
A2A22 DS1
DISCRETE PULSE GENERATOR
A2A24 DS1
COORD CONV BUFFER OR DECODER
A2A26 DS1
HEIGHT LOOK UP
A2A14 DS1
SHIFT PULSE
A2A30 DS1
SHIFT PULSE
B
C
MODE PROGRAM SIGNALS
MODE SELECTION SIGNALS
INPUT UNIT OUTPUT UNIT
IN ERROR
INTERFACE ERROR
INPUT UNIT
BATTERY DATA LINK INPUT ERROR SENSOR
RACK A3 ERROR SENSOR
RACK A3 ERROR
RACK A3 ERROR LAMP 36A2A22-DS1
BATTERY DATA LINK OUTPUT ERROR SENSOR
BATTERY DATA LINK INPUT ERROR
BATTERY DATA LINK OUTPUT ERROR
PERFORMANCE MONITOR GROUP OA-3232 GPA-73 (V)
INPUT UNIT ERROR DETECTOR
IN ERROR
IN ERROR LAMP 36A3A26-DS1
INTERFACE ERROR DETECTOR
INTERFACE ERROR
INTERFACE LAMP 36A3A25-DS1
SEQUENCER ERROR DETECTOR
SEQUENCER ERROR
SEQUENCER ERROR LAMP 36A2A22-DS1
RACK A2 ERROR LAMP 36A3A13-DS1
OUTPUT UNIT ERROR DETECTOR
OUT ERROR
OUT ERROR LAMP 36A3A17-DS1

LOCATION	PANEL NAME	REF DES	COLOR	FUNCTION
Receiver drawer	RECEIVE STATUS			
	ON LINE	XDS2	White	Indicates this receiver drawer (A or B) is selected to load a buffer drawer
	REPEAT REQUESTED	XDS1	Yellow	Indicates the gating out of a receive request repeat character
	TIMING CKT	XDS3	Red	Indicates malfunction in time pulse generator circuit of this drawer
		XDS4	Red	Indicates that receive link serial digit of new message is not correctly inserted into link serial digit detector circuit of this drawer
				- an error in received message of this only, as detected by horizontal pulses

Figure 2-4. Technical order fault indicator information.

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orders. These three examples are not the only methods used, but they represent the extremes. Figure 2-4,A, shows all of the indicator lights, their locations, their purposes, and their connections. When any one of these lights turns on, the RECEIVE light also turns on. Figure 2-4,B, shows a portion of a table that identifies each lamp on a status panel by number, title, and color. Under the Function heading of the table, a brief description of the lamp's purpose is given. Finally, in C of the figure, the indicators show a rack (36A2, rack A3) error light as well as the functional error lights. Notice that any functional error causes an output from a higher order sensing unit (input or output) to the highest order sensing unit within the cabinet. For example, the figure indicates an input unit error that causes an output from the higher order battery data link sensor, which, in turn, provides an input to the rack A3 sensor.

Obviously, your job of troubleshooting is simplified when system TOs contain fault detection information such as outlined in figure 2-4. That is, this is so if you know how to use the information to work back through the error indicators to the end item—the failing unit. Once there, you can use standard troubleshooting procedures to replace or repair the faulty component.

Power-Generating Equipment. When monitoring your system operation, you must not forget the support equipment. Normally, commercial power will be used as the primary source of power for the system you maintain. However, when adequate commercial power is not available, Air Force facility generated power or transportable generators are used as the primary source. The maintenance and operation of this power-generating equipment is not usually your responsibility. However, you may be responsible for the monitoring of equipment operation to insure the proper inputs to your computer or switching system. In this case, alarm lamps and metering circuits are provided to indicate the output voltage of each phase of the generating equipment. The metering circuits are usually capable of measuring the output voltage and the current simultaneously for any particular phase that is selected.

Power Storage Equipment. In addition to monitoring power-generating equipment, your system may require that you monitor power storage equipment. The power storage equipment refers to batteries and battery chargers. Battery chargers and charging systems are often equipped with metering and alarm circuits. These circuits indicate the charged potential and charging or discharge rates of the batteries. There are a wide variety of batteries and chargers in use with Air Force equipment. For specific information concerning the monitoring of your equipment's power systems refer to the appropriate technical orders or manuals.

Environmental Control Units. The reliability of your equipment will often depend upon the environment in which it must operate. Therefore, the need for monitoring environmental conditions and the operation of any environmental control units (heaters, air conditioners, etc.) is quite evident. There are two main reasons for environmental control units. They are:

(1) To improve component reliability and life.
(2) To stabilize circuit performance.

The effects of temperature on circuit components is usually one of the following:

- A sudden, total failure.
- A shortened life.
- A temporary change in value.
- A permanent physical or chemical change leading to total failure prematurely.

The effects of humidity (the moisture content of air) are similar to the effects of temperature. Because water is a good conductor, it can act as a low resistance path in electronic equipment. This moisture can cause insulators to break down or circuits to short. The end product of high humidity is the growth of fungus and corrosion, which we will discuss in Chapter 4.

Now let's look at temperature again. How can temperature be monitored easily? With a thermometer. Similarly, as regards humidity, one of the most convenient devices for measuring it is the wet-bulb thermometer. It will provide you with a reliable measurement if you use it properly. In its simplest form, a wet-bulb thermometer is an ordinary thermometer whose sensing bulb is covered by a moistened cloth wick. You ventilate this kind of thermometer by whirling it in a calm atmosphere or by exposing it to forced-air circulation. Now for measuring both temperature and humidity, a dry bulb and a wet bulb are included in the same instrument. This device is called a psychrometer. Many more complicated techniques are used for the direct reading of air moisture content. If you are required to monitor humidity, you will receive training locally in the proper procedures.

Exercises (409):

1. List the two uses of indicator assemblies.

2. In order for a remote facility panel to properly display the status of circuits indicated by the lamps, what conditions must be present in the circuits?

3. How does a register help maintenance specialists check data flow?

4. What do the common elements of indicator panels provide as aids for troubleshooting?

5. List the different technical orders that identify fault and status indicators.

6. How is power-generating equipment monitored?

7. What is power storage equipment?

8. Name at least three effects of temperature on circuit components.

9. What effect will humidity have on electronic equipment such as insulators and circuits?

10. What is a psychrometer?

2-3. Cabling and Cross Connects

Switching systems and many computers must receive inputs from a wide variety of equipment and locations. Once the switching or processing of the data is completed, outputs to the same or different locations and equipment must also be provided. The connections between equipment, inputs, and outputs are accomplished with cabling and cross-connectors at distributing frames.

410. Identify the function of the main distribution frame and specify types of distribution frames and their components.

First, distributing frames, and second, distributing frame components will occupy us here. Five subareas are discussed under distributing frames; four, under components of these frames.

Distributing Frames. The distributing frame is part of the wire facilities of a communications station. In practice, there may be more than one distributing frame installed at a single communications center. This depends upon the types and complexity of circuits associated with the facility. Even the smallest station requires a certain amount of wiring to connect the various equipment or circuit components together.

The various types of distributing frames are distinguishable on the basis of how each is actually used. The names used to describe the various frames are main distributing frame, combined distributing frame, intermediate distributing frame, black distributing frame, and red distributing frame. The basic term "distributing frame," is defined for reference purposes as a structure for terminating permanent wires of a communications system (e.g., technical control facilities and telephone central offices). It also permits easy change of connections between them by means of temporary cross-connecting wires.

Now, let's discuss each frame individually, beginning with the main distributing frame.

Main distributing frame (MDF). Figure 2-5 illustrates a section of a floor-type distribution frame. From outward appearances, all distributing frames look the same and vary only in size and usage. The main distributing frame is so named because it is normally much larger than other frames and is the terminal point for all outside lines coming into a station.

Outside lines are terminated on the vertical blocks of the frame through protective devices. Horizontal blocks carry all in-station equipment circuits which must be connected to outside lines. Connections between the two sides are made by cross-connections, which we will discuss later in this BOF segment.

Intermediate distributing frame (IDF). This type of frame has been borrowed for military use from the commercial telephone industry. It is officially defined as a distributing frame on which the subscriber line multiple appears on one side and the subscriber line circuit on the other for interconnection. You will generally encounter

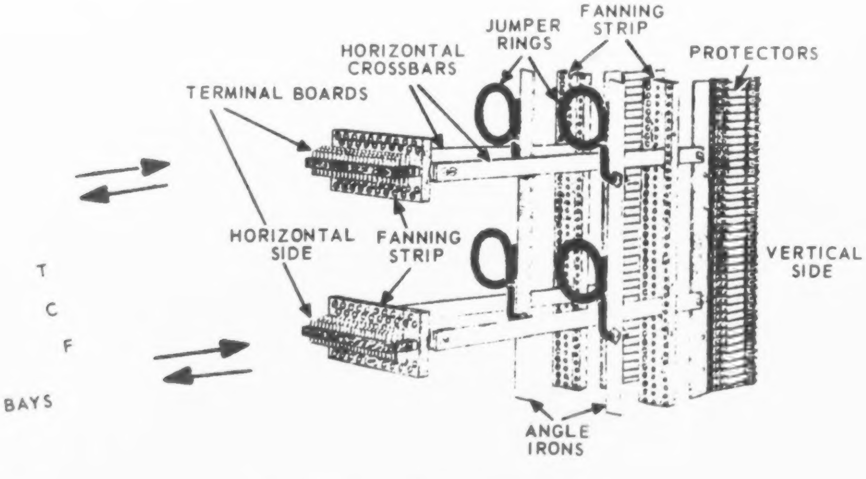


Figure 2-5. Floor-type distribution frame.

this type of frame at a communications center where telephone switchboard facilities are provided. A subscriber line multiple is a circuit accessible at a number of switchboard positions so that more than one operator may have access to the same line. The term "intermediate distributing frame" has also been used to describe a frame facility positioned at an intermediate point between a main distributing frame and the technical control patching facilities. In this case, it doubles as the black distributing frame associated with the red/black concept.

Combined distributing frame (CDF). This type of frame combines the functions of a main distributing frame and an intermediate distributing frame. Part of this frame is used to connect all outside lines entering the station. Another part is used to connect cables that terminate in various electronic devices and other equipment located within the station. This arrangement permits the association of any outside line with any desired terminal equipment.

Red distributing frame. The red distributing frame is used to make connections between red circuits, patching facilities, and equipment. Wiring which terminates equipment, such as transmitter distributors and reperforators, is connected to one side of the red distributing frame. Wire connections for the unencrypted side of cryptographic devices, battery isolation relays, red circuit control, switching, and monitoring devices are made on this same portion. The other side of the red distributing frame is used to connect red patching facilities and the positive and negative rectifiers that furnish battery.

Black distributing frame. The black distributing frame is used to make connections between black circuits, patching facilities, line and channels, and equipment. The black frame has the same configuration as the red frame. At many stations the red frame is much smaller, and it is sometimes included in a cabinet. One side of the black distributing frame is used to connect analog and digital patching facilities and the positive and negative battery supplies. The other side is used to connect the following items: all landlines, both analog and DC; VF channels derived from radio media; encrypted side of cryptographic devices; battery isolation relays; and any black circuit control, switching, or monitoring devices used in the technical control facility.

Distributing Frame Components. In addition to the metal frame structure itself, a distributing frame consists of a number of detachable component parts, such as terminal boards and wire guides.

Terminal boards. Terminal boards are insulated bases, or slabs, provided specifically to mount a group of wiring terminals. Wood, ceramic, and plastic are among the materials that are used in their construction. The two parts of a terminal board are the wiring terminal support and a mounting board, which also serves as a wire guide. The terminal boards are secured to the metal frame structure by screws so that they may be added or removed as required.

All of the terminal boards on one side of a distributing frame are positioned vertically. This side is called the vertical side, and the terminal boards located there are called vertical terminal boards. The other side of a distribution frame has terminal boards positioned horizontally. They are called the horizontal terminal boards. On the terminal boards there are insulated terminals to which two or more wires may be connected. The terminals, called tie points, are usually of different length, with the longer ones positioned toward the rear to make wiring and soldering easier.

Wire guides. There are two types of wire guides: jumper rings and fanning strips. Jumper rings are heavy metal loops positioned between the vertical and horizontal sides to guide cross-connecting wires. Fanning strips are wooden guides through which a number of small holes have been drilled; they are positioned close to the terminal boards or protectors to guide wires to these devices. A fanning strip associated with the cable protectors is usually one continuous guide reaching the entire height of the vertical side of the frame. The other fanning strips are of the same length as the terminal board and are considered part of it, as we mentioned earlier.

Permanent wiring. Permanent wiring is found on the left side of the vertical terminal boards and the bottom of the horizontal boards. As the name implies, permanent wiring is fixed permanently to the frame. This wiring connects such equipment as outside cables, multiplexing equipment, teletype equipment, COMSEC equipment, battery taps, and patch panels, which do not change, to the frame. Patch panels, battery, and ground taps are wired to the bottom side of the horizontal boards. All other equipment is wired to the left side of the vertical boards. Heat coils serve as the vertical terminal boards for landline connections. These heat coils are protective devices which, when heated above a predetermined temperature, allow a mechanical device to move, opening the circuit.

Temporary wiring. Cross-connections, also called jumpers, are wired from the right side of the vertical boards (i.e., equipment subject to reconfiguration or change) to the top of the horizontal boards (i.e., the outside cables). These jumpers are loose connections (an individual wire or a twisted pair), so they can be changed easily to suit the needs of the station. Cross-connections make it possible to change the routing of a circuit without having to open a cable.

Exercises (410):

1. Explain briefly the function performed by the main distribution frame.

2. What is an IDF?

3. What other wire connections than wiring which terminates equipment are connected to one side of the red distributing frame?

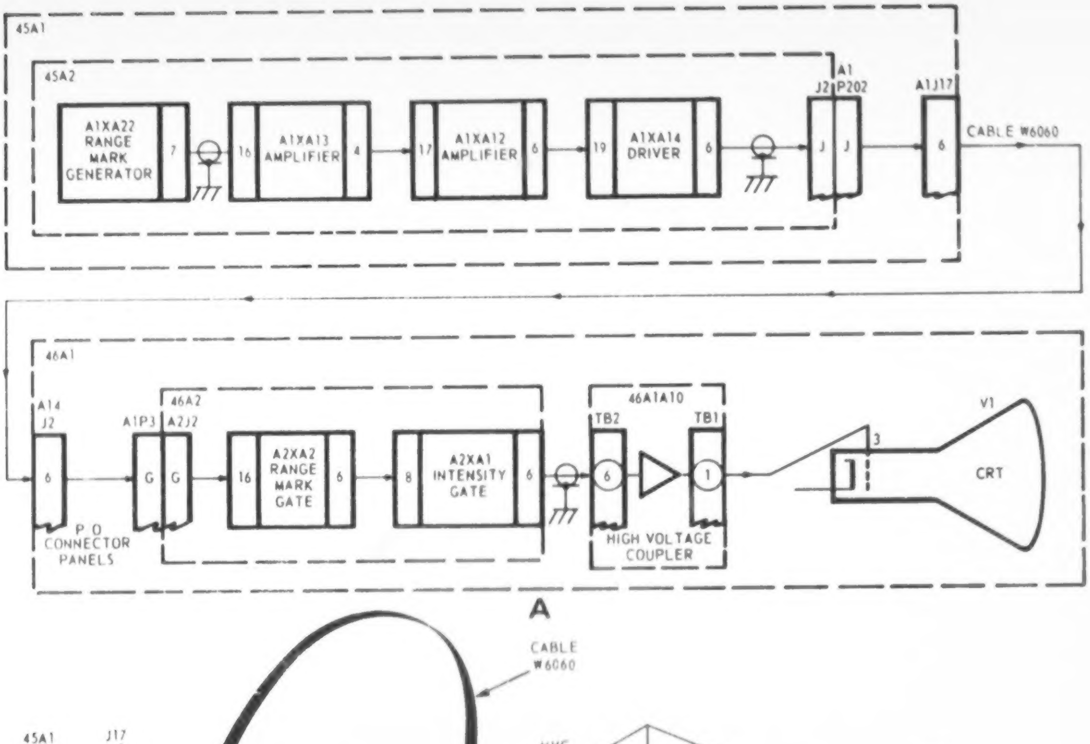

45A1
45A2
A1XA22 RANGE MARK GENERATOR
7
16
A1XA13 AMPLIFIER
4
17
A1XA12 AMPLIFIER
6
19
A1XA14 DRIVER
6
A1
J2
P202
J
J
A1J17
6
CABLE W6060
46A1
A14
J2
6
A1P3
A2J2
G
G
46A2
16
A2XA2 RANGE MARK GATE
6
8
A2XA1 INTENSITY GATE
6
46A1A10
TB2
6
TB1
1
HIGH VOLTAGE COUPLER
V1
3
CRT
P.O. CONNECTOR PANELS
A
CABLE W6060
45A1
J17
XA22
XA14
XA13
XA12
A2J2
45A2
HVC
46A1
XA2-6
XA1-6
J2
46A2
A14
J2
B

Figure 2-6. Range mark routing.

4. On horizontal terminal boards, (a) what are the terminals called, (b) where are the lower ones positioned, and (c) why are they positioned like this?

5. What is the permanent frame wiring?

6. What is the temporary frame wiring?

411. Identify the interconnecting connectors of a data signal from its origin to its point of use.

Interpreting Wiring Diagrams. Interpreting wiring diagrams is an extremely important task of any qualified maintenance specialist. This is especially so when you realize that your equipment is often made by different contractors and is linked together through cables. Each unit, operational amplifier (OA) group, assembly, or subassembly has some form of interconnecting wiring. Each unit contains interconnecting cables within the unit. It, therefore, follows that a complete understanding of the data flow between units and within units and a comprehensive knowledge of the techniques employed by contractors to interconnect components is essential for you. To meet this objective you will follow one signal that is routed through components, jacks, cabinets, and cables so that you can visually trace the signal as it proceeds from point to point. You must identify each connecting point and, by forming the alphanumeric code, relate the number to a real place in the equipment. By proper full alphanumeric formulation and sequential listing of the numbers, you will know easily when you have exited a chassis, rack, bay, or cabinet.

Refer to figure 2-6,B, and locate module location XA22 in cabinet 45. This is the origin of the range marks. Follow the connecting lines through XA13, 12, and 14; out of the rack jack J2; out of the cabinet jack J17; through cable W6060; into connector panel A14, jack J2 of cabinet 46; through rack jack J2; into module XA2; then to module XA1; to the high-voltage coupler (HVC); out of the coupler into the rear of the CRT and to the displayed range marks on the CRT face. When you have to identify this routing data, compile it as shown in figure 2-6,A; then it is complete. However, when you try physically to locate these points and the signal is routed, as you can see, from chassis to racks to cabinets to other cabinets, your wiring list takes on a physical dimension, and you must translate these physical characteristics into knowledge and understanding of the nomenclature of the connectors as well as their physical placement.

Exercises (411):
For both exercises 1 and 2, refer to figure 2-6, using A for 1 and B for 2.

1. In the spaces provided, list, by using full alphanumeric code and the vertical listing method, the assemblies, jacks, plugs, and cables in their proper order from the range-mark generator to the CRT.
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)
(14)
(15)

2. In the spaces provided, list the jack/plug and terminal board connectors for chassis and cabinets, using the full alphanumeric code.

Chassis	*Cabinet*
(1)	(1)
(2)	(2)
(3)	
(4)	

412. Identify and list the connecting points of a multiused signal, using figures 2-7 and 2-8 as required.

Multiused Signal. In this objective you will begin with data generated from module 611, which is to be used in various portions of the fine grain data (FGD) equipment. It is also routed to two remote units, the selective identification feature (SIF) unit and the SM-137 Simulator. Again, you must study this circuitry with the approach that data transferred to other areas and units must be routed by cables through connectors, and all of the connecting points must be identified.

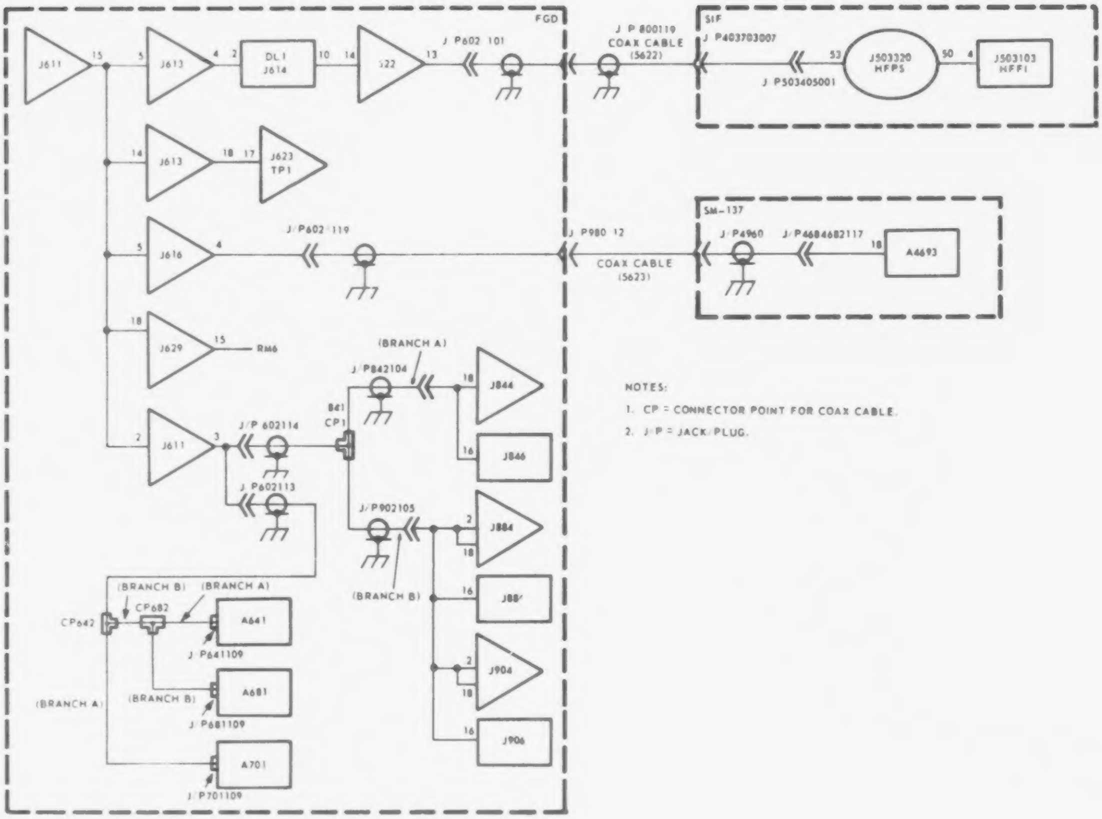
Refer briefly to figure 2-7 first. Observe in this figure that the original generator 611 is distributing its output to five main paths. Three paths complete their action in the FGD cabinet, while of the other two, one goes to the SIF and one to the SM-137.

Now follow along and compare the schematic wiring diagram of figure 2-7 to the pictorial view provided in figure 2-8 to see how the signal routing is accomplished. Begin by finding card location 611, *the darkened rectangle in the FGD cabinet, bay 600,* subassembly 601-640; then do these six things:

(1) Follow the solid line from 611 to 629. The termination of this leg generates a new data signal (RM6).

(2) Follow also the line from 611 to a pin on 613, and see by the line between 613 and 623 that the signal is fed through 613 to 623, where it generates another signal (TP1).

(3) Follow again the line from 611 to 613 (but to another pin) to 614, through 622, through jacks and plugs, to bay 800, through more jacks and plugs, out of the FGD cabinet, into the SIF cabinet and more jacks and plugs in the top of bay 400, to drawer 503, and jacks and


FGD
J611
15
5
J613
4
2
DL1
J614
10
14
J622
13
J P602 101
J P 800119
COAX CABLE
(5622)
SIF
J P403703007
53
J503320
HFPS
50
4
J503103
HFFI
J P503405001
14
J613
18
17
J623
TP1
SM-137
5
J616
4
J/P602 119
J P980 12
COAX CABLE
(5623)
J/P4960
J/P4684682117
18
A4693
18
J629
15
RM6
(BRANCH A)
J/P842104
18
J844
841
CP1
2
J611
3
J/P 602114
16
J846
J P602113
J/P902105
2
J884
18
(BRANCH B)
16
J886
2
J904
18
16
J906
(BRANCH B)
(BRANCH A)
CP642
CP682
A641
J P641109
(BRANCH A)
(BRANCH B)
A681
J P681109
A701
J/P701109

NOTES:

1. CP = CONNECTOR POINT FOR COAX CABLE.
2. J/P = JACK/PLUG.

Figure 2-7. Signal RM3 routing.

cards in rows 3 and 1 of drawer 503. This signal terminates in card 503103 of the SIF unit.

(4) Now follow another output from 611 to 616, then through the jack and plug 602119, out of bay 600, into the lower portion of bay 800/900, to location J/P980112. This signal exits bay 800 here and is routed by coax lead to lower rack jack 4960 of bay 4800. From there it goes to jack plug 4682117 and then into card 4693018. The signal is terminated at A4693.

(5) Start at 611 again and trace the line leading from it to J/P602113 and 114. Note that two circuits on module 611 are used before the connection at 602113 is made. J/P602113 coax lead is fed to the three units A641, A681, and A701. The CP connections are coax T connectors.

(6) Notice that the lead from J/P602114 goes to bay 800 and 900. In bay 800 it is tied at CP841, and one line is fed to J/P842104, which feeds two modules, 844 and 846; while the other branch of the tie is fed to J/P902105 and feeds four modules, 884, 886, 904, and 906.

You have just followed a multipath signal. A signal which started in a card in a bay has been distributed to chassis, other bays, and other cabinets each time a connector, jack, or connecting point was used. This is the second application of interpretation of wiring diagrams, and some very definite characteristics become evident here. They are:

a. Originating signals are generally fed to a connecting point, such as a jack.

b. Multiply routing of a signal is accomplished with jacks and connectors.

c. Each point of a junction is identifiable by a location number.

d. The data for making a complete signal wire list may have to be extracted from various technical orders (such as the TO on the FGD, SIF, and SM-137 equipments in this example) and, within the TOs, from selected chapters or sections providing connecting point listings (jack listings).

Exercises (412):

Consult figures 2-7 and 2-8 as necessary for exercises 1 through 6. Use the wiring list of signals and list in order, in the blanks provided, the connecting points of each separate path. Do this by identifying the jacks, plugs, cables, and assemblies in each path. Identification of inputs and output pins on jacks is indicated at the rear of the jack number in this way:

in out
J611014/018

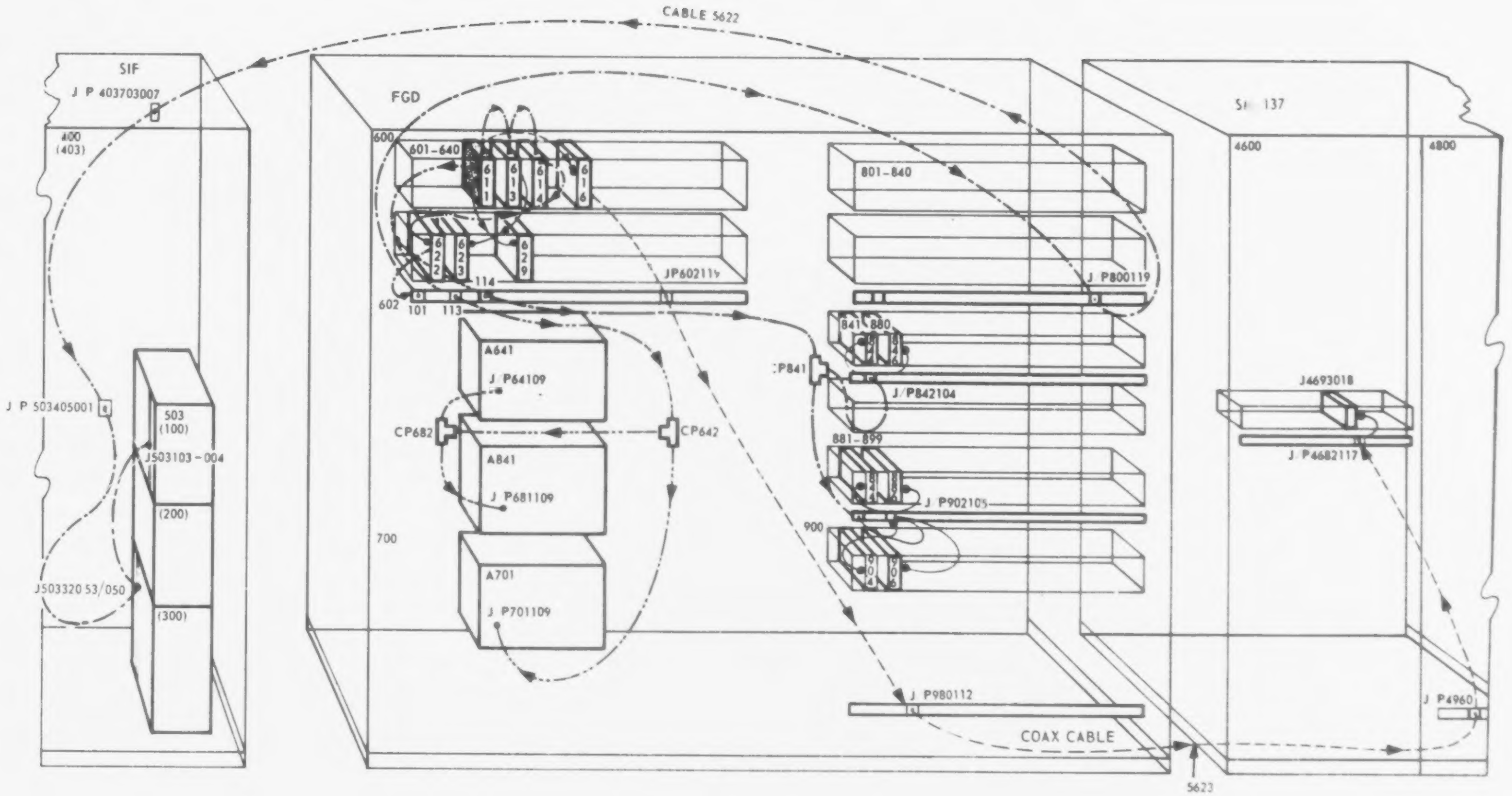

CABLE 5622
SIF
J P 403703007
400
(403)
J P 503405001
503
(100)
J503103 – 004
(200)
J503320 53/050
(300)
FGD
600
601–640
611
613
614
616
622
623
629
JP602114
114
602
101
113
A641
J P64109
CP682
CP642
A841
J P681109
700
A701
J P701109
801–840
J P800119
841 880
CP841
J/P842104
881–899
J P902105
900
904
906
J P980112
COAX CABLE
5623
S 137
4600
4800
J4693018
J P4682117
J P4960

Figure 2-8. Signal RMS routing pictorial.

1. Origin (RM3 to RM6) ______ ______.
   Terminating Jack
2. Origin (RM3 to TP1) ______ ______ ______.
   Terminating Jack
3. Origin (RM3 to SIF) __ __ __ __ __
   Bay Jack/ Plug   Bay Jack/ Plug

   ____ ______ ______ ______ __________.
   Cable   Cabinet Jack   Drawer Jack   Terminating Jack
4. Origin (RM3 to SM-137) __ __ __ __ __ __
   Bay Jack   Bay Jack   Cable   Rack Jack

   ______ __________.
   Rack Jack   Terminating Jack
5. Origin (RM3 to Assemblies in Bay 600)

   ______ ______ ______ ______
   Bay Jack   Connector Pt

   Branch A ______ __________.
   Jack/Plug   Terminating Assembly

   Branch B __________ ______ __________.
   Connecting Pt A to Jack/ Plug   Terminating Assembly

   ______ __________.
   B to Jack/ Plug   Terminating Assembly
6. Origin (RM3 to Bay 800-900)

   ______ ______ ______ ______ ______
   Bay Jack/Plug   Connector Pt   Branch A Jack/ Plug

   ____
   Branch B Jack/ Plug

   Branch A ______. Branch B ______. ______.

   ______.   ______. ______.
   Terminating Jacks   Terminating Jacks

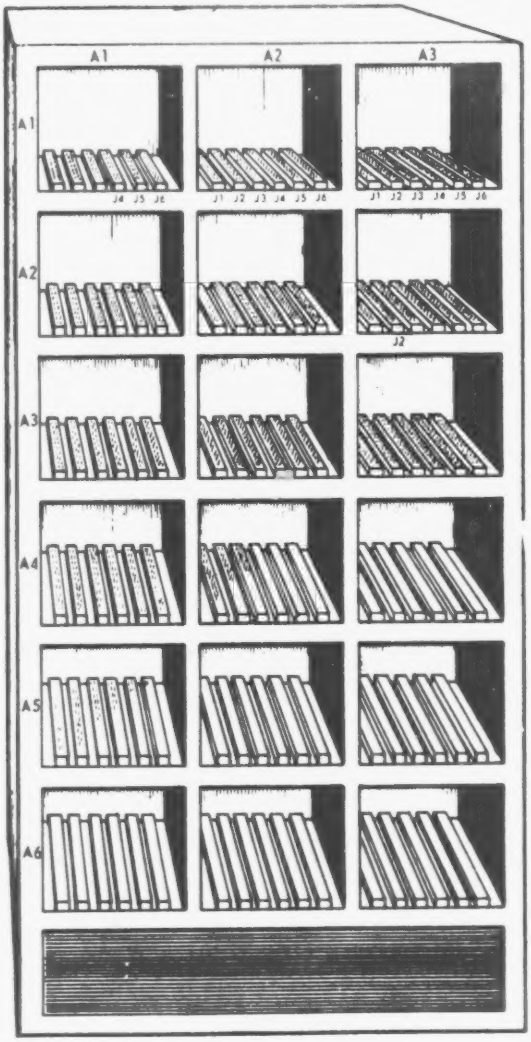


Figure 2-9. Main distribution frame.

413. Consulting the wiring table (fig. 2-10) and routing (fig. 2-11), locate and identify specific interconnecting cables between the main distribution frame and various units, as shown on figure 2-13.

Locating Cables. Before you try to fulfill this objective, you must recall what a main distribution frame is and its relative position in a system wiring scheme. Having studied distribution frames earlier in this chapter, if you refer to figure 2-9, you will recognize there a pictorial representation of one type of frame. The discussion in this BOF segment is based upon the use of a main frame, but the principles of usage involved would be the same if, instead of a frame, a filter box or junction box were used. It is only because the frame is the most complex of the three that we have selected it for study here.

Returning to figure 2-9, observe how this unit is made up of rows, columns, and tiers or planes. Accordingly, each location is identifiable by a coordinate number—one consisting of a row, a column, and a plane number. This number is usually given a "J" prefix. Each pin connection on each jack further identifies the exact point of connection. Generally, all connections from a unit are located within specific groups of rows and columns. Signals are usually transferred to another unit by the use of single-strand wire from point to point within the frame. In order to facilitate the installation and tracing of signal paths, tables are formed, with the main frame being the focal point of the table.

Refer now to the table layout illustrated in figure 2-10. Any table like this will very likely contain these columns and this data:

Input

(1) A connector point.
(2) A pin number in the connector.
(3) The color of the wire.
(4) The size of the wire.
(5) A cable number.

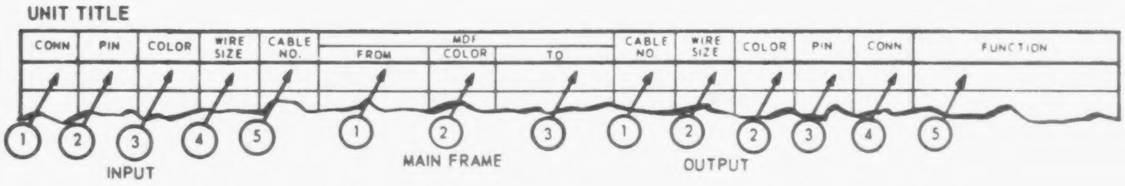


Figure 2-10. Table layout.

Main Frame Connectors

(1) The point of connection of the input cable.
(2) The color code of the wire.
(3) The point of connection to the output cable.

Output

(1) The output cable.
(2) The size and color of the wire.
(3) The pin number.
(4) The connector number.
(5) The functional requirement of the signal.

Having all of this information, we can begin to analyze a situation/problem. To do this, we will use figure 2-11. Our task, once again, is to use figure 2-11's table to identify and locate the interconnecting cables between the main frame and the units.

Follow along as we use views A and B, fig. 2-10, and the routing data below in figure 2-11. Let's suppose that you are required to determine where data bit "DO" was routed to understand a modification change. Look at the table fig. 2-11, observing particularly the expanded area labeled "A". The DO data signal is transferred from J6, pin r, of the console through cable W59 to the main frame, where wire r is connected to A2-A3-J1-15—vertical row A2, horizontal row A3, first terminal row J1, and contact 15. From that point the route is by a color #9 wire to A2-A2-J8-12. Pin 12 has one lead from W11 with a color #209 wire connected, and the other end of cable W11 wire color #209 is connected to J1, pin N, on the line store (memory unit) functional assembly. Actually, it is quite easy to perform this task once you have analyzed the path.

In the analysis just made, we examined how the main frame is used as a connecting point between units. From this it should be easy to understand how useful this unit is, because of its great flexibility. The task of tracing connectors and connector connections is simplified when the pictorial view is associated with the tables and cable layout drawings. If, instead, a filter box layout or distribution box layout were used in the analysis just completed, the following data would have been needed:

- Cable numbers for incoming and outgoing signals.
- Jack and plug numbers.
- Pin numbers on jacks.
- Filter or terminal board connector points.

Thus far we have been tracing wiring diagrams, using cables, jacks, and plugs. Figure 2-12 illustrates a few examples of how you may see jacks and plugs laid out in logic wiring diagrams.

We have described here some of the typical wiring situations found in data processors, where the task of interpreting wiring diagrams is employed. In each situation we have identified the components necessary for a list to be compiled, so that a complete picture of the signal path involved can be obtained. As we proceeded, we identified and explained some terms you should know. Note that, when using wiring diagrams and tables in forming a list or tracing a signal to find its connecting points, you may sometimes double back upon yourself. This means that, while going from jack to jack, etc., and flipping pages of logic, you can reverse your direction and return to the starting point. To keep this from happening, you must record in your list a complete understanding of jack/plug nomenclature and a complete nomenclature of all connectors involved. Having this data, you should be able to spot any reversal trend. We have identified and used both the vertical listing technique and the horizontal listing technique in the three situations presented. You should develop your own adaptations of these techniques after a study of your equipment configuration so that you completely understand the signal routing.

Let's list once more the points that we have identified which should aid you in interpreting wiring diagrams:

a. Cables are numbered with "W" on both incoming and outgoing lines.

b. Jacks and plugs each have numbers prefixed with J, X, or P.

c. Jacks are indicated at the *point* of the double arrow or the rectangle on schematics.

d. Plugs are indicated on the *back side* of the double arrow and on the *rounded corner* rectangle on schematics.

e. Each pin has a letter or number, or both, on jacks and plugs. All letters are used, except i, o, and q.

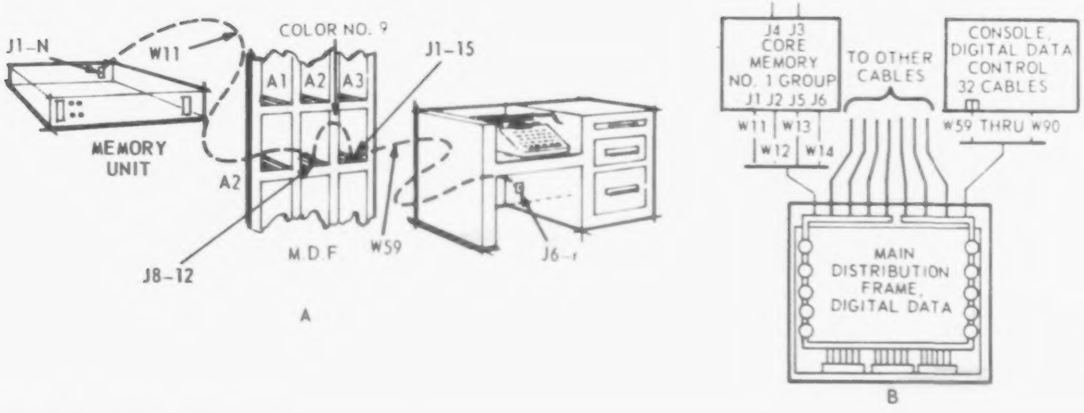
f. Uppercase and lowercase letters are used.

g. Terminal boards normally use numbers in preference to letters for connecting points.

h. Main frames, filter boxes, and junction boxes provide the same basic functions, except that the filter box also provides isolation by filtering.

i. You will need logic and wiring diagrams and wiring tables, cable listings, and rack jack listings to perform this analysis.

Exercises (413):
For exercises 1 and 2, using the vertical listing method, list in correct order, the connector points, cables, jacks, etc., of each signal path shown in figure 2-13. Start at the


J1-N
W11
COLOR NO. 9
J1-15
A1
A2
A3
MEMORY UNIT
A2
J8-12
M.D.F
W59
J6-r
A
J4 J3 CORE MEMORY NO. 1 GROUP J1 J2 J5 J6
TO OTHER CABLES
CONSOLE, DIGITAL DATA CONTROL 32 CABLES
W11
W13
W12
W14
W59 THRU W90
MAIN DISTRIBUTION FRAME, DIGITAL DATA
B

CONSOLE, DIGITAL DATA CONTROL

CONN	PIN	COLOR	AWG	CABLE NO.	MDF FROM	MDF COLOR	MDF TO	CABLE NO.	AWG	COLOR	PIN	CONN	FUNCTION
J6	A	0	22	W59	A2-A3-J1-1	0	SEE A2-A2-J8-10	W11	16	903	HH	J1	CIRCUIT GROUND
	P	39			-14		-4			[illegible]	D		CLEAR TO LINE STORE
J6	r	35			-15	9	-12			209	N		DATA BIT D0 TO LINE STORE
	t	90			-17		-13			509			DATA BIT D1 TO LINE STORE

ROUTING DATA

Figure 2-11. Signal routing through MDF.

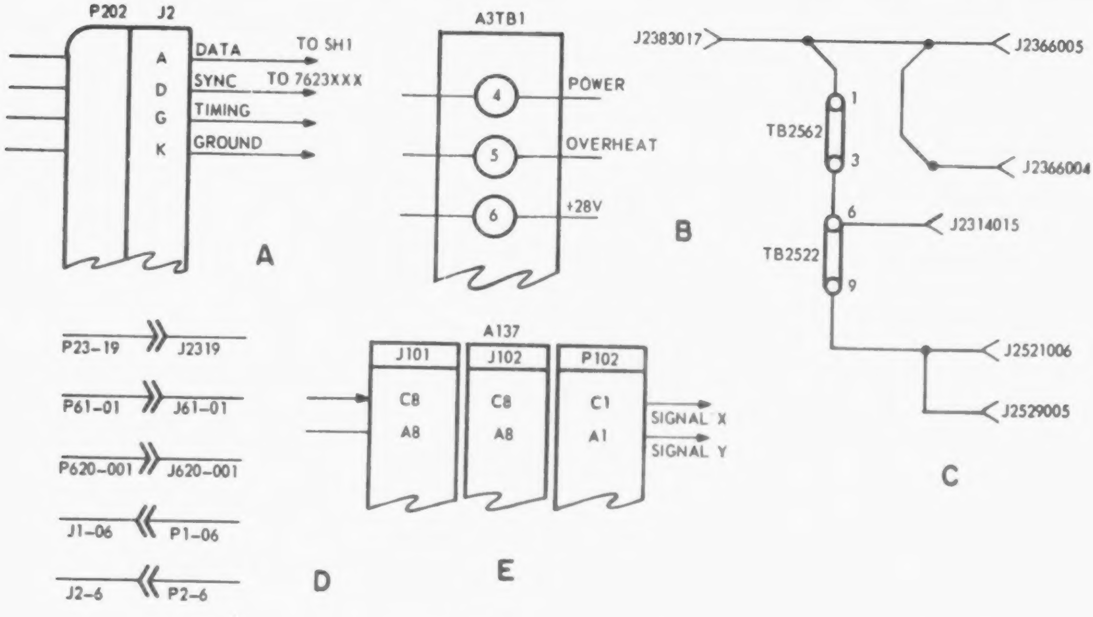
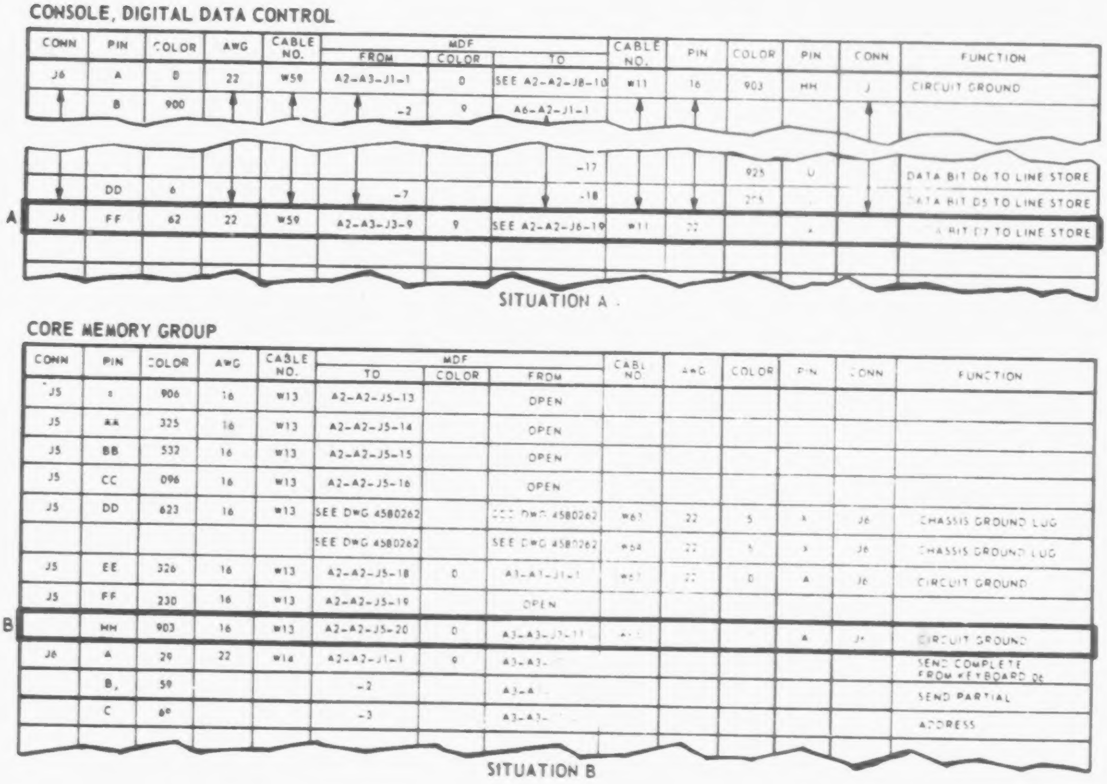

P202
J2
A
D
G
K
DATA
SYNC
TIMING
GROUND
TO SH1
TO 7623XXX
A
A3TB1
4
5
6
POWER
OVERHEAT
+28V
B
J2383017
J2366005
TB2562
1
3
J2366004
6
J2314015
TB2522
9
J2521006
J2529005
C
P23-19
J2319
P61-01
J61-01
P620-001
J620-001
J1-06
P1-06
J2-6
P2-6
D
A137
J101
J102
P102
C8
A8
C8
A8
C1
A1
SIGNAL X
SIGNAL Y
E

Figure 2-12. Jack connector symbols.



CONSOLE, DIGITAL DATA CONTROL

CONN	PIN	COLOR	AWG	CABLE NO.	MDF FROM	MDF COLOR	MDF TO	CABLE NO.	PIN	COLOR	PIN	CONN	FUNCTION
J6	A	0	22	W59	A2-A3-J1-1	0	SEE A2-A2-J8-10	W11	16	903	HH	J	CIRCUIT GROUND
	B	900			-2	9	A6-A2-J1-1						
							-17			925	U		DATA BIT D6 TO LINE STORE
	DD	6			-7		-18			[illegible]			DATA BIT D5 TO LINE STORE
J6	FF	62	22	W59	A2-A3-J3-9	9	SEE A2-A2-J6-19	W11	22		X		DATA BIT D7 TO LINE STORE

A

SITUATION A

CORE MEMORY GROUP

CONN	PIN	COLOR	AWG	CABLE NO.	MDF TO	MDF COLOR	MDF FROM	CABL NO.	AWG	COLOR	PIN	CONN	FUNCTION
J5	Z	906	16	W13	A2-A2-J5-13		OPEN						
J5	AA	325	16	W13	A2-A2-J5-14		OPEN						
J5	BB	532	16	W13	A2-A2-J5-15		OPEN						
J5	CC	096	16	W13	A2-A2-J5-16		OPEN						
J5	DD	623	16	W13	SEE DWG 4580262		SEE DWG 4580262	W63	22	5	X	J6	CHASSIS GROUND LUG
					SEE DWG 4580262		SEE DWG 4580262	W64	22	5	X	J6	CHASSIS GROUND LUG
J5	EE	326	16	W13	A2-A2-J5-18	0	A1-A1-J1-1	W63	22	0	A	J6	CIRCUIT GROUND
J5	FF	230	16	W13	A2-A2-J5-19		OPEN						
	HH	903	16	W13	A2-A2-J5-20	0	A3-A3-J[illegible]-11	[illegible]			A	J6	CIRCUIT GROUND
J6	A	29	22	W14	A2-A2-J1-1	9	A3-A3-						SEND COMPLETE FROM KEYBOARD D6
	B,	59			-2		A3-A						SEND PARTIAL
	C	69			-3		A3-A3-						ADDRESS

B

SITUATION B

Figure 2-13. MDF routing.

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console in question 1; begin at the memory group in question 2. Refer to figure 2-11 for the routing you need to follow.

1. a.
   b.
   c.
   d.
   e.
   f.
   g.
   h.

2. a.
   b.
   c.
   d.
   e.
   f.
   g.
   h.

2-4. Preventive Maintenance

The best maintenance is preventive in nature with potential problems detected and corrected before they have a chance to develop. Preventive maintenance consists of the measures taken periodically (or when needed) to achieve maximum efficiency in performance, to insure continuity of service, to reduce major breakdowns, and to lengthen the useful life of the equipment or system.

The general maintenance functions performed by most 305X4s fall in the category of preventive maintenance routines and the repairing or replacing of electronic components. Included are such tasks as service, inspect, repair, replace and validate, and the performance of operational checks associated with these tasks. To help achieve a clear understanding of your job responsibilities in relation to the tasks, it becomes important for you to analyze why a task is performed and to understand the consequences if you fail to accomplish the task. What are some of the features of maintenance routines? What is accomplished by their performance? What areas of responsibilities are included? What repairing tasks will you need to perform and what problems will you encounter? What repair skills will you need to develop? This section presents basic answers to these questions.

414. State the purpose of preventive maintenance routines, define PMI terms, and indicate the uses and areas of workcards in the inspection cycle.

After examining service routines and inspections here, we take up, respectively, routine analysis and workcards. Two subareas are gone into under service routines and inspections.

Service Routines and Inspections. Generally, a maintenance routine requires you to clean and service equipment so that optimum equipment operation is obtained. Improper performance of these tasks can and does result in equipment status deterioration, intermittent error problems, and corrosion. In the following paragraphs you will read about situations that arise because these routines are performed haphazardly and when, how, and why repairs are made to components of a system. You, the maintenance specialist, are the only one who can insure that the operations personnel have workable equipment.

Daily and phase inspections. Your equipment preventive maintenance inspections (PMIs) are performed as scheduled maintenance and are repeated over and over again for the life of the equipment. Maintenance Control schedules the routines and with this schedule you know exactly when, where, and what PMIs you are to accomplish. Maintenance PMIs are scheduled by days 1, 7, 14, 21, 28, etc. For this reason they are also called calendar inspections. An inspection cycle is every 28 days, which is considered a maintenance month. Some routines or inspections on systems are known as phase inspections. Using this inspection system, you are doing one of two things: (1) you are doing the same workcard each 28 days but on a different cabinet or assembly, or (2) you are accomplishing different workcards on the same assembly. The phased system allows maintenance personnel to distribute their workload and to still meet the time intervals required of equipment inspections.

Inspection tasks are related to both mechanical and electrical parts of your equipment. You must understand the equipment operation pertaining to inspection areas and know where to find specific information concerning the inspection routine. This is in the equipment technical order (TO) which ends in -6WC. The -6, whether it is 106 or 36, identifies this TO as the workcard series. That is also what the two letters "WC" stand for—workcard. The TO series number would precede these designators.

Service routines. Service routines often use more man-hours than any other category of maintenance. Service maintenance routines include the tasks related to equipment moving or repositioning, corrosion control, painting, lettering, and equipment or facility cleaning.

Routine Analysis. Routine analysis as related to your performance of tasks must be clearly understood in order for you to become a skilled maintenance specialist. Fortunately, in the electronics career field, all steps in our analysis are logical and consist of:

(1) Determining the objective. This is done by identifying the task to be performed; i.e., perform a PMI, replace a lamp, etc.

(2) Determining the steps involved in accomplishment of the task. In preventive maintenance routines, the steps are already listed. In the removal and replacement of components, the steps may or may not be listed in the TO, but they must be identified.

(3) Determining what principles or characteristics or specific requirements must be considered while the task is being performed. These areas include: (1) possible impact on the system, such as power requirements, interruption of system operation, and partial loss of system capability; (2) physical adjacent of subelements involved; (3) removal of other units to facilitate repair;

and (4) the use of associated test equipment and testing procedures.

Workcards. The workcard obtained from your -6WC technical order will be identified by the PMI schedule from Maintenance Control. This may not be direct; however, the schedule does identify the equipment and type of routine—7 day or 28 day, etc. With this information, the proper workcard set and particular workcard are identified. We have already said that the workcard has a step-by-step procedure to follow, but this is not all. The workcard has three major areas. They are:

(1) The test equipment required.

(2) The materials required; this would include oil or grease by type, any cleaning solvents required, lint-free cloth, etc.

(3) The procedure to follow; this is the step-by-step action you are to take.

Other information found on the workcard includes:

- The inspection cycle, such as 7-day.
- Whether power is on or off during the inspection.
- Whether the equipment will be in or out of service during the PMI.
- The number of people required to perform the routine.
- The average time required to perform the routine.

Additional information may be found, depending on your equipment and routine requirements. Some workcards include work unit codes or identify specialists of other AFSCs required to assist you in accomplishment of the routine.

The visual appearance of your equipment and its high degree of operational readiness or operational capability will reflect how well you perform the preventive maintenance routines and maintenance on your equipment.

Exercises (414):

1. What is the purpose of PMIs?

2. What is a maintenance month?

3. What is a service routine?

4. What are the three major areas of a workcard?

5. How do you determine what workcards to accomplish?

6. What additional information may be found on a workcard?

415. Identify specified conditions, precautions, and problems which can be found during preventive maintenance inspections.

Finding Problems During Preventive Maintenance. While you are performing preventive maintenance routines, you should be alert continuously to potential defects in the equipment, such as worn parts and overheated components. Find the cause of these defects and correct the trouble. If you perform PMs properly, you greatly reduce the possibility of future failures and malfunctions.

Technical manuals outline the step-by-step procedures to follow when you inspect, clean, and lubricate equipment. The purpose of this section is to acquaint you with the general principles upon which these procedures are based.

One of the most important steps in performing preventive or corrective maintenance is a complete visual inspection. Many defects in electronic equipment are found this way. You must inspect the equipment visually for discolored, burned, or cracked resistors and capacitors; loose connections; loose mountings; faulty tubes; sluggish or dirty relays; overheated transformers and motor housings; and defective insulators. The importance of the visual inspection cannot be overemphasized. Make this inspection very carefully. Many simple troubles have been overlooked and correcting them has become time-consuming because someone neglected to perform the visual inspection properly.

At times, potential troubles can be found by touch. For an example, feel the coupling transformers. They should be cool even after the equipment has been operating a relatively long time. If they are hot, something is wrong. The transformers in the power supplies should be rather hot, but not hot enough to burn your hand.

During the inspection, carefully note the areas that will require special attention when you start cleaning the equipment. You can remove most dust with a vacuum cleaner, but more stubborn dirt, grime, grease, and corrosion require other methods of cleaning.

The first step in cleaning electronic equipment is to remove dust, dirt, and foreign particles with a vacuum cleaner or compressed air. In cleaning with compressed air, be careful that is does not damage fragile parts. You can prevent damage by not using excessive air pressure and by carefully handling the air hose. A soft dust brush has some advantages if you use it carefully. After you have removed the loose dirt from the equipment, use a clean lintless rag moistened with an *approved* cleaning solvent to remove any remaining dirt and grease spots.

Proper precautions must be observed in the storage and use of cleaning solvents. Trichloroethylene is one solvent that is recommended for cleaning electronic equipment. Note, however, that trichloroethylene is toxic, so you should use it *only* in a well-ventilated room. Do *not* use this solvent for cleaning thermoplastics, "doped" coils, or natural rubber.

Remove any corrosion found during the visual inspection. Clean dirty, corroded tube pins and relay

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prongs with crocus cloth or fine (#0000) sandpaper and then wipe them clean with a dry cloth. Clean fuse ends and cable connector pins in the same manner.

For lubrication instructions, use the applicable equipment technical orders in your organization. Equipment technical manuals give you specific instructions about the types of lubricants to use, how to apply them, and the intervals at which they should be applied.

Exercises (415):

1. List the conditions you should look for during a visual inspection.

2. How can you find potential troubles by touch?

3. Briefly describe the procedures involved in a cleaning routine.

4. Describe briefly the precautions that you must observe when using trichloroethylene.

5. Where can you find information about the lubricants to use in a lubricating routine?

2-5. Operational/Performance Checks

This section presents a study of tasks associated with the performance checks of equipment operation. Components are being manufactured with more reliability because of major breakthroughs in engineering. The adoption of solid-state devices, using crystal structures, silicons and quartz, thin films, and doping, together with the techniques used in the manufacturing of these devices, have led to the development of maintenance techniques that you must understand, so that you can maintain your equipment properly.

416. Specify selected methods and particular devices used in performing operational checks in specific sections of computer and data processing units.

In sequence, this unit covers methods of operational/performance checks, meter checks, oscilloscope checks, CRT displays (C), printouts (O), and lamps and audio alarms (I/O/C). Along the way we go into 22 subareas of these six major topics.

Methods for Operational/Performance Checks. Operational/performance checks are performed by various methods. Some of these methods are:

- With various meters.
- With an oscilloscope.
- By use of display CRTs.
- By use of printouts.
- By interpretation of lamps, audio alarms, and internal tests.
- By visual examination of mechanical assemblies.

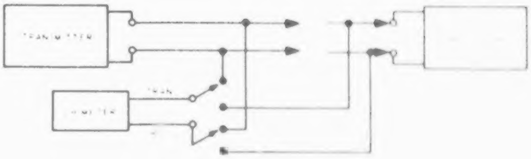

Figure 2-14. Metering data lines.

The -6WC series technical order applies to the tasks of operational and performance checks. The phase period of the task may range from daily to annually. The time interval is based upon statistical data accumulated through MDC and engineering data.

During your study of performance checks you will:

- Identify preferred methods of doing the tasks.
- Determine the reason that a check is made at certain specific points in the equipment.
- Examine technical data concerning the task or circuit being tested.

Meter Checks. The performance checks accomplished in various areas using AC voltmeter (RMS), DC voltmeters, and differential voltmeters and VOMs are examined in the following paragraphs dealing with line data, power supplies, and reference voltages.

Line data. (Applies to input and output units.) A method for determining line or data quality is by using an AC voltmeter (dB meter). This unit is usually connected to the lines or at the common point in the modulators and demodulators. By reading the meter (dBm scale) and comparing the value to prescribed values for transmit and receive, it is easy to determine line quality. Refer here to figure 2-14. You can see that it is relatively easy to connect the unit. One important factor to remember, however, is that the sensitivity of the meter must be very good or attenuation of the input and output signal will occur, and as much as 3-dB loss can occur. NOTE: A loss of 3 dB results in 50-percent power loss and can easily interrupt data.

Power supplies. (Applies to input/output and system central units.) The performance checks used on power supplies require the use of DC meters for measurement of output amplitudes of DC power supplies and AC meters for AC power supply output measurements. The power supply may use a current (micro or ma) meter to measure current load output. The power supply may be equipped with a differential (null) DC meter where the output voltage is measured against an internal reference voltage. A deviation voltage reading from the null indicates improper output voltage.

Reference voltages. (Applies to system central units.)

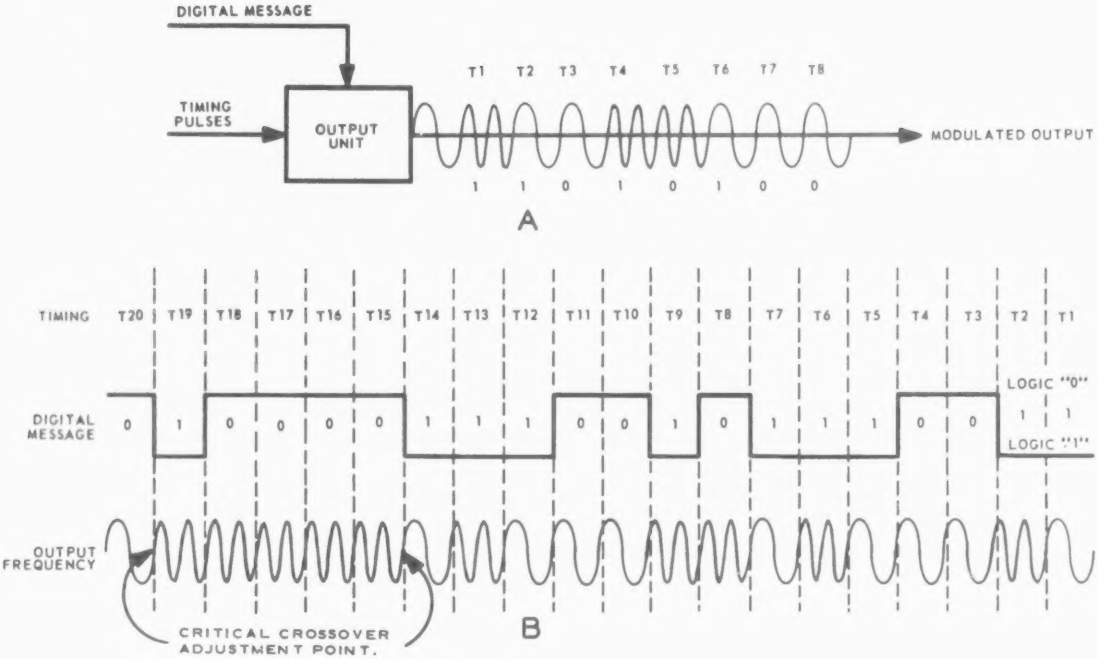

Figure 2-15. FSK crossover point.

Within many data processors and computers, selected circuits generate DC reference voltages in order to insure proper linear circuit operation. These are generators other than power supplies. Performance checks on these voltage sources require the use of DC volt and differential meters.

Oscilloscope Checks. We will next discuss the performance of operational checks by use of the oscilloscope, beginning with line data.

Line data. (Applies to input/output units.) Oscilloscopes may be required to perform operational checks on modulators and demodulators, especially where a system is using an FSK system or frequency modulation system, or where data, sync, and timing pulses are transmitted separately. A critical point of inspection for FSK is at the coincident point (refer to fig. 2-15), where one frequency of FSK meets with the other frequency. The crossover point must be at the zero-volt level, and the first frequency must be ending a cycle while the second frequency must be starting a cycle.

CRT displays. (Applies to system central units.) Oscilloscopes are frequently used on performance checks of CRT displays to measure waveforms, such as ramps, generator outputs, timing circuits, deflection and intensity circuits, and input signal data to the CRT. Check to see that each signal measured contains all of the elements of the waveform and compare the waveform to a standard, if possible. Some of the elements may be:

- Pulse width.
- Signal amplitude.
- Linearity of ramp signals, sine waves.
- Proper operating voltage levels.
- Pulse recurrence times (PRT).
- Phase.
- Polarity.
- Proper waveform; i.e., no overshoot or undershoot of square wave (such as ramps, timing, deflection intensity, and generator outputs).
- Ringing (noise).
- Data content.

Servo units. (Applies to input/output units.) The oscilloscope is used to validate waveform data from servos for nulling operations and reference voltage checks. Polarity, phase, and amplitude measurements must be determined and compared with standards. Amplifier chain waveforms may be compared to standards. Feedback loop signals may be measured for phase and amplitude.

Radar data. (Applies to input units.) Oscilloscopes are the primary measurement tool for determination of the accuracy and content of radar data. Common defects or missing components of a waveform, as shown in figure 2-16, can only be detected with a scope. These defects may be (1) no system trigger, (2) no noise or improper level of noise, (3) no video (hit) returns, and (4) excessive noise (clutter or jamming). The circuits which first receive radar inputs are usually the point of inspection. In these circuits, you must establish that video is present and that it is of the proper amplitude and polarity. Therefore, the operational check usually contains instructions to:

- Identify the points to measure and the controls to adjust.
- Measure the input level of the radar returns at various ranges.
- Measure and adjust the circuit output for a desired level and phase or polarity.

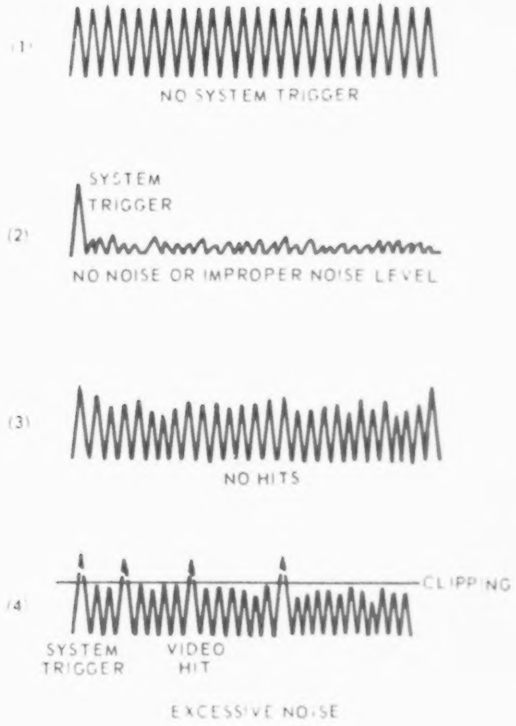

Figure 2-16. Defective radar returns.

The instructions in the TO may also provide a video return drawing that resembles figure 2-16. If the regulating circuit is designed to adjust the amplitude of the video return by resistive means, weak signals and noise signals will be amplified or attenuated just as strong signals are. If the circuit is designed to adjust the amplitude of the video return by capacitive means, then amplification or attenuation of weak signals and noise can be controlled more than strong signals. This condition exists because a weak return may be only slightly stronger than the noise being received. Both of these components of the video return consist of sharp spikes of very narrow pulse width, and a pulse with a narrow pulse width may be expressed as a high-frequency pulse, especially when it is taken in relationship to the time for one radar trigger period. Therefore, we must be conscious of which type of control we are using when examining and adjusting these inputs.

Video amplifier circuit. An oscilloscope is used to measure video amplification, and performance checks show where the likely measurable points are. Refer here to figure 2-17. You will see that video is fed to a differential amplifier through a coaxial cable. The shield of the cable is connected to the other input of the differential amplifier. These signals are forced by the amplifier to present the difference signal at the output. A variable current source is used to supply sufficient current for amplification and drive. This current source control is resistive. The video output is then fed to an amplifier circuit where a capacitive control is installed in the emitter portion of the circuit and is called a *peaking adj.* Since capacitors control high-frequency pulses more than low-frequency pulses, as we have stated previously, this control can, if misaligned, eliminate weak returns. The output of the amplifier is then fed to an emitter follower (EF) that supplies a current gain, no voltage gain, and no signal inversion. The EF output is routed to a gated amplifier that provides a control over the intensity of the video through a video intensity control. Therefore, a video return can be attenuated by three means—two are resistive, and one is capacitive. The object, of course, is to establish a desired video output with sufficient amplitude and current to present a reasonably strong signal to a display CRT or to a detection circuit that is designed to store these pulses. Let us now consider another type of input unit that processes raw or normal radar video.

Quantizer video unit. A quantizer (refer to fig. 2-18) transforms video information from radar returns into distinguishable pulses for target determination. An oscilloscope is used to verify signal amplitudes. Performance checks require adjustment of various controls in selected portions of the quantizer. The unit contains elements that aid in the detection of video and in the elimination of noise, clutter, and jamming. It provides a digitized video pulse output. There are various quantizers designed using vacuum tubes, solid-state

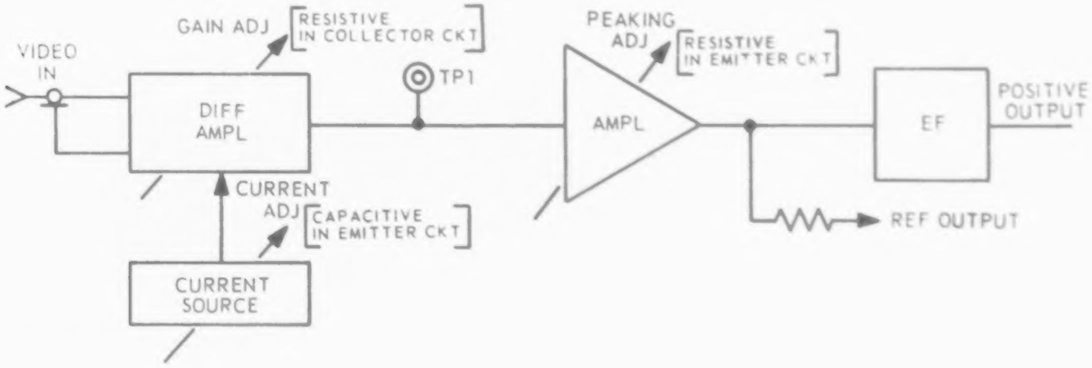

Figure 2-17. Video amplifier circuit.

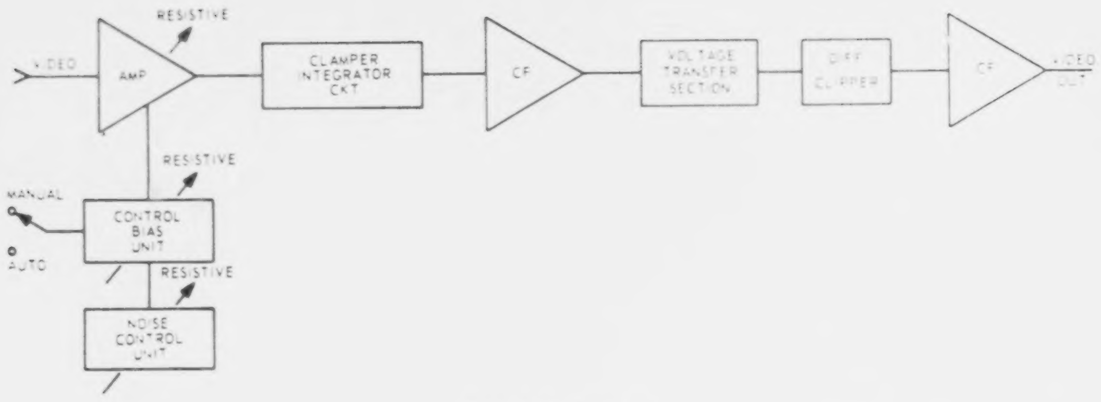
RESISTIVE
VIDEO
AMP
CLAMPER INTEGRATOR CKT
CF
VOLTAGE TRANSFER SECTION
DIFF CLIPPER
CF
VIDEO OUT
RESISTIVE
MANUAL
AUTO
CONTROL BIAS UNIT
RESISTIVE
NOISE CONTROL UNIT

Figure 2-18. Quantizer.

devices, and integrated circuits; however, their functions are similar. Each uses a noise meter to establish an acceptable level of noise that must be present to insure that weak video returns are not eliminated from processing. The first control in the circuit is a video amplifier (resistive) control. Since the quantizers may be operated in a manual or automatic mode, bias level controls are included in these circuits and they are resistive. These bias adjustments cause amplifiers to pass only selected peak amplitudes of returns, but they must be adjusted to include a percentage of noise.

One final point needs to be made about the use of a noise meter—that is that once its threshold has been exceeded, it blocks all video returns for the remainder of the radar period and part of the next radar period. The obvious conclusion is that the noise meter circuit can:

- Affect valid video returns by elimination.
- Be very effective during a jamming situation.
- Control the noise level of all video being processed.

Radar orientation validation (input). Oscilloscopes are used as coincidence detectors for insuring that the north mark and the prescribed number of ACPs occur. The scope is also used to check phase and amplitude signals from radar servos which are compared to a standard established for the system.

CRT Displays (C). Video or symbol or digital displays have examinations performed during operation and the checks quickly pinpoint defects. Refer to figure 2-19 for some of the operations that must be included in the checks:

- Use of CRT voltage controls for intensity, focus, positioning, and astigmatism.
- Symmetry and linearity of range marks.
- Callup operations of console.

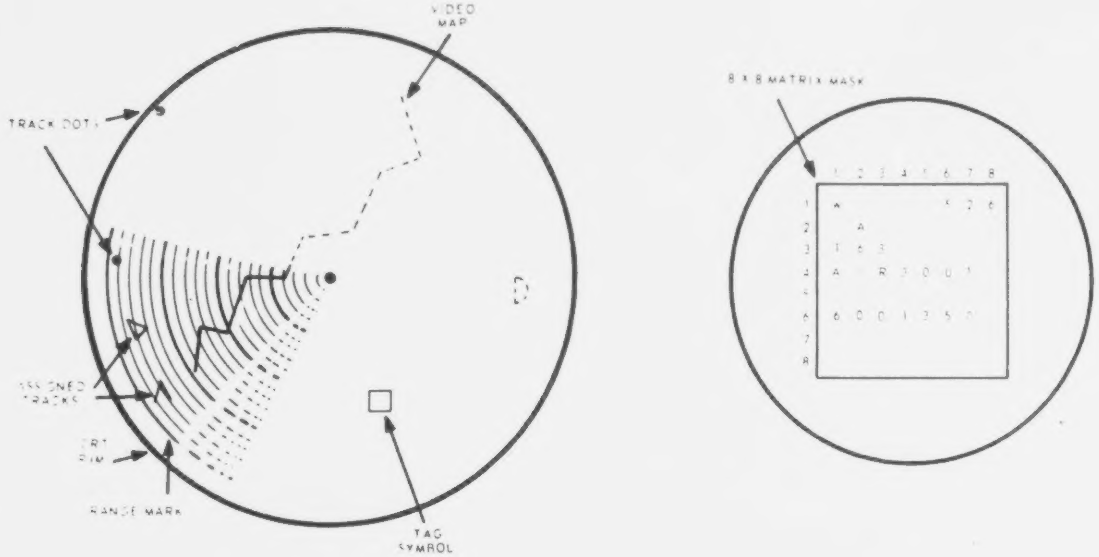
VIDEO MAP
TRACK DOTS
ASSIGNED TRACKS
CRT RIM
RANGE MARK
TAG SYMBOL
8 X 8 MATRIX MASK
1 2 3 4 5 6 7 8
1 A 5 2 6
2 A
3 T 6 3
4 A R 3 0 0 1
5
6 6 0 0 1 3 5 0
7
8

Figure 2-19. CRT displays.

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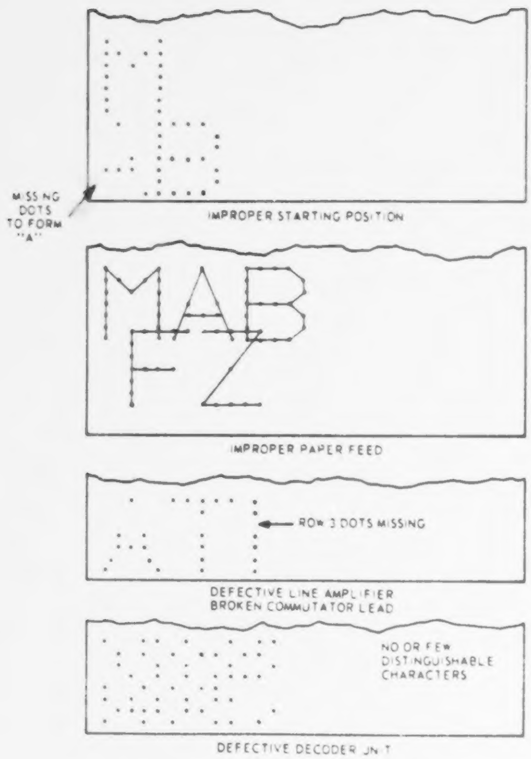

Figure 2-20. Defective printout.

- Printing capability of the digital display by use of test pattern.

If complete, this test also exercises all character generators.

Printouts (O). In the next few paragraphs we cover the use of printouts as a check for operational quality.

Electrographic printers (O). The printout determines the operational capability of this printer. An accurate printout satisfies performance requirements for quality and accuracy. A defective printout such as that shown in figure 2-20 indicates (1) improper starting position of commutator brushes, (2) defective paper feed, (3) defective line amplifier or a broken commutator lead, or (4) defective decoder unit.

Impact printer (O). Printouts which display all characters and numbers validate operational quality. Print selection circuits, mechanical assemblies, and character decoding circuits are the most frequent sources of trouble.

Central processor data (C). Printouts that are generated as a result of data taken from peripheral equipment or I/O equipment and which process through the DPC may be used to validate DPC operational quality.

Lamps and Audio Alarms (I/O/C). Next, we discuss the use of lamps and audio alarms. We range here from line data lights (I/O) to tape units (I/O).

Line data lights (I/O). Interpretation of lamps or alarms usually verifies that sync group (audio signal data preceding the data message) signals are present or absent. They may be called *busy bit, sync group,* or *no message characters.* A synchronization circuit samples sync bits and provides visual lamp failure indications and audio tone failure indications.

Parity lights (I/O/C). Lamps provided for these circuits show that a circuit designed to count each bit of an incoming or outgoing message detects overall correct parity. Failure may be indicated on fault facility panels or confidence indicator units or other convenient panels where lamp and audio indicators alert failure.

Power supplies (I/C). Lamps indicate operational quality; green or white for power on, amber for overload, and red for voltage failure.

CP units (C). Lamps indicate counter operations, sequences, data flow (yellow or white), and failure (red). Sampling circuits may use live data or test data, depending upon design.

Tape transport units (I/O). Sequence lamps, failure lamps, and command and control lamps indicate the status of the unit. Interpretation of lamps may relate to specific areas where operation ceases.

Visual Examination of Mechanical Assemblies (I/O/C). Some examples of visual examination to find defects are given below.

Servo units (I/O). Noisy or binding gear trains are the only visual examinations possible on these units.

Electrographic printer (O). Noisy drive unit or clutch assemblies and improper paper feed are all signs of visual defects.

Impact printer (O). Visual indications of improper or proper operations of cams, motors, paper feed, impact hammers, and other related units provide reliable visual examination of this printer. Interpretation of the printout also provides reliable performance data.

Tape units (I/O). Proper orientation of tapes, operation of servos, takeup reel tension, and photolamp illumination or vacuum pump operation are all visual indications of proper or improper operational performance.

Exercises (416):

1. What are the devices usually used to perform operational checks?

2. What are the areas of a computer system which usually require the use of a meter during performance checking?

3. Checking line data where the critical point of inspection for FSK is the coincident point and one frequency of FSK meets the other frequency, what device may be required?

4. The oscilloscope is used extensively for equipment

validation. List some of the elements within an oscilloscope display to check during performance checks.

5. Using the oscilloscope to check radar data operationally, what does that check usually contain instructions to do?

6. How is the oscilloscope used to check a quantizer video unit operationally?

7. How is radar data entry usually verified?

8. Give in list form some operations that must be included in CRT display checks.

9 What are the two types of devices usually included in DC power supplies that aid in verification of performance?

10. Lamps are used to verify operationally that audio signal data preceding the data message signals are present or absent. What may these signals be called?

11. Concerning lamp or audio alarm operational checks of tape units, what are the visual indications of proper or improper performance?

417. Cite certain considerations required when checking transmission lines for proper operation, and define terms relevant to transmission lines.

Transmission Lines. System input and output requires the use of indicators, meters, and switches. To aid you in understanding why and how performance checks are performed in this area, let's first explore what is necessary in order for data to be transmitted and received. Then let's identify for you how the input/output equipment can sense the correctness of data and errors in data.

Whenever data is accumulated at a station, it may be of value to higher headquarters. That is why almost all command and control systems have data links. For the most part, these data links are conventional telephone (TELCO) lines or microwave units of a telephone company. In oversea areas and under tactical situations in the United States, Air Force personnel and equipment replace a commercial company.

Since data must be transmitted and received over these media, a problem arises in that any signal entered into a long wire loses power. The reason for this is that wire has resistance that impedes the flow of a signal. How this power loss is compensated for is illustrated in figure 2-21. There, as you can see, TELCO repeater stations are placed every 6 or 7 miles with capabilities of taking in a very small signal and boosting it to a high enough power rating to reach the next repeater station. The amplifiers in

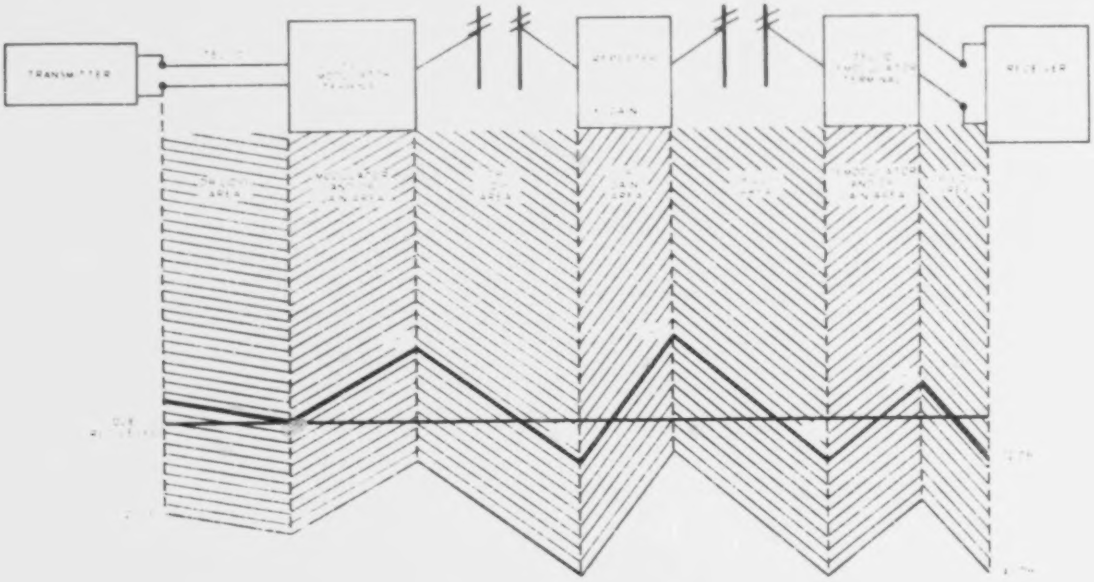

Figure 2-21. Repeater stations.

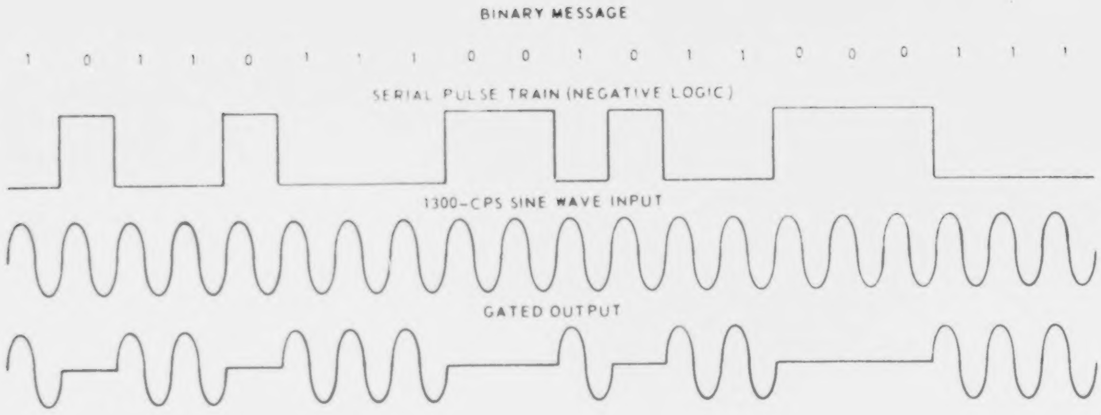
BINARY MESSAGE
1 0 1 1 0 1 1 1 0 0 1 0 1 1 0 0 0 1 1 1
SERIAL PULSE TRAIN (NEGATIVE LOGIC)
1300-CPS SINE WAVE INPUT
GATED OUTPUT

Figure 2-22. Dipole data.

the repeater station are linear-type amplifiers, with automatic frequency and gain controls built in. They can raise the power level of the output signal with no loss of signal data.

To get the data to a TELCO line properly, you may have a modulator or transmitter in your equipment. This unit prepares the digital data for the line. In one system, it may change the digital data to dipole data. Refer to figure 2-22. There dipole data is shown making clear that a change of binary one, zero to 1 (1 0 1) in a message results in a change from cycle pulse to a level to a cycle. Your further examination of figure 2-22 will show you that each binary one results in one cycle pulse. Another system currently in use uses *frequency shift keying* (FSK). This method, shown in figure 2-23, uses two audio frequencies. A change in frequency represents a binary one. No change in frequency for successive time periods represents binary zeros.

Line quality. Selection of the bit rate of a message is determined by the quality of the local TELCO lines. If the noise levels, cross-talk, or other factors related to audio transmission cause the line quality to be low, then data must be transmitted at the slowest rate possible. On the other hand, a noise-free interference-free line can handle data at a fast bit rate and is called a high-quality line.

Decibel. Now you need one final bit of information; then you can fully understand what this discussion is meant to convey. This information concerns the decibel (dB) and dBm. The dB is a unit of power ratio, while the

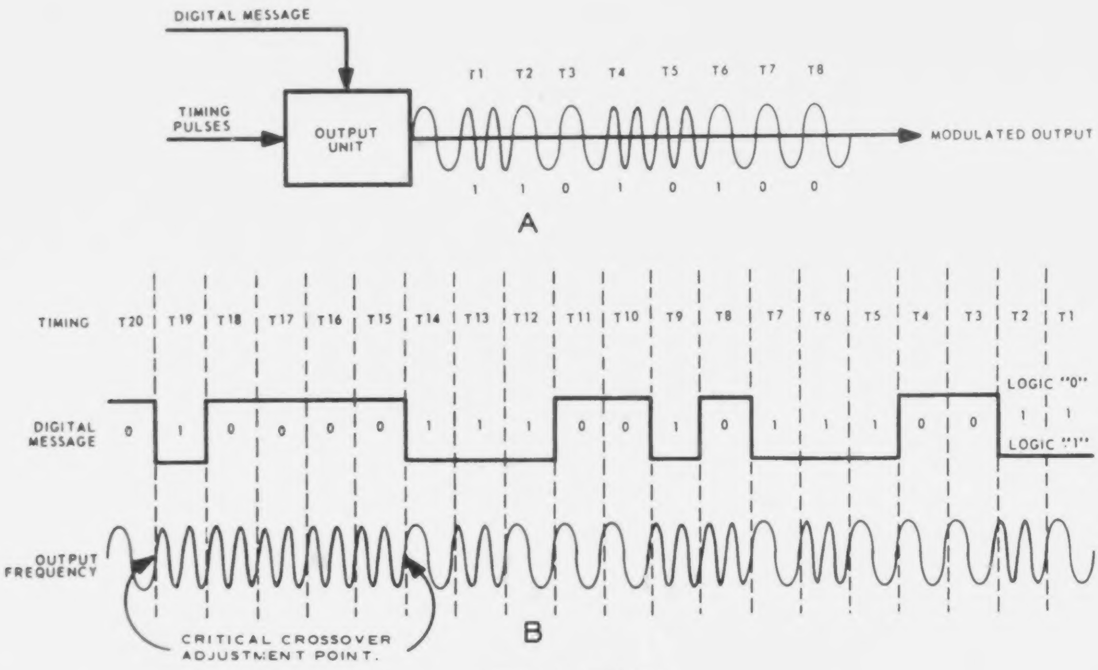
DIGITAL MESSAGE
TIMING PULSES
OUTPUT UNIT
T1 T2 T3 T4 T5 T6 T7 T8
MODULATED OUTPUT
1 1 0 1 0 1 0 0
A
TIMING
T20 T19 T18 T17 T16 T15 T14 T13 T12 T11 T10 T9 T8 T7 T6 T5 T4 T3 T2 T1
LOGIC "0"
DIGITAL MESSAGE
0 1 0 0 0 0 1 1 1 0 0 1 0 1 1 1 0 0 1 1
LOGIC "1"
OUTPUT FREQUENCY
CRITICAL CROSSOVER ADJUSTMENT POINT.
B

Figure 2-23. FSK data.

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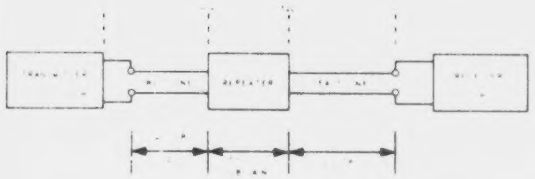

Figure 2-24. dB loss and gain.

dBm is a measure of absolute power as compared with a reference level of 1 milliwatt. One milliwatt of power is equal to 0 dBm. Refer here to figure 2-24. As you can see, the line loss from the transmitter (west line) is 10dB—transmitter output equals 0 dBm, repeater inputs equals − 10 dBm. This loss of 10 dB represents a power loss of 90 percent; so if the signal injected into the line were 1000 Hz at 1 milliwatt of power, then the repeater would receive a .1-milliwatt signal at 1000 Hz. The repeater amplifiers are adjusted to provide a +30-dB gain. This provides a power-ratio factor of 1000, and the output is 1000 × .1 = 100, or a +20-dBm signal, since a power ratio factor of 100 = 20 dB. The east line loss is − 10, and the receiver input is +10 dBm.

Transmission path. Refer once again to figure 2-21 as we take up the transmission path. The transmitter signal enters the phone line from the modulator or transmitter at a fixed dB level, usually between +6 to − 25 dB. It may pass through one or more repeaters until it reaches the high-frequency terminal equipment. Here the data is modulated onto a high-frequency carrier and sped on its way to the receiver. Periodically along the line, repeater stations amplify the signal so that it has sufficient power to reach the next station. At the receiving end, the high-frequency carrier is removed, and the audio-frequency data is fed to the receiver at the proper dB level. The receiver demodulates the signal by a reversal of the process used to modulate it—dipole to digital or FSK to digital as examples. Processing within the equipment then begins.

Exercises (417):

1. How is attenuation of signals in transmission lines compensated for?

2. What does the term "line quality" mean?

3. Define "decibel."

4. At what stage does the decibel level of a signal usually enter a transmission line?

2-6. Adjustments and Alignments

Adjustment is the act whereby a device is used to alter a condition to make it fit or correspond. This means, for purposes of this discussion, the physical change of a variable component to make the circuit provide a discrete output.

The word "alignment" means to bring into line or straight line. For the purpose of this text, alignment refers to adjustments that are combined within a functional unit to provide a discrete output.

In many circuits, reactive components are the adjustable units and, when these are arbitrarily turned, extreme results are produced. Selected frequencies may be attenuated or lost; waveforms may be distorted, causing improper data flow and loss of digital data quality; and operating levels may be affected, causing a shift in amplifier operation.

This section identifies reactive controls, gives their characteristics, and shows how they are used in various circuits.

418. Give the purposes of variable controls, identify common types, and supply their characteristics and uses in various circuits.

After talking about the purpose of variable controls in this segment, we next look at variable control types. Then, lastly, we go into principles of operation.

Purpose of Variable Controls. Each time that a variable control is included in a circuit, it serves a distinct function in the operation of that circuit. It is a compensation device used because the inputs to the circuit are variable signals that must be regulated to provide a specific output. Within the circuit, this may cause increase or decrease in bias voltage or current, a change in frequency, or a shift in frequency. Any one of these changes causes the circuit to operate outside its designed operating level. The signal may be affected by distortion, limiting, attenuation, or amplification. Variable controls are used to alter the output waveform to meet specifications. However, if the input signal strength causes the circuit to operate beyond the control of the variable device, no amount of adjustment can correct the output waveform. This last is a significant factor to consider when studying the purpose of a variable control.

Variable Control Types. Study figure 2-25. Each component shown is a variable control, even though physical appearances vary. Two common types of *variable capacitors* are the tubular type (A) with an adjustable core and the button type (B) with a variable rotor. In either case, different values of capacitance are obtained by varying overcoupling of the plates. For most frequencies up to 30 MHz, these are adequate. For frequencies above 30 MHz, the variable capacitor must be so constructed that no RF voltage is developed. This is often done by having the external circuit connected to two sets of stator plates and using the rotor to increase or decrease the total capacitance between the plates. In this arrangement, no RF current flows, since the rotor is not a link between the stator plates. Figure 2-25,C, shows a typical

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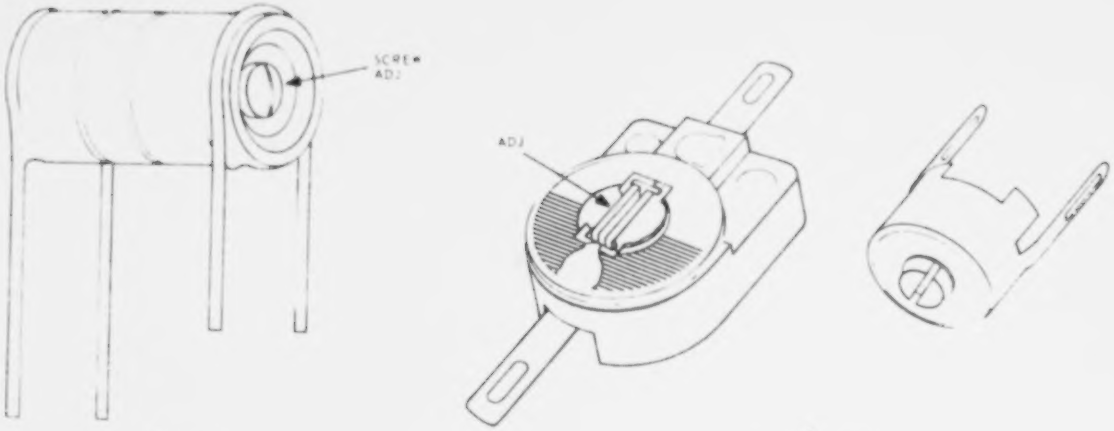
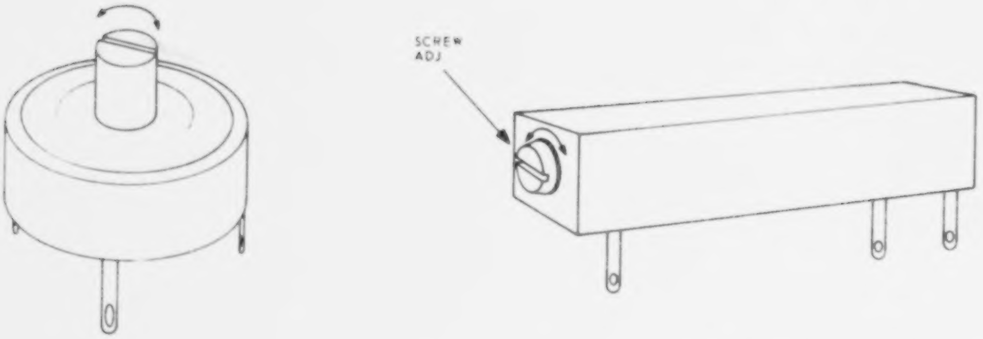


A
TABULAR TRIMMER

B
BUTTON TRIMMERS



C
POTENTIOMETER

D
POTENTIOMETER

Figure 2-25. Variable components.

potentiometer. This control uses a rotor; however, the rotor is in contact with the resistive element. The output voltage or current is tapped off at the point of contact. Figure 2-25,D, is an example of a potentiometer commonly found on printed circuit cards. Its control is a screw-type shaft which, when turned, causes a contact point on the screw to mate with the resistive element. This provides an output voltage or current proportional to its wiper arm position. The control shown usually has from 8 to 26 full turns.

Inductors and coils may also be variable and are used extensively in electronic equipment. However, variable coils are seldom used in data processing and computer circuitry, so no further coverage is included.

Principles of Operation. Variable capacitors are manufactured using different material as dielectrics. Some materials are ceramic, mica, glass (piston), polystyrene, teflon, and air. Each of these materials has a different dielectric constant. The basic principle of a variable capacitor involves positioning the rotor with respect to the stator. The area of electrode (plate) is fixed. Turning the rotor from 0° to 180° varies the amount of plate surface exposed, thereby varying the amount of capacitance. Refer to figure 2-26 and note that the metallized rotor surface may overlap any part of the metallized stator surface. With this arrangement, the capacitance varies, depending upon the amount of metallized plate overlapping and the dielectric constant. To vary capacitance requires either varying the dielectric or varying the overcoupling of the electrode plates.

In most trimmer capacitors used in computer and data processing circuits, the variable change in capacitance is linear throughout its rotation, as shown in figure 2-27. The figure shows linear increase and decrease in capacitance through 360° of rotor rotation. Variable capacitors or trimmers are frequently used as filters in oscillators and as attenuators in displays and counters.

Let's review some characteristics of the newer types of capacitors which can create problems for us. Most ceramic capacitors have a maximum life of 250 turns. Some tubular types have 1000 or more turns of life expectancy. Adjustments must be made with tuning wands, since most trimmers connect the stator or rotor to

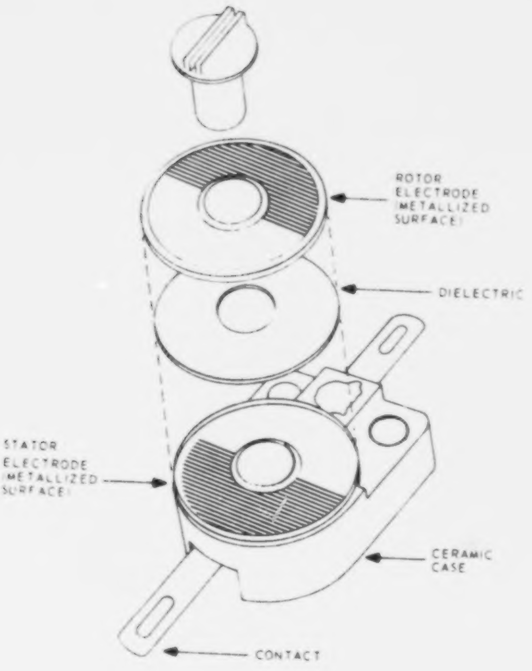

ROTOR ELECTRODE (METALLIZED SURFACE)
DIELECTRIC
STATOR ELECTRODE (METALLIZED SURFACE)
CERAMIC CASE
CONTACT

Figure 2-26. Variable capacitor.

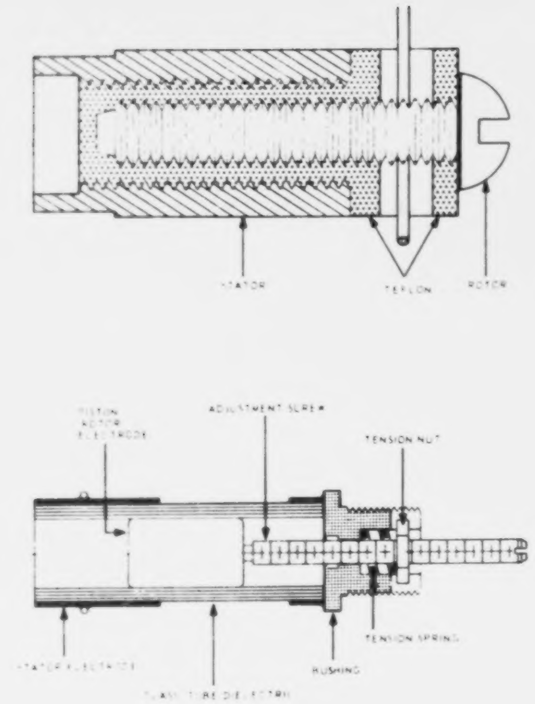


Figure 2-28. Tubular capacitor.

the end frame or turning screw. Placing a metal screwdriver on the turning screw changes the effective area of the metallized plated surface of either the rotor (usually) or the stator, thereby altering the characteristics of the capacitor. The size of these units is being reduced to meet demands of industry for microelectronics. As a result, the voltage breakdown values have been drastically reduced.

Tubular type variable capacitors, such as shown in figure 2-28, are now satisfying industry's requirements for microelectronics. These capacitors possess a characteristic not unlike potentiometers in that small, critical adjustments can be made on them. The sliding action of the rotor, controlled by the screw, changes the plate area opposite the stator, thereby varying the capacitance.

Potentiometers are variable resistance components. They may be either carbon pile or wire wound. The wirewound potentiometers are usually used as rheostats rather than as potentiometers.

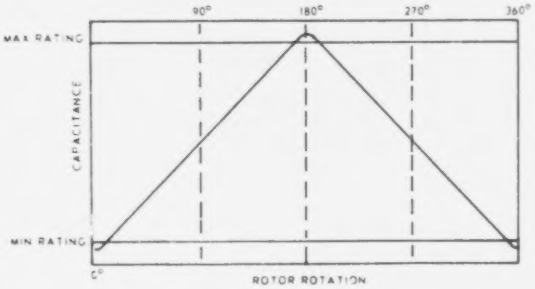


Figure 2-27. Linearity through 360° of rotor rotation.

Potentiometers, or "pots," are used extensively in computer and data processing equipment. Usually, they are carbon and resemble those shown in figure 2-29,A and B. Notice that figure 2-29,C, indicates that a brass slide is positioned by the turning screw to some point along its path of travel (pickoff point). Its position is manually selected and the resultant output voltage is fed to the using circuit. In the manufacture of these units, the adjusting screw is isolated from the carbon resistor and the metal turning shaft by a nonconductive substance, such as epoxy. Figure 2-29,D, shows the internal structure of the pot shown in figure 2-29,B. Notice that the resistive element is circular in shape and that each end is connected to an external terminal. The variable slider or wiper is isolated from the turning screw. The slider has continuity to the third terminal through the circular ring. Two factors must be identified and explained here. First, when the turning device of the rectangular pot is turned to its end, it may make an audible clicking sound signifying that no further turning in that direction is possible. Second, the pot shown in figure 2-29,D, usually has a mechanical stop at each end of the resistor, and further turning of the screw results in shearing the stop pin or destroying the pot screw, or both.

Since we are discussing the adjustment of circuit components and the variable resistor, we must recognize another manufacturing characteristic of these components. Variable resistors and pots are made linear and tapered. The linear pot is so made that its resistance is distributed evenly over its entire length. When an ohmmeter is used to measure its resistance, the wiper arm

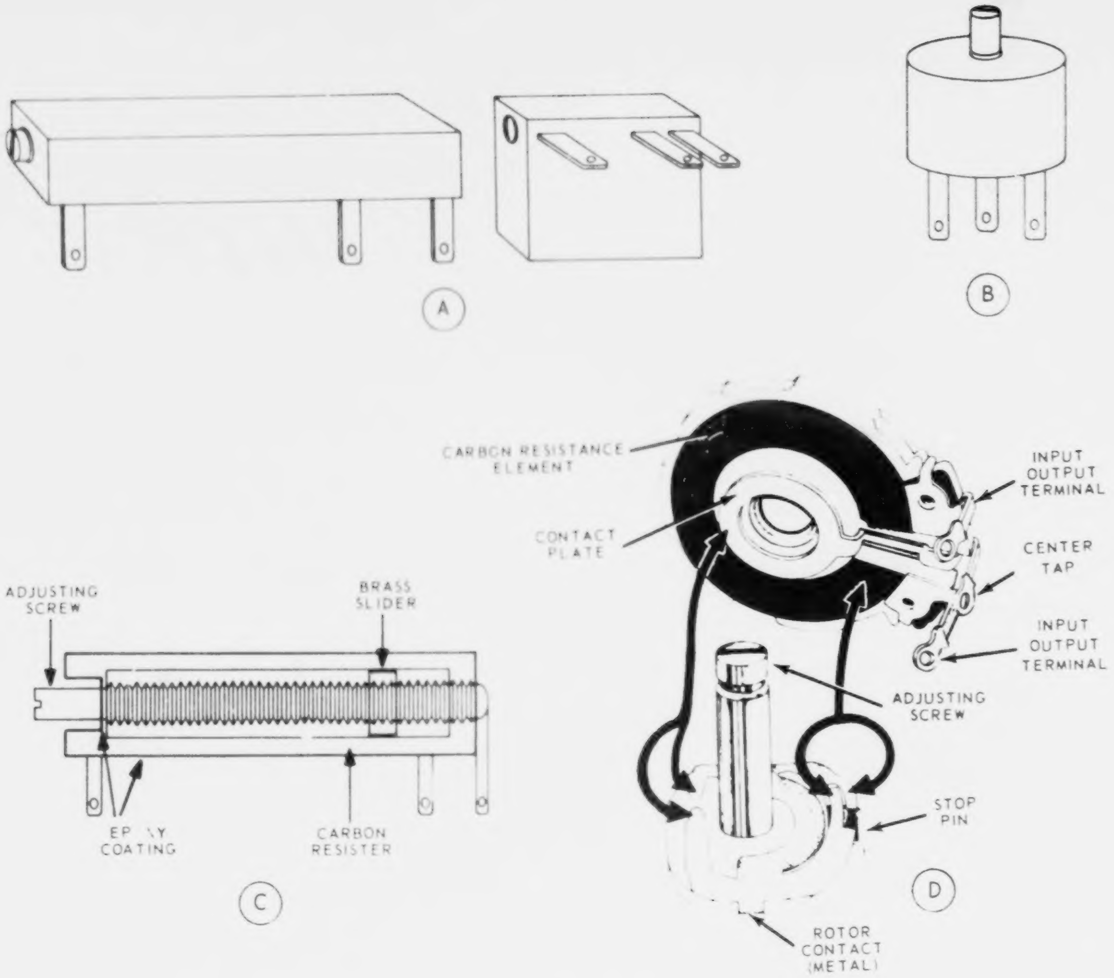

A
B
ADJUSTING SCREW
BRASS SLIDER
EPOXY COATING
CARBON RESISTER
C
CARBON RESISTANCE ELEMENT
CONTACT PLATE
INPUT OUTPUT TERMINAL
CENTER TAP
INPUT OUTPUT TERMINAL
ADJUSTING SCREW
STOP PIN
D
ROTOR CONTACT (METAL)

Figure 2-29. Potentiometers.

output resistance causes an even deflection of the meter needle for the entire length of the resistor. The tapered pot is so made that one-tenth of the total resistance is available between one extreme and the midpoint of the adjustment cycle, and the other 90 percent of resistance is available between the midpoint and the other extreme of the adjustment cycle. If you use an ohmmeter to measure the resistance of a tapered pot, placing one lead on the input terminal and the other lead on the wiper (rotor) terminal, you can see that, as you turn the wiper, the resistance increases (from zero) very slowly and gradually until you reach a point midway on the pot. From the midpoint on, as you continue to turn the wiper shaft, the resistance increases much more rapidly in comparison with the first half pot rotor rotation.

Exercises (418):

1. List any three purposes of variable components.

2. Name two common types of variable controls (variable capacitors).

3. List six dielectric materials used in capacitors.

4. Is the trimmer capacitor used most frequently in a computer system linear or nonlinear?

5. What is a common problem encountered with the variable compacitor?

6. Name the two types of variable resistors.

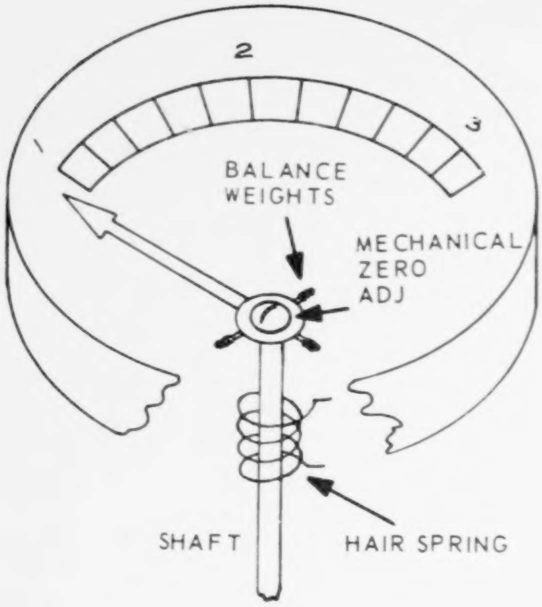


Figure 2-30. Mechanical needle adjustments.

7. Of the two types of variable resistance components, which is usually used when a wire-wound resistance is needed?

8. Explain the "pickoff" principle of a potentiometer.

9. List two manufacturing methods that are used to indicate the extreme ends of a potentiometer adjustment screw's turning capacity.

10. Name the two different methods of manufacturing carbon resistance deposits within a potentiometer.

419. Cite the adjustment procedures for meters and dials.

Adjust Meters and Dials. Adjustments that you can make on meters and dials are usually restricted to centering the needle and calibrating it with the calibrating voltage and adjustment control. The only exceptions to these adjustments are those where you are required to perform category 1 or 2 test procedures for test equipment.

Balancing. Positioning the needle on a meter or dial requires you to use a small screwdriver and to carefully adjust the screw until the pointer aligns with the proper mark on the meter face. Refer to figure 2-30 and you will see that this adjustment is mechanical and that no voltage or current is involved. You merely twist the control and position the pointer, which is pressed onto the shaft, to the correct position. Balancing the meter needle requires disassembling the meter and repositioning the weights on the needle shaft; these adjustments are performed by PME Laboratory personnel.

Centering. Adjusting a meter before it is used requires a check of internal electrical components. This is called *zeroing in the meter.* For ohm adjusting, short the two probes together. This should cause 100-percent deflection of the needle. A potentiometer in the meter circuit will adjust current from the battery to cause 100-percent needle deflection. When you change ohm scales on your meter, you change the sensitivity of the meter. Therefore, you must adjust the needle deflection again by use of the adjustment of zero pot. To adjust a meter such as a differential voltmeter, apply a source voltage to the balancing circuit. Most differential voltmeters work on the same principle. Refer to figure 2-31 for a simplified circuit of a differential voltmeter application. As you can

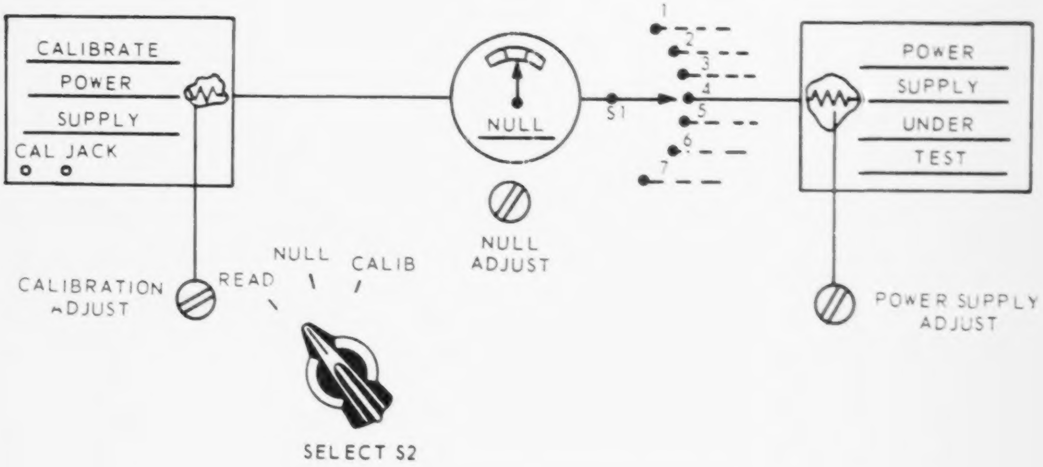


Figure 2-31. Simplified differential meter circuit.

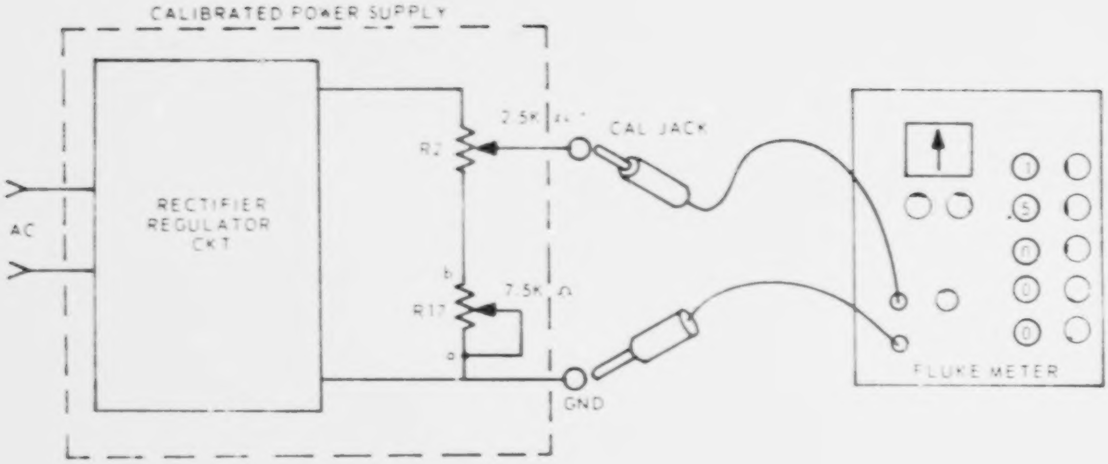

CALIBRATED POWER SUPPLY
RECTIFIER REGULATOR CKT
AC
R2
2.5K
CAL JACK
b
R17
7.5K Ω
a
GND
FLUKE METER

Figure 2-32. Calibrate adjustment.

see, the calibrated power supply is permanently installed as part of the equipment. It feeds its output to one side of the meter. The power supply under test has its output sampled under load conditions, and if both voltages are exactly the same, there is not deflection of the null meter needle.

Two factors become important to the analysis. First, before the power supply can be used as a standard, it must be calibrated. A shop standard can be used to calibrate the power supply. Then you can use the power supply as an equipment standard. Second, having a calibrated source voltage available in the equipment allows an accurate check of all power supplies that use that same voltage. By use of a selection switch (S1 in figure 2-31), any or all units can be tested rapidly.

Calibration adjustments. Figure 2-32 shows an application of potentiometers. R17 is a 7.5K potentiometer connected as a rheostat. It can, by variation, change the output voltage for the full range of the 7.5K potentiometer because when the wiper arm is at point "a," the full resistance is in the circuit. If the wiper is moved to point "b," then all of the resistance is removed from the circuit. R2 in figure 2-32 is a 2.5K potentiometer used to pick off a portion of the voltage, depending upon its position. R2 and R17 combine to make a voltage divider.

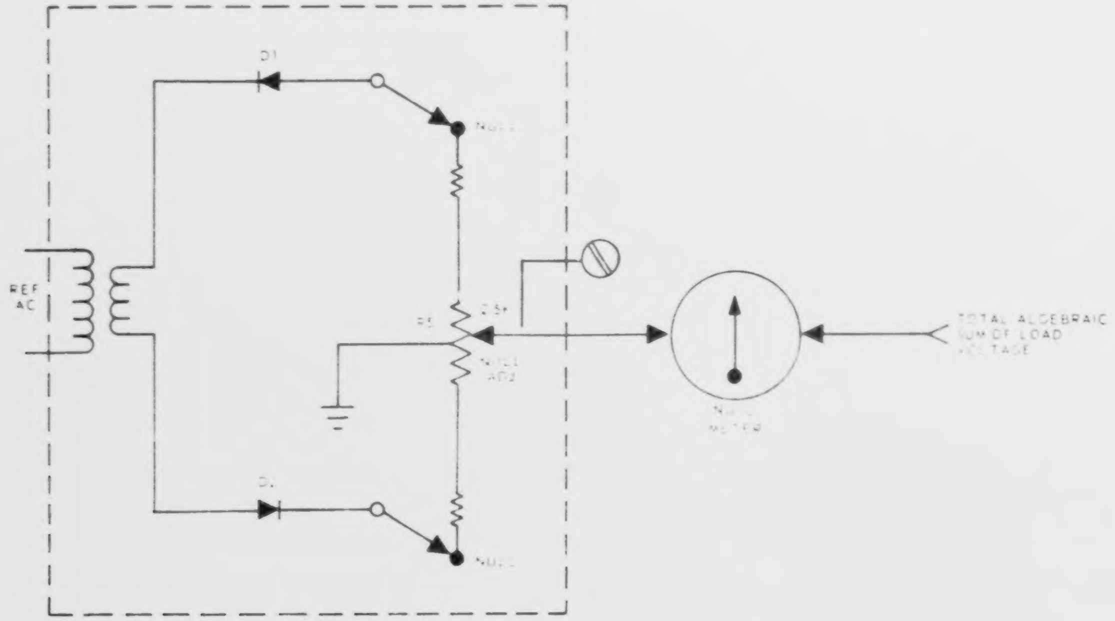

D1
NULL
REF AC
R5
NULL ADJ
NULL METER
TOTAL ALGEBRAIC SUM OF LOAD VOLTAGE
NULL

Figure 2-33. Null adjustment.

By plugging in a differential voltmeter and setting it for the exact output voltage, adjustment of R2 and R17 can provide an output that can act as the standard.

Null adjust. In figure 2-33, the null adjustment pot incorporates a center tap pot and, in this application, the center tap is grounded. The variable control then has the ability because of the conduction of diodes D1 and D2. The *pickoff* voltage is matched against the algebraic sum of the load voltages of the power supply under test.

Finally, the power supply under test is adjusted to the calibrated voltage power supply. This is done by switching to the read position, as shown in figure 2-31, and the power supply voltage under test is fed to the meter. If deflection occurs out of the limits prescribed in the TO, adjustment of the pot for that supply increases or decreases the voltage to the null meter and effectively calibrates the power supply to the preset calibrated value.

The examples of centering and null adjusting begin to identify the versatility of the potentiometer. Each example shows how the pot acts as a resistance factor and that the wiper arm selects a voltage proportional to its position. You can see that meters and dials require the use of potentiometer adjustments and screws to prepare them for use as measuring devices, just as amplifiers and pulse generators need them for amplification and bias control.

Exercises (419):

1. Which adjustment is made to a meter or dial with voltage removed?

2. How is a meter balanced?

3. What adjustment is made to a meter with voltage applied?

4. How is a meter centered?

5. What condition is indicated if a meter needle is in the null position of a differentiating measuring circuit?

420. Provide the purposes of variable components in amplifiers and pulse generators and pinpoint significant output and other adjustments in amplifiers and pulse generators.

Amplifier and Pulse Generator Adjustments. In many cases, amplifiers and pulse generators incorporate variable components. The primary purposes of variable components in these circuits are (1) to alter the gain ratio of the circuit, (2) to control the pulse duration, or (3) to act as a phase-shifting device. To understand these uses of the pot or variable capacitor, examine the basic amplifier and relate its principles to some of the more complex circuits.

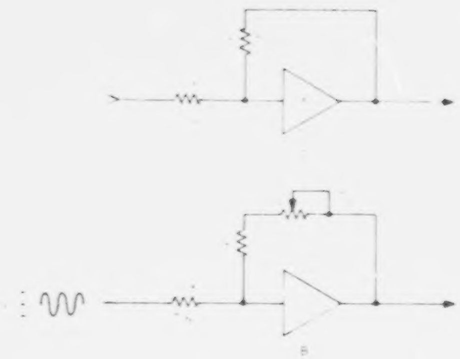


Figure 2-34. Operational amplifier.

Operational amplifiers. An operational amplifier is a circuit consisting of three basic parts: (1) an input resistance, (2) a high-gain amplifier, and (3) a feedback resistance. Refer here to figure 2-34,A, and note that R_{in} is the input resistance and has an assigned value of 100K. Therefore, the circuit has a gain of unity ($\frac{R_{fb}}{R_{in}}$ = gain). For example, a 5-volt signal into R_{in} results in a 5-volt signal output from the amplifier. Now look at figure 2-34,B. By the insertion of 10K pot, the circuit is made to provide a variable amplitude output. For example, apply a 5-volt 60-Hz signal into the amplifier to see what effect the pot will have.

First, establish the parameters of the circuit. R_{in} = 100K; R_{fb} = 100K ± R2, or 10K. Therefore, the gain of the circuit is from unity in the case where the wiper of R2 is at point A, or 10 percent where the full pot is in series with R_{fb}. With 5V peak-to-peak (PP) input and the pot at minimum, or point A, the output equals 5V PP—unity. Consider the full pot in the circuit. The feedback loop equals 110K; R_{in} = 100K. Therefore:

$$\frac{R_{fb}}{R_{in}} = \frac{110}{100} = 1.1\text{gain}$$

Therefore, 5V PP × gain of 1.1 = output of 5.5V PP, or a gain of 0.5V PP.

Based on these conditions, the maximum variation that the circuit can have is .5V PP. Change the size of any component and apply the formula, and you can obtain the maximum and minimum gain.

Miller circuits. Now, alter the basic circuit again. This time replace R_{fb} with a fixed capacitor. This simple change results in development of a Miller integrator circuit. Refer here to figure 2-35,A, and see that a rectangular wave input produces a sawtooth output. The Miller integrator is a special amplifier, using a feedback capacitor instead of a resistor. It provides a linear rising (or falling) output voltage when the input level is suddenly decreased or increased. Basically this circuit is an RC circuit with the time constant increased by the amplifier gain. Since long time constants can be obtained by using high gain, the output is very linear.

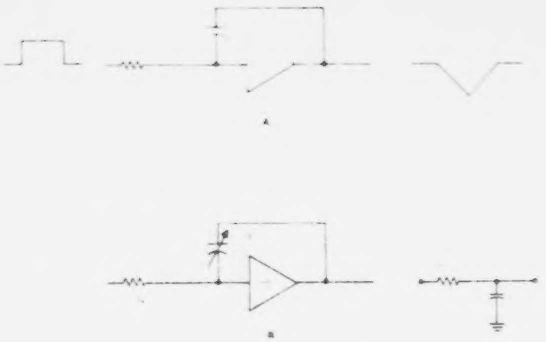


Figure 2-35. Miller circuit.

Now refer to figure 2-35,B, and see that, by replacing the fixed capacitor with a variable capacitor, the capacitor provides a capability for altering the overall time constants of the circuit. Selecting any position of the variable capacitor affects the amplitude of the output waveform since the input pulse is constant. All RC networks contain specific time constant values to charge to full potential. Therefore, if the time is restricted, as in our example, any change in capacitance results in a charge being accumulated on the capacitor for the same time duration each cycle. Study the following example:

$T = RC$

Where:

$R = 1000$
$C = 6 - 45\ \mu\text{fd}$

Therefore:

(1) $T = 1 \times 10^3 \times 6 \times 10^{-6}$
$= 6 \times 10^{-3}$
$= .006$ seconds or 6 milliseconds

or:

(2) $T = 1 \times 10^3 \times 45 \times 10^{-6}$
$= 45 \times 10^{-3}$
$= .045$ seconds or 45 milliseconds

The output waveform can be altered to have one time period for charge from 6 milliseconds to a maximum of 45 milliseconds. Now, by applying a fixed input waveform to control the output, as shown in figure 2-36, you can see that the output waveform becomes a sawtooth. Also, by studying the graph you can see that for a pulse duration of 1 millisecond:

a. The circuit with a capacitance of 6 μfd allows a charge of 20 percent before discharge begins.

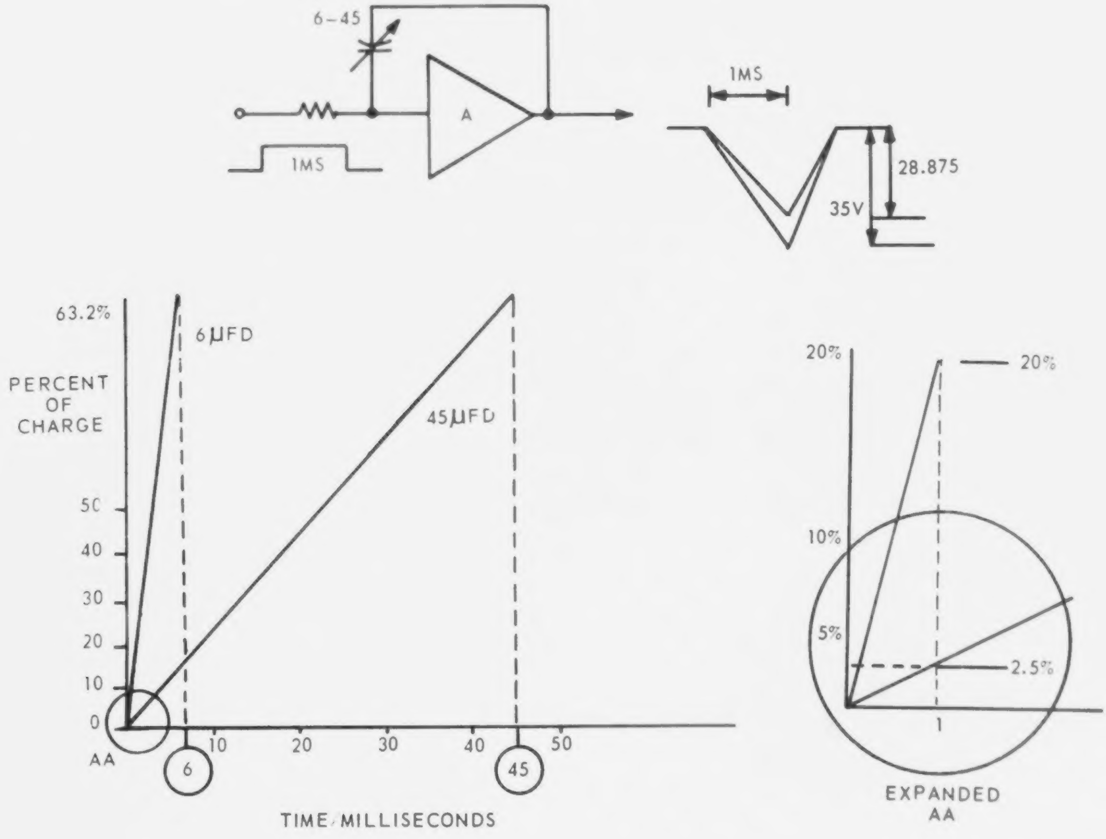


Figure 2-36. Miller circuit with variable capacitor.

b. The circuit with a capacitance of 45 μfd allows a charge of 2.5 percent before discharge begins. From these conclusions, then, the output waveform varies in amplitude, depending upon the position of the variable capacitor.

To go one step further, you can calculate the maximum and minimum points or the maximum variable gain. Assume that the output can have a maximum voltage of 35 volts with a control input gate of 1 millisecond. This would mean that the variable capacitor would have a capacitance of 6 μfd. Turning the control to the other end, or 45 μfd, decreases the amplitude 17.5 percent to 2.5 percent of charge.
Therefore:

$$17.5\% \text{ of } 35\text{V} = 6.125\text{V charge}$$

or:

$$\text{Min to max range} = 28.875\text{V to } 35\text{V}$$

Pulse generators. A pulse generator, such as a one-shot MV, single-shot MV, or monostable MV, can be designed to provide a variable pulse width output signal. Most frequently, the device used is a pot.

Use of RC time constant. The pot may be installed either in the input circuit or in the output circuit. In either case, it is usually installed in the emitter or collector circuit of a transistor MV. Its primary function is to alter the RC time constant of the circuit, thereby causing a shorter or longer decay time. This allows the circuit to provide a varied or adjustable output pulse width. Refer to figure 2-37 for an example of miniature potentiometers being used with an integrated circuit. The operation of pots R3 or R4 is very similar to the uses we have already described. Their primary function is, once again, variable control; when each is used with a 3.3K resistor and an 8-picofarad capacitor, an RC network is formed. Study figure 2-37 closely during the discussion of pots used in pulse generators.

Integrated circuit with RC pulse width control. The circuit consists of integrated units Z1 and Z2, and external to the ICs are pots R3 and R4, both 20K. Resistors R5 and R6 are 3.3K each, and capacitors C1 and C2 are 8 pfd. On each half of the IC, Z2 is a Schmitt trigger circuit. The primary function of a Schmitt trigger is to provide a rectangular waveform output whenever the input is caused to change states. If the input is a low-frequency AC signal (i.e., 60 Hz), the input circuit delays its reactions to the input until the controlling slope of the signal reaches an amplitude sufficient for the change to occur. No change in output results until the reaction occurs.

For instance, if the input waveform takes 50 μsec to rise high enough to bring the input circuit out of cutoff, the output has no reaction until the change takes place. On the other hand, if the input is rectangular and the rise time is 20 nanoseconds or faster, the output reacts almost instantaneously. Considering these factors, by examining the circuit in figure 2-37, you can see that the input AND-gate Z2A requires three high inputs on pins 1, 13, and 14, plus a high from pot R3. Since this AND-gate has pins 13 and 14 tied to +5 VDC, pin 1 causes the Schmitt trigger to start operation. R3, R5, and C1 form an RC network for pulse width control. The maximum and minimum times derived from the formula T = RC reveal these two conditions: (1) a time of 20 nanoseconds with the pot effectively removed, and (2) a time of 187 nanoseconds with the full pot in the circuit. This variable component controls the conduction times of the input circuit of the Schmitt trigger; consequently, it delays the completion of the rectangular output waveform.

The Z1A NAND-gate provides a pulse when the inputs to pins 12 and 13 are high. A negative pulse is fed to pin 1 of IC Z2 AND-gate Z2A. On the rise of the output signal from NAND-gate Z1A, the trigger is turned on, and an output is generated from the Schmitt trigger. The length or pulse width of the output pulse is dependent upon the value of the RC circuit, consisting of R3, R5, and C1. Their sizes provide a time constant value, which causes the Schmitt trigger to stay in its on state. The delay resulting effectively stretches the pulse. R4, R6, and C2 and the second Schmitt trigger unit produce the same result.

With this understanding of circuit operation,

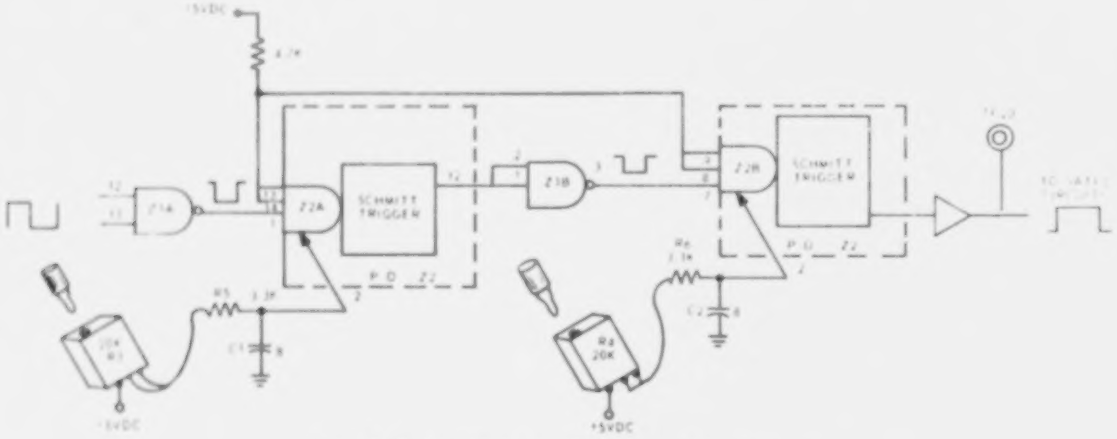


Figure 2-37. Variable pulse-width generator (Schmitt trigger).

performance of the adjustment routine shown here has these meanings:

a. Set up scope for 5V at 0.1 nanosecond—each channel.

b. Adjust trailing edge control R3 fully clockwise.

c. Adjust leading edge control R4 for maximum value (as near to 600 nanoseconds as possible) while looking at TO20 on channel 1 of the oscilloscope.

This is a primary example of the simplicity of instruction taken from a -9 (alignment) TO, and it focuses on the point of this discussion that a knowledge of circuit operation is needed if for any reason the pulse width does not measure 600 nanoseconds.

Exercises (420):

1. What are the purposes of variable components used in amplifiers and pulse generators?

2. How is the output amplitude of an operational amplifier adjusted?

3. How is the output of a Miller circuit adjusted?

4. How will an adjustment to a Miller circuit with a variable capacitor which applies a fixed waveform to control the output affect the output waveform?

5. How is the output from a variable pulse width generator altered?

6. How does an adjustment adding RC pulse width control to an integrated circuit affect both (a) the reaction of the input circuit of the Schmitt trigger and (b) the completion of the rectangular output waveform?

421. Name the devices used to adjust the power supply and tell how power supply adjustments may be made.

Power Supply Adjustments. The following four quotes from PMIs show the simplicity of power supply adjustment instructions:

Adjust power supply control R25 for a 15V ± 0.1V output.
Adjust R8 for a meter reading of −15 VDC.
Adjust the 390-VDC power supply for 390V ± .5V.
Adjust R16 for a voltmeter reading of 15 VDC.

The first and third examples reflect an exact percentage of deviation and, because they do, the use of a differential voltmeter is required. On the other hand, instructions two and four specify voltage taken from a meter installed on the power unit. The adjustment of any of these pots consists of varying the resistance to the load at the output of the supply. By varying this component, conduction in the circuit is varied and output voltage indications show the new value.

If adjustments are made using a differential meter, the output of the power supply is measured against the output of the calibrated meter and the adjustment potentiometer on the power supply provides the control.

Most regulated power supplies are complex units and require extensive study. For this discussion on adjustments, a brief review of their makeup provides the basis for understanding. The output of a regulated supply is distributed to many circuits. The output voltage is usually adjustable within limits. The output current may or may not be adjustable and visually measured; however, its value is considerable. It may be as much as 100 amps.

Low voltage. To have this much current at the low voltage required for transistor and integrated circuit operation necessitates the use of extensive front-end circuitry. Such common electronic components as silicon-controlled rectifiers, zener diodes, thermistors, and thyratron semiconductor devices are all used to provide current and voltage regulation. Filtering is accomplished by extensive use of coils, capacitors, and resistors. Finally, the source input is frequently 400 Hz instead of 60 Hz because it is easier to filter.

In figure 2-38, VR1 and VR2 are zener diodes used in conjunction with R1, a 500-ohm pot. They provide a variable +15V signal to one input of a differential amplifier. The other input (pin 4), also a +15V signal, is inverted in the first stage of the circuit. The output is regulated by developing a difference between the two inputs which, when added to the gain of the amplifier, regulates the output voltage to +15V ±0.5V. The RC network provides filtering for high frequency induced by amplification of noise. In this example, the control is included in the input circuitry. This illustration points out again the usefulness of potentiometers and the variations of their arrangement in circuits.

High voltage. Most high-voltage power supply test points and adjustment controls are isolated. Frequently, the potentiometer is connected to a voltage divider network from infinity on one end to ground on the other. The wiper arm is tied to the power supply. However, this wiper arm has a very high potential since it has a voltage equivalent to the power supply. Caution must be used because of the high voltage present, even though the controls and test points are isolated.

Exercises (421):

1. How are DC power supplies usually adjusted for precise outputs?

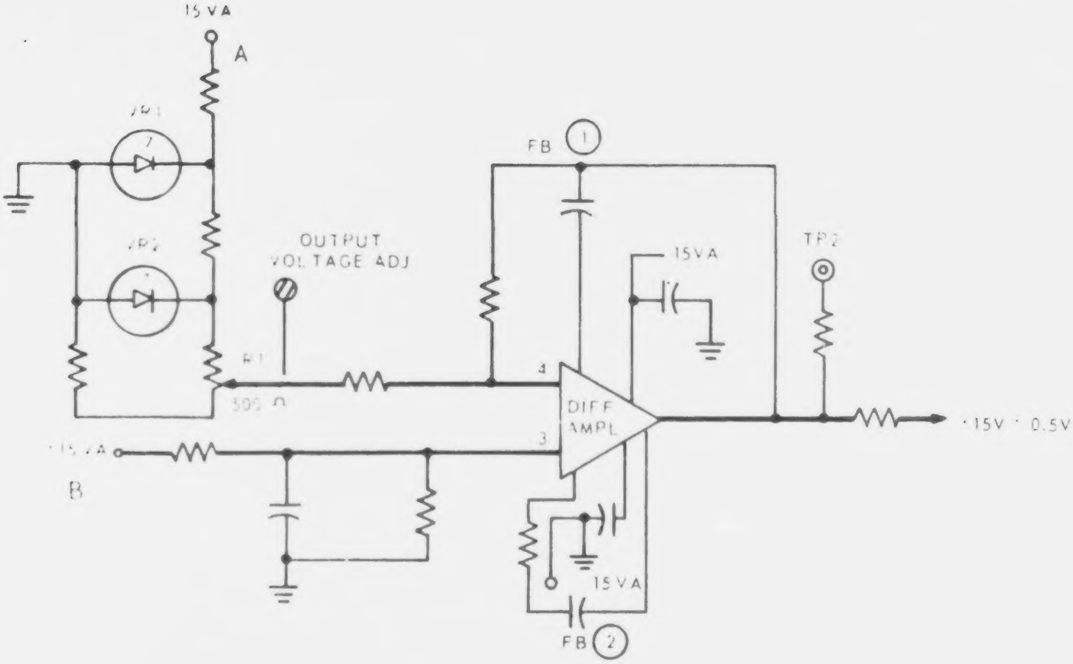


Figure 2-38. Differential amplifier voltage regulation.

2. What component devices are used to adjust power supplies?

3. How is a potentiometer often incorporated for adjustment of high-voltage power supplies?

422. Name timing circuits which may require adjustment and state the functions performed by adjustments.

Timing Adjustments. Almost without exception, timing units incorporate crystals. The extremely high stability of these solid-state structures has accounted for remarkable advancements in newer computer equipment. Many crystals are encased in ovens in order to insure proper operating frequencies. Many crystals are also cut for negative or positive coefficients that require engineering solutions. Advanced technology and manufacturing skills have provided solutions to most of industry's demand, and the result is that little maintenance of the timing units in newer computers is required. However, some of the older systems are still in use, and so you may be required to make timing adjustments.

One system uses a 3-megahertz timing reference generator. Its crystal-controlled timing generator is set by tubular capacitor adjustment to 3 MHz + 100 Hz ± 10 Hz. From this reference generator:

(1) The computer master clock (CMC) is set by the adjustable capacitor to a frequency of 3,000,100 Hz ± 10 Hz.

(2) Each slave clock (SC) is set for a frequency of 2,999,900 Hz ± 10 Hz.

(3) The memory master clock (MMC) is set for exactly 3 MHz ± 10 Hz.

With these frequency variations, it becomes easy to see that the CMC does all controlling when operative and causes the slave clocks to speed up to 3 megahertz. If the CMC clock fails, the MMC clock, which is still running faster than the slaves, causes the slaves to speed up and the system still runs at 3 megahertz. If both MMC and CMC fail, the system fails; however, the SCs are used for local testing.

One modem in the Air Force uses a crystal-controlled reference generator. This unit uses ovens for frequency stability. Its requirements are for 100 kilohertz, plus or minus 1 hertz. Adjustable trimmer capacitors (button type) are included for frequency adjustment.

Another modem used in tactical control equipment uses a crystal which is also encased in an oven. However, this crystal and the associated circuit have no frequency compensation controls. Its crystals are cut to oscillate at 10.36 MHz and 1.0752 MHz. The crystals feed frequency dividers, which are manufactured with variable pulse width and amplitude resistive controls.

In addition to central or master timing, many other timing circuits are used. Some of these are:

- Free-running oscillators.
- One-shot multivibrators (MV).
- Blocking oscillators.
- Time-sharing generators.

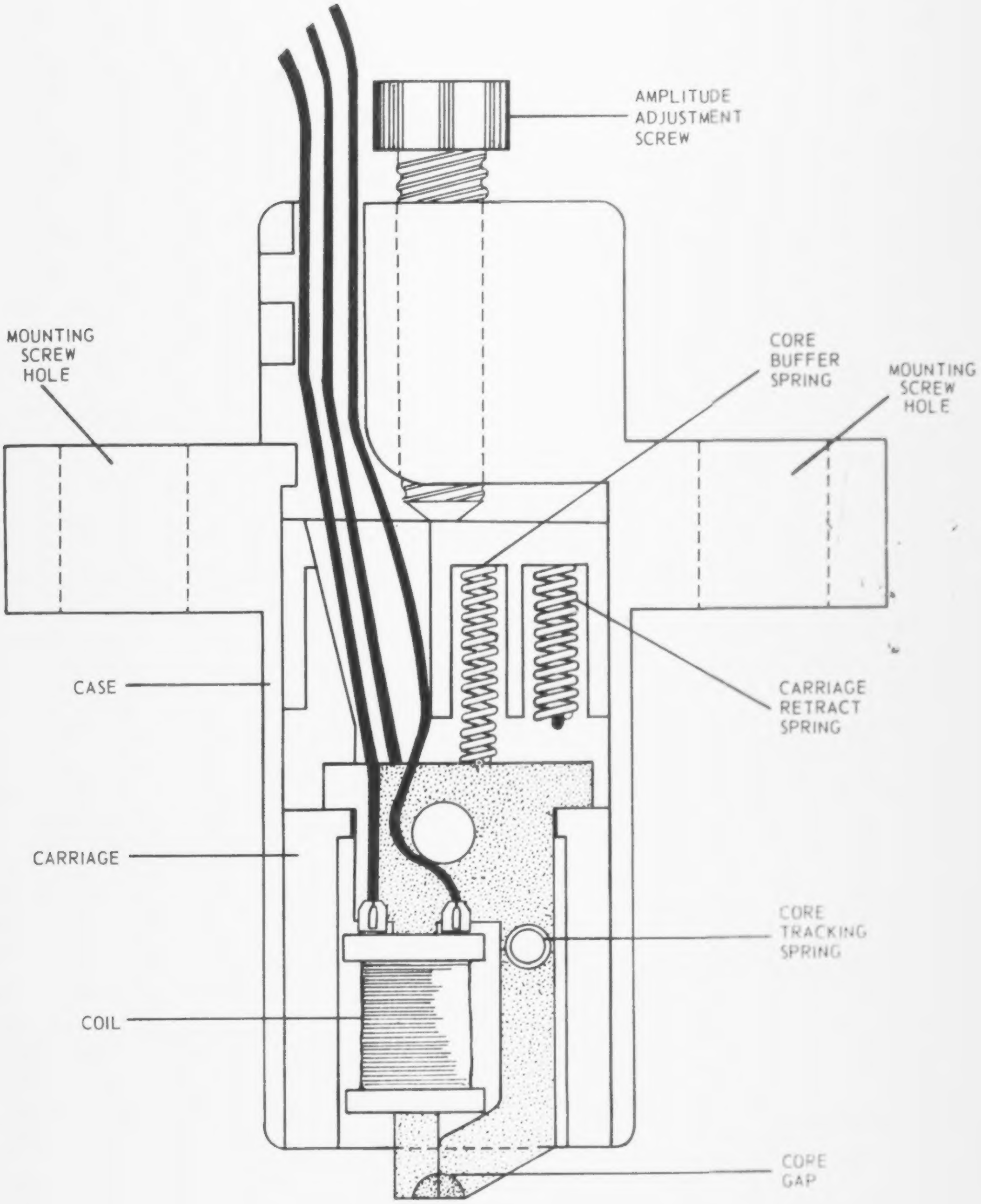

AMPLITUDE ADJUSTMENT SCREW
MOUNTING SCREW HOLE
CORE BUFFER SPRING
MOUNTING SCREW HOLE
CASE
CARRIAGE RETRACT SPRING
CARRIAGE
CORE TRACKING SPRING
COIL
CORE GAP

Figure 2-39. Read/write head.

- Automatic gate length (AGL) generator for use with radar returns.

In each case, a variable control is usually incorporated, and frequently it is resistive, used for control of voltage amplitude.

Let's look at the facts we have covered so far. First, variable capacitors of both the button and the tubular type are used for controlling frequency. Normally they are found in circuits used for master timing, and they are often found in display timing units. Second, resistive variable controls in master timing units are usually in the output for amplitude control. They are also used in other timing circuits to control pulse width, pulse repetition rates, and amplitude.

Timing adjustments fall into two broad categories:

- The frequency adjustment of a crystal-controlled oscillator.
- The adjustment of a duty cycle.

The frequency adjustment is made with a frequency counter connected externally to the oscillator output. The frequency control is adjusted until the counter reads the precise value of the performance standard.

The duty cycle adjustment is usually measured on an oscilloscope. A basic reference pulse is usually displayed on either A or B trace, and the waveform of the circuit to be adjusted is displayed on the other trace. Calibration of the waveform is performed and adjustment of the duty cycle is performed by altering the variable component in the circuit under measurement. If an amplitude variable is included, the instructions usually specify the amplitude plus or minus a specified deviation.

Exercises (422):

1. What in the system with a 3-MHz timing reference generator does all controlling when operative and needs frequency adjustment when inoperative?

2. Name some types of timing circuits which make use of variable components.

3. What two functions are performed by timing adjustments?

423. Indicate mechanical and electrical adjustments associated with storage devices and detail what is accomplished, or how, by particular adjustments.

We examine here storage device adjustments, mechanical adjustment principles, and electrical adjustment principles, together with their subareas.

Storage Device Adjustments. The adjustments performed are divided into two separate, significantly different subtasks. One is mechanical adjustment and the other is electrical adjustment using an electronic component. One might say that any adjustment, even a pot, is mechanical, and in the truest sense, this is correct. In this study, however, mechanical adjustment indicates the physical altering of components to specific distance, even though the distance is measured in voltage amplitudes. Electrical adjustment is construed to mean a variation of a pot or capacitor to provide a standard waveform or level.

Based on these premises, mechanical adjustment can be readily associated with drum systems, tape systems, and disk systems, since each has the same principle of depositing data and extracting data through a magnetic head. The electrical adjustments can be associated with the systems listed above and also with core systems, thin film, electrostatic storage tube systems, delay line storage systems, and some integrated circuit storage systems.

Mechanical Adjustment Principles. The *drum storage device* consists of many channels, and each channel has read/write heads and, usually, an erase bar. Each head is secured to a frame that is designed to place the head very close to the drum surface.

Drum head. Refer to figure 2-39 as we proceed. The assembly is approximately $1\frac{1}{4}$ inches wide by $\frac{3}{8}$ inch thick. It contains two mounting screw holes on the flanges and internal coil, the heart of the unit. The amplitude adjustment screw allows the carriage to move up or down, closer to or farther away from the drum surface. The adjustment routines require that data in the form of a binary ONE be written onto the drum channel being adjusted. The pulse is measured on a dual-trace oscilloscope, with one trace measuring the input waveform and the other trace measuring the output waveform. A typical adjustment requires that an output voltage be measured at 125 to 150 millivolts peak to

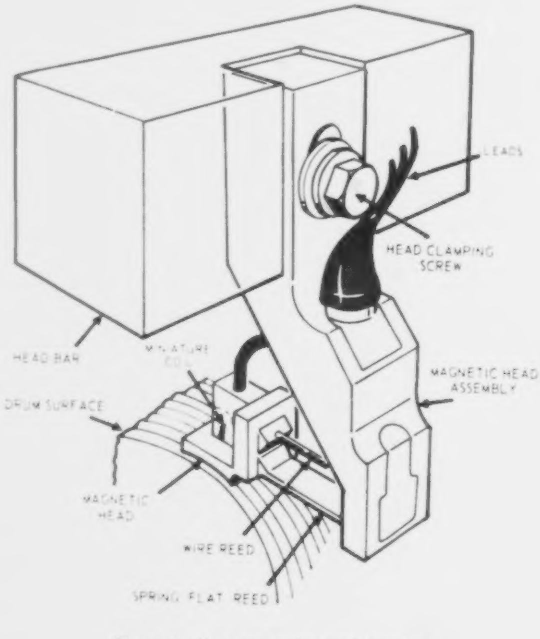


Figure 2-40. Read/write head installed.

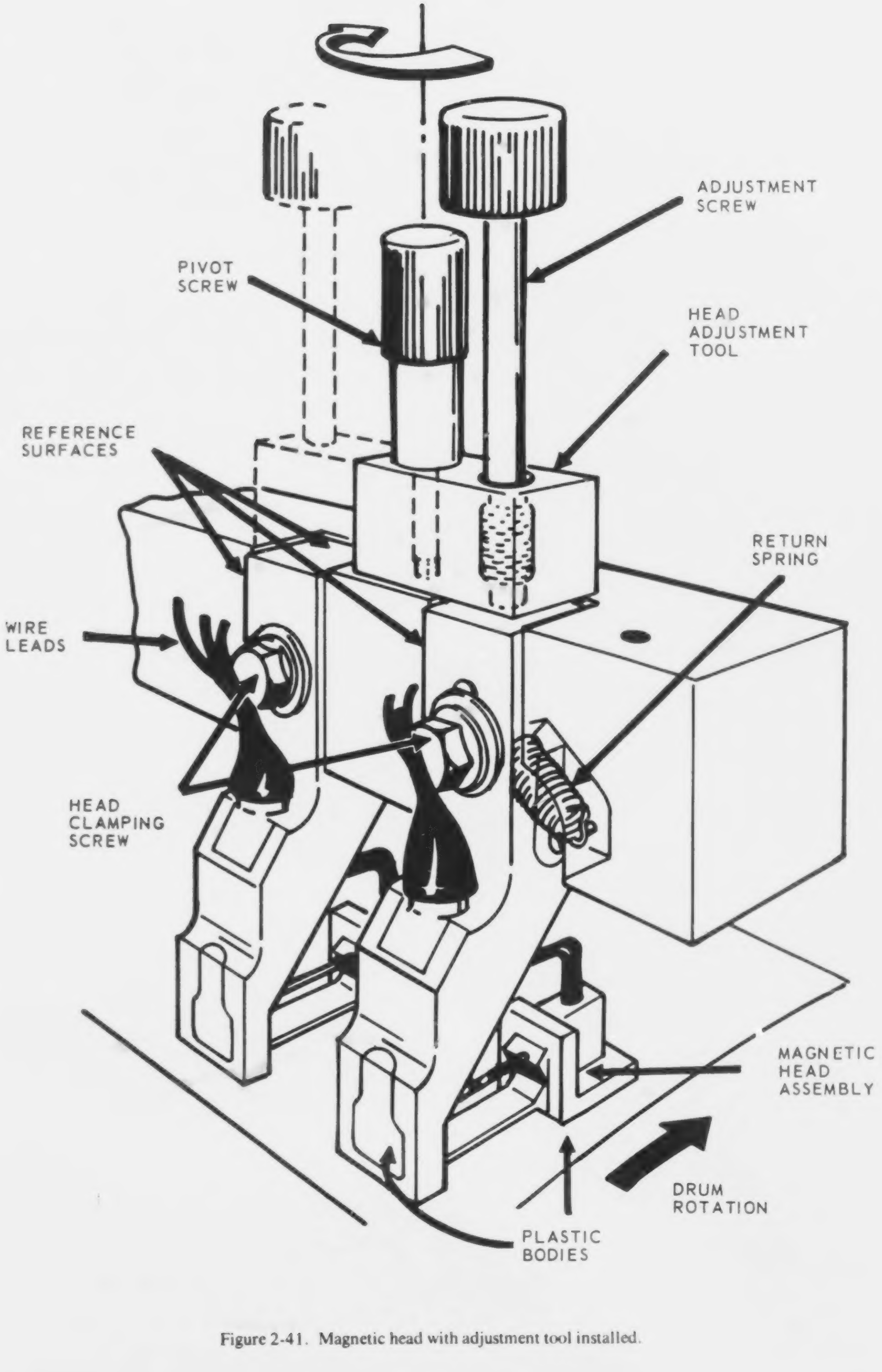

ADJUSTMENT SCREW
PIVOT SCREW
HEAD ADJUSTMENT TOOL
REFERENCE SURFACES
RETURN SPRING
WIRE LEADS
HEAD CLAMPING SCREW
MAGNETIC HEAD ASSEMBLY
DRUM ROTATION
PLASTIC BODIES

Figure 2-41. Magnetic head with adjustment tool installed.

peak. The steps to arrive at this voltage output are such that the head is lowered to the stopped drum surface and then raised until 75 percent of the voltage waveform is displayed on the scope.

Years of progress and advanced technology have brought simplification to the drum head units, as shown in figure 2-40. This read/write head is smaller and simpler than those used previously and uses spring steel (spring flat reed) to hold the recording head near the drum. It incorporates a miniature coil that is approximately 1/8 inch square. The techniques for adjustment are similar to those for adjusting the older models in that a binary ONE is written into the channel and the readout voltage is measured while adjustment is being made. Special tools are required to adjust this system. The pivot screw, shown on the left in figure 2-41, secures the adjustment tool to the head mounting bar, and the adjustment screw controls the positioning of the head. When the head clamping screw is tightened, the task is complete.

Tape drive. On tape drive systems, mechanical adjustments are usually associated with the drive mechanism rather than with the heads. Most heads are installed in a metal container and are recessed from the outer surface of the container 3/1000th to 7/1000th of an inch, thereby providing the required gap for magnetizing the tape. One tape system uses shims to raise the tape .003 to .005 inch from the tape head.

Mechanical adjustments vary in accordance with the design features; however, they are common in that the proper drive speed, stop, start, and tension must be maintained.

On the tape drive units, a pinch roller is adjusted by use of shims, and so is the brake. The vacuum pump adjustment is made so that the water gauge shows a reading of 40 inches, plus or minus 5 inches. Also, adjustments are made on belt-driven assemblies at the time that corrective maintenance is performed. They involve the driven capstan, vacuum pump motors, and rewind motors.

Delay line. The magnetorestrictive delay line storage system incorporates a mechanical adjustment device, tunable to a precise position. The principle of storage with this device is shown in figure 2-42. A silver wire is used as the storage element, with approximately the last 16 microseconds variable. Current in the form of a short duration pulse is entered into the wire at one end. It travels down the wire at the rate of approximately 1100 feet per second. Since its rate of travel is linear, the selection of a precise length then identifies two facts: (1) The time delay of the pulse is known by the length of the wire times the rate of travel; and (2) if the pulse (data bit) occupies a precise measurement of length along the wire, a specific number of data bits or words may be stored. Access to data at the output is sequential, and any selected data can be sampled if its entry time and the total length of the storage line are known. The adjustment of the last few microseconds becomes a critical factor, and precise timing is necessary. Two methods are used for making the adjustments. First, an oscilloscope using two traces may be used. On one trace the input pulse is shown; on the other trace the output pulse is shown. Since these are the same pulse, the measurement of time between input and output reveals the delay or storage time. Adjustment can be made to display a precise known delay storage time. The second method is performed by using a test setup designed and built for adjusting these storage devices. The principle used there is that switches program the tester's internal circuits, thereby providing pulses and measuring pulses at specific times. The pulses are then displayed by use of neon lights. The first light to come on is interpreted as that a close setting has been achieved, and the second light indicates an exact setting.

Disk memory. The disk memory system is related to the juke box in that the disk rotates and the heads are placed above and below the recording disk. Figure 2-43 shows a cutaway view of a disk memory unit. As is true with other storage devices using magnetic recording, there are mechanical and electrical adjustments. The mechanical head assemblies are adjusted by screws installed in pivot arms. These are shown in the breakout of figure 2-43. The heads are adjusted with shims and the use of a micrometer. Looking at figure 2-43, you can see that the heads are placed in various positions around the disk. Examine callout 1 of figure 2-43 and you will see that the head bar has an adjustment called a *pivot screw*. The head bar is shown more clearly in callout 2 of figure 2-43. Once again, extensive use of mechanical adjustment is made on storage devices.

Electrical Adjustment Principles. Current is required to write a ONE into a storage device, and all systems use drivers to accomplish this. The current is almost always the result of a decoding action of data. A binary ONE will usually cause a circuit action, which converts the digital ONE into a current pulse of proper polarity for use in a magnetic storage medium. The device most generally used is the write amplifier.

Read/write amplifier. Most systems use write amplifiers and read amplifiers. These amplifiers usually have potentiometers installed for fine adjustment. They may be current limiting or voltage limiting, or both. They are usually adjusted to specifications as performance routines. It's been revealed that all tape storage units have either a read amplifier or a write amplifier adjustment pot, but some drum storage systems have neither. One drum system uses a current-limiting memory protection circuit with adjustment pots to regulate the current requirements for the entire drum unit.

Thin film circuit. Thin film memory systems provide a nondestructive readout after storage of data. This is done by reading a current amplitude of slightly less than switching current or hard state, as is shown in figure 2-44. The adjustments associated with this memory system are made on the read/write amplifier units. Coincidence of two pulses is required to provide the switching current necessary for storage of data.

The principle for write needs a coincident address current plus a write current sufficient to cause switching. To read requires a coincident current, but one that is not high enough in amplitude to cause switching. The diagonal dashed line shown in figure 2-44 is the read value for either a ONE or a ZERO.

Storage tube. The electrostatic storage tube is a device

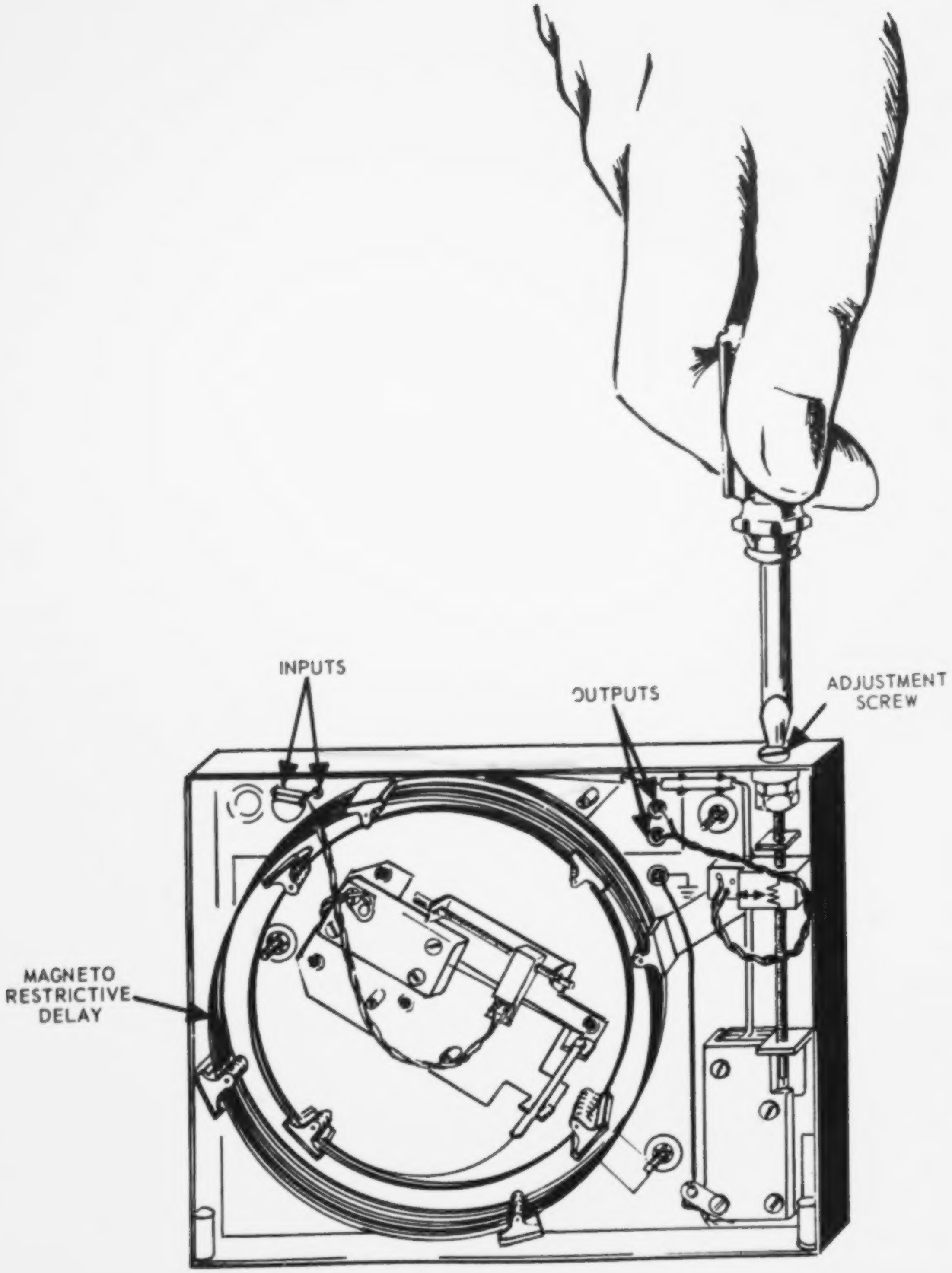

INPUTS
OUTPUTS
ADJUSTMENT SCREW
MAGNETO RESTRICTIVE DELAY

Figure 2-42. Magnetorestrictive delay line.

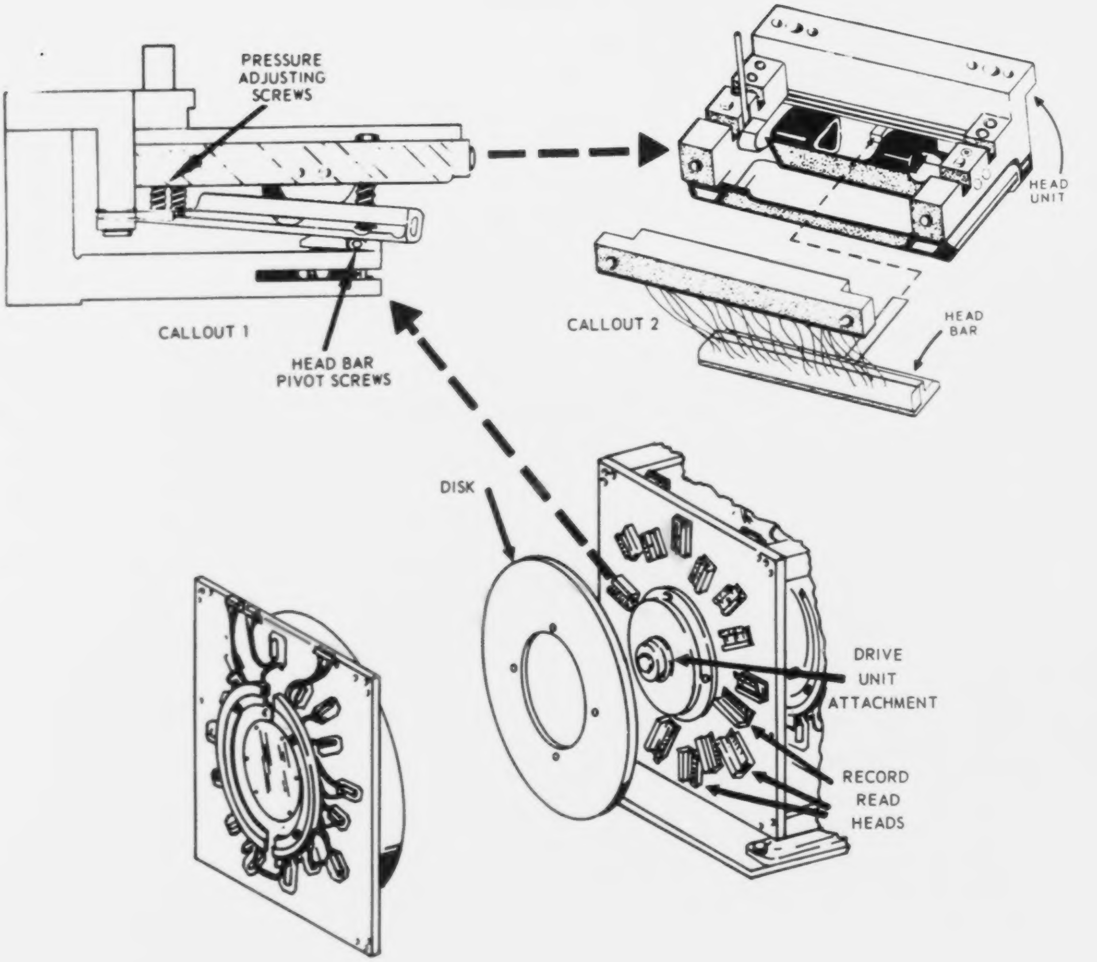


Figure 2-43. Disk memory.

using a modified CRT to allow operators to view its stored data. You may use variations of this tube. One is called the *memoscope*. The principle of operation is shown in figure 2-45. Data is written by the high-velocity write gun through the collector screen onto the storage screen. The flood guns scan the screen and every point on the storage screen where data is present (+ voltage). The flood voltage penetrates and illuminates the CRT phospher. As is true in drums and core storage, the applied voltage and current are controlled by pots. They control scanning, unblanking, video data levels, flood gun intensity, and storage and collector screen erase.

Integrated circuit display (CRT). One system previously using the storage tube had the circuit redesigned to use a simpler more modern design. Foldout 1 (bound at the back of this volume) shows a view of the control panel, including all of the potentiometers; a view of the CRT and integrated circuit packages; and logic and circuit diagrams. The simplified circuit eliminated the storage scope with its six mechanical centering controls for pitch and yaw, its eight stepping voltage adjustments (four for horizontal and four for vertical), and its two intensity controls. The new system operates on a principle of storing the data to be displayed in a recycling storage buffer (not shown in foldout 1). The data from the buffer programs the memory IC storage, shown in foldout 1,B, which provides an output to digital-to-analog converters 1 and 2, shown in foldout 1,D. The character voltage from the D/A converter is added to a vertical and horizontal stepping voltage, and these voltages are applied to the defection plates. During intensity time, the character is painted. The controls, all pots, adjust for the following, as shown in foldout 1,A:

- Character width and height.
- Position vertical and horizontal.
- Character spacing vertical and horizontal.
- Intensity.

Let's study foldout 1,A, the alignment panel of the digital informational displays (DID) unit. The upper third contains three potentiometers, all contained in a serial voltage divider network with one end tied to source voltage +13 volts and the other end to ground. Tracing

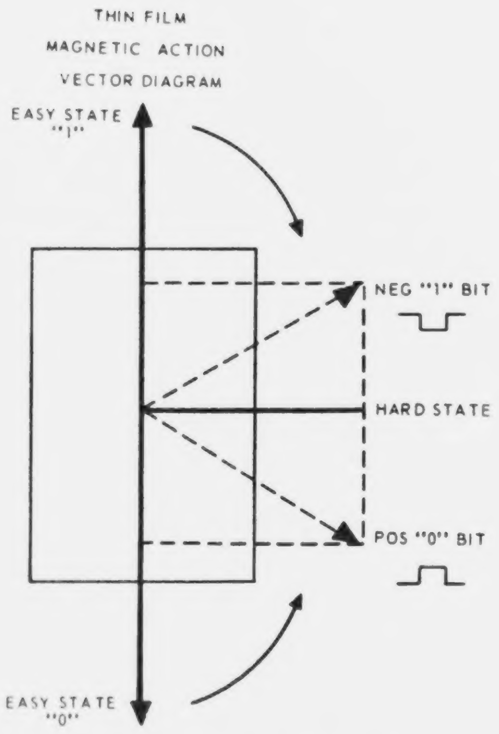


Figure 2-44. Vector diagram thin film memory.

back to its use, each wiper arm feeds to the D/A converter board. R11, vertical gain, feeds to an amplifier (shown in 2 of the D/A converter, D) to the high-order bits decoder. The symbols shown are really transistors acting as switches. The output voltage of the high-order bits is determined by the binary count input. It may be 0 through 15. Each count biases one or more of the transistors and the algebraic sum of the four, plus or minus the variable gain of R11, though the amplifier provides a deflection voltage for the vertical deflection plates. The unit is capable of providing 16 stepping voltages; however, if you look at foldout 1,C, you will see that only 10 vertical positions are used.

The next in the series of pots is the character height pot. It allows the increase and decrease of the vertical size of the individual characters. The voltage from the pot is fed to the lower order bits decoder. The variation in size, therefore, is restricted by the allowable parameter of the decoder.

The third control (vertical position) voltage is fed to the differential amplifier. This control determines when the difference output occurs. It does not alter the character size. It provides a control for positioning the characters in a particular position on the CRT.

To show you the effects of the pot as displayed on the CRT, look at callouts 1, 2, and 3 of foldout 1,C. Callout 1, the vertical gain, alters the stepping voltage to the plates. Therefore, it provides more or less stepping voltage and causes the display to vary as shown. Callout 2, the character height pot, controls the size of the character within the space allotted for the character. The difference in size is shown in callout 2 of foldout 1,C. Callout 3, the vertical position control, moves the display up and down, as shown in foldout 1,C, but it does not affect the size.

Returning again to the schematic of the alignment panel (foldout 1,A), the upper shaded area of the panel shows a similar arrangement for the horizontal control of characters. Notice, though, that R5 is 2.5K ohm, whereas R11 in the vertical unit was 1K ohm. The additional variable resistance is provided because the display is wider across than down and more stepping voltages (16) are generated. The controls provide the same functions as the vertical controls do.

The right side of the alignment panel (foldout 1,A) shows a bezel (rim) light control knob and, more important, an intensity amplitude control for overall brightness of the CRT display.

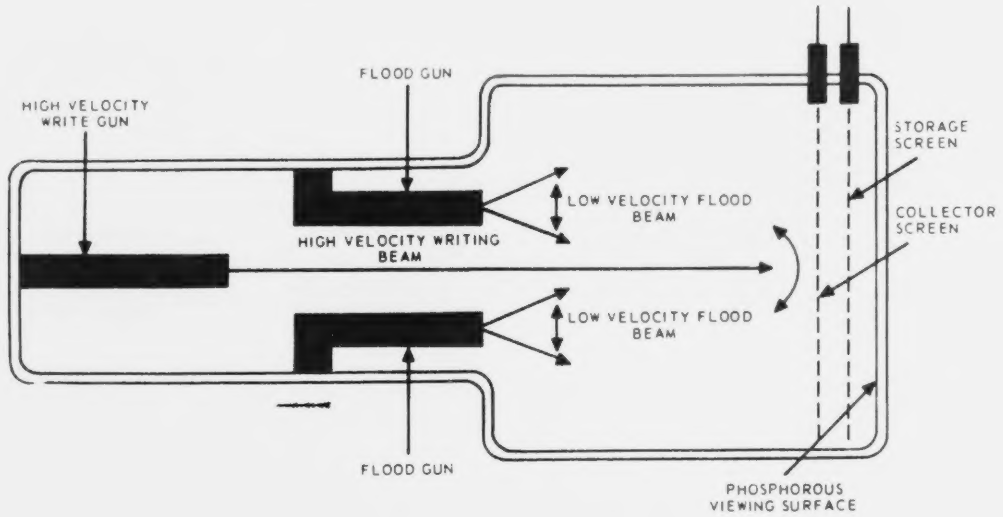


Figure 2-45. Electrostatic storage tube.

Exercises (423):

1. What types of storage devices require mechanical adjustments as defined in this text?

2. How are head adjustments performed for drum, tape, and disk systems?

3. Cite the typical mechanical adjustment routine steps by which a drum head's amplitude adjustment screw is adjusted to the required voltage waveform.

4. What do the adjustments on tape drive belt-driven assemblies involve when corrective maintenance is performed?

5. Describe briefly the first method by which the necessary precise adjustment of the last few microseconds of the delay line (magneto restrictive) storage system is accomplished?

6. In memory units containing devices that are not adjustable, what circuitry associated with the memory is usually adjustable?

7. On what units are the required adjustments associated with the thin film memory system accomplished?

8. What three basic characteristics of the display in foldout 1 are controlled by potentionmeter adjustments?

9. Consulting foldout 1 as necessary, indicate both (a) the pot related to the vertical size of individual character and, as regards adjustments, (b) how the variation on size is restricted.

424. Cite main requirements and typical settings for certain electrical alignments.

The alignment of sweep generator circuits that is typical, and the alignment of intensity/unblanking and high voltage that is likewise typical—these are this segment's two major topics.

Typical Electrical Alignment for Sweep Circuits. Generally, the sweep alignments fall into broad categories. One is the sweep generator and the other is the centering. The sweep generator alignment is performed to bring sweep voltage amplitudes to specification. It may also prescribe specifications for pulse duration, slope angle, and proper phasing. Alignments will usually require isolation of basic sweep generators during a phase of the alignment. Prerequisites usually require verification of timing waveforms, because an improper pulse width affects the duty cycle of the sweep generator. After alignment of the sweep generator, alignment of the combining or controlling circuits usually follows. Frequently, capacitors (trimmers) are used in the controlling circuits to compensate for variables in the operation of these circuits. This allows for a proper overall display.

The centering alignments usually require the use of meters and isolation of the sweep driver circuits. Voltages, sometimes DC and sometimes AC, are read simultaneously while individual adjustments are performed. When both meters read the same voltages within tolerable allowances, centering is complete. It may be necessary to consider the front panel horizontal and vertical positions of these controls. If they are included while centering is performed, their positions must be at the 50-percent point within the control. This allows for operator positioning of the sweep in all possible directions equally. In addition to sweep and centering alignments, intensity and high-voltage alignments are performed.

Electrical Alignment of Intensity/Unblanking and High Voltage. Intensity and unblanking circuits contain pots and trimmers. The pots usually control amplitudes of different gate outputs that cause more or less intensification on the CRT. Each gate amplitude ultimately results in bias control for succeeding circuits and the CRT. Video and data are usually imposed on top of the intensity gate. Therefore, the gate amplitude must be high enough for proper intensification, but low enough for the video data to cause a further intensification of this display.

Trimmer capacitors, used in aligning these circuits, provide two functions. First, they allow for squaring of gate waveforms (gate shaping), and second, they allow for amplitude control of high-frequency (short pulse width) data and video pulses. Generally, considerable variations in amplitude are possible when using these trimmers.

Specifications must be followed, especially when aligning gate amplitudes. Assume, for example, that the maximum signal into a high-voltage coupler is 15V and that the CRT turn-on voltage is 7V. If an adjustment within the alignment is performed and the gate level is set incorrectly at 12V, the conduction of electron flow within the CRT will be almost maximum (extremely high intensity). Add data or video to the top of the gate (amplitude 5V), and clipping within the high-voltage coupler (HVC) occurs.

The video or data displayed would be hard to see because of the clipping action. However, with proper alignment, a 5V gate and a 5V data or video pulse can pass through the HVC to the CRT without clipping and cause a display with a good contrast (signal-to-noise) ratio.

Focus and other high-voltage controls mainly consist of pots. These may, however, be alignment controls on circuits using the high voltage that compensate for ripple. Some of these circuits are the high-voltage coupler and focus compensation circuits, which correct the focus at the extreme edges of the CRT.

To recap, alignment of intensity/unblanking and high voltage includes the following:

- Pulse width (duty cycle) control.
- Pulse shaping (squaring) control.
- Amplitude (gate, levels, and data) controls.
- Focus controls.
- High-voltage controls.

Exercises (424):

1. What are the three main requirements for alignment of intensity and unblanking circuits?

2. What two settings are usually required when aligning a high-voltage power supply?

425. State the objectives and indicate requirements of typical alignments to electromechanical devices.

The three main topics discussed in this unit are electromagnetic alignments, servo alignments, and keyboard-printer-punch space alignment. A number of subareas are covered as we proceed.

Electromechanical Alignments. For the discussion of alignment on electromechanical devices, only two examples are provided. These are aligning a servo unit and aligning part of a printer. The principles of understanding an alignment in this area are unique in that, in addition to normal electronics, some mechanical changes occur. Electronic pulses (voltages or currents) are converted into mechanical actions or work, or mechanical actions are converted into electronic data (voltage or current). One sample examines the alignment of a servo unit which converts two positional data messages into a vector voltage magnitude. The vector voltage causes actions further on in two forms: (1) the electronic displacement of sweep voltages to a display unit, and (2) the conversion to mechanical readout unit through a chopper unit. The other example presents a representative selection of an alignment of a mechanical element in a printer. Keyboards, card readers, punches, tape units, and printers fall into a classification with electromechanical devices. Therefore, the discussion on the printer alignment can also provide an example for analysis of alignments on these other devices. The interaction of mechanical and electrical assemblies is closely related in all units.

Servo Unit Alignment. In aligning the range servo unit, the purpose or objective is to measure and adjust individual controls to specifications in order to allow for the generation of voltages through coupling by mechanical means for positioning the displays on a console. The purpose clearly states that all adjustments must be aligned to specifications in order to provide an overall alignment of the servo unit. It also indicates that mechanical coupling is involved in the servo unit. This shows that feedback positioning, although measured in voltage form, is performed by mechanical means. The title indicates that range data (X and Y) are involved. Therefore, feedback voltages from resolvers are to be included in the analysis.

Figure 2-46 shows a simplified block diagram of a servo unit. It shows an input unit, an amplifier chain, a servomotor unit, a feedback pickoff device (which can be electrically or mechanically linked), a nulling device or point, a rate feedback, and a power source. In the example given in this text, the feedback is primarily electrical through mechanical coupling from the drive motor.

Nulling. Servoloops operate on the principle of so positioning a feedback pickoff device that the feedback voltage can be summed with the input signal to produce a

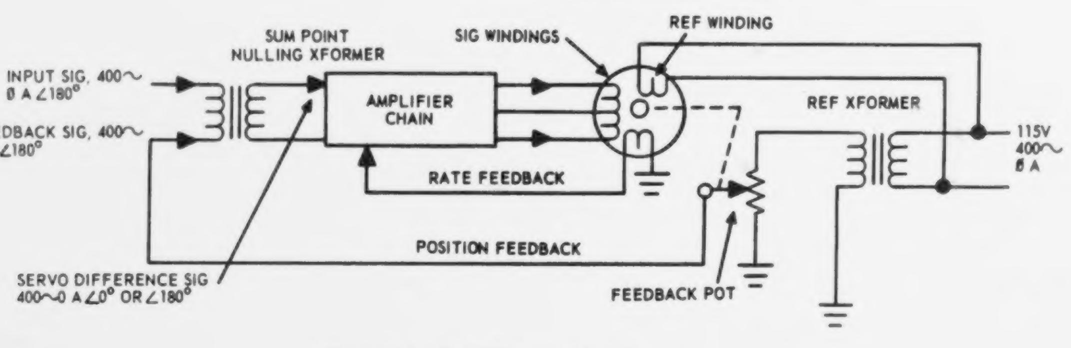

SERVOMOTOR
SUM POINT NULLING XFORMER
SIG WINDINGS
REF WINDING
INPUT SIG, 400~ Ø A ∠180°
FEEDBACK SIG, 400~ Ø A ∠180°
AMPLIFIER CHAIN
REF XFORMER
115V 400~ Ø A
RATE FEEDBACK
POSITION FEEDBACK
SERVO DIFFERENCE SIG 400~0 A ∠0° OR ∠180°
FEEDBACK POT

Figure 2-46. Simplified servo block diagram.

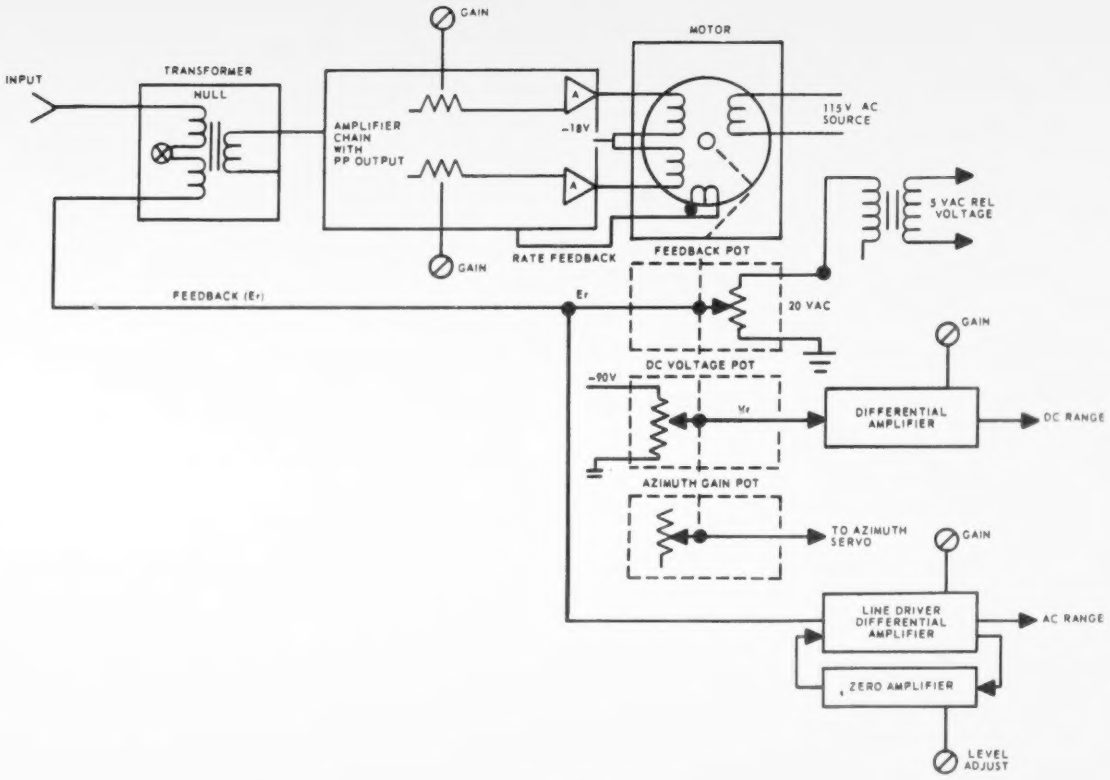

GAIN
MOTOR
INPUT
TRANSFORMER
NULL
AMPLIFIER CHAIN WITH PP OUTPUT
A
-18V
A
115 V AC SOURCE
5 VAC REL VOLTAGE
GAIN
RATE FEEDBACK
FEEDBACK POT
FEEDBACK (Er)
Er
20 VAC
GAIN
DC VOLTAGE POT
-90V
Vr
DIFFERENTIAL AMPLIFIER
DC RANGE
AZIMUTH GAIN POT
TO AZIMUTH SERVO
GAIN
LINE DRIVER DIFFERENTIAL AMPLIFIER
AC RANGE
ZERO AMPLIFIER
LEVEL ADJUST

Figure 2-47. Servo subelements.

null. The difference between the input and feedback signals is fed through a chain of amplifiers to the signal windings of a 2-phase 400-hertz motor. The motor also contains a reference winding, which is connected to a constant power source. For motor operation, both sets of windings must receive power, and the direction of rotation is a function of the phase relationships between the two sets of windings. Typical feedback pickoff devices are potentiometers, synchros, and resolvers. When the motor is correctly positioned, the feedback will null the input signal, leaving no further drive power to the motor signal windings. The drive motor will stop at the desired point.

Rate feedback. A refinement is present in the form of a negative rate feedback—one whose amplitude is a function of motor rate of rotation. Without this feedback, the motor would have a tendency to "coast" beyond the actual null point and would receive an acceleration in the reverse direction. This could, in turn, cause an overshoot in the reverse direction followed by another reversal, etc., which would set up a continuing oscillation. The rate feedback tends to reduce drive power as the motor picks up speed, but it gives virtually no opposition at very low speeds, such as in the immediate vicinity of the null. Therefore, it helps to eliminate oscillation or hunting without destroying null accuracy.

Direction of rotation. In the 2-phase AC motor, the direction of rotation is a function of the phase relationship between the signal and reference windings. A reversal of current direction (phase) in either, but not both, will reverse motor direction.

When the input signal changes (which should drive the servo to a new position), the difference between input and feedback signals will result in a signal either in phase or 180° out of phase with the reference signal; this will determine the direction of rotation.

It should be noted that a reversal of connections on either, but not both, sets of motor windings will reverse the current direction and, consequently, the motor direction. If these phase relationships are incorrect, the servo will drive away from the null position instead of toward it.

Using this information and figure 2-46, we see that a voltage input signal into the resolver provides a signal to the amplifier chain. The phase and amplitude of the signal cause the servomotor to rotate. The feedback is coupled to the null point. A difference value to the amplifier chain causes the motor to rotate in a direction that reduces the voltage into the amplifier chain. This action continues until the signal into the amplifier chain is reduced to null.

You must identify the subelements, circuits, and components of the unit to be aligned. Figure 2-47 illustrates these elements. They are, left to right:

a. The *input transformer,* which provides a method for coupling any difference between the input signal and feedback signal into the secondary of the transformer. If no signal is coupled, it may be assumed that the feedback voltage equals the input voltage.

b. The *amplifier chain,* which converts the single voltage input into push-pull outputs by inverting the input to one leg of the output. Two gain pots are used, one for each line. Noninverting amplifiers provide amplification of the signal to motor windings.

c. The *drive motor,* which reacts to the amplifier inputs based upon the amplitude of the signal; one signal wire is in phase and the other is 180° out of phase with the reference winding. The motor rotates, and its shaft rotates the wiper arms on three pots.

d. The *three pots. Er* is an AC pot which provides a feedback voltage for servo null and provides an AC range voltage to the console through the line driver board. *Vr* is a DC pot that is mechanically linked to the motor shaft and provides a DC range voltage through an amplifier board. The *AZ gain* pot provides a rate control to the azimuth servoloop by regulating the rate of change, depending upon the range of target data.

e. Reference voltages that are provided for the motor and for pickoff voltages for the pots.

f. The *GAMI* and *LDRI* boards that provide adjustable outputs to other functions.

Before proceeding, let's review the extent of the work involved:

- All controls are pots; therefore, they are measurable on meters as AC or DC and on oscilloscopes.
- Two gain amplifier controls are included in the amplifier chain.
- Each output circuit has a gain control.
- A level control is also included in both output circuits.
- Potentiometer controls on the assembly are mechanically positioned by the shaft of the motor.

You must establish where the data inputs are coming from and how they are interrelated.

Range voltage, as an input to the servo, is a product of digital-to-analog conversion. It is composed of two distinct and separate sources that are electronically combined in a servo unit. This brings these points into the analysis:

- Generation of X and Y data.
- Range data (X and Y coordinates).
- Digital-to-analog conversion.
- Resolver action to combine the coordinates into one range value.

Taking the reverse method of identifying the interrelated functions, you will discover that the resolver feeds the range voltage to the servo unit (refer to fig. 2-48). The resolver has two inputs: an X coordinate range voltage and a Y coordinate range voltage. These voltages (AC) are developed from the amplifier chain and digital-to-analog converter circuits from X and Y digital range data.

A review of the text on this circuitry gives us the following specifications about the interrelated functions:

a. X and Y data can be programmed by selecting the off-line test mode of operation, and a range coordinate of 64 miles is equal to the reference voltage of 5 VAC.

b. The feedback pot of the amplifier chain is 10K ohms in series with 100K ohms and is thereby limited to 10 percent. Further, since the signal is in AC in the range of 5 VAC, a 10 percent or less change is not measurable on an oscilloscope; an RMS (AC meter) is required.

From these items, we can see that a definite interrelationship of functions exists. The following prerequisites are given that now have meaning:

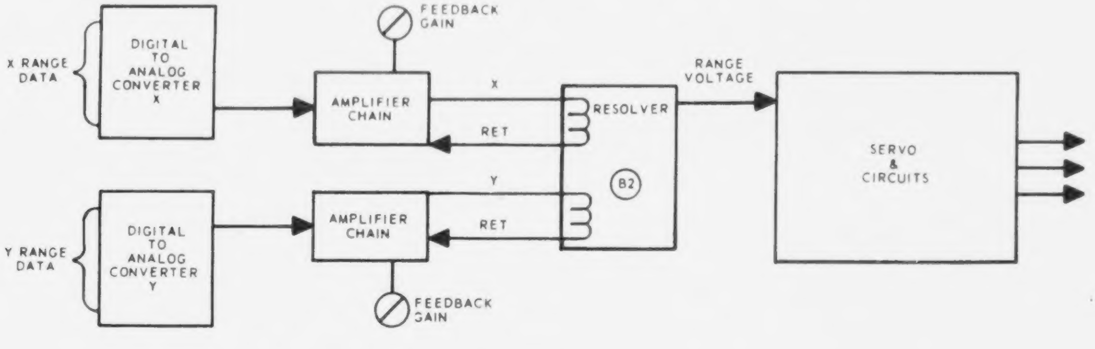
a. The alignment is performed in off-line test mode.

b. Selected switch settings are used to provide X and Y range data to the D/A converters.

c. Gain ratios of related functional amplifier chains are to be in unity.

d. Resolver B2 (part of the azimuth servo) must be properly oriented.

These four prerequisites definitely establish a sequence of operations that must be properly verified before alignment of the servo unit. At this point, we are substituting the complete pictorial of the servo and interrelated functions shown in foldout 2 (which is bound at the back of this volume). We do this now so that you can grasp the full significance of this discussion.



INTERRELATED FUNCTIONS

Figure 2-48. Interrelated functions and servo unit.

Prerequisite verification. Involved here are these steps: *Step 1:* Verify digital data. *Step 2:* Verify unity gain from the amplifier chain for both X and Y measured at AZA4XA7-6 and XA8-6 of the driver boards, respectively. *Step 3:* Verify that the output from R3 measured A2A2XA8-4 is equal to the output from the amplifier chain. This completes the verification of interrelated functions. One factor not identified here, but significant, is that for verification of R3 output to equal 64 miles, either disabling of X while measuring Y or disabling of Y while measuring X is paramount. A combination of X and Y results in a coordinate range other than 90° or 180°. *Step 4:* Requires that a sequence of alignment be established with reference to interrelated functions.

Refer then to foldout 2 and locate the test chart between the D/A converters. This chart shows test 4 with 64 miles in an X coordinate and test 5 with 64 miles in a Y coordinate.

The next phase is that of determining the sequence of functions of interrelated units. Obviously, the D/A converter and amplifier chain preceding the servo unit must be aligned properly in order to align the servo accurately. Since there are two paths, one for X and one for Y, we have a parallel situation. Either one may be aligned first. Verification of range data in binary form as inputs to the D/A converter is a prerequisite. Verification of the 5-VAC reference voltage is a prerequisite. Operation of the azimuth servo unit (since resolver B2 is a part of this unit) is a prerequisite.

Align the servo unit. Step 5 is the actual alignment of the servo unit. Two points are examined: First, a new unit is to be installed and aligned, and second, an existing unit is aligned.

a. Before installation positioning of the pots Er, Vr, and AZ gain, adjustments must be made. Using an ohmmeter, set all three pots for very close to a short: for Er, pins 2 and 3; for Vr, pins 7 and 8; and for AZ gain, pins 9 and 10. After the installation and power check, alignment is performed on zero amplifier boards A2A5XA7 and XA3, which are shown on the right-lower portion of the drawing (FO 2).

b. The remainder of the alignment is the same for either a new installation or realignment of an existing unit. Use a pure 64-mile either X or Y into the servo. Er must measure 5 VAC. With proper operation of the null point transformer, measured voltages at both test points in the servoamplifier chain are set. The output of the line driver board processing Er signal is set to a gain of unity. Finally, the GAMI board gain is set to the value of 17.24 VDC with the entire test problem 4 inserted (X and Y reference chart). The alignment is complete. All internal subunits operate properly. All interrelated functions have been identified and verified or aligned. A complete picture of the unit is presented, and an understanding of its operation, purpose, and function is clear.

Keyboard-Printer-Punch Space Alignment. Looking into alignment involving the space magnet, space pawl stop plate, and space pawl clearance here, we intend to examine the objective or purpose involved. This is threefold: First to adjust the clearance between the space pawl and the carriage rack teeth when the armature is energized. Second, to position the space magnet and armature when the armature is energized. Third, to adjust the clearance between the stop plate and the space pawl when the armature is energized. This alignment may be completely foreign to many computer technicians, because it involves mechanical alignment; therefore, we provide this brief review of the printer. In the operation of this impact printer, two characters are activated within a specific time interval (print cycle). The characters are

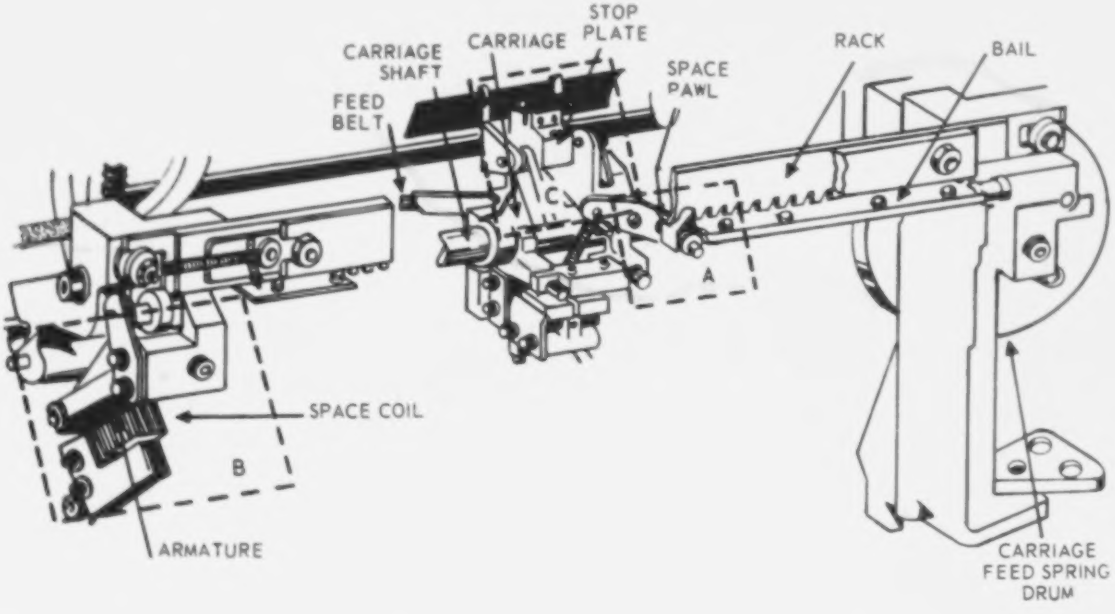


Figure 2-49. Mechanical printer carriage.

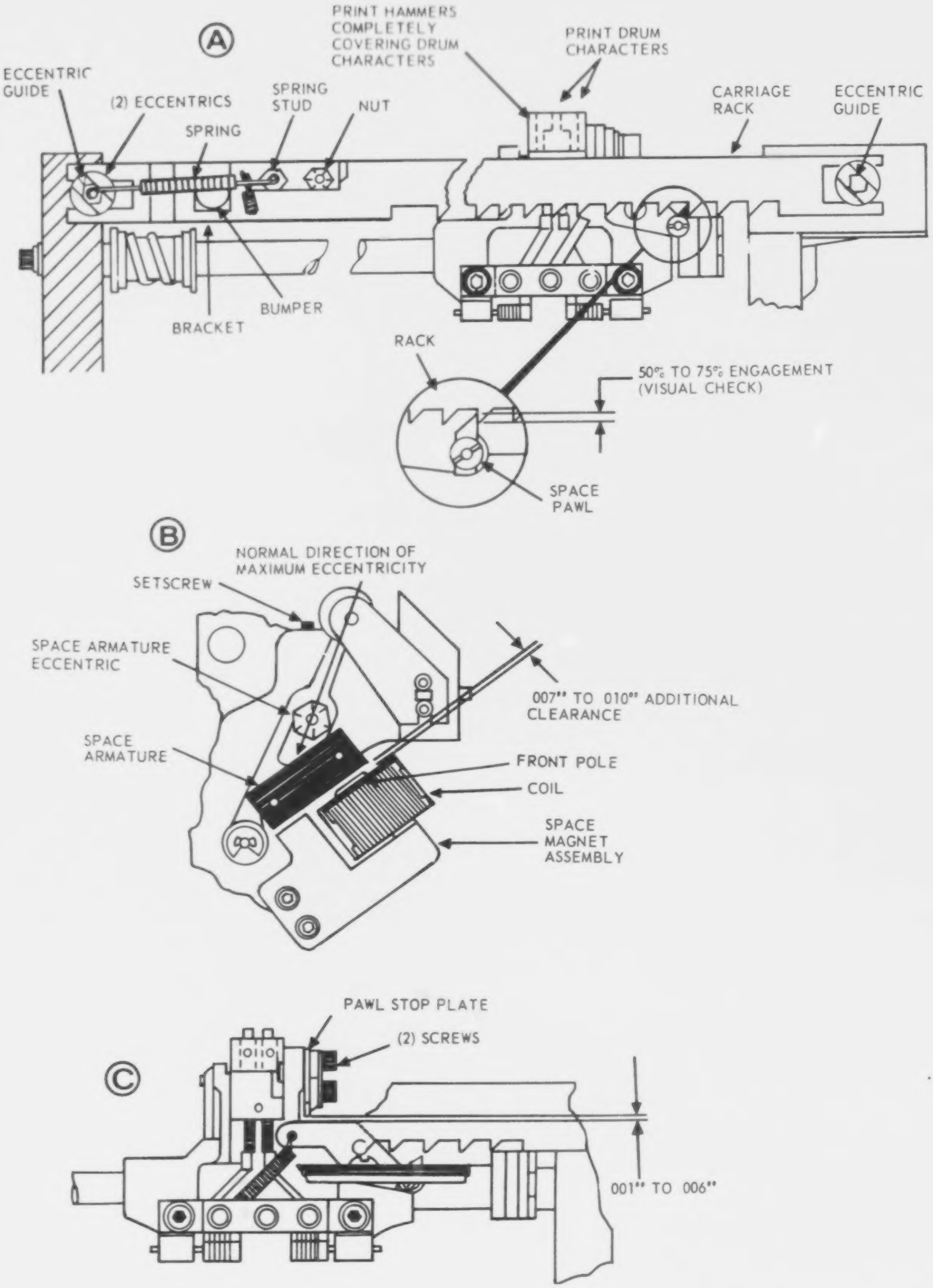

A
PRINT HAMMERS COMPLETELY COVERING DRUM CHARACTERS
PRINT DRUM CHARACTERS
ECCENTRIC GUIDE
(2) ECCENTRICS
SPRING STUD
NUT
SPRING
CARRIAGE RACK
ECCENTRIC GUIDE
BUMPER
BRACKET
RACK
50% TO 75% ENGAGEMENT (VISUAL CHECK)
SPACE PAWL
B
NORMAL DIRECTION OF MAXIMUM ECCENTRICITY
SETSCREW
SPACE ARMATURE ECCENTRIC
.007" TO .010" ADDITIONAL CLEARANCE
SPACE ARMATURE
FRONT POLE
COIL
SPACE MAGNET ASSEMBLY
PAWL STOP PLATE
(2) SCREWS
C
.001" TO .006"

Figure 2-50. Exploded view of space alignment elements.

printed on the paper by hammers. After printing the characters, the carriage is moved to the left, and the operation is repeated. A space between words is treated by the machine as a character. A rather complex mechanical assembly (shown in fig. 2-49), controlled electronically, is incorporated into the printer. The logic package provides decoding, which releases a pawl for spacing and allows a spring to pull the carriage to the next position. It is in this carriage that the alignment must be performed.

Spacing theory. An explanation of the spacing theory follows:

The spacing mechanism, shown in figure 2-50, consists of a magnet (coil), an armature, a bail, a rack, a pawl, and a carriage feed spring. The carriage feed spring exerts a constant pull to the right on the carriage. The carriage is kept from moving by the engagement of the pawl in the rack. The pawl is mounted on the carriage in a way that allows it to engage the spacing rack. When the circuit emits a space impulse, the magnet energizes and causes the armature to move down. As it does, the bail rotates counterclockwise when viewed from the left side. The bail contacts the bottom of the spacing pawl, causing the pawl to move down and out of engagement with the rack.

The magnet is held energized for approximately 4-6 milliseconds. This is just enough time to get the pawl out of engagement and allow the carriage feed spring to pull the carriage a short distance to the right. When the magnet deenergizes the mechanism is reset by the bail spring and the pawl spring.

The rack is spring-loaded to the left. When the pawl leaves engagement with it, the rack spring causes it to move toward the left. As the pawl reengages, the rack will move slightly. This slight movement is enough to absorb the energy which the carriage has built up. The rack stops against a small rubber bushing that cushions the bounce.

Two methods of spacing. Two methods result in providing ground to the space coil and thereby activating the space mechanism. These are shown in foldout 3 (bound at the back of this volume). The first method is that of depressing the *spacebar* on the keyboard. This action results in bail latches closing and generating a binary code of 0000010. This code is detected in printer logic in the *function detection* and is sent through the *function register* to the manual input of the *space circuit.* The second method is the automatic sensing of the end-of-print cycle. Since time is allocated for printing two characters before spacing, the print cycle ends with detection of both hammers fired. This action sets the automatic detection gates in the space circuitry and provides a ground to the coil.

Align the printer space elements. Refer now to figure 2-49 again, which illustrates a view of the carriage assembly and shows each of the elements of the space mechanism. To repeat them and identify each as shown, they are:

a. Magnet (labeled space coil), lower left.
b. Armature, lower left.
c. Bail, upper right.
d. Rack, upper right.
e. Pawl, upper center.
f. Carriage feed spring, lower right.
g. Stop plate, upper center.

The three objectives of this alignment are shown in the blocked-in areas. Blocked-in area A is for space pawl and carriage clearance, blocked-in area B is for the space magnet and armature, and area C is for the space pawl and stop plate. Each of the blocked areas is expanded for discussion in figure 2-50. When studying this figure, combine the use of figure 2-49 and those in blocked areas A, B, and C. Specific tolerances of individual adjustments are not included now but are listed in the final element.

Refer here to foldout 3, which illustrates the interrelationship of the adjustments to other functions. The mechanical assemblies and electronic assemblies are shown in block diagram form: the mechanical, in dash-inclosed blocks; and the electronic, in solid-line inclosed blocks.

The interrelationship serial and parallel sequence, as required, is as follows: Before the alignment of space pawl clearance, space magnet, and space pawl/stop plate adjustments, the space pawl rack clearance is accomplished. Before this alignment, space bail is positioned. Before these two alignments, space armature and shaft end play adjustments are made. This shows you that four elements are prerequisite to the alignment in this analysis in the mechanical area.

In each case of this alignment, the coil must be energized. Therefore, an electrical path is obtained through ground to energize the coil. Already identified are the two paths for obtaining ground—manual and automatic. Note in foldout 3 that R4 of the space circuit is a control in the single-shot circuitry; it provides a variable pulse width. Consideration must be given to this circuit output when operation of the printer spacing is performed. Too short a time interval may provide insufficient time for proper operation and may mislead you into adjusting space clearance. The opposite is also possible, too long a time could cause a skip or double space and again lead you astray. Farther back in the circuitry, the hammer control circuits also have pulse width controls. Improper adjustment of these may influence the spacing and cause improper selection of space timing. Finally, although this subject of troubleshooting is not included, a processing or decoding failure could lead you into realignment of these units when misalignment is actually not the cause.

For the final element, figure 2-50 provides an exploded view of areas A, B, and C, as previously noted. In each case, specifications of tolerances are included for visual acknowledgement. The routine requires:

a. Verification of input data, completion of prerequisite spacing alignments, and power.

b. Alignment instructions that identify each screw to be turned, loosened, and tightened and the final securing of screws.

Completion of the task is relatively simple. Verification of mechanical prerequisites requires use of one of the systems outlined in the first part of this section. Verification of correct pulse width of the ground enable pulse is measurable on an oscilloscope. Complete understanding, verification of prerequisites, validation of entries, and accurate alignment of the steps listed in the routine insure operational capability.

Exercises (425):

1. What does "electromechanical" imply?
2. Explain the major objective of a servo alignment routine.
3. Referring to the typical servo shown in figure 2-47, where can you expect to find the null point in servo units?
4. When adjusting servos, can you expect to find interrelationships with other units? Explain briefly.
5. What are the subelements, circuits, and unit components of the range servo unit to be aligned?
6. Alignment of a servo unit would probably call for what type of measurement equipment?
7. Range voltage input to the servo is a product of what?
8. Before alignment of the servo unit, what four prerequisites establish an operations sequence which must be verified?
9. What three steps make up prerequisite verification of interrelated functions involved in alignment?
10. Identify the threefold objective requirements in alignment involving space magnet, space pawl, stop plate, and space pawl clearance.
11. What is a common requirement of the three parts of the typical keyboard-printer-punch unit as explained in the text?
12. Identify the two methods which result in the carriage moving during spacing on the keyboard-printer-punch.
13. Using foldout 3, identify the serial and parallel interrelationship required to perform the spacing alignment.
14. Using figure 2-50, list the two-step routine involved.

CHAPTER 3

General Maintenance Techniques

THIS CHAPTER presents information for three general maintenance areas. The first area covered is equipment identification, which will enable you to properly identify units, modules, rows, etc., within the equipment you maintain. The second area covers test equipment, while the third area is an introduction to the configurations of Air Force computer and switching systems.

3-1. Equipment and Component Identification

The Air Force purchases electronic equipment from contractors. Some are items as small as a volt-ohm-milliammeter (VOM), while others are as large as an entire satellite command and control equipment complex or site installation. Numbering a VOM is simple, but numbering the parts within a satellite command and control complex with its many units, modules, sets, end items, etc., becomes a large task. To aid with this task, the American National Standards Institute, Inc., published a standard for numbering equipment. The Department of Defense adopted this standard and has required contractors to number equipment in one of three methods prescribed in the standard. These methods are:

- Unit numbering method.
- Location numbering method.
- Location coding method.

To help you obtain a clear understanding of these numbering systems, often called alphanumeric coding systems or designators, the following text will (1) explain the systems, (2) show how each is used, (3) compare a logic sheet module number to its physical location, and (4) identify a component on a chassis or printed circuit board (PCB) by its full alphanumeric designator. You will participate in this explanation by making an alphanumeric designator and then finding the exact location of a component by breaking down its alphanumeric code into parts.

In some systems the numbering system is used in the fault location guide. Troubleshooting and system validation can be done with the aid of a number list and a test instrument. Now let's examine the types of American National Standards Institute numbering systems. During this discussion, you should determine which system is used on your equipment.

426. Cite characteristics of alphanumeric designators and locate and identify certain units or components.

In this BOF unit we discuss the unit numbering method, the location numbering method, and the location coding method and their subareas, in that order.

Unit Numbering Method. The unit numbering method employs only one basic reference symbol for each single element in an entire system. With the use of this system, no two items have the same reference symbols. A class letter is used to identify each portion of the equipment down to and including small components, such as parts on a printed circuit board or ICs on a card file. A number is also assigned to the component that identifies its specific location. Examples are "R" for resistor and "R14" for the 14th resistor in the circuit. The symbol "C7" means a capacitor and the 7th one in the circuit. PCBs and other units handled or exchanged as a unit assume the class (letter) of the unit, and the affixed component has the unit designation and individual class for the component. Example: AR 14:A—assembly (PCB), R—resistor, 14—14th resistor on the PCB.

Refer here to figure 3-1, which shows a typical system subdivision and set for the unit number breakdown. Each division of the system requires a further breakdown or designator to identify the precise location. See if you can identify how the number below will lead you to a specific location:

2	A1	A2
Unit	Assembly	2nd Assembly

or

3	A1	A5	R1
Unit	Assembly	Subassembly	Resistor #1

To locate a given area and find or compare its location to a technical order logic sheet, schematic diagram, or illustrated parts breakdown, you must be able to construct a number. Using figure 3-2, write the complete numbers for each item in units 1 and 2, indicated below:

Unit 1:
Triangle #_______
Rectangle assembly in center_______
Resistor affixed to the unit_______
Square assembly next to the resistor_______

Unit 2:
Jack 1_______

607

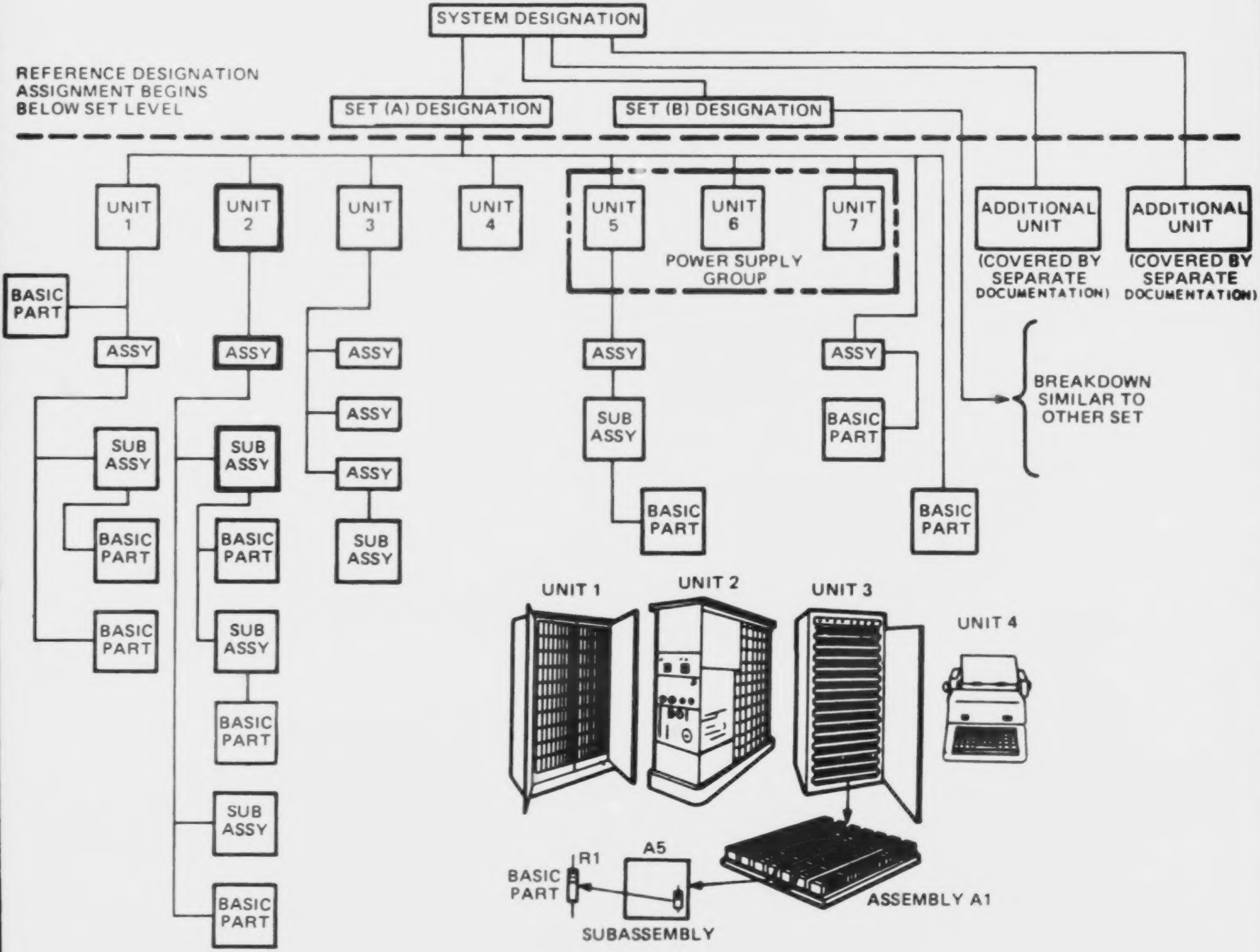

SYSTEM DESIGNATION
REFERENCE DESIGNATION ASSIGNMENT BEGINS BELOW SET LEVEL
SET (A) DESIGNATION
SET (B) DESIGNATION
UNIT 1
UNIT 2
UNIT 3
UNIT 4
UNIT 5
UNIT 6
UNIT 7
POWER SUPPLY GROUP
ADDITIONAL UNIT
(COVERED BY SEPARATE DOCUMENTATION)
ADDITIONAL UNIT
(COVERED BY SEPARATE DOCUMENTATION)
BASIC PART
ASSY
SUB ASSY
BREAKDOWN SIMILAR TO OTHER SET
R1
A5
BASIC PART
SUBASSEMBLY
ASSEMBLY A1

Figure 3-1. System subdivision.

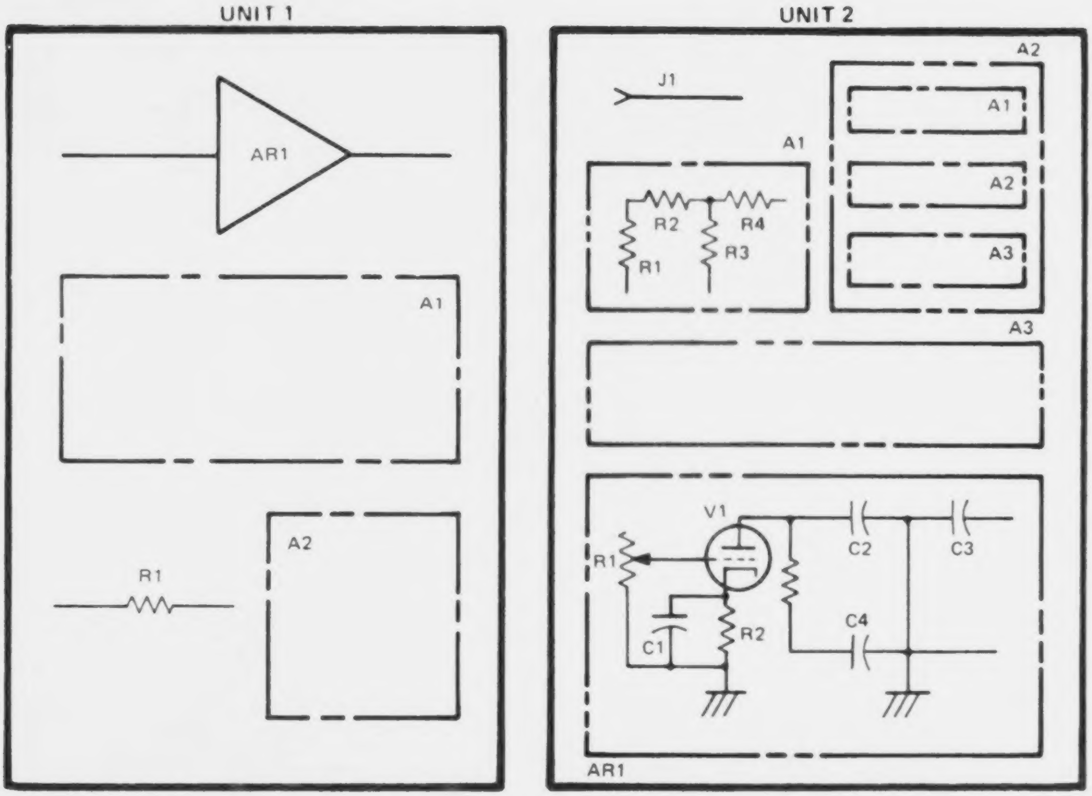


Figure 3-2. Assemblies and subassemblies.

Assembly with 4 resistors (label each resistor)
R1________ R3________
R2________ R4________
Assembly A3________
Assembly AR1________
Resistor R1________
Tube V1________
Capacitor C1________
Resistor R2________
Capacitor C2________
Capacitor C3________
Capacitor C4________
Assembly A2 with subassemblies
A1________
A2________
A3________

Your analysis of the unit and construction of the location number should have provided you with the following list:

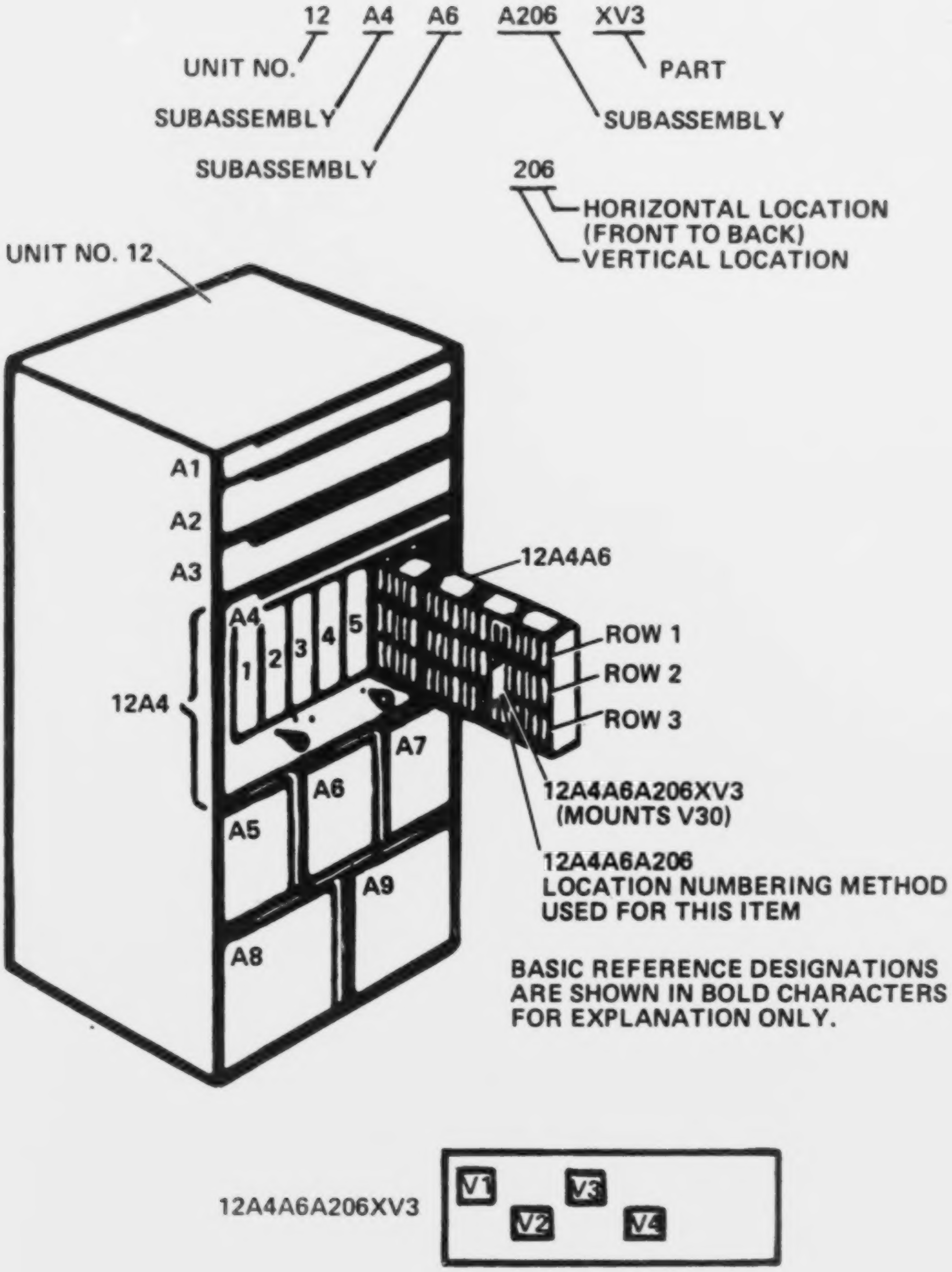
Unit 1
1AR1—Triangle #.
1A1—Rectangle assembly in the center.
1R1—Resistor affixed to the unit.
1A2—Square next to the resistor.
Unit 2
2J1—Jack 1.
2A1R1, R2, R3, and R4—Board with four resistors.
2A3—Assembly A3.
2AR1—Assembly AR1 with:
  2AR1R1—Resistor R1.
  2AR1V1—Tube V1.
  2AR1C1—Capacitor C1.
  2AR1R2—Resistor R2.
  2AR1C2—Capacitor C2.
  2AR1C3—Capacitor C3.
  2AR1C4—Capacitor C4.
2A2A1—Board A2 with assembly A1.
2A2A2—Board A2 with assembly A2.
2A2A3—Board A2 with assembly A3.

Upon examination, it should be evident to you that all components are related to the next higher assembly by numbering. Therefore, by using this arrangement, you will be able to locate every single component since it has its own location identifier.

Before examining the other two numbering methods, let's tell you where you can find the numbering system for your equipment. In furnishing this information, we will discuss the service manual, the circuit diagrams manual, and the preventive maintenance manual.

Technical order series-2, service manual. Chapter 1 of the service manual for a piece of equipment contains the general description of the equipment. This chapter also provides the numbering of the units, assemblies, and subassemblies of the equipment.

Technical order series-3, circuit diagrams. The circuit diagrams manual uses an alphanumeric system in identifying the components, subassemblies, and assemblies. Partial or basic reference designations may be used on the diagrams if appropriate unit and subassemblies are evident. Quite often, the common elements of the entire alphanumeric code are listed on the first sheet of a series of logic sheets under the Notes


12
A4
A6
A206
XV3
UNIT NO.
SUBASSEMBLY
SUBASSEMBLY
SUBASSEMBLY
PART
206
HORIZONTAL LOCATION (FRONT TO BACK)
VERTICAL LOCATION
UNIT NO. 12
A1
A2
A3
A4
1
2
3
4
5
12A4
A5
A6
A7
A8
A9
12A4A6
ROW 1
ROW 2
ROW 3
12A4A6A206XV3 (MOUNTS V30)
12A4A6A206
LOCATION NUMBERING METHOD USED FOR THIS ITEM
12A4A6A206XV3
V1
V2
V3
V4

BASIC REFERENCE DESIGNATIONS ARE SHOWN IN BOLD CHARACTERS FOR EXPLANATION ONLY.

Figure 3-3. Sequential numbering.

column. This note usually looks like "REF DESIG PREFIX." If more than one prefix is involved, an additional note having the same intent should be added to the drawing.

Technical order series -6WC, preventive maintenance routines. PMIs use alphanumerics quite extensively when specifying a task to be performed on a piece of equipment. Example: "Adjust video level at 3A6A7R11 for 1 volt ± .05V."

Location Numbering Method. The location numbering method of assigning reference designations is an adaptation of the unit numbering method wherein the number portion is based on the physical location of the item in the unit, assembly, or subassembly, and the letter "N" is used to identify areas that are not assemblies. Either of two methods may be used—sequential or coordinate.

Sequential numbering. Sequential numbers are assigned to recognizable areas, assemblies, subassemblies, or parts within units, assemblies, and subassemblies. Figure 3-3 illustrates a typical sequential number assignment.

Coordinate numbering. In coordinate numbering the number portion of the reference designation is determined by the coordinates of the upper left-hand corner of the zone (row and column) in which the designated item appears. The numbering contains the vertical position designation (top to bottom) first, and then the number of the horizontal position (left to right). To restate, numbers are assigned top to bottom, left to right, and front to rear. For a visual understanding of this system, study figure 3-4 and locate the two areas that include dots. The numbers of these locations are 0407 and 1012; a 0 precedes the 4 and 7 because of a rule which states that each number part will have digits equal in number to the largest coordinate location; e.g., 002 for systems having coordinates numbered to 999.

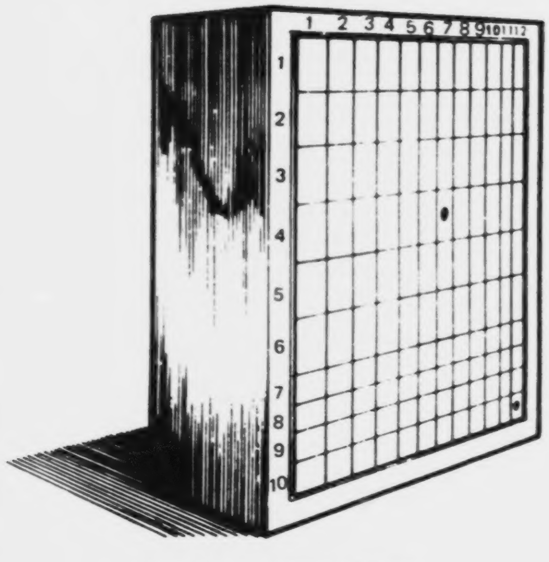


Figure 3-4. Coordinate numbering.

Location Coding Method. The location coding method of assigning a code that serves as a reference designator is a form of the location numbering system in which letters as well as numbers are used to identify items and to specify their physical locations in equipment. Again, either of two procedures for assigning codes—sequential or coordinate—may be used. In either case, the number starts with the unit number.

Sequential coding. In sequential coding the numbering sequence within each level, within assemblies, and within subassemblies starts with a "1" or an "A." Letters and numbers normally are assigned to alternate levels of the equipment; numbers to the odd levels—first (unit level), third, fifth, etc.; letters to the even levels—second, fourth, etc. Refer to figure 3-5 and note that a letter precedes each number. For example: PCB(C) shown as part of N2 has a number N2A825A608R101, or broken down:

N2	A	825	A	6	08	R	101
Unit	Assy	Assy#	Asbly	Row 6	Card	Resistor	Coordinate
2			(PCB)		Pos 8		position
							Row 1
							Col. 01
							Located
							on PCB

Now look at example B on the figure and break down this number:
N1A40A106R21. Compare your answer to the answer below. If correct, proceed with the text. If you made an error, restudy the text:

N1	A40	A106	R21
Unit	Assy 40	Assy	Resistor
		Row 1	Row 2
		Card 06	Pos 1

Coordinate coding. Any suitable increment may be used for coordinate coding based upon the equipment configuration to determine rows and columns. The code is determined by the coordinate of the upper left-hand corner of the zone. Numbers are used in one direction, and letters are used in the other direction. Therefore, both a number and a letter are required to locate any specific location. This coding is used in the same sequence to locate the smallest component. Example: Refer to figure 3-6 and locate subassembly B on subassembly D on unit 12. The rule for coordinate coding is illustrated as:

No.	Alpha	No.	Alpha No.	Ref Desig
12	D	6	B5	Q3
Unit	Subassy	Subassy	Row B	Part No.
			Card 5	Transistor
			Subassy	No. 3

In studying number systems or alphanumeric coding systems, you have examined three basic systems. Your examination should have made you aware that the numbering system employed in your system will help you in signal tracing and in locating the defective part in troubleshooting. It also tells you exactly which control to turn or to adjust when you perform preventive maintenance routines. It is of further help when you

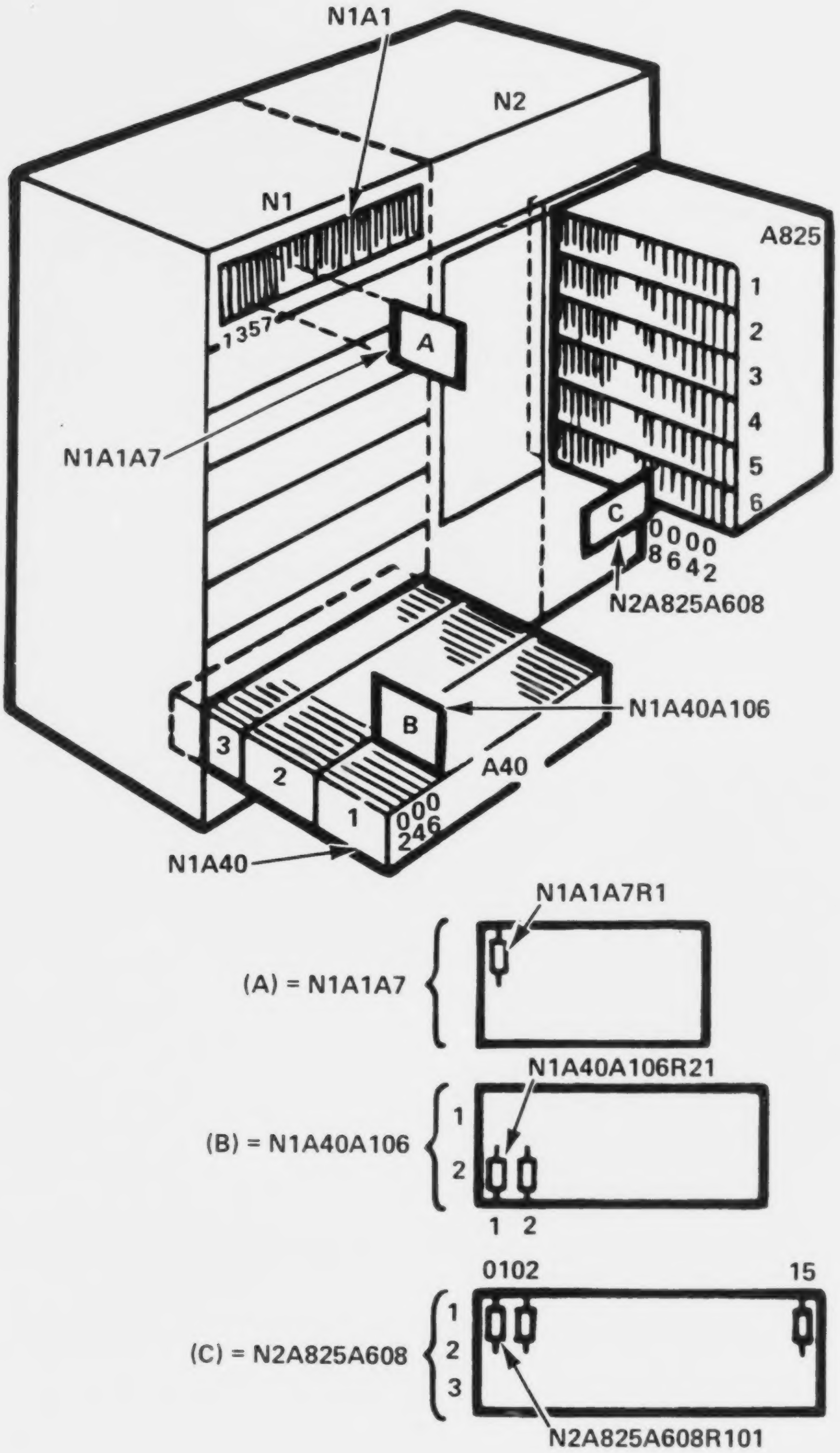

N1A1
N2
N1
A825
1
2
3
4
5
6
1357
A
N1A1A7
C
0000
8642
N2A825A608
N1A40A106
B
3
2
1
A40
000
246
N1A40
N1A1A7R1
(A) = N1A1A7
N1A40A106R21
(B) = N1A40A106
1
2
1 2
0102
15
(C) = N2A825A608
1
2
3
N2A825A608R101

Figure 3-5. Location sequential coding.

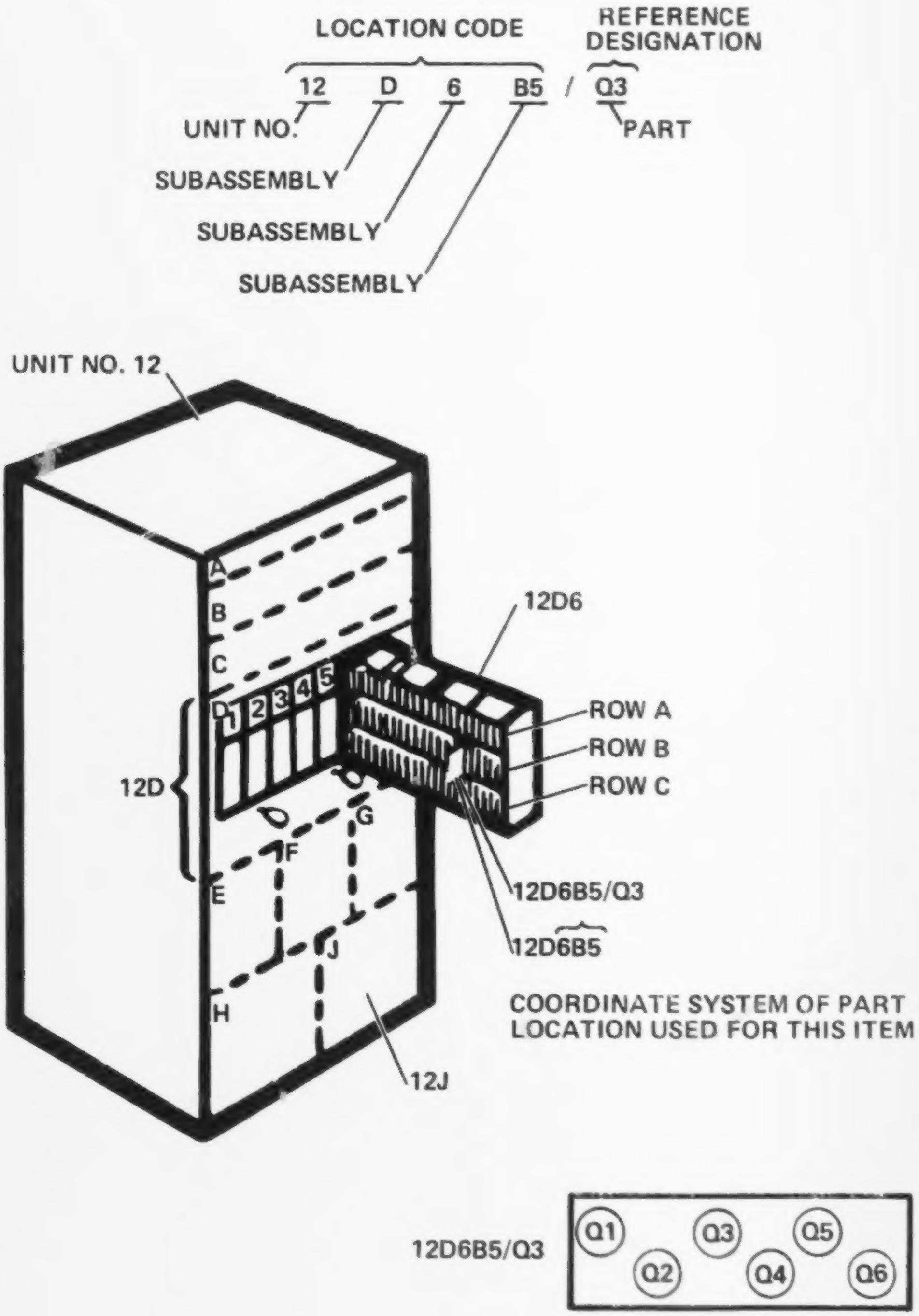

LOCATION CODE
REFERENCE DESIGNATION
12 D 6 B5 / Q3
UNIT NO.
SUBASSEMBLY
SUBASSEMBLY
SUBASSEMBLY
PART
UNIT NO. 12
A
B
C
D
1
2
3
4
5
E
F
G
H
J
12D6
ROW A
ROW B
ROW C
12D
12D6B5/Q3
12D6B5
COORDINATE SYSTEM OF PART LOCATION USED FOR THIS ITEM
12J
12D6B5/Q3
Q1
Q2
Q3
Q4
Q5
Q6

Figure 3-6. Location coordinate coding.

analyze a problem in logic, because the reference designation is included on the logic sheet and clearly identifies the area you are examining. Because your knowing these numbering systems helps you in these ways on the job, you should determine which numbering system is used in your equipment so that you will be a knowledgeable technician. Who knows, you may find that more than one of the numbering or coding systems is used in the system to which you are assigned. Consequently, the review of the basic methods just given will serve as a reminder to you in your future maintenance efforts.

Exercises (426):

1. Why, using the unit numbering method, do no two items have the same reference symbols?

2. Using the unit numbering method, what does the number AR102 mean?

3. Given the alphanumeric designator of 2A1V2, where and in what would the part be located?

4. In what TO series, and how, are alphanumerics used very extensively?

5. What does the prefix letter "N" identify in the location numbering method?

6. Coordinate numbering, whether using the location numbering method or location coding method, requires assignment of alphanumerics in what manner?

7. Referring to figure 3-3 of the text, what would be the identification assigned to the drawer in the lower right corner of the rack?

8. Give two of the ways in which your knowing the alphanumeric numbering systems will help you on the job.

427. Given a part number or reference designator, identify its proper location by using -4 series technical order extracts.

Use of the Illustrated Parts Breakdown for Location. Technical data supplied with equipment to the Air Force contain a wealth of information. Much of this information, however, is never used, simply because personnel do not realize the information exists or how to find it. One example of this is the illustrated parts breakdown (IPB), the -4 technical order. This discussion is limited to location of components, but you should be aware that the introduction section of all publications will inform you of uses and techniques to properly use the manual. Study these to keep yourself informed.

There are times when you know what an item does and where it goes, but you may not know the part number. At other times, you may know the part number or reference designator, but locating where to install it is a problem. The following discussion should help you solve such problems.

Part number is not known. Assume you need to order a replacement part for your equipment. You will require the part number as part of this process. You should already know the function and application of the part. All you do now is to turn to the table of contents of the applicable -4 series TO and select the major assembly for the part (see fig. 3-7). Next, turn to the page indicated and locate the desired part on the illustration (see fig. 3-8). From the illustration, obtain the index number assigned to the part desired. Refer to the accompanying description, given in figure 3-9, and you have the part number and can continue the ordering process.

Part number or reference designator is known. Assume now that you have the part number, but your problem is knowing where to install it. As you know, we work with huge systems. Consequently, no one can remember the location of everything. You should therefore refer to Section III of the series -4 TO. The part numbers are listed in numerical order, as shown in figure 3-10. So locate the part number and note the figure and index number assigned to the part number. Now turn to the figure number indicated, as figure 3-9 illustrates, and locate the index number referenced in the numerical list. If you need to use a pictorial representation of the part or to find its location, refer to the same index number on the accompanying illustration, as figure 3-8 shows. When, on the other hand, you know the reference designation, refer to Section IV, Reference Designation Index, as shown in figure 3-11.

Locate here the reference designation and note the figure and index number and the part number assigned. Then turn to the figure indicated, as figure 3-9 illustrates, and locate the index number referenced in the reference designation index. If you want to use a pictorial representation of the part or need to know its location, refer to the same index number on the accompanying illustration; i.e., figure 3-8.

Exercises (427):

1. If a reference designator is known, the exact pictorial location can be found in the _______ series TO.

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  Test Control Group OQ-118(V)1/GKC-1(V), OQ-118(V)2/GKC-1(V), OQ-118(V)3/GKC-1(V) and OQ-118(V)4/GKC-1(V) 2-2
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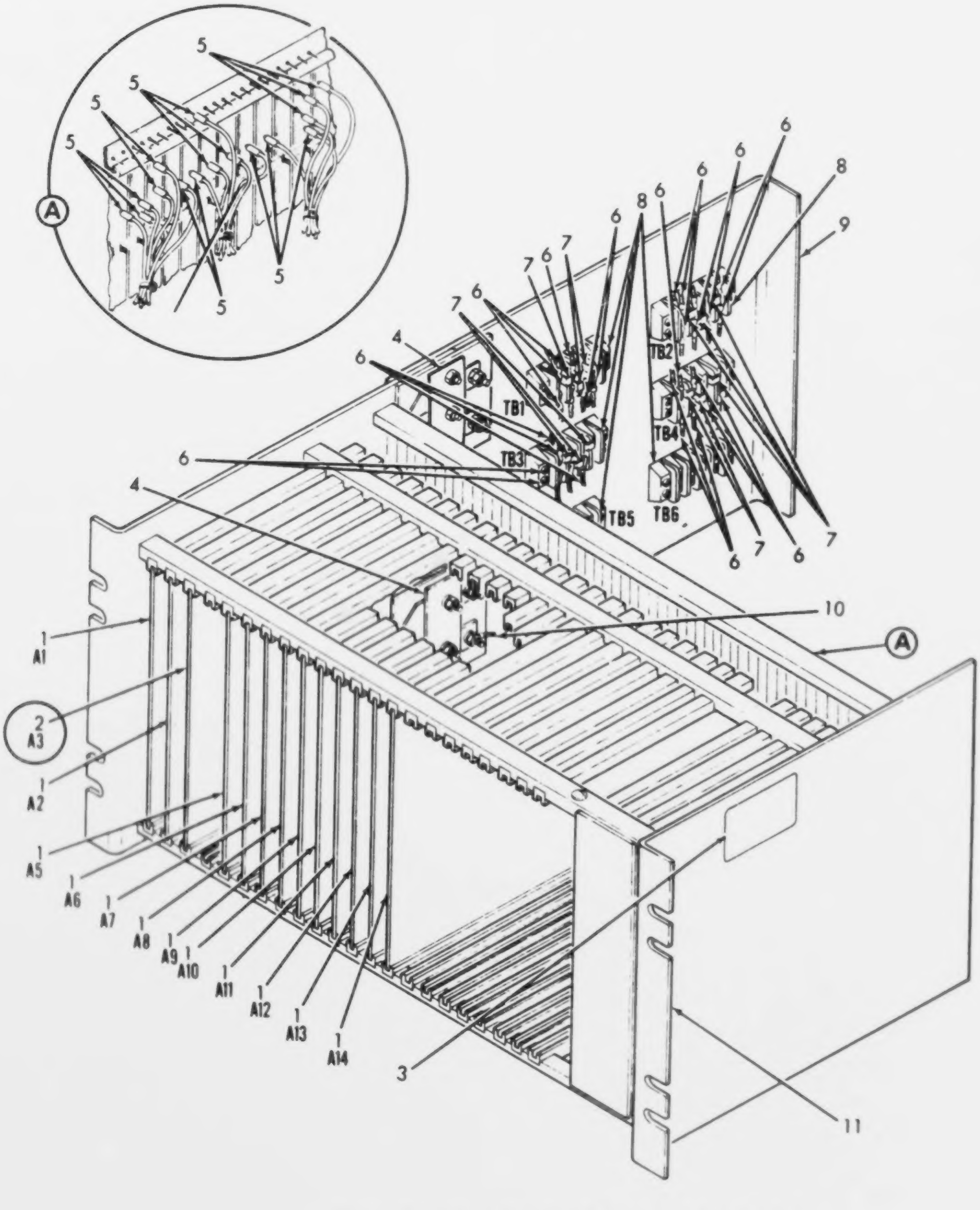
IV REFERENCE DESIGNATION INDEX 4-1

Figure 3-7. Table of contents extract.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A9
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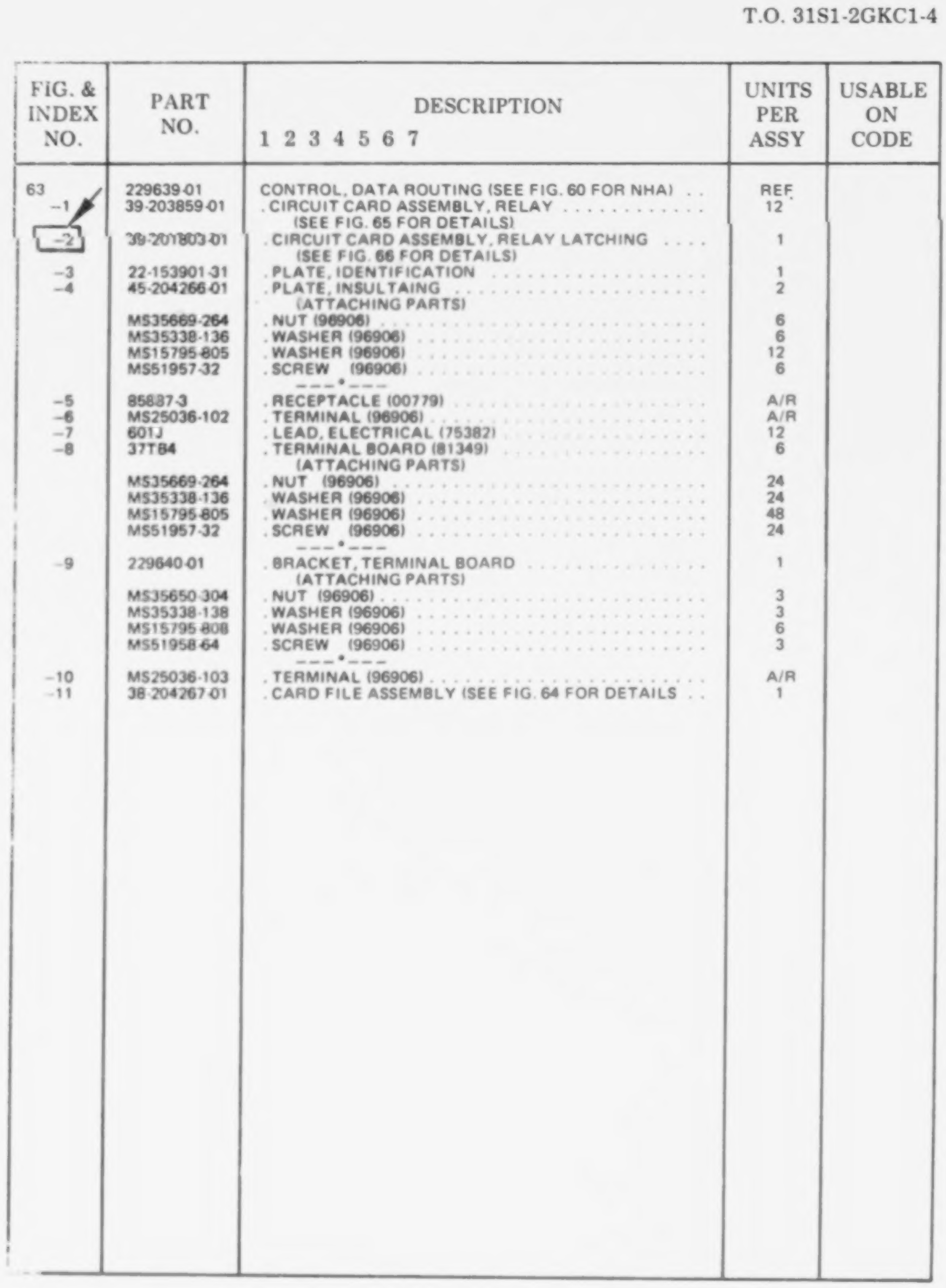
Data Routing Control Assembly (39A6)

Figure 3-8. Pictorial representation.



T.O. 31S1-2GKC1-4

FIG. & INDEX NO.	PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE
63	229639-01	CONTROL, DATA ROUTING (SEE FIG. 60 FOR NHA)	REF	
-1	39-203859-01	. CIRCUIT CARD ASSEMBLY, RELAY (SEE FIG. 65 FOR DETAILS)	12	
-2	39-201803-01	. CIRCUIT CARD ASSEMBLY, RELAY LATCHING (SEE FIG. 66 FOR DETAILS)	1	
-3	22-153901-31	. PLATE, IDENTIFICATION	1	
-4	45-204266-01	. PLATE, INSULTAING (ATTACHING PARTS)	2	
	MS35669-264	. NUT (96906)	6	
	MS35338-136	. WASHER (96906)	6	
	MS15795-805	. WASHER (96906)	12	
	MS51957-32	. SCREW (96906)	6	
		---•---		
-5	85887-3	. RECEPTACLE (00779)	A/R	
-6	MS25036-102	. TERMINAL (96906)	A/R	
-7	601J	. LEAD, ELECTRICAL (75382)	12	
-8	37TB4	. TERMINAL BOARD (81349) (ATTACHING PARTS)	6	
	MS35669-264	. NUT (96906)	24	
	MS35338-136	. WASHER (96906)	24	
	MS15795-805	. WASHER (96906)	48	
	MS51957-32	. SCREW (96906)	24	
		---•---		
-9	229640-01	. BRACKET, TERMINAL BOARD (ATTACHING PARTS)	1	
	MS35650-304	. NUT (96906)	3	
	MS35338-138	. WASHER (96906)	3	
	MS15795-808	. WASHER (96906)	6	
	MS51958-64	. SCREW (96906)	3	
		---•---		
-10	MS25036-103	. TERMINAL (96906)	A/R	
-11	38-204267-01	. CARD FILE ASSEMBLY (SEE FIG. 64 FOR DETAILS	1	

Figure 3-9. Reference designation index.

PART NUMBER	FiG. & INDEX NO.	QTY PER ART	SOURCE CODE	REPAiR CODE
323933	6-12			
	6-24			
	6-28			
	6-51			
	6-58			
	6-59			
	6-61			
	6-65			
	6-68			
	6-77	A/R		
	6-80			
	6-86			
	6-90			
	6-93			
	6-97			
	6-102			
	6-107			
	6-115			
323934	4-149	54	P1	
323934GRN	4-54	154	P1	S
	4-75			
	4-00			
	4-103			
	4-113			
	4-120			
	4-125			
323937V10	4-121	8	X2	
327138	5	A/R	P1	S
	5-8	A/R		
	5-17	A/R		
	5-28C			
	5-28			
	5-35			
	5-40			
	5-61			
	5-79			
	6			
	6-8			
	6-17			
	6-31			
	6-36			
	6-55			
	6-72			
327139	5-20	40	P1	S
	6-20			
35-142577-01	76-17	3		
35-148247-01	76-13	3		
35-148248-01	76-14	1		
35-153427-01	76-25	1		
35-153427-03	76-24	1		
35-153428-01	76-10	126		
351-25807-001	8-1A	1	P1	S
37TB4	63-8	REF	P1	S
38-201845-01	19-26	1	X2	
38-204260-01	64		X2	
38-204267-01	63-11	REF	X2	
	64	REF		
38TB10	8-37	3	X2	
38TB6	67-12	1	P1	S
39-194072-05	33-18	4	P1	S
39-194702-05	33-1	4	P1	S
39-194703-05	33-16	1	P1	S
39-194706-05	33-6	2	P1	S
39-197789-01	8-27	11	P1	F
	9	REF		
	10-38			

PART NUMBER	FIG. & INDEX NO.	QTY PER ART	SOURCE CODE	REPAIR CODE
	11-15			
	12-31			
	28-12			
	29-21			
	30-7			
	75-13			
39-200059-05	33-12	2	P1	S
39-200060-05	33-11	2	P1	S
39-200061-05	33-5	2	P1	S
39-200062-05	33-15	2	P1	S
39-200064-05	33-27	2	P1	S
39-200065-05	33-3	1	P1	S
39-200066-05	33-25	1	P1	S
39-200067-05	33-10	2	P1	S
39-200069-05	33-4	1	P1	S
39-200142-05	33-13	2	P1	S
39-201557-01	61-33	1	P1	F
	62	REF		
39-201803-01	63-2	REF	P1	F
	66	REF		
39-202317-01	19-25	1	P1	F
39-202321-01	19-22	1	P1	F
39-202323-01	19-24	1	P1	F
39-202327-01	19-20	1	P1	F
39-202331-01	19-23	1	P1	F
39-202335-01	19-21	1	P1	F
39-202626-07	33-8	10	P1	S
39-203859-01	63-1	12	P1	F
	65	REF		
39-204262-01	64		X2	
39-204406-01	64		X2	
39TB14	37-12	1	P1	S
4-40X1-4LG	72			
	72-35	8		
4XCL17-5CRBBLKCL	51-18	2	P1	S
80GRSPSTA42UARO	52-3			
4XCL17-5CRBBLKCL	54-7	1	X2	
80GRSPSTA42UARO				
40-010	49-11	6	X2	
	53			
40-014	53	4	X2	
40-018	49-8	1	X2	
40-20SSJ	5	A/R	X2	
41-203574-03	68-10	1	X2	
41-203574-04	68-1	5	X2	
	68-6			
41-203788-01	5-150	4	P1	
	5-155			
	6-103			
	6-108			
41-203788-02	68-15	3	X2	
41-204283-01	2-67	3	X2	
41-204283-02	2-73		X2	
	2-71	2		
41-204284-01	2-69	7	X2	
41-204284-02	2-72	2	X2	
41-204285-01	2-66	3	X2	
41-204285-02	2-70	2	X2	
41-204286-01	2-68	4	X2	
42574-3	5-151	122	P1	
	5-155A			
	6-104			
	6-109			
	28-19			
42575-3	2-75	A/R	P1	S
	5	A/R		

Figure 3-10. Extract from Section III.

REFERENCE DESIGNATION	FIG. & INDEX NO.	PART NUMBER
31W76	4	CABLE ASSY
31W76J4	4-143	MS3128E10-6S
31W76P3	4-142	KPSE06SN10-6P08A
31W77	4	CABLE ASSY
31W77P4	4-141	MS3126F10-6P
31W78	4	CABLE ASSY
31W78J5	4-145	MS3128E10-6SW
31W78P4	4-144	KPSEO6SN10-6PW8A
31W79	4	CABLE ASSY (W79)
31W79P5	4-146	MS3126F10-6PW
39	60	229636-01
39A1	60	20-170241-59
39A2	60-4	8190-656
39A3	60-5	8190-655
39A4	60	20-170241-58
39A5	60-8	229661-01
39A5AT1 THRU	61-21	TA5MN
39A5AT4	61-21	TA5MN
39A5AT6 THRU	61-21	TA5MN
39A5AT8	61-21	TA5MN
39A5A1	61-33	39-201557-01
39A5A1CR1 THRU	62-1	1N649
39A5A1CR18	62-1	1N649
39A5J1 THRU	61-24	M39012/03-0005
39A5J4	61-24	M39012/03-0005
39A5J6	61-24	M39012/03/0005
39A5J7	61-32	MS3128F16-26S
39A5J8	61-25	MS3128F14-5P
39A5K1	61-22	811C00100
39A5K1P7	61-18	M39012/05-0003
39A5K1P12	61-18	M39012/05-0003
39A5K2	61-22	811C00100
39A5K2P8	61-18	M39012/05-0003
39A5K2P13	61-18	M39012/05-0003
39A5K3	61-22	811C00100
39A5K3P10	61-18	M39012/05-0003
39A5K3P15	61-18	M39012/05-0003
39A5K4	61-22	811C00100
39A5K4P9	61-18	M39012/05-0003
39A5K4P14	61-18	M39012/05-0003
39A5K5	61-22	811C00100
39A5K6	61-22	811C00100
39A5K6P11	61-18	M39012/05-0003
39A5K6P16	61-18	M39012/05-0003
39A5K7	61-39	136C00100
39A5K7P1	61-37	RTK06-8-7S
39A5K7P2 THRU	61-38	M39012/01-0008
39A5K7P6	61-38	M39012/01-0008
39A5P1	61-8	6A43
39A5S1	61	10H3A1C1F4J14LW*MIN 3R256V17
39A5S2	61-9	2D72
39A5XA1	61-35	00-6024-036-980-001
39A6	60-14	229639-01
39A6A1	63-1	39-203859-01
39A6A1CR1 THRU	65-1	FD111
39A6A1CR20	65-1	FD111
39A6A1K1 THRU	65-2	M5757/9-003
39A6A1K10	65-2	M5757/9-003
39A6A2	63-1	(SAME AS 39A6A1)
39A6A3	63-2	39-201803-01
39A6A3CR1 THRU	66-1	JAN1N647
39A6A3CR20	66-1	JAN1N647
39A6A3K1 THRU	66-2	LF6201K00
39A6A3K10	66-2	LF6201K00

REFERENCE DESIGNATION	FIG. & INDEX NO.	PART NUMBER
39A6A5 THRU	63-1	(SAME AS 39A6A1)
39A6A14	63-1	(SAME AS 39A6A1)
39A6TB1 THRU	63-8	37TB4
39A6TB6	63-8	37TB4
39A7	60	20-170241-58
39A8	60-15	82-201078-01
39A8E1	67-14	25-170206-04
39A8PS1	67-27	LMG280VY
39A8TB1	67-12	38TB6
39A9	69-29	85-202636-03
39A9CB1	70-5	AM12MG6-20
39A9DS1	70-8	80EA1C4F1WH1L2N*
39A9M1	70-2	620H
39A9TB1	70-14	9-85-4
39A9TB2	70-14	9-85-4
39A10	69-31	KPSRR726
39A10B1	71-10	HF3G005N
39A10S1	71-14	KV3
39A10S2	71-16	RP9
39A10T1	71	VT-3
39A10T1	71-15	10B
39A11	60-65	229638-01
39A11J10 THRU	60-61	MS90159-30E
39A11J14	60-61	MS90159-30E
39A11J42 THRU	60-64	31-220
39A11J44	60-64	31-220
39DS1	69-1	80EA1C4F1AH1L2N*
39FL1	69-21	027-431-002
39N1001	68	CABLE ASSY (N1001
39N1001A5JA24	68-5	43-204419-11
39N1001J1	68-2	MS3128F16-26S
39N1002	68	CABLE ASSEMBLY (N10 02)
39N1002A2P4	68-14	PT06A14-19S(SR)
39N1002J2	68-11	MS3128F14-19S
39N1003	68	CABLE ASSY (N1003
39N1003J3	68-7	MS3128F16-26S
39N1004	68	CABLE ASSY (N1004
39N1005	68	CABLE ASSY
39N1005A5JA25	68-5	43-204419-11
39N1005J5	68-2	MS3128F16-26S
39N1006	68	CABLE ASSY
39N1006J6	68-7	MS3128F16-26S
39N1007	68	CABLE ASSY
39N1008	68	CABLE ASSY
39N1008A5JA26	68-5	43-204419-11
39N1008J8	68-2	MS3128F16-26S
39N1009	68	CABLE ASSY
39N1009J9	68-16	MS3128F20-41S
39N1010	68	CABLE ASSY (N1010 T HRU N1014)
39N1010A5P1	68-19	UG1682/U
39N1010J10	68-19	UG1682/U
39N1011	68	CABLE ASSY
39N1011A5P2	68-19	UG1682/U
39N1011J11	68-19	UG1682/U
39N1012	68	CABLE ASSY
39N1012A5P3	68-19	UG1682/U
39N1012J12	68-19	UG1682/U
39N1013	68	CABLE ASSY
39N1013A5P4	68-19	UG1682/U
39N1013J13	68-19	UG1682/U
39N1014	68	CABLE ASSY
39N1014A5P6	68-19	UG1682/U

Figure 3-11. Extract from Section IV.

2. What are the reference designators of the terminal boards on figure 3-8?

3. What is the part number of the card that fits into the fifth slot from the left on figure 3-8?

3-2. Test Equipment

As an electronic computer and switching systems specialist, you know that you have the responsiblity for the maintenance of complex equipment—i.e., equipment that is *not* complex because of the individual circuits but which is complex because of the vast number of circuits involved. Your ability to maintain this equipment depends largely upon your knowledge of the use and care of test equipment. Since you have already completed an apprentice-level training course, you have a good knowledge of the principles of test equipment. However, you must continue to work with and study your test equipment to develop a thorough understanding of its uses and capabilities.

Do not limit yourself to thinking of the standard pieces of test equipment such as scopes, voltmeters, and counters. Expand your knowledge of specialized test circuits as well. Specialized test circuits are not limited to auxiliary units. They also include test circuits and error indicators that are built into the data processors and which function as an integral part of the equipment.

Electronic test equipment is designed and constructed to perform a wide variety of tests. These tests are used to determine the proper operation or alignment of electronic sets, circuits, or parts. The performance of data processing equipment depends in a large measure on the accuracy of the test equipment and on the integrity of the maintenance specialist. Without test equipment, very few electronic devices could be kept in operating condition; therefore, you must use test equipment properly. Operating instructions are sometimes found on the front cover of the test equipment; however, explicit instructions are contained in the -1 series of applicable technical orders (TOs). To insure that the system is operating at its maximum capability, it is mandatory that you be thoroughly familiar with the operation of the test equipment necessary to maintain the system at its peak performance.

There is a -1 technical order for each piece of test equipment you have in the shop. To obtain the necessary TOs, check TO 0-1-33 (test equipment index) for listings of publications applicable to the test equipment in your inventory. The missing TOs should be ordered through the channels established by your organization.

428. State operating characteristics of multimeters.

Multimeters. The typical multimeter, also known as a volt-ohm-milliammeter (VOM), contains voltmeter, ammeter, and ohmmeter circuits which use a single meter movement. Some use a movement that requires only 50 μA for a full scale deflection. This movement is used to achieve a 20,000-ohms-per-volt sensitivity, which is adequate for most DC measurements. Less sensitive meters have 1000-, 5,000-, or 10,000-ohms-per-volt sensitivity. The AC voltmeter circuits are usually designed for 1000 ohms per volt.

The most common multimeters are those which measure only DC voltage, direct current, and resistance; and those which measure AC and DC voltage, direct

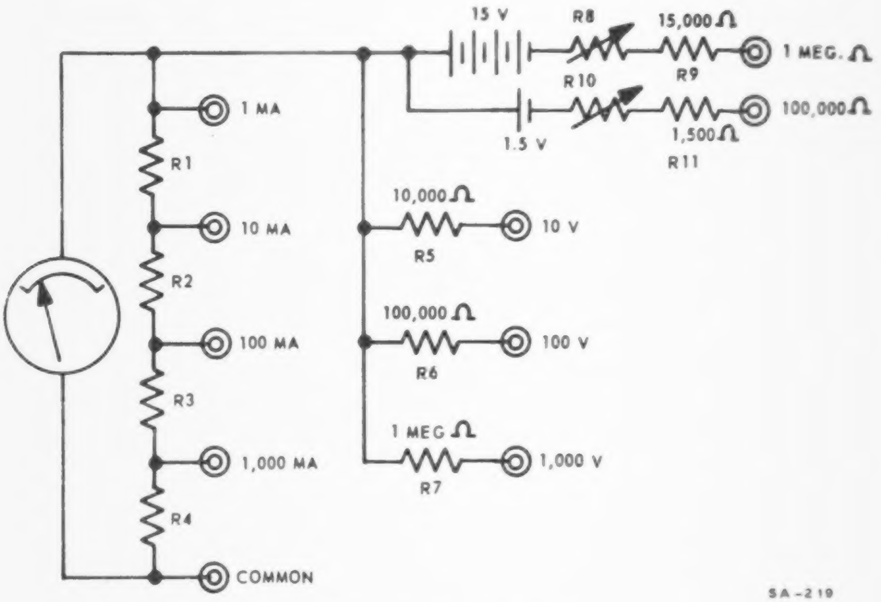


Figure 3-12. DC volt-ohm-milliammeter.

current, and resistance. The circuits contained within these instruments are the circuits we have discussed in the last section. Thus, the operating principles are the combined principles of instruments already studied. Let us analyze two relatively simple multimeters so you will become convinced of this fact.

The schematic of a volt-ohm-milliammeter that is capable of measuring direct current, DC voltage, and resistance is shown in figure 3-12. For current requirements less than 1 mA, the test leads are plugged into the pin jacks marked "1 mA" and "COMMON." The current divides between the meter and the shunt (R_1, R_2, R_3, and R_4 in series). For higher current measurement, note that part of the resistance is in series with the meter and the remaining part comprises the shunt. For example, when you are measuring a current between 10 mA and 100 mA, the resistors R_1 and R_2 are in series with the meter; R_3 and R_4 shunt the meter. This, you learned earlier, is a ring or universal shunt circuit. Regardless of the current range selected, the current through the meter is the same for full-scale deflection.

When you are measuring voltage, the meter is shunted by resistors R_1, R_2, R_3, and R in series (as in the case in the 0-1 mA range). Full-scale deflection is established by the multipliers, R_5, R_6, and R_7, for the 10-volt, 100-volt, and 1000-volt ranges, respectively. If we plug the test leads between the pin jacks marked "100V" and "COMMON," R_6 is in series with the shunted meter, and full-scale deflection occurs when 100 VDC is applied. A lesser voltage, of course, produces proportionally less deflection. The circuit is basically the same for the other two voltage ranges; the only difference lies in the value of the multiplier resistor in series with the shunted meter.

For resistance measurements, either the 1 MEG jack or the 100,000 jack is used with the jack marked "COMMON." Depending upon which jack is selected, the current from the negative terminal of either the 15-volt or the 1.5-volt battery flows through the OHMS-ZERO-ADJ resistor (R_8 or R_{10}), the multiplier resistor (R_9 or R_{11}), the resistor being measured, the meter and its shunt, and into the positive terminal of the battery. Since this is essentially a series-type ohmmeter, the resistance scale is calibrated from *right to left*; the larger the resistance, the smaller the current and the smaller the deflection.

Figure 3-13 shows the schematic of a bolt-ohm-milliammeter that can be used to measure AC and DC voltage, direct current, and resistance. The additional capability of measuring AC voltage is acquired by incorporating a half-wave shunt rectifier between the multiplier resistors and to the meter movement. The capacitor blocks any DC component that may be present in the applied voltage, thereby preventing erroneous readings and possible damage to the meter. Except for the rectifier portion, the AC voltage-measuring circuit is similar to the DC voltage-measuring circuit. In the

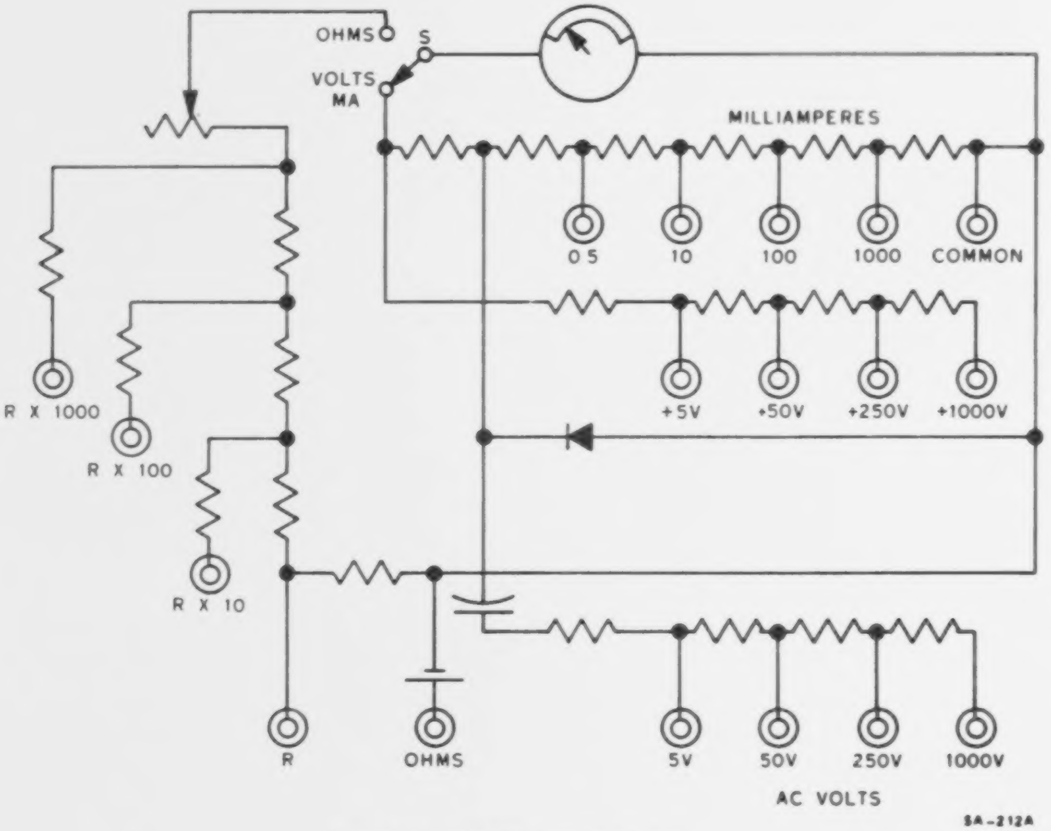


Figure 3-13. VOM that measures AC or DC.

milliammeter circuit, you should recognize the ring-shunt arrangement used for the measurement of current. Note, however, that when the switch S is in the OHMS position, the milliammeter shunt circuit is disconnected. To measure resistance, the test leads are plugged in the jack labeled "OHMS" and the R, R × 10, R × 100, or R × 1000 jack, depending upon the range desired. When the R × 1000 jack is used, an additional battery is necessary to supply a current sufficient for a good scale reading. In tracing out the ohmmeter circuits, you will find that this is a series-type ohmmeter which uses multipliers and a ring shunt for multirange operation.

Exercises (428):

1. When using a ring or universal shunt to measure higher current, how is the resistance changed?
2. When using a VOM for measuring voltage, to read higher voltages what must be done to the resistance in series?
3. What is the purpose of the capacitor in the multimeter diagram in figure 3-13?
4. In what circuits is the ring shunt arrangement used in figure 3-13?
5. What type of ohmmeter is used in figure 3-13?

429. List the advantages and disadvantages of the multimeter.

Multimeter Operational Considerations. The greatest advantage of a multimeter is that no external power source is required for its operation. Other advantages are its portability, versatility, and freedom from calibration errors due to aging electron tubes, line voltage variations, etc.

Disadvantages of the multimeter are its circuit loading characteristics, short scale, and danger of damage to the meter movement due to negligence during testing procedures.

There are several precautions you should observe when using a multimeter:

(1) Protect the meter by using the highest range for the initial measurement of a current or voltage of unknown magnitude.

(2) Observe polarity on all direct-current measurements; however, damage will not occur to a meter movement due to polarity reversal as long as the current or voltage being measured is within the range of the meter.

(3) Be careful to avoid dropping a meter or subjecting it to excessive mechanical shocks that may damage the delicate mechanism or cause the permanent magnet to lose some of its magnetism.

(4) Never attempt to measure the internal resistance of the meter movement with an ohmmeter, as the movement may be damaged by the relatively high current required for ohmmeter operation.

(5) Do not leave the range selector switch in a resistance measurement position when the meter is not in use because the test leads may become shorted and discharge the internal battery. It is also possible that the instrument may be connected across a voltage accidentally, causing damage to the meter.

(6) During a maintenance routine, check the multimeter each time you wish to make a measurement to determine not only the type of measurement the meter is set up for, but the range as well. This type of check will prevent meter burnouts and pointer bendings.

Know the condition of the internal battery used for the ohmmeter function of the multimeter. If the battery is not in good condition, you not only may experience difficulty in obtaining full-scale deflection but also you are likely to obtain an erratic or erroneous resistance indication.

Exercises (429):

1. Answer True or False: One of the advantages of a multimeter is that no external power source is required for its operation.
2. What are the advantages of a multimeter?
3. What are the disadvantages of the multimeter?
4. As a part of one disadvantage of a multimeter, why shouldn't you measure a meter movement's internal resistance with an ohmmeter?

430. Specify advantages of the TRVM over the VTVM and state the precautions you should observe when using the VTVM.

Beginning with the vacuum-tube voltmeter, then looking at transistorized votlmeters, we will compare the VTVM and TRVM and also list some VTVM precautions here.

Vacuum-Tube Voltmeter. The electronic multimeter, commonly referred to as a vacuum-tube voltmeter (VTVM), is an instrument used for measuring AC voltages, DC voltages, and resistances. The scales of this type of meter sometimes include a decibel scale and a

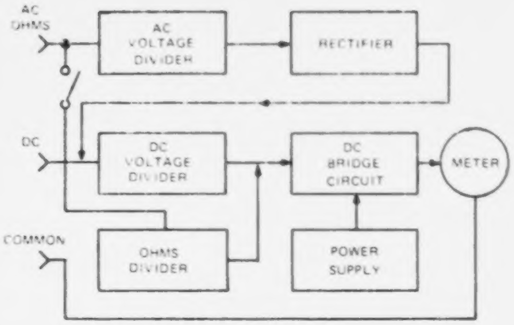


Figure 3-14. VTVM, block diagram.

chart to permit the use of the electronic multimeter as an audiofrequency (AF) level indicator. Refer here to figure 3-14.

When you are measuring DC voltages with a VTVM and you observe a change in polarity, as indicated by the meter, do not reverse the test leads as you would if you were using a nonelectrical multimeter. Use the polarity reverse switch; otherwise, physical contact with the voltmeter case and ground could give you a severe electrical shock.

Also, avoid any prolonged use of the low-resistance range (R × 1), if possible, because the current drain on the internal battery is heaviest on this range. When you are making measurements below 2 ohms, short the test probe together and reset the zero adjust control until the meter indicates zero. This procedure eliminates the effect of the series test lead resistance, which would give an erroneous meter indication. After you have completed the measurement, return the zero adjust control to the normal position.

When you are measuring high values of resistance, keep your fingers away from the tips of the test probe and away from the pigtails or terminal lugs of the resistor. This will eliminate possible errors due to leakage and stray pickup. This type of operational care is especially important on the R × 10,000- and the R × 1-megohm ranges.

With VTVMs using internal batteries for the ohmmeter function, know the approximate condition of the internal battery. When the battery is new, the deviation of the meter pointer changes very little with changes of the ohmmeter range switch. However, as the battery becomes exhausted, large variations occur in the meter indication as the range control is changed. The deviation from the full-scale indication (∞) changes by different amounts, depending upon the range control position. The reason for this, of course, is that a progressively greater current drain is placed on the battery as the ohms range is reduced.

In addition, do not leave the range selector switch in a resistance measurement position when the meter is not in use, because the test leads may become shorted together and reduce the life of the internal battery. It is also possible that the instrument may become accidentally connected across a voltage and cause damage to the VTVM. This applies also to those VTVMs that do not use internal batteries for the ohmmeter function.

Transistorized Voltmeters. A number of voltmeters that capitalize on the advantageous features of transistors have been developed. The transistor voltmeter (TRVM) is superior to a VTVM in that transistors require no heater current and draw so little collector current that battery operation is very practical. Thus, by using batteries, the VTVM is free of AC pickup. Also, no warmup time is required, and the instrument can be very compact. Since extremely high amplification is attainable with transistors, a TRVM can be designed to have a full-scale range as low as the 10V (1 × 10^{-35}V). We should point out, however, that the TRVM has one important limitation—the comparatively low input impedance of a transistor amplifier. As you know, this limitation is a characteristic of transistor operation, because the transistor is inherently a current-actuated device. Even when you use the common-collector configuration, input impedance greater than 1 megohm is very difficult to obtain. In the microvolt range, the input impedance is about 10K.

One way to acquire a high input impedance is to precede the transistor amplifier by a vacuum tube cathode follower. The cathode follower is designed to operate at a relatively low plate voltage so that battery operation is still quite practical.

Figure 3-15 shows the transistorized portion of this hybrid-type voltmeter. Part of the resistance in series with each emitter is unbypassed in order to provide negative feedback action. Additional feedback is obtained from the rectifier in order to further insure high stability. The common-emitter amplifiers are directly coupled together. Although NPN transistors are used in this circuit, PNP transistors can be used if negative biasing is preferred. You can readily see that this voltmeter is an amplifier-rectifier type. Thus, like the vacuum-tube version, it is most suitable for the measurement of small AC voltages in high-impedance circuits.

Exercises (430):

1. Why should prolonged use of the R × 1 range be avoided, if possible, when you are using a VTVM?

2. How can possible errors due to leakage and stray pickup be eliminated when you are measuring high values of resistance with the VTVM?

3. Answer True or False: Leave the range selector switch on the VTVM in a resistance measurement position when the meter is not in use.

4. What is an advantage of the TRVM over the VTVM?

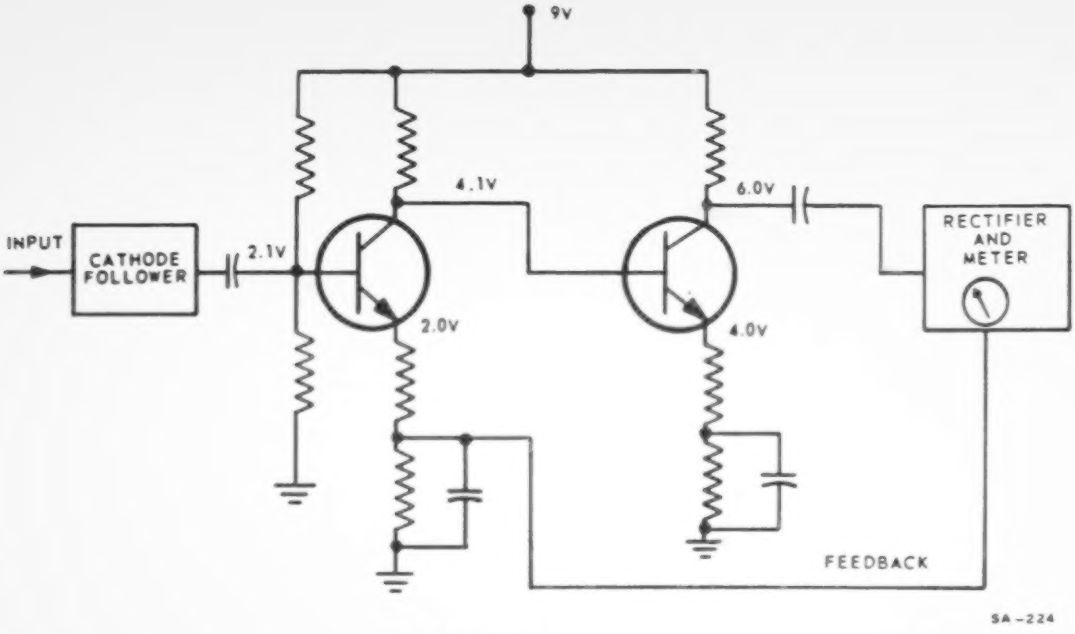


Figure 3-15. Transistorized voltmeter.

431. Cite the principle upon which the DC differential voltmeter operates, identify control and switch settings for specific functions, and specify high resistance measurement procedures.

Differential Voltmeter. The differential voltmeter is a highly accurate, portable instrument capable of precise AC and DC voltage measurements. This instrument can be used as a VTVM, a precision potentiometer, and a megohmmeter for measuring high resistance. It can also be used to measure the excursions of a voltage about some nominal value. The voltmeter is basically used for measurements of DC and AC voltages. Some differential voltmeters also contain a recorder output that makes the voltmeter particularly useful for monitoring the stability of a voltage.

When used as a DC differential voltmeter, the voltmeter operates on the potentiometric principle. An unknown voltage is measured by comparing it to a known adjustable reference voltage with the aid of a null detector. An accurate standard for measurements is obtained by setting the reference supply with a standard cell. One differential voltmeter uses a known adjustable reference voltage provided by a 500-VDC power supply and 5 decade resistor strings that are set accurately by 5 voltage readout dials. In this way, the 500 volts can be precisely divided into increments as small as 10 microvolts. The unknown voltage is then simply read from the voltage dials. When it is used as an AC differential voltmeter, a voltmeter operates in essentially the same way as for DC differential measurements. The AC input voltage is converted to a DC voltage, and this DC voltage is measured by comparing it to a known adjustable reference voltage.

Figure 3-16 is an illustration of the layout for a common differential voltmeter. The range control is effective only when the null control is in the VTVM position. At this time, the range dial indicates the voltage needed at the input terminals to deflect the indicator full to one side of the scale from the center. When the null control is in any of the numbered positions, the range control has no effect. The numbers on the null control indicate the full range of the meter indication about the value indicated by the voltage readout dials. Assume the null is in the 10 position, the readout dials indicate 24,368 volts, and the needle rests halfway between the center and the edge. The dial readings are now 5 volts away from the actual input voltage.

Normal operation. When you get ready to use the differential voltmeter, you should use a normal setup. This includes turning on the power and warming up the equipment for a period of time and setting the range and null switches. The normal setup for the range and null switches should be the highest range for the range switch and VTVM for the null switch. Other preliminary operation procedures will depend on the particular equipment you are working with. In any case, use the applicable TO or manufacturer's manual if available.

After you have set up the voltmeter, turn the range dial to the lowest range that will still give an on-scale indication of the input voltage. Note the input voltage indication. Set the readout dials to this voltage. Then turn the null switch to the first scale next to VTVM. After that turn the readout dials to make the indicator needle return to the center on the scale. Repeat the last step on the rest of the null positions. The voltage in can now be read directly from the dials.

VTVM operation. The differential voltmeter can be

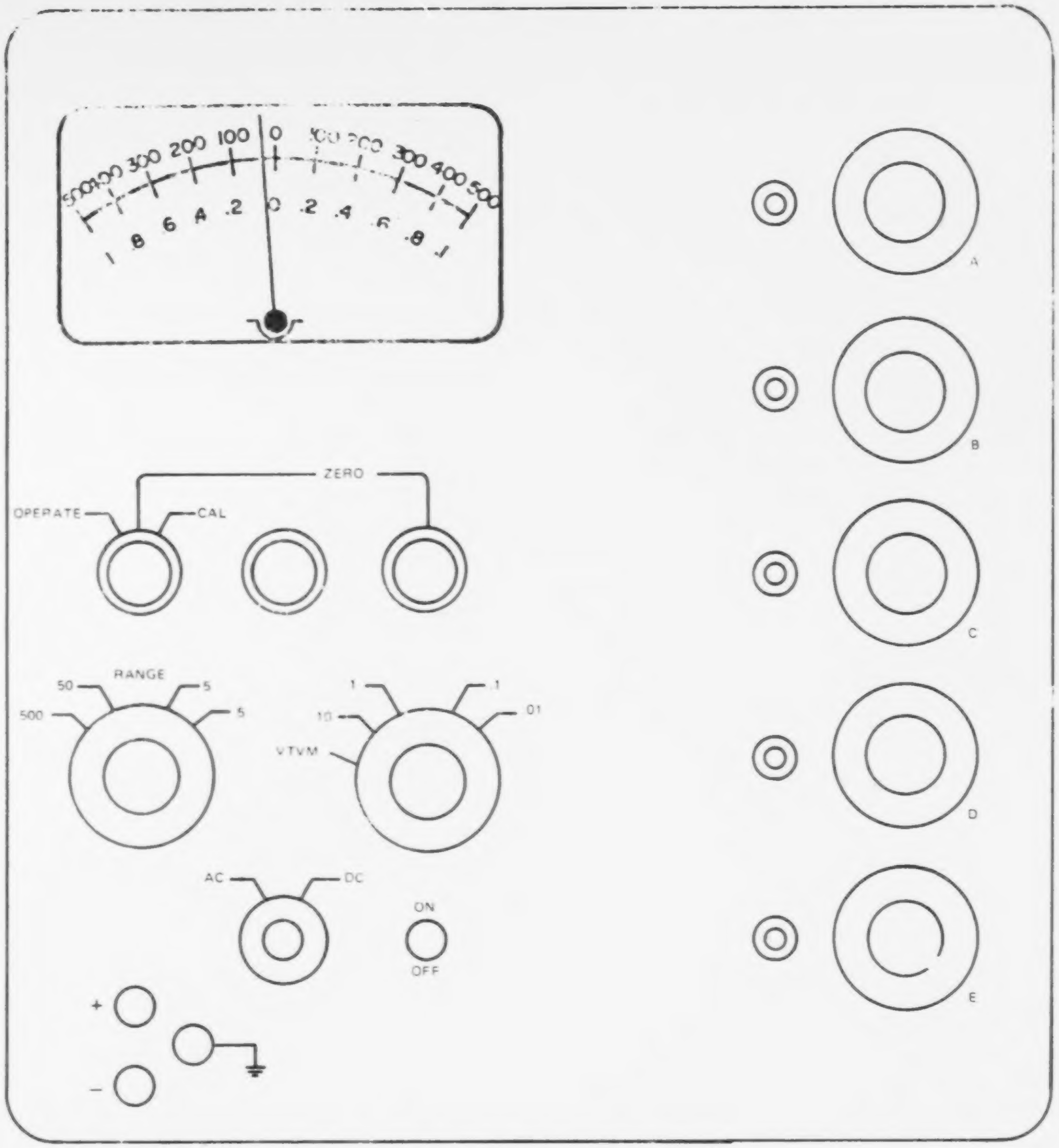


Figure 3-16. Differential voltmeter.

used as a normal VTVM. With the null switch in VTVM, the range switch determines the range of voltages to be measured. When the null is on any of the numbered ranges and the dials are at zero, you can measure plus and minus voltages up to the amount indicated on this null setting you are using. In effect you have a VTVM with an extended number of ranges.

Measurement of voltage excursions about a nominal value. In order to read the voltage excursions, set up the voltmeter to read the input voltage. Then set the null switch to the most sensitive setting that will still allow the meter indicator to stay on the scale. The voltage deviations can then be read from the meter. Many differential voltmeters have a recorder output. For long-term voltage excursion measurements, hook a recorder to this terminal and study the excursions later.

Measurement of high resistance. One of the important features of the voltmeter (as shown earlier in fig. 3-16) is its ability to be used as a megohmmeter for rapidly measuring high resistance from 1 megohm to 250,000 megohms. The following equation may be used to compute the resistance in megohms of an unknown connected to the input terminals:

$$R_x = 10 \frac{E}{E_m} - 1 \text{ megohms}$$

where:

R_x = unknown resistance in megohms
E = voltage indicated by voltage readout dials
E_m = voltage indicated on meter
10 = megohms of input resistance of VTVM circuit on 10, 1, and 0.1 null range

When connecting the unknown resistance to the input terminals, use short isolated leads to prevent measuring leakage resistance between the leads.

a. Resistances from 1 to 500 megohms. Perform proper preliminary procedures:

(1) Set the range switch to 500 and the null switch to 10.

(2) Connect the unknown resistance between input terminals.

(3) Adjust the voltage readout dials for full-scale meter deflection.

(4) Subtract 10.00 from the amount set on the voltage readout dials to find the resistance of the unknown in megohms.

b. Resistances from 500 to 5000 megohms. For this range the setup is the same except:

(1) Set the null switch to 1.

(2) Subtract 1.00 from the amount set on the voltage readout dials and multiply the result by 10 to find the resistance in megohms.

c. Resistances from 5000 to 50,000 megohms. For this range the setup is the same as for 1 to 500 megohms:

(1) Set the null switch to 0.1.

(2) Multiply the amount set on the voltage readout dials by 100 to find the resistance in megohms.

d. Resistances from 50,000 to 250,000 megohms. The setup is the same as for resistances between 5000 and 50,000 megohms. To read out the value of the resistance:

(1) Divide the amount set on the voltage readout dials by the amount of voltage indicated on the meter.

(2) Multiply the result by 10 to find the resistance in megohms.

Exercises (431):

1. What principle does the voltmeter in figure 3-16 operate on when used as a DC differential voltmeter?

2. For range control on the differential voltmeter to be effective, the null control must be in what position?

3. What is the normal differential voltmeter setup for the range and null switches prior to usage for voltage measurements?

4. What does the range switch measure when the null switch is in the VTVM position?

5. In order to read the voltage excursions on the differential voltmeter, what is the voltmeter set up to read?

6. Identify the feature of a differential voltmeter that allows it to measure high resistances. What values can be measured?

7. If you are attempting to measure an unknown resistance and you cannot obtain full-scale deflection on the readout dials, what action should you take?

8. What is the multiplier to be used for the indication of the voltage readout dials if the unknown resistance is between 5 and 50 kilomegohms?

432. Briefly describe a digital voltmeter and name the types of probe tips used with a sampling voltmeter.

Digital Voltmeter. The digital voltmeter is a compact, accurate, multifunctional device with a rapid response. The basic unit is a solid-state voltmeter that uses plug-in preamplifiers. The selection of a plug-in unit determines the operation of the unit.

A sampling voltmeter has the ability to accept waveforms that have large crest factors. These large crest factors insure accurate measurements of nonsinusoidal voltages. Measurements may be performed from 1 Hz up to 1 GHz and from 1mV to 1 volt full scale. The sampling voltmeter can be used in conjunction with true root mean square (RMS) or with peak-reading meters. A wide application is possible because of the availability of a variety of versatile probe tips. Voltages in receivers, amplifiers, and coaxial transmission lines can be measured with this instrument. The voltmeter is capable of retaining the indication on its meter until the indication is no longer needed. The sampling voltmeter uses an incoherent sampling method which has many of the advantages of conventional sampling.

Samples picked up by the probe are applied through attenuators and amplifiers to the zero-hold circuit, as shown in figure 3-17. Each sample is stored in the zero-hold circuit until the next sample is taken. The output of this circuit can be taken from the external terminals when measurements of 10 mV and higher are to be made. If these are RMS measurements, the RMS voltmeter is used; when these are peak measurements, then a peak-reading voltmeter is used. The output of the zero-hold circuit is also applied to a signal processor which has noise-reducing circuits for the lower ranges. A DC output is also available for an external recorder.

The probe tips that can be used with a sample voltmeter are a blocking capacitor probe tip and a tee-

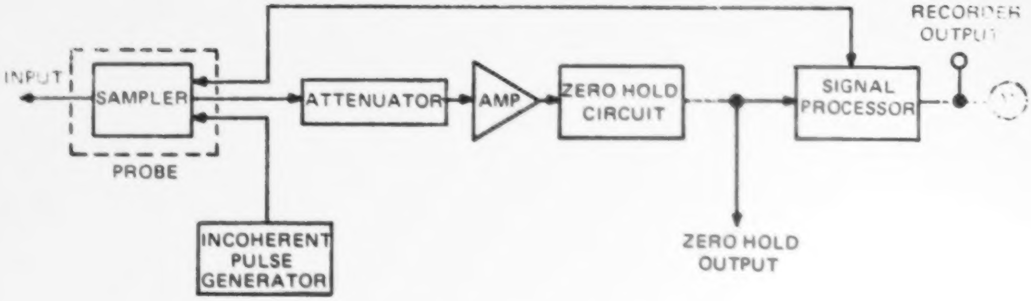

INPUT
SAMPLER
PROBE
ATTENUATOR
AMP
ZERO HOLD CIRCUIT
SIGNAL PROCESSOR
RECORDER OUTPUT
INCOHERENT PULSE GENERATOR
ZERO HOLD OUTPUT

Figure 3-17. Digital voltmeter, block diagram.

connector probe tip for coaxial line measurement. A feature of these probes makes it possible to retain a meter indication when you find it difficult to place the probe in the circuit under test and observe the meter at the same time. The meter indication is retained by using a pushbutton on the probe. By holding the pushbutton down, you retain the meter indication. By releasing the pushbutton, the voltmeter may be used to tab another measurement.

Exercises (432):

1. What is a digital voltmeter? Explain briefly.

2. What probe tips can be used with a sampling voltmeter?

433. Identify various measurements and measurement methods that can be made by an electronic counter.

In sequence, here we discuss the basic frequency counter and then high-frequency measuring methods. Under the first we examine eight subareas. Under the second we talk about four subareas.

Basic Frequency Counter. Electronic counters (often referred to as frequency counters) are the most accurate, convenient, and flexible of all the available instruments for making frequency and time interval measurements. Vacuum tube and solid-state electronic counters cover a wide variety of features. Features allowing counters and associated equipment to measure frequencies from 0 Hz to 40 GHz (4×10^9 Hz) and to measure time intervals from 10 nanoseconds (10×10^{-9} second) to more than 100 days.

Uses. An electronic counter is used for comparing an unknown frequency or unknown time interval with a known frequency or known time interval. The counter's logic is designed to present this information in an easy-to-read numerical display. The accuracy of this measurement depends, to a great extent, on the stability of the known frequency. This known frequency is obtained from the internal oscillator of the counter.

An electron counter best suited for a particular application is dependent upon the range and type of measurements to be performed. Types of counters available range from the basic instrument through complex units using input and output devices, such as digital recorders, digital clocks, digital-to-analog converters, scanners, and magnetic and optical tachometers.

Operation. An electronic counter has several basic functional sections. When these sections are interconnected, many different types of measurements can be made. The most important of these sections are:

(1) The decade counting assemblies whose numerical system totalizes and displays the count.

(2) The signal gate, which controls the count start and stop with respect to time.

(3) The time base, which furnishes the exact amount of time for controlling the gate for a frequency or pulse train measurement.

(4) Signal shaping, display control, logic control, and binary coded decimal output sections.

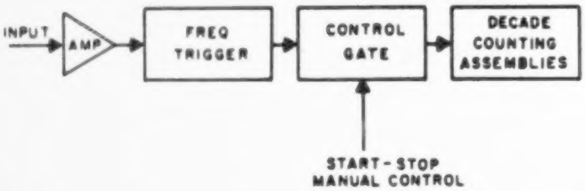

INPUT
AMP
FREQ TRIGGER
CONTROL GATE
DECADE COUNTING ASSEMBLIES
START-STOP MANUAL CONTROL

Figure 3-18. Electronic counter totalizing method, block diagram.

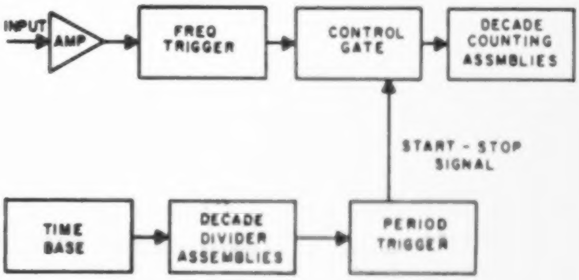

INPUT
AMP
FREQ TRIGGER
CONTROL GATE
DECADE COUNTING ASSMBLIES
START - STOP SIGNAL
TIME BASE
DECADE DIVIDER ASSEMBLIES
PERIOD TRIGGER

Figure 3-19. Electronic counter frequency measurement, block diagram.

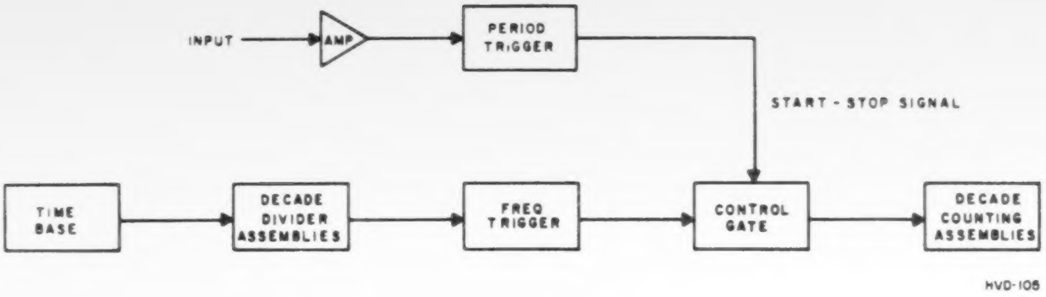

INPUT
AMP
PERIOD TRIGGER
START - STOP SIGNAL
TIME BASE
DECADE DIVIDER ASSEMBLIES
FREQ TRIGGER
CONTROL GATE
DECADE COUNTING ASSEMBLIES
HVD-106

Figure 3-20. Electronic counter period measurement, block diagram.

Totalizing measurements. An electronic counter can be operated in the totalizing mode with the control gate flip-flop controlled by the manual start-stop switch illustrated on figure 3-18. With the switch at START, the decimal counter assemblies totalize (add) the input pulses until the control gate is closed by changing the switch to STOP. The display on the counter then show the pulses received during the interval between manual START and manual STOP.

Frequency measurements. For frequency measurements, the input signal is first applied to a signal shaper, which changes the input signal to uniform pulses. The output of the shaper is next applied to the decade counting assemblies, often passing through a gate which is controlled by the time base of the counter, as illustrated in figure 3-19. The number of pulses, totalized in the decade counting assemblies for the desired period of time, represents the frequency of the input signal. The counted frequency is shown on a numerical readout with a positioned decimal point. This reading is held until a new sample is taken. The sample rate control decides the display time of the frequency measurement being performed. The sample rate control also starts counter reset and the next measurement cycle. The time-base selector switch determines the gating interval, positions the decimal point, and selects the proper measurement units.

Period measurements. The electron counter makes period measurements with its functions arranged as in figure 3-20. An unknown input signal controls the gate time. The time base frequency is counted in the decade counting assemblies. The input shaping circuit uses the positive-going zero axis crossing of successive cycles as a trigger for opening and closing the gate.

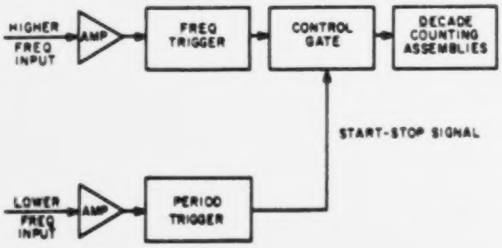

HIGHER FREQ INPUT
AMP
FREQ TRIGGER
CONTROL GATE
DECADE COUNTING ASSEMBLIES
START-STOP SIGNAL
LOWER FREQ INPUT
AMP
PERIOD TRIGGER

Figure 3-21. Electronic counter ratio measurement, block diagram.

A period of measurement gives a more accurate measurement of an unknown low-frequency signal because of increased resolution. A frequency measurement of 100 Hz on a counter, with a 10-second gate time, is displayed as 0000.1000 kHz. When you are using this same counter, a single period measurement of 100 Hz, with 10 MHz as the counted frequency, would be displayed as 0010000.0 microseconds. Therefore, it can be seen that resolution is increased by a factor of 100.

Ratio measurements. We arrive at the ratio of two frequencies by using the lower frequency signal for gate control and by having the higher frequency signal counted as in figure 3-21. By using the proper transducers, you can apply ratio measurements to any phenomena, providing the phenomena can be represented by sine waves or pulses. For example, using the ratio method, you can measure clutch slippage, gear ratios, frequency dividers, and frequency multipliers.

Rate measurements. By using a preset counter, or a counter with a preset plug-in unit, frequency measurements can be changed automatically to rate measurements by proper selection of the gate time. A plug-in unit may be set to a gate time of 600 milliseconds.

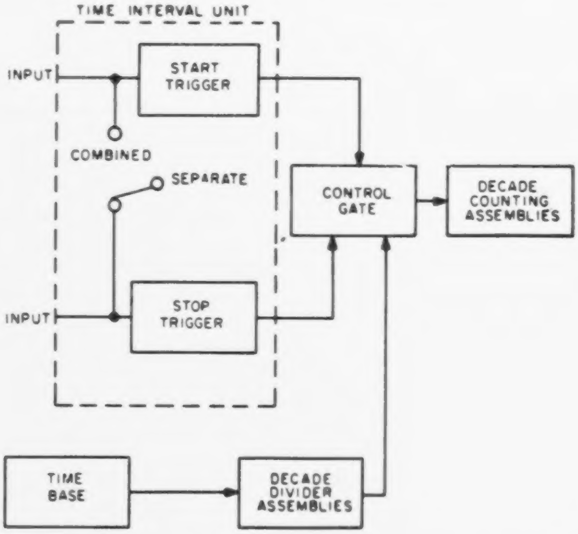

TIME INTERVAL UNIT
INPUT
START TRIGGER
COMBINED
SEPARATE
CONTROL GATE
DECADE COUNTING ASSEMBLIES
INPUT
STOP TRIGGER
TIME BASE
DECADE DIVIDER ASSEMBLIES

Figure 3-22. Electronic counter time interval measurement, block diagram.

This setting causes an input from a 100-pulse-per-revolution tachometer to be displayed directly in revolutions per minute.

Time interval measurements. Time interval measurements are similar to period measurements; the only exception is that the trigger points on the single waveform or waveforms are adjustable. Figure 3-22 illustrates that separate signals may be used as the start and stop signals, and when the COM-SEP switch is placed in the COM position, measurements may be made from one point on a waveform to another point on the same waveform. Triggering polarity, slope, and amplitude are selected for each channel separately. The time interval is displayed in microseconds, milliseconds, or seconds.

A time interval counter is available that can measure extremely short time intervals (10 nanoseconds to 0.1 second). A 1-MHz external frequency standard is multiplied to 100 MHz in order to obtain 10-nanosecond time increments as the counted frequency, resulting in good resolution.

High-Frequency Measuring Methods. Precise high-frequency measurements are possible because of several innovations in quartz oscillator crystal design. These innovations have resulted in a superior electron counter time basis. Ambient temperature affects the frequency by less than ±2 parts in 10^{10} per degree C throughout the range from $-20°$ to $+50°$C. The accuracy of the counter is limited by the time-base oscillator stability, because this oscillator circuit furnishes the definite time information for a measurement. The time base must be calibrated periodically, since the drift rate causes a cumulative deviation in frequency which can result in a measurement error. The accuracy of precision quartz oscillators is usually expressed as long-term stability and short-term stability.

Long-term stability refers to slow changes in average frequency with time due to physical material changes in the resonator or other elements of the oscillator.

Short-term stability refers to changes in average frequency over a time sufficiently short so that the change in frequency due to long-term effects is negligible.

Four methods have been developed which extend the digital frequency measuring capability of electronic counters. These methods are the prescaling method, the heterodyne method, the transfer oscillator method, and the automatic method. We shall explain each of the four methods and show the basic principles of operation in block diagrams.

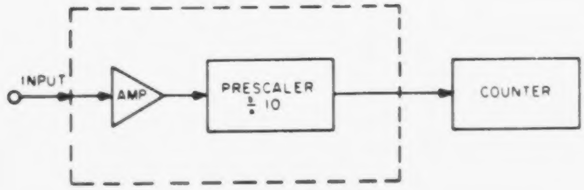


Figure 3-23. Electronic counter prescaling method, block diagram.

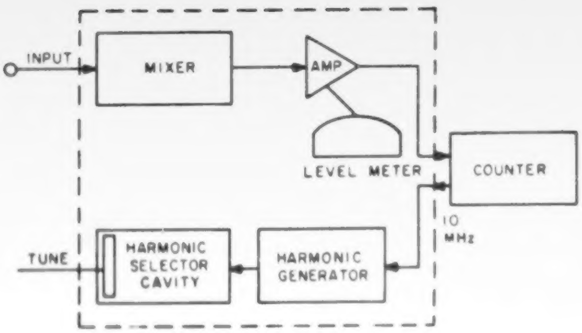


Figure 3-24. Electronic counter heterodyne method, block diagram.

Prescaling method. Figure 3-23 illustrates the prescaling method. The input signal is amplified and scaled by a decade in order to divide the input frequency by a factor of 10. The input to the counter from the prescaler is now within the direct measuring range of the counter. For example, if the prescaler is used in conjunction with a 10-MHz electronic counter, then the direct measuring range of the counter would be extended to 100 MHz.

Heterodyne method. The heterodyne method, illustrated in figure 3-24, is a high-frequency measuring method based on subtracting known reference frequencies until the difference frequency is within the direct measuring range of the electronic counter. The harmonic generator produces all of the harmonics of 10 MHz. The harmonic selector cavity is manually tuned until the selected harmonic, mixed with the input, produces a difference frequency that is fed through an amplifier. Then the output of the amplifier is applied to the counter. A level meter indicates when the harmonic selector has reached the proper reference frequency.

To find the frequency being measured, the reference frequencies are added to the electronic counter display. This addition usually involves nothing more than placing one or two digits before the counter reading.

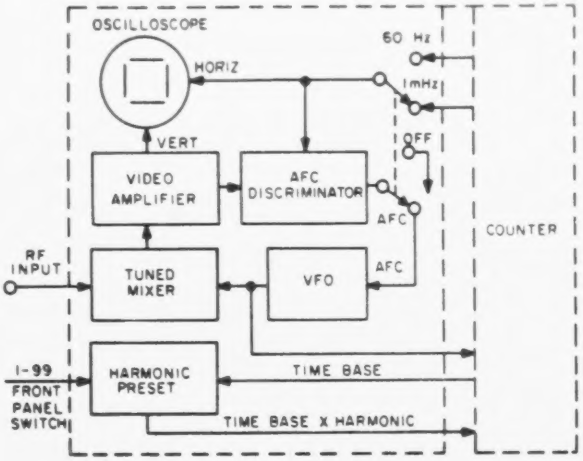


Figure 3-25. Electronic counter transfer oscillation method, block diagram.

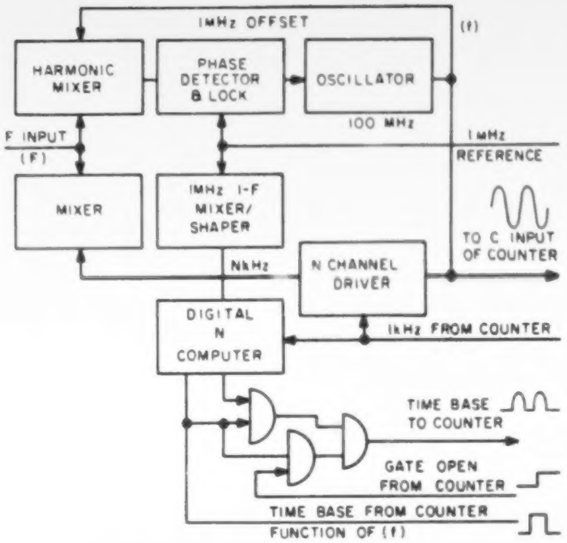


Figure 3-26. Electronic counter automatic method, block diagram.

Transfer oscillator method. This method provides an extremely wide measuring range with counter accuracy and is illustrated by figure 3-25. The transfer oscillator is used in conjunction with a 50-MHz electronic counter. The transfer oscillator method compares harmonics of a fundamental frequency with an unknown frequency.

When you are performing a measurement, adjust the fundamental frequency to the point where one of the harmonics is at the same frequency as the input signal. This is accomplished by beating harmonics against the input signal in a mixer and varying the fundamental frequency until the difference frequency is zero. The results can be observed on an oscilloscope. The counter is able to read out the unknown frequency when the fundamental frequency is multiplied by the harmonic number by use of the front panel harmonic preset switches. The proper harmonic number automatically expands the counting period of the counter. This expansion results in a direct presentation of the input frequency in the readout of the counter.

The transfer oscillator includes a phase-lock designed to synchronize itself with the input signal. Any tendency in frequency change in either the input signal or the transfer oscillator can be compensated for. This compensation is accomplished by changing the transfer oscillator frequency with the input signal.

Automatic method. Figure 3-26 is a block diagram of the automatic method. This method makes it possible to obtain instantaneous direct readings of unknown microwave inputs. An unknown signal (F) is fed into a harmonic mixer. A sweep oscillator frequency (f) is applied to a mixer and harmonics are generated and mixed with the input signal. A 1-MHz signal from the counter time base is used as a phase detector and locking frequency for the output signal of the mixer. This circuitry phase-locks the proper harmonic (N) of the sweep oscillator (f) with the input signal (F) at a precise 1-MHz offset.

The input signal (F) is also applied to a second mixer that has the same sweep oscillator signal (f) but with the addition of a 1-kHz signal from the counter. When the phase detector locks the sweep oscillator, the signal in this second mixer is N (f + 1 kHz), which is mixed with the input frequency (F). When the offset is exactly 1 MHz, the F = fn ± 1 MHz. The output of the second mixer is 1-MHz plus N kHz. The MHz signal from the counter is mixed with the output of the second mixer, and the resultant signal is N kHz. The mixed signal (N kHz) is then applied to a digital N computer circuit along with the 1-kHz signal from the counter. This circuit then divides the N kHz by 1 kHz, and the result is N pulses. The N pulses are gated in conjunction with the counter time-base signal. This gating extends the time base to N times the time-base switch position. This extension multiplies f × N ± MHz so that the counter can read out the unknown input frequency directly with the 1-MHz offset.

Exercises (433):

1. What is the function of an electronic counter?
2. What section of an electronic counter controls the count start and stop with respect to time?
3. What determines the gating interval when making a frequency measurement?
4. When using the electronic counter for making totalizing measurements, what does the display indicate?
5. Which type of measurement would be used to measure frequency dividers or frequency multipliers?
6. What does a time interval measurement display and how?
7. What is the purpose of using a prescaler with an electronic counter?
8. When using an electronic counter heterodyne method, how do you calculate the frequency being measured?

9. The automatic method features what type of readings?

434. Classify and name the types of signal generators, and state the basis of subdividing signal generators functioning in the lower frequency range.

Signal Generators. A signal generator is a test device that generates an alternating-current signal suitable for test purposes. It is, in effect, a small radio transmitter that can generate a signal of a desired frequency. The generated signal may be modulated or unmodulated, and it is used for the following tests or checks: alignment of tuned circuits, dynamic troubleshooting (signal tracing), sensitivity measurements, field-intensity measurements, and approximate frequency measurements.

The use last mentioned above is limited because the signal generator is not a frequency meter and cannot be relied upon as a frequency standard. Therefore, the signal generator is used principally in the alignment of tuned circuits.

Signal generators are classified according to frequency. There are of two types—audiofrequency and radiofrequency. Audiofrequency generators are sometimes called audio oscillators and are capable of producing signals whose frequencies range from 20 to 20,000 hertz per second. Radiofrequency generators provide practical outputs ranging from 10 kilohertz per second to about 10,000 megahertz per second.

No single generator completely covers all of the existing radiofrequency ranges. However, various radiofrequency generators covering specified portions of the radiofrequency spectrum are available. Many of these also have an audio output which is available through a separate front panel jack. (Generally, frequencies of 400 and/or 1000 Hz are provided.)

The shape of the output waveform permits a further classification of audiofrequency and radiofrequency generators. That is, audiofrequency generators are subdivided into sine-wave and square-wave (pulse) generators. Pulse generators may provide positive or negative pulses with variable repetition rate, width, and amplitude. They are frequently used with card test sets. Many are capable of being triggered externally, internally, or manually. By comparison, radiofrequency generators provide either a pure radiofrequency or a radiofrequency with amplitude modulation, frequency modulation, or pulse modulation.

Exercises (434):

1. How are signal generator types classified?

2. What are the types of signal generators?

3. What is the basis of subdividing signal generators used in the lower frequency range?

435. Explain briefly the use and advantages of digital logic probes, clips, and pulsers.

Logic Probes, Clips, and Pulsers. Logic probes, clips, and pulsers provide a faster less costly approach to the troubleshooting of logic circuits. Your understanding and proper use of these test instruments will simplify the troubleshooting of equipment using integrated circuits.

Logic probes. The logic probe is a state checker indicating the presence of a high (1) or low (0) at the point being tested. It is safer than the multimeter is. How? Because the logic probe lets you keep your eye on both the IC and the point you are testing, thus avoiding possible shorting of pins by test leads. It is simpler to use than the oscilloscope. Why? Because you need only connect the probe clip to the power supply of the circuit under test. Then you place the probe tip at the point to be tested and monitor the probe indications. Many designs are used for logic probes, but all will indicate either a 1 or 0 condition at the point being tested. Some logic probes have the ability to indicate an "undefined" condition at the point being tested (neither at 1 nor 0; a potential between the two levels). Some probes will indicate the presence of pulses. Still others have a switch selectable memory mode. In this mode the leading edge of a pulse will set a flip-flop to keep the pulse LED on the probe lighted. This latter type may often be used in place of a storage scope. A logic probe may be compatible with only one logic family TTL and DTL. Others allow the selection of CMOS with a selector switch.

Logic clip. The logic clip is an IC operation monitor. Clamped over an IC DIP package and two rows of LEDs, the logic clip instantly indicates the logic states of all pins of the package. No controls are involved, not even a power lead to connect. The clip automatically locates the positive and ground potentials of the package being tested or monitored.

The logic clip can give indications faster than a logic probe with static or slowly changing signal conditions. However, you will experience some limitations when you use logic clips. For example, you cannot monitor many fast-changing LEDs at the same time. You must also consider the voltage requirements of the IC being checked. In addition, some clips are limited to 7 volts, while others may be used for higher voltage levels. Furthermore, clips also operate with positive voltage logic families, which means they will not work with some MOS ICs and ICs requiring more than one voltage level. Also, the logic clip cannot indicate a bad level. It will only indicate a high (1) or low (0).

Logic pulser. The logic pulser is a high-quality pulse generator without controls. It is used to manually trigger the circuit being tested. You just clip the pulser's leads to the power supply of the circuit under test, touch the pulser probe to the point to be activated, and press the pulse button. The pulse thus generated will momentarily drive all circuits connected to this test point to their opposite state. Outputs as well as inputs are driven to the opposite state, whether the test point is high or low. Holding the pulse button in will generate a series of pulses or a pulse chain. The logic pulser is usually used in conjunction with a logic probe or clip when checking circuit operation.

Exercises (435):

1. Briefly indicate how to use a logic probe.

2. What is the advantage of a logic clip?

3. How do you use a logic pulser for testing ICs?

436. Specify types of special-purpose test sets and the general functions they perform.

Special-Purpose Testers. Each type of computer or switching system may have test sets that apply to only that system. These test sets may be portable or may be part of the system. Each will have its own function or purpose in the maintenance of that system.

Trouble analyzers. The trouble analyzer is used to test suspected assemblies without their being removed from the equipment cabinet. Data processors usually process data in both serial and parallel form, and the circuits that process the data must be checked. The trouble analyzer, for example, can compare two serial words bit for bit. One word is produced by the analyzer and is used as a standard. This standard word is processed by the circuits under test and then fed back to the analyzer for comparison with the original word. The analyzer may also be of the type that injects a signal or frequency into the circuits under test and then compares the circuit outputs to a given standard. The office routiners or circuit testers of switching systems operate on this principle. Essentially these test sets analyze system operation by simulating connections through the system. They may also test the signaling capability of circuits used to connect subscribers or terminals to the system.

Drawer testers. The drawer tester is used within some systems for the testing and troubleshooting of equipment drawer or shelf assemblies. When a system malfunction has been isolated to a particular drawer assembly, the suspected drawer is removed and connected to the test set. Depending upon the type of tester, an appropriate program is selected. The programmer may be a pluggable program board, a series of switch settings on the tester, or even a tape or card program.

Each of these test sets operates in basically the same way. The drawer is tested by the test set automatically exercising each circuit in the drawer in a preprogrammed sequence. The input and output signals of the drawer are evaluated at each programmed step by comparator circuits. Each satisfactory response indicates a GO (sequence advance) signal, which causes the drawer test set to advance one step and automatically evaluates the next programmed function. In some cases, circuit complexity makes it impractical to perform the entire test procedure automatically. Auxiliary test equipment is connected to the tester in order to make the necessary additional checks manually. During these manual operations, the automatic sequencing of the test advance is interrupted, but it is resumed after the manual test has been completed. You may also be able to select the manual mode of operation so that you can examine outputs at any particular test step.

The manual mode of operation will often permit the use of visual comparison of signals instead of using the test set comparator. The test set control circuits provide the required control and timing signals that cause the signal generator to activate the drawer under test. The drawer outputs are then checked at the test points with auxiliary test equipment and compared with prescribed performance standards. If the indications are correct, the STEP, START, or ADVANCE pushbutton is depressed to advance the test set to the next test step.

When a malfunction occurs during the performance of a test procedure, it is necessary to determine the location of the trouble by using:

- Test block diagrams.
- Test set logic diagrams.
- Drawer under test logic diagrams.

Some drawer testers will isolate a trouble and identify the printed circuit card at fault. Your placement of the printed circuit card returns the drawer and system to operating status. However, you may be required to repair the circuit card.

Card testers. Each different type of card requires specific input and output conditions for accurate testing. Since the using system often requires thousands of cards, you could conclude that the problem of designing a card tester would be insurmountable if each type of card had a different requirement for testing. This is not true, however, because designers of modern-day equipment have developed a system for the standardization of cards.

In any system there are requirements for basic circuits, such as AND-gates, OR-gates, and diode matrices. The number of combinations of these basic circuits is almost unlimited; however, the number of different types of individual circuits is limited to a relatively small number. Cards are assembled, using capacitors, resistors, diodes, and other components necessary for the formation of one or more basic circuits. All components and circuits on the card are connected to a connector strip at one edge of the card. This procedure makes it possible to use variations in external wiring to connect various components on the card to form the required circuits. One card, for example, may be connected to form four flip-flops with their associated input and output components. When four of these cards are used, a 16-stage shift register, storage register, or counter can be constructed simply by making variations in external wiring. A small number of different kinds of cards can be used to form the many circuits required by the computer or switching system. Some data processors use as few as five different kinds of cards. This standardization of cards also makes card testers practical in that they need be programmed to check only a limited number of standard cards. Test sets generate test signals and provide test loads and voltages that simulate actual input and output operating conditions for the plug-in cards or modules under test. Setups and programs for card testers vary; however, all of them simulate operating conditions when testing cards. Most testers have test jacks at which circuit functions are available for application to external test equipment such as the oscilloscope.

Exercises (436):

1. How does a trouble analyzer test set check equipment operation?

2. What is the function of a drawer tester?

3. In the manual mode, how may drawer testers operate?

4. What does the use of connector strips make possible with card testers?

5. How is a card tester used for repair of subassemblies?

437. List safety precautions applying to test equipment.

Test Equipment Safety Precautions. There are numerous safety precautions that you must observe while using portable test equipment to avoid injury to personnel. We have divided this into two areas, as indicated next.

Precautions applicable to all electrical measuring instruments. Three basic precautions that apply to all electrical measuring instruments you must work with are:

a. Avoid mechanical shock. Instruments contain permanent magnets, meters, etc., which are sensitive to shock. Heavy vibrations or shock can cause loss of calibration to the instruments.

b. Avoid exposure to strong magnetic fields. Strong magnetic fields may permanently impair the accuracy of an instrument by leaving residual magnetic effects in the magnet, iron parts, or in the magnetic materials used to shield the instruments. Locations subjected to strong magnetic fields include regions near the pole pieces of large motors and generators, degaussing coils, and radar magnetrons.

c. Avoid excessive current. This includes various precautions, depending upon the type of instrument. When in doubt, use the maximum scale range of the instrument. You should make connections while the circuit is deenergized, if possible, and then check all connections to insure that the instrument will not be overloaded before energizing.

Precautions observed to avoid instrument damage. Certain safety precautions for you to observe to avoid instrument damage include the following:

a. Avoid contacting the coils of wattmeters, frequency meters, and power meters, because they may carry excessive current even when the meter pointer is on scale.

b. Never short-circuit the secondaries of current transformers when the primary is energized.

c. Never short-circuit the secondaries of potential transformers when the primary is energized.

d. Insure that meters in motor circuits can handle the motor starting current, which may be as high as six or eight times normal running current.

e. Never leave an instrument connected with its pointer off scale or deflected in the wrong direction.

f. Never attempt to measure the internal resistance of a meter movement with an ohmmeter, as the movement may be damaged by the current required to operate the ohmmeter.

g. Never advance the intensity control of an oscilloscope to a position that causes an excessively bright spot on the screen or permits a sharply focused spot to remain stationary for any length of time.

h. When checking electron tubes with a tube tester, always perform the interelement short test first. If the tube is shorted, make no further tests.

i. Before measuring resistance, always discharge capacitors in the circuit to be tested. Note and record any points not having bleeder resistors or discharge paths for capacitors.

j. Always disconnect voltmeters from field circuits or other highly inductive circuits before opening the circuit.

The unsafe use of portable test equipment there can produce hazardous situations—situations extremely dangerous to personnel. For example, you may have an oscilloscope plugged into one receptacle, an electronic voltmeter plugged into another, and a soldering iron in still another, using an extension cord, or many other combinations. Some of these hazards presented by such situations are coming into contact with live terminals or test leads, or accidentally throwing the equipment to the deck, thereby perhaps entangling personnel in the leads or cords and causing severe or fatal shocks. In addition, if the situation is such that a potential difference exists between the metal cases of two or more instruments, this potential may be sufficient to cause harmful shocks.

Wires attached to portable test equipment should extend from the back of the instruments away from the observer if possible. If this is not possible, they should be clamped to the bench or table near the instruments. When used in places where vibration is present, the instruments should be placed on pads of folded cloth, felt, or similar material.

Exercise (437):

1. List the three basic precautions that apply to all test equipment.

2. List certain safety precautions to observe to avoid damaging instruments.

3. Indicate some hazards presented by the unsafe use of portable equipment.

438. Identify certain factors which contribute to breakdown of the test equipment, and tell how to prevent or minimize moisture and dust effects on electronic equipment.

Care and Handling of Test Equipment. You must be extremely careful in handling any test equipment, even though you may not use it in your own maintenance program. (Prevent damage to organization test equipment of all types.) Some of the test equipment you use may require specific handling procedures. However, there are several things which are detrimental to all precision test equipment—rough handling, moisture, and dust. Bumping or dropping a test instrument (even a short distance) destroys the calibration of the instrument and can cause circuit damage. Careless handling of test cables can damage connections and thereby affect cable characteristics. Even minor cable damage can affect the accuracy of measurements.

Moisture is another common cause of test equipment failure. Moisture is minimized in many of the more complex items of electronic test equipment, such as signal generators and oscilloscopes, since they have built-in heaters. These heaters should always be operated for several minutes before you apply the operating voltages to the tester. Although most items of test equipment are not tropicalized and fungus-proofed to reduce the danger of high-voltage breakdown, some components of the testers—such as relays, connectors, and tube sockets—cannot be so treated. Always store such test equipment in a dry place if possible.

Excessive dust and grime inside an item of test hardware may also affect its accuracy and reliability. Be sure that all of the assembly screws which hold the case of the tester in place are secure. As an added precaution, always replace dust covers when the tester is not in use. If a tester has a case, and if the environment is not temperature and humidity controlled, replace the tester in its case after use. Test equipment that contains meter movements is especially delicate. Make certain that the amplitudes of all input signals are within the range of a meter if you want the movement to retain its accuracy. Keep all testers with meter movements away from strong magnets.

The instructions (included with each item) for properly stowing test equipment cables and other accessories should be strictly adhered to. Improper stowage of accessories causes changes in their characteristics, intermittent troubles, and in general, unreliable indications.

All of the procedures we have mentioned are basic and simple, but they are very often neglected. It takes only a few minutes to heed these precautions and to follow these procedures. Still, they can save you many hours of wasted effort.

Exercises (438):

1. What are the three factors that adversely affect test equipment?

2. How can you prevent or minimize the effects of moisture and dust that collect in and on electronic test equipment?

439. Give the purpose and unit or level responsibilities of a preventive maintenance program for test equipment.

Preventive Maintenance. Exercise preventive maintenance with all maintenance-support equipment. The idea of preventive maintenance is applied to all test equipment. You should anticipate and seek out possible troubles which can lead to test-equipment breakdown. The location of your particular organization and your test equipment inventory determines exactly what preventive measures you must observe. Basically, your preventive maintenance program should include systematic inspection of all test equipment in your inventory. We will elaborate on this later when we discuss the different categories of test equipment.

The responsibility for having operational test equipment rests entirely upon your organization. The responsibility for maintenance of the test equipment can be either partly or entirely upon your organization, depending upon what equipment you are authorized. A preventive maintenance program for test equipment should be set up and maintained. This program, in addition to correcting minor troubles and caring for specialized test equipment, must use the services of the *precision measurement equipment laboratory* (PMEL). A PMEL has the tools, standards, parts, and equipment for precision calibration of common commercial and military standard test equipment. They also have the training and facilities to perform services and repairs that require subsequent readjustment, realignment, and recalibration of these test items. Test equipment maintenance charts or procedures should include periodic inspections of test equipment to determine when

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such equipment must be rotated for PMEL inspection and calibration, or for higher level maintenance.

Unless you have fully trained test equipment maintenance personnel in your activity and have all of the proper equipment needed to perform the maintenance, you should perform only the most superficial maintenance on common commercial and military standard test equipment. This type of maintenance is limited to such things as resetting the pointers of meters to zero when the meters are equipped with external adjustments, or of placing tape on a cracked glass or case to keep out dust and moisture temporarily. Only in a dire emergency or in a grave tactical situation should you attempt maintenance on test equipment which does not fall within your normal scope of maintenance. Even then, you should get the approval of the maintenance officer. When such repairs are made, they should be noted on a tag, and the tag should be attached to the instrument. Permanent repair by the PMEL should then be made at the earliest opportunity.

Remember that normally you are limited to only that maintenance you can perform on test equipment and still have it function accurately and reliably. Your maintenance is limited when you do not have the training, the tools, the maintenance equipment, the standards, and/or the spare parts necessary—and when directives prohibit such maintenance. You must realize the limitations. Do not make repairs when there is a possibility of circuit misalignment or calibration inaccuracies unless you are directed to perform such maintenance by the proper authority. You should carefully review TO 00-20-14, *Air Force Metrology and Calibration Program.* The list that follows is included so that you can compare the definitions for the four equipment categories and establish differences between them. When these differences are established, you have no trouble deciding the category number for a given item of equipment.

Category I. This is operational equipment installed in systems, subsystems, or equipment the performance parameters of which are to be measured, verified, or tested.

Category II. Included here is the peculiar precision measurement equipment used to check out, maintain, and calibrate Category I equipment. ("Peculiar" applies to precision measurement equipment designed for and used only on one system, subsystem, or equipment as contrasted with "common" items which have general-purpose cross-system applications.)

Category III. In this category comes common commercial and military standard precision measurement equipment used for maintenance, troubleshooting, testing, verification, and calibration of Categories I and II equipment.

Category IV. Standards and accessories used to calibrate Categories II and III equipment belong in this category. This equipment normally is located in and used by the base PMEL.

Two organizations have the primary responsibilities for maintaining all equipment in Categories I and II. They are (1) the using organization of which you are a part and (2) the base's PMEL. As part of the using organization, you are responsible for the calibration of all Category I and Category II equipment, with the following exceptions:

a. Base PMEL calibrates all general-purpose and commercial Category II test equipment that can be moved to the PMEL. This does not include test equipment that must be calibrated while it is in your bench equipment.

b. Maintenance of test equipment that requires special skills or special equipment (whether it be Category I or Category II) that is available only at the PMEL is the responsibility of the base PMEL.

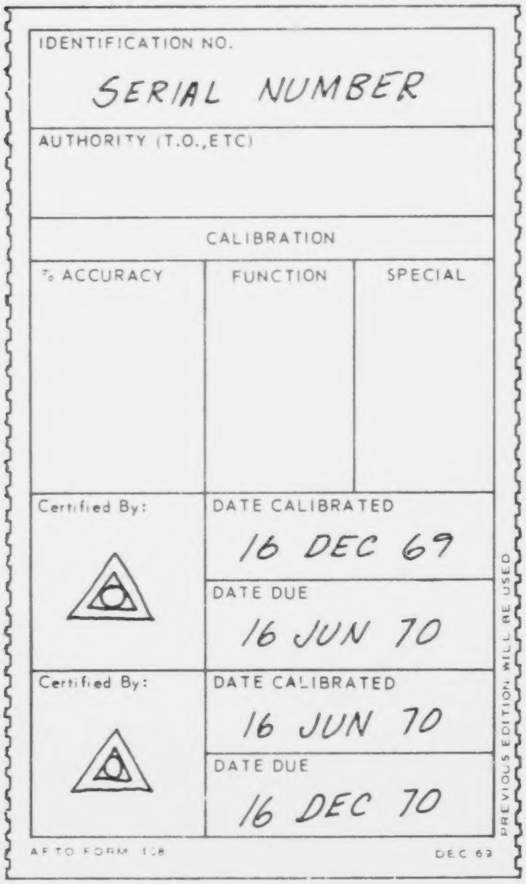
If you are in doubt as to whose area of responsibility a specific piece of test equipment falls into, go to your technical order file and refer to TO 33K-1-01, *Calibration Procedures and Responsibilities.* This TO lists all test equipment in the Air Force inventory, tells who is responsible for its calibration, lists any applicable TO containing the procedures for calibration, and lists the maximum number of days between required calibrations.

Exercises (439):

1. What is the purpose of a preventive maintenance program?
2. What is there about a PMEL makes it best qualified to be responsible for precise calibration of common commercial and military standard test equipment?
3. Normally, to what extent can you perform maintenance on test equipment?
4. Who is responsible for maintenance of Category IV test equipment?
5. Who is responsible for maintenance of Category I and Category II test equipment?
6. Where should you look when in doubt about who is responsible for specific equipment?

440. State which TOs assign scheduling responsibilities, list all of the types of certification labels (AFTO forms) used on test equipment, and cite specific characteristics of selected labels.

PMEL Equipment Scheduling Procedures. You will recall from our discussion of maintenance documentation reports that the maintenance supervisor receives a report which identifies test equipment that is



IDENTIFICATION NO.

SERIAL NUMBER

AUTHORITY (T.O.,ETC)

CALIBRATION

% ACCURACY | FUNCTION | SPECIAL

Certified By:

DATE CALIBRATED

16 DEC 69

DATE DUE

16 JUN 70

Certified By:

DATE CALIBRATED

16 JUN 70

DATE DUE

16 DEC 70

AFTO FORM 108

DEC 63

PREVIOUS EDITION WILL BE USED

Figure 3-27. AFTO Form 108, certification label.

due an inspection. The reason for this is that the PMEL section should automatically schedule your test equipment and call for it when calibration is required. Normally, the materiel control office in the maintenance organization is responsible for the equipment being delivered to PMEL on the date scheduled and then returned to the maintenance work center when calibration is completed. Materiel Control also normally handles unscheduled maintenance requests on equipment for which the PMEL is responsible. However, test equipment that is an integral part of your equipment or system and which cannot be removed, but requires special skills and equipment for calibration, may be calibrated by the using organization with the assistance of PMEL personnel.

TOs which govern test equipment scheduling and calibration are TO 33-1-14, *Calibration and Certification of PME,* and TO 33K-1-100, *Calibration Technical Orders—Responsibilities and Calibration Measurement Areas.* These TOs govern the handling and scheduling of test equipment that you will be using.

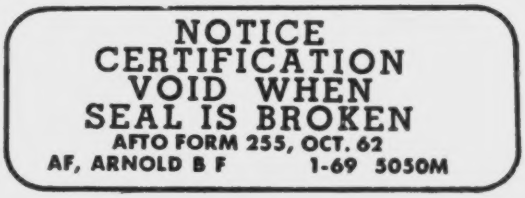
The following sections cover the forms and labels that you will encounter most frequently when using precision measuring equipment.

Certification Label (AFTO Form 108). This label, shown in figure 3-27, is completed and affixed to standards and PME certified by all Air Force calibration laboratories. It is also employed by the using organization to record calibration of equipment. Authorized PMEL personnel fill out and affix this label.

As indicated in figure 3-27, when the piece of equipment is calibrated, the technician puts a certification stamp in the Certified By block. The next due date is then entered in the adjacent Date Due block. After the second inspection and when all blocks have been filled, the label is removed and a new one is affixed by authorized PMEL personnel at the next inspection. The only time you, as a technician, will make entries on this form is when you are authorized by special order to certify calibration.

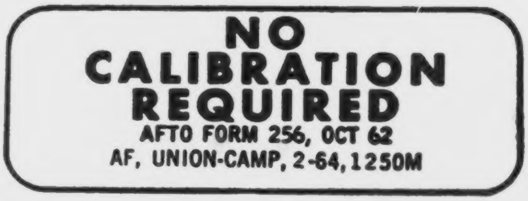
Notice Certification Void When Seal Is Broken (AFTO Form 255). Refer for this to figure 3-28. This is a seal that PMEL attaches to all standards and to all items of PME which have adjustments that affect calibration. This seal is not required on mechanical zero adjustment screws located on electrical indicating meters. The seal is applied in such a manner that any attempt to repair or adjust the equipment will result in breaking the seal. When it is broken, certification of calibration accuracies is no longer valid. Recertification must be accomplished by PMEL if calibration accuracy is in question.

No Calibration Required (AFTO Form 256). Use TO 33K-1-100 to determine which items are to be labeled with AFTO Form 256, which is shown in figure 3-29. Obtain the forms from the local PMEL. Usually, PMEL will furnish a stamped or initialed form to the user for application. However, the form can be certified by the user simply by initialing it. Other forms and labels are used in conjunction with PME; however, these mentioned here are the most common.



NOTICE
CERTIFICATION
VOID WHEN
SEAL IS BROKEN
AFTO FORM 255, OCT. 62
AF, ARNOLD B F 1-69 5050M

Figure 3-28. AFTO Form 255, certification void seal.



NO
CALIBRATION
REQUIRED
AFTO FORM 256, OCT 62
AF, UNION-CAMP, 2-64, 1250M

Figure 3-29. AFTO Form 256, No Calibration Required.

Exercises (440):

1. List the TOs which cover the scheduling and handling of test equipment.

2. Name the AFTO form which is commonly affixed to test equipment.

3. Which of the AFTO forms mentioned in BOF segment 444 may be certified by the user without special orders?

3-3. Air Force Computer and Switching Systems

The number of computer and switching systems used by the USAF prohibits the covering of each in this text. Therefore, we will only look at a few of the major systems which you may encounter.

441. Define AUTOVON and AUTODIN, and cite basic AUTOVON and AUTODIN configurations and functions.

Here we go into AUTOVON 490L first and AUTODIN second. Six subareas are covered in these two topics.

AUTOVON 490L. The *overseas automatic voice network* (overseas AUTOVON) is the Defense Communications Agency's (DCAs) direct distance dialing telephone network. This network links overseas defense installations and other official users and, together with similar facilities in the continental United States (CONUS), provides these users with rapid-access high-quality worldwide telephone and data communications.

In broadest terms, the AUTOVON switch facility is a circuit-switched telephone switching center that enables subscribers to dial telephones on a worldwide basis.

All switching is performed automatically, on a four-wire basis, in response to addressing signals received from the caller or stored in the originating switching center. Long-haul connections are established by forwarding the addressing information from switching center to switching center, as requested by each center added to the chain. Automatic alternate routing is provided, and all sending of addressing information is done by the controlling switching center. A normal connection through the AUTOVON network is completed in approximately 4 seconds.

The switch facility includes correed (encapsulated relay contact) matrices to perform the circuit switching on a space-divided basis; a random-access, electrically alterable memory; and electronic, space-divided and time-divided common control and marker circuits. Dial pulse (DP), 2/6 multifrequency (MF) nonconfirmation, 2/6 multifrequency (MF) confirmation, and 2/8 dual-tone multifrequency (DTMF) address signaling modes are used as applicable for the source and destination of each call.

The switching (correed) matrices are housed in five-drawer cabinets, while the electronic and other electromechanical equipment is housed in gate cabinets. Dial service assistance (DSA) operator, supervisor, and training consoles, battery racks, power rectifier cabinets, distributing frames, and cable racks are used as needed to house other equipment and intercabinet cables. Figure 3-30 shows the physical arrangement of a typical AUTOVON switch facility.

Switch facility functions and features. Each AUTOVON switch facility performs its switching functions in this manner:

a. Operates as a four-wire automatic switching center.

b. Functions as a common control, space-divided switching system, employing a solid-state memory array for programming traffic handling in the switching equipment.

c. Is capable of handling all voice and analog signals that can be passed over wideband voice circuits.

d. Accepts addressing signals from four-wire subscriber subsets arranged for DTMF signaling.

e. Accepts DP signals from private branch exchange (PBX) trunks and sends DP signals to PBX installations equipped for direct inward dialing.

f. Performs all tandem switching functions with other AUTOVON switching centers on a four-wire basis, using MF confirmation address signaling.

g. Is equipped with two or more DSA operator positions if the switch facilities have DSA. Here the operator gives special services for completing calls, placing delayed calls, arranging random conference calls, etc. Calls requiring operator service from switch facilities without DSA equipment are routed to the nearest DSA-equipped switch facility on general-purpose interswitch trunks.

Precedence levels. AUTOVON has five levels of precedence in accordance with the joint uniform telephone priority system. Here are these five levels:

4 - ROUTINE
3 - PRIORITY (P)
2 - IMMEDIATE (I)
1 - FLASH (F)
0 - FLASH OVERRIDE (FO)

The caller selects the precedence for each call, dependent upon the highest authorized level stored for that individual's line in the serving switching center memory. Memory of the precedence of each call is stored at each switching center in the call path. Thus, when a precedence call (i.e., a call with precedence higher than routine) encounters an all-trunk-busy condition, or if the call line is busy, the switching center at which the busy condition is encountered preempts a trunk serving a call of lower precedence or, in the case of a busy line, preempts the line if the call in progress is of lower precedence. The preempting switching center sends a measured supervisory signal in both directions to instruct

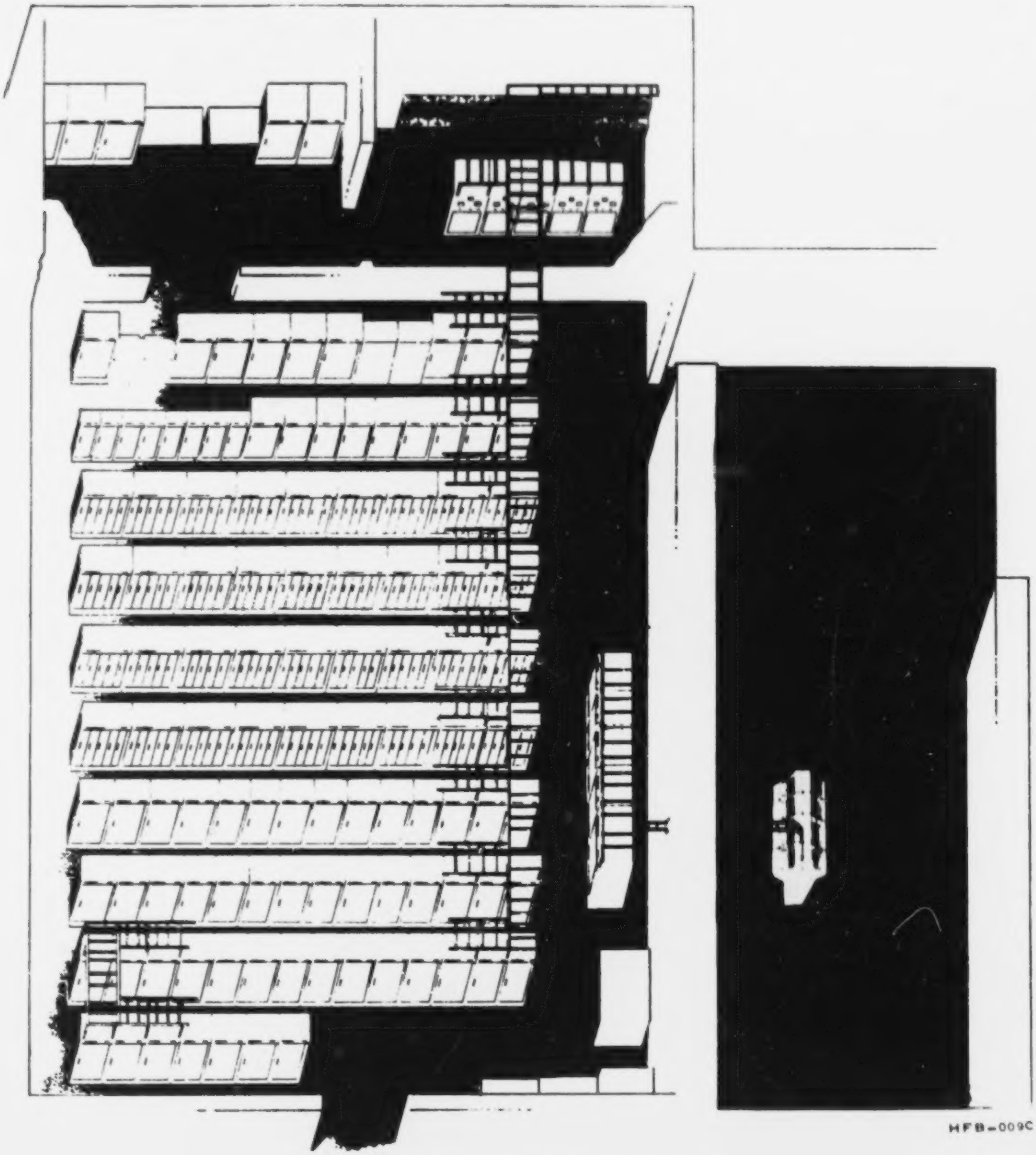


Figure 3-30. Typical AUTOVON switching facility.

all other switching centers in the call path to release the connection. The originating and terminating switching centers send a distinctive preemption tone to their respective affected stations until the user hangs up. If the preempting call is destined for a busy line, the station begins to ring at the precedence rate as soon as the user hangs up. Note that both the ringing signal and the audible ringing tone (ringback signal) are interrupted at an accelerated rate for precedence calls to indicate an urgency above the routine.

AUTODIN. The *automatic digital network* (AUTODIN) is a highly complex computerized communication system designed to transmit and receive narrative messages and data traffic from originators to addressees quickly and securely. AUTODIN is the world's largest, most advanced, high-speed digital communication system.

The AUTODIN consists of all AUTODIN switching centers (ASCs) and all connected terminal stations. This fully automatic switching network is designed, engineered, and programmed to provide continuous operation with a minimal loss of service and no loss of traffic. A general purpose communication network, it

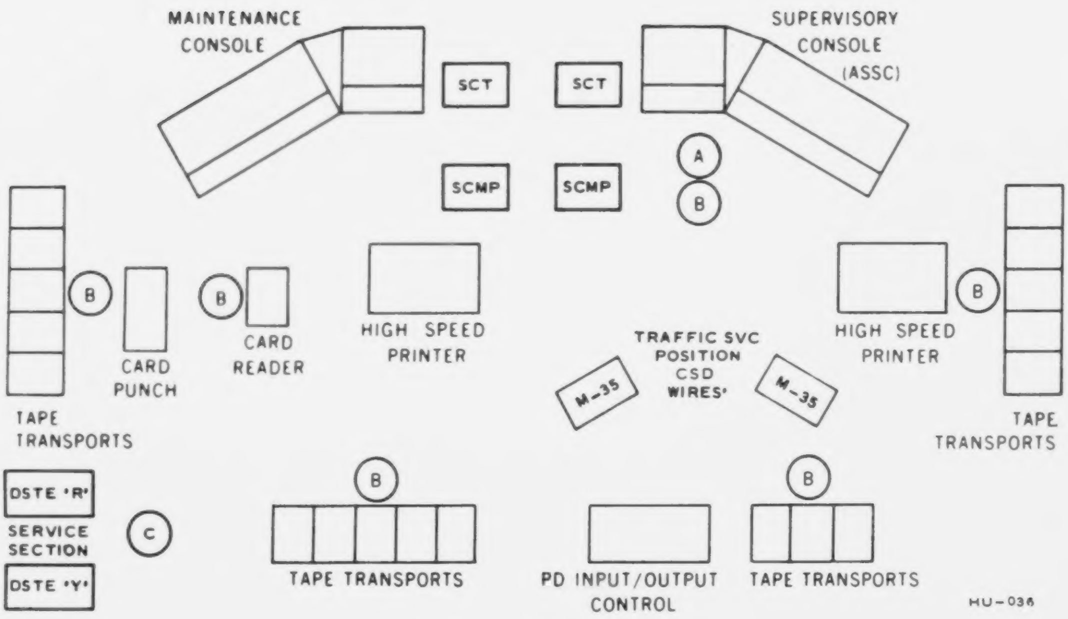


Figure 3-31. Typical ASC floor plan.

provides record communication service to Department of Defense (DOD) and other Federal Government agencies. It is used to transmit and receive administrative, operational, logistical, and statistical message traffic. In its present configuration, the system consists of 17 automatic switching centers (ASCs) and approximately 1500 subscriber terminal stations. The continental United Stated (CONUS) portion of the network is made up of 8 ASCs and about 950 terminal stations, while the overseas portion consists of 9 ASCs and approximately 550 terminals. The eight CONUS ASCs and one overseas ASC (Wahiawa, Hawaii) are leased from and maintained by Western Union Telegraph Company. The remaining overseas switches are Government owned and are maintained and operated by the military departments.

Various types of media can be accommodated by the network. These medias are paper tape, electronic accounting machine (EAM) cards, and magnetic tape. The individual applications of the media are defined as language media format (LMF). Depending upon the needs of the facility being served and with the proper equipment configuration, any combination of these language media can be used at terminal locations.

The system will also accept, convert, and process variations of digital data codes. The conventional teletypewriter five-level code known as International Teletypewriter Alphabet Number Two (ITA#2) can be processed along with the more sophisticated eight-level codes known as Fieldata and American Standard Code for Information Interchange (ASCII). Whereas the latter two codes have the capability of maintaining character integrity through assignment of parity and control characters, the former has no such capability. The system accepts and converts, back and forth, between the Hollerith and ASCII codes for EAM cards.

The AUTODIN switching centers (ASCs) are the facilities that integrate all diverse facets of the network into a common system. Figure 3-31 shows a typical ASC floor plan. Each ASC uses computers to process the messages. It uses buffers to compensate for differences in speed by using a combination of magnetic disks, mass memory units, and magnetic drums to temporarily store messages while they are in the ASC. It uses magnetic tapes to make permanent recordings of the messages processed and to keep a history of the processing surrounding each message. Each ASC operates on a full-time basis.

At the ASC, messages are queued and dispatched sequentially within each precedence level. The ASC interprets precedence level prosigns and will interrupt a lower precedence for the highest precedence level (FLASH) traffic. Messages that have been interrupted for FLASH traffic are queued and subsequently retransmitted.

Traffic is processed in accordance with digital data code, precedence, language media format, security classification, and subscriber identifying routing indicators.

As you will see in the following paragraphs, the AUTODIN system was developed to provide the maximum attainability in speed, security, accuracy, and reliability.

Speed. AUTODIN circuit speeds vary with a range from 75 baud (94-100 wpm) to 4800 baud (6000 wpm), depending upon the type of equipment used and the communication requirement of the using activity. Trunk circuits used between ASCs operate from 2400 to 9600 baud. NOTE: The word per minute (wpm) rate can be determined from the baud rate. Divide the baud rate by 4 and then add the quotient to the dividend. For example:

$$\begin{array}{r} 1200 \text{ (quotient)} \\ 4\sqrt{4800 \text{ baud rate (dividend)}} \end{array} \qquad \begin{array}{r} 4800 \\ +1200 \\ \hline 6000 \text{ wpm} \end{array}$$

Security. The AUTODIN system uses link encryption. Each circuit link with a requirement for passing classified information is secured by cryptographic equipment that insures the protection of all classified information. The ASC also provides a means of detecting and preventing the transmission of classified information over those circuits which are nonsecured.

Accuracy. Accuracy is obtained through the use of error detection codes and correction functions. These methods insure that each character of a message is accurately preserved from the time it is introduced into the network until it reaches its final destination. Automatic accuracy control features at both the ASC and tributary stations insure that not more than one error in 10,000,000 characters processed goes undetected. ASCs are engineered to automatically correct detected errors or to initiate an alarm to the operator identifying the errored condition. Processing of other traffic continues while alarm conditions are being presented to the operator for action.

Reliability. Each ASC has two identical computers for processing of message traffic. Other spare peripheral equipment is available, thereby providing a complete backup for the on-line system. One computer remains on-line at all times processing traffic, while the other computer may be used by Maintenance, programmers, and for off-line operational functions. These computers are periodically reversed to permit testing and maintenance which does not affect the normal processing of daily traffic.

AUTODIN is a solid-state transistorized digital transmission system. The built-in capabilities of the AUTODIN system are supplemented by special features which make it a unique communications system.

Exercises (441):

1. What is AUTOVON?

2. How does each AUTOVON switch facility perform its switching functions?

3. What is AUTODIN?

4. Name three codes—one five-level and two eight-level—the AUTODIN system can process, tell which is (are) superior, and explain briefly why.

5. What is the range of the functioning circuit speeds at which AUTODIN works?

6. The AUTODIN system uses ________ encryption to maintain security.

7. To maintain functional reliability through testing and maintenance while, at the same time, not affecting normal daily traffic processing, what is done with which AUTODIN computers?

442. Specify certain configurations, elements, and equipment related to 407L TACS and indicate selected functions or operations performed in TACS.

Tactical Air Control System (TACS/407L). The tactical air control system includes the organization and equipment needed to plan, direct, and control tactical air operations and to coordinate air operations with other services. It is composed of control agencies and communications-electronics facilities that provide the means for centralized control and decentralized execution of missions.

The TACS/407L is the system designed to fully exploit the flexibility of air power in a tactical environment. As a mobile system, it provides a component commander with the equipment and information necessary to plan, to direct, and to control tactical air operations. The heart of the system is the Hughes 4118 computer and its associated peripheral equipment. The peripheral equipment may contain up to 14 display consoles on which video display devices indicate the air-ground situation.

The 407L TACS is designed to meet the operational needs of rapidly changing tactical situations—it is mobile, can be expanded quickly, and permits flexible use of operations and maintenance personnel. Refer to figure 3-32 for a simplified view of the elements of 407L TACS. Notice the tactical airbase (TAB) at the upper left; here is where the aircraft are based, maintained, and loaded for combat support missions. The TACS equipment here includes radios, teletype, and telephone systems to meet the communications needs of en route and terminal air traffic control. At the far right side of figure 3-32, we show several blocks representing Army units—these are the people who receive the air support from the TAB; they are linked to the TACS by radio or field phones not parts of the 407L TACS. Directly to their left in figure 3-32, is the close-in part of the TACS—the DASC (direct air support center), ALOs (air liaison officers), and FACs (forward air controllers) mounted in jeeps or possibly on foot. The ALO/FAC (also called the TACP for tactical air control party) have radio contact with the DASC, which in turn requires both radio and telephone systems. The center portion of figure

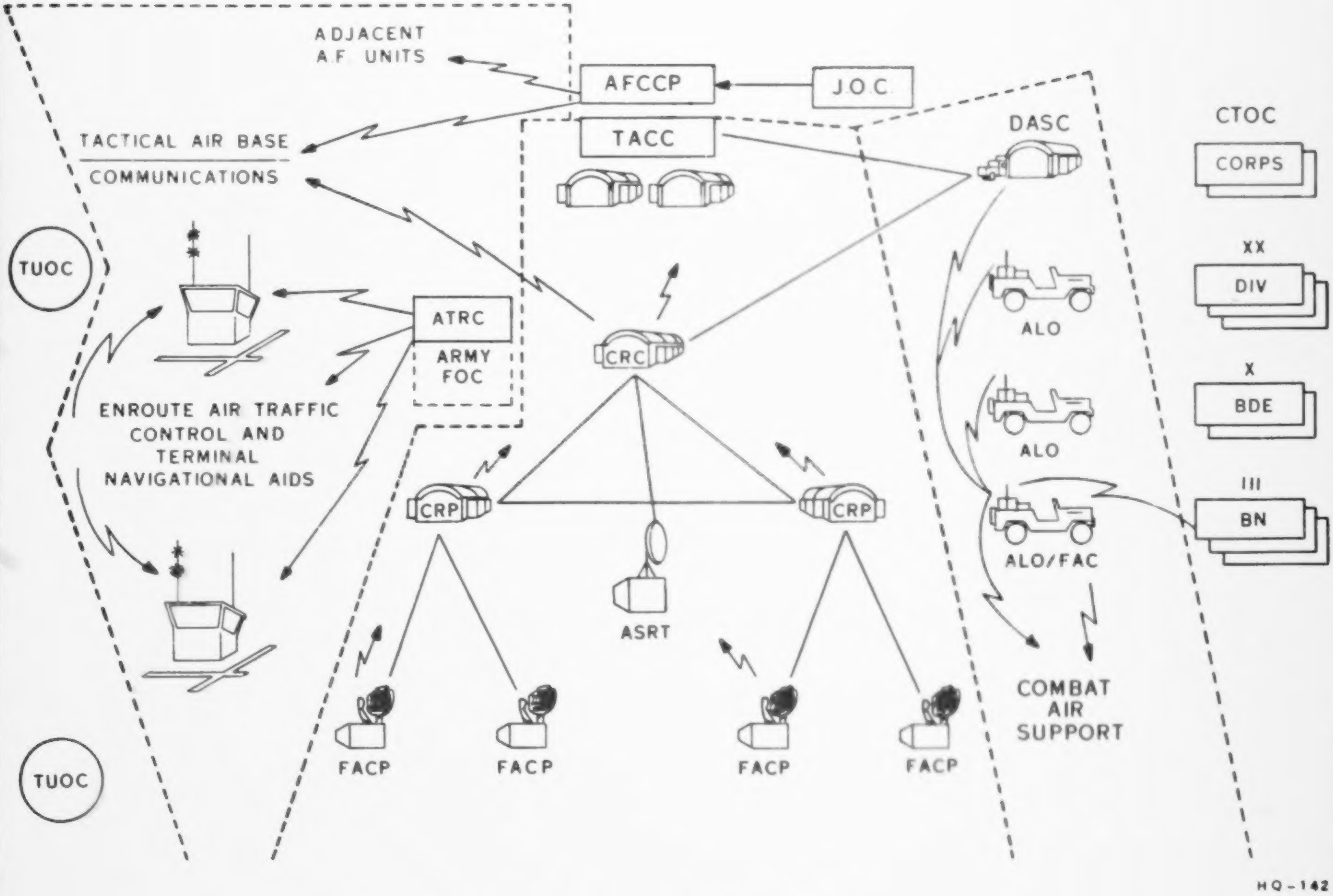

ADJACENT
A.F. UNITS
AFCCP
J.O.C.
TACC
TACTICAL AIR BASE
COMMUNICATIONS
DASC
CTOC
CORPS
XX
DIV
X
BDE
III
BN
TUOC
ATRC
ARMY
FOC
CRC
ALO
ALO
ALO/FAC
ENROUTE AIR TRAFFIC
CONTROL AND
TERMINAL
NAVIGATIONAL AIDS
CRP
CRP
ASRT
COMBAT
AIR
SUPPORT
FACP
FACP
FACP
FACP
TUOC
HQ-142

Figure 3-32. 407L tactical air control system.

3-32 includes the AFCCP (Air Force component command post) and TACC (tactical air control center). These are the headquarters for planning and executing the tactical air support missions. The communications and electronic systems here include radar, radio, and telephone equipment. Below them, in figure 3-32, we show the CRC (control reporting center) and two CRPs (control reporting posts), together with their associated radar equipment. These are linked to the overall system by telephone, teletype, and radio equipment.

The amount and types of 407L equipment deployed for a given tactical situation depend upon the size and physical location of the components of the joint task force. A minimum configuration would include one TACC; one CRC, with two associated FACP forward air control posts to furnish navigation and surveillance information to the TACC; and one DASC, with the required number of TACPs. If the tactical air capability needed by the Army is larger, the minimum configuration is expanded by adding a CRC with associated CRPs, FACPs, and TACPs as necessary. Only one DASC is used, but its size and equipment content is increased to support the added TACPs.

TACS equipment that you may be called on to maintain includes AN/TTC-30 central offices located at the TAB, TACC, CRCs, and CRPs; the AN/TTC-32, a 40-line manual switchboard located in the DASC; communications patch bays located at each operations module; and various end instruments (telephone subsets) located throughout the TACS. Now that we have had a quick overview of the 407L system, let's now look at the elements that utilize 305X4 maintenance personnel.

AN/TTC-30. Central to voice communications within the TACS is the AN/TTC-30. The AN/TTC-30 provides the high-speed, transportable switching necessary for communications for this weapons system.

This system is designed to be highly practical for transportable communications. It has many advantages over older systems. For example, it is smaller in size, lighter in weight, and consumes less power. It is computer organized, which means that the maintenance person does not use wired options. Instead, by simply altering the information stored in a program memory, that individual quickly changes the class of service a subscriber receives—which may include anything from a direct line to nonpriority dial service. An AN/TTC-30 tactical unit has far greater communications possibilities under combat conditions than any of its processors. This ESC (electronic switching center), with the exception of the lines or cables, can be moved quickly from one location to another in two trailers either towed or airlifted with a helicopter. Therefore, should the enemy threaten to overrun a headquarters position, the ESC can easily and quickly be moved with the headquarters.

The AN/TTC-30 ESC provides automatic call processing functions requested by any one of the subscriber or trunk lines. Essentially, the ESC consists of a transmission network and a special purpose real-time computer. The transmission network contains transmission lines and associated electronic switches for each line. These electronic switches are activated on a time-shared basis to establish continuity and, therefore, a connection between lines. Activation of these switches is controlled by the computer. The ESC performs the following functions to provide automatic call processing:

(1) Checks the status of each line every 10 milliseconds.

(2) Detects lines requesting service during the line status check and orders appropriate processing to satisfy the request.

(3) Accepts keyed office code and/or directory number digits from the calling line and performs appropriate processing to establish a connection to the called line represented by the keyed digits.

(4) Generates supervision tones (dial tone, preliminary ring tone, answer tone, warning tone, seizure tone, and release tone) for signaling to the calling and called lines.

(5) Controls the activation of the electronic switches in the transmission network on a time-shared basis to establish and maintain a connection between terminals.

(6) Updates the status of each line during the line check to reflect the present conditions for the line.

(7) Initiates processing for disconnect when a call is completed.

Elements of 407L TACS. As we cover the various 407L elements, continue to refer to figure 3-33 to get an idea where these elements fit into the overall picture. As we have stated earlier, our primary concern will be the elements that utilize our AFSC.

Air Force component command post. The AFCCP is the headquarters facility for the Air Force component of the JTF. It is the operating location where general planning, command, administrative, and logistics supervision operations are conducted. The AFCCP is collocated with the TACC.

The tactical air control center (TACC) shelter complex (TSQ-92) is the operations center of the AFCCP and is the focal point for all air activities within the TACS. The TACC plans and coordinates the employment of tactical air effort and air control functions in the area of operations. The flexibility of types and amounts of communications equipment used will provide the operational requirements for the highest or lowest ground force field command responsible for planning and directing daily combat operations. This may range from a division up to a field army.

Figure 3-33 is an illustration of a one-cell minimum configuration assembly sequence for a TACC, CRC, or CRP operations center. Part 1 depicts the furnishing module, and part 2 is a group display module. These two modules contain all of the equipment for the interior: display boards, desks, chairs, and communications equipment. Part 3 shows the shelter side panels extended and mated to form the operations center floor. The double-wall elastomer-coated synthetic fabric shelter inclosure is inflated to 4 psi to complete the formation of the shelter, as illustrated in parts 4 and 5 of figure 3-33.

Control reporting center/air traffic regulation center. The CRC/ATRC is subordinate to the TACC. It utilizes radar to control inflight, aircraft and perform surveillance

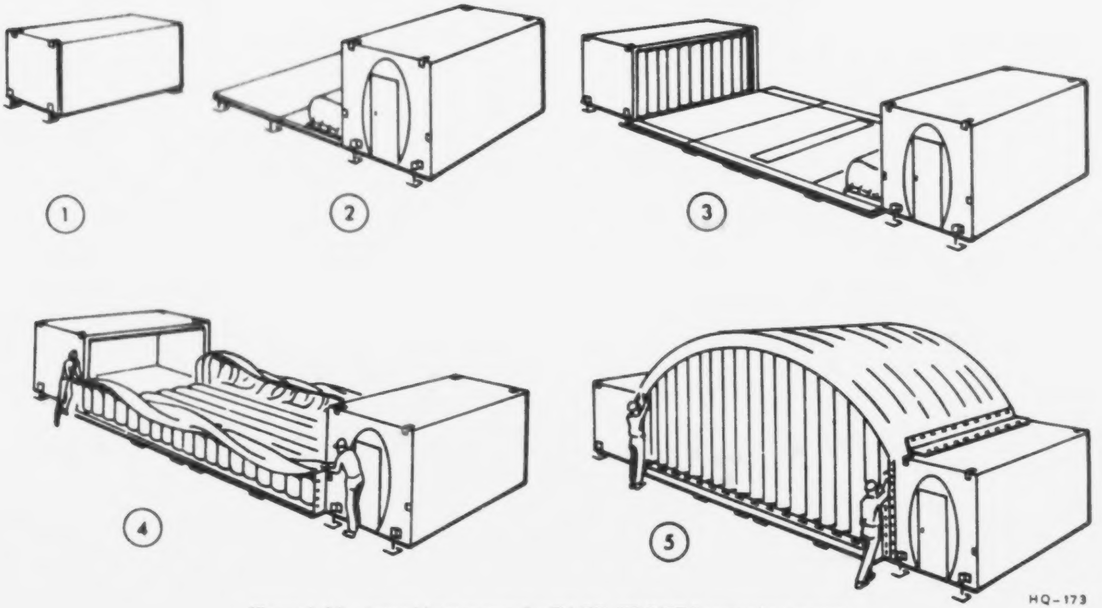


Figure 3-33. Assembly sequence for TACC, CRC/CRP operations center.

within its assigned area of a combat zone. The CRC coordinates and controls the 407L system's AC&W radar, which is located at the CRPs and FACPs. These elements provide the air situation information through the CRC to the TACC. The CRC is the focal point of the AC&W capability to display, evaluate, and distribute information on air activity within its sphere of influence.

The ATRC function of the CRC provides coordination of area Air Force air traffic with the Army, Navy, Marines, civil, and Allied Forces. Figure 3-34 is an illustration of a typical CRC/ATRC field deployment. The CRC shelter and equipment are designated as the AN/TSQ-91.

Control and reporting post. The CRP is subordinate to the CRC and provides radar control and surveillance within an assigned area forward of the CRC. During an emergency it has the capability of assuming CRC functional responsibilities. It combines information from its subordinate FACPs and its own radar and then forwards the information to the CRC. The CRP also provides navigational assistance and direction to aircraft on offensive and defensive missions.

Direct air support center. The DASC is a highly mobile, air transportable facility designed to operate with the Army tactical operations center. It is a forward element, as shown in figure 3-33, and it is subordinate to the TACC. The DASC receives, plans, and coordinates Army requests for immediate close air support, tactical air reconnaissance, and assault airlift from the TACP (tactical air control party). When air effort is allocated for these requests, the DASC directs its employment. It also acts as an advisory agency to the Army commander on the feasibility of requests for air support.

The DASC (minimum) operations center (AN/TSQ-93) is comprised of two functional operating modules—the communications module and the operations module.

The communications module handles teletype and voice communications; it also provides equipment for technical control requirements. The functional capabilities are telephone switching (DASC switchboard, AN/TTC-32), secure and nonsecure teletype and telephone, and the interfacing of equipment.

Normally, the operations module will be mated (electrically, mechanically, and physically) to the communications module. The operations shelter contains radio and telephone patching equipment through which the operational positions are provided secure and nonsecure telephone and ground-to-air radio service. The module is also provided with display boards for plotting and posting tactical situations.

Tactical air base communications/terminal air traffic control facility. The TAB Comm/TATCFs are 407L elements collocated at the airbase. They are composed of the TAB communications equipment and the TTACF air traffic control equipment required to support the deployed tactical Air Force unit. These elements are transportable, mobile facilities consisting of a telephone central office, 2 control centers, 2 teletypes, and miscellaneous radio equipments.

Exercises (442):

1. What is the heart of the 407L system?

2. Identify (a) TACS equipment you may be asked to maintain and (b) where this equipment is found.

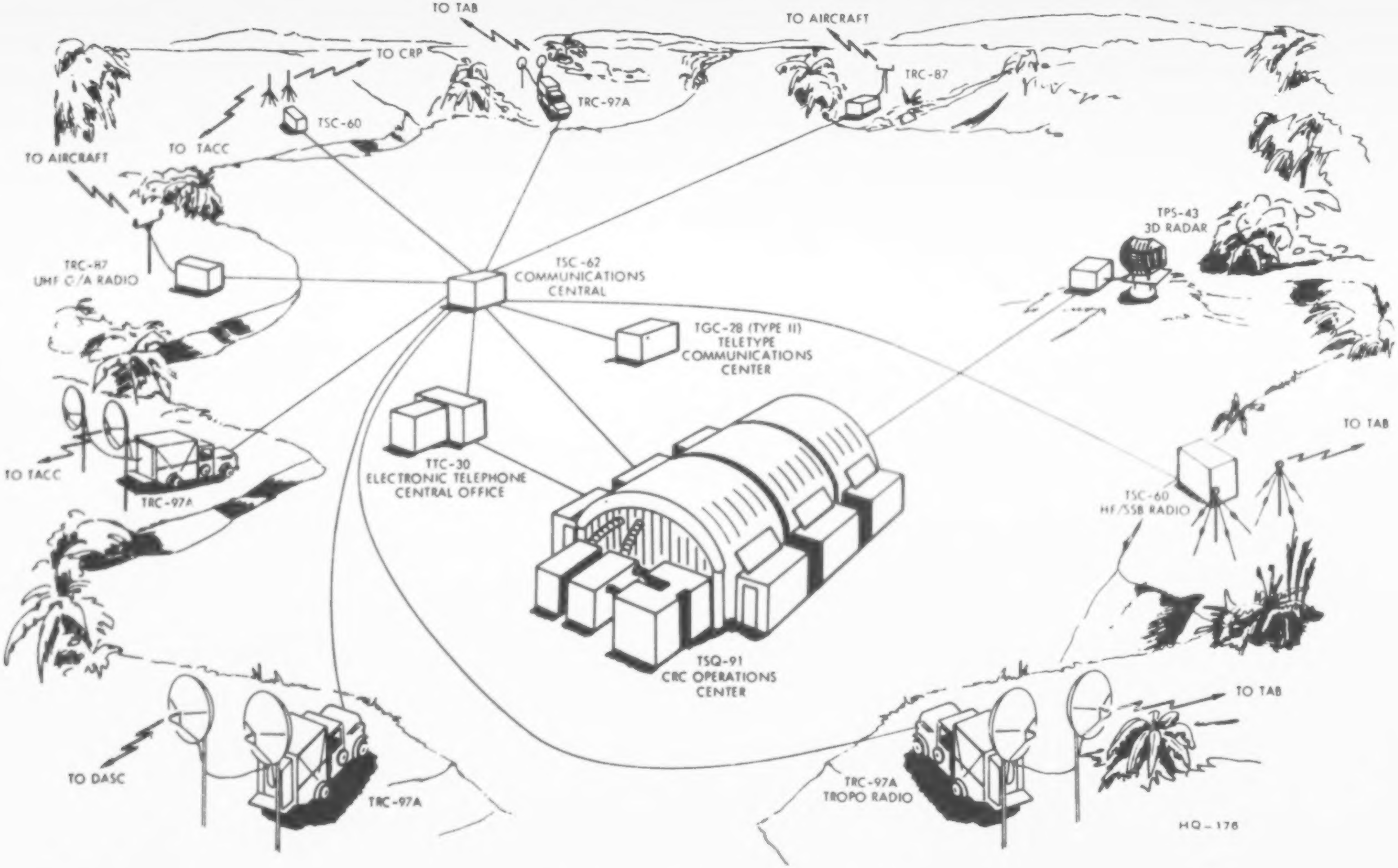

TO TAB
TO AIRCRAFT
TO CRP
TRC-87
TRC-97A
TSC-60
TO AIRCRAFT
TO TACC
TPS-43
3D RADAR
TRC-87
UHF G/A RADIO
TSC-62
COMMUNICATIONS
CENTRAL
TGC-28 (TYPE II)
TELETYPE
COMMUNICATIONS
CENTER
TO TAB
TO TACC
TRC-97A
TTC-30
ELECTRONIC TELEPHONE
CENTRAL OFFICE
TSC-60
HF/SSB RADIO
TSQ-91
CRC OPERATIONS
CENTER
TO TAB
TO DASC
TRC-97A
TRC-97A
TROPO RADIO
HQ-178

Figure 3-34. Typical CRC/ATRC field deployment.

3. **What is the central to voice communications within the TACS?**

4. **List any four of the functions the AA/TTC-30 ECS performs to provide automatic call processing.**

5. What are the elements of the TACS?

6. Operationally, what does the CRC coordinate and control, and as the local point of AC&W capability, what functions does the CRC fulfill?

7. What equipment comprises a DASC (minimum) operations center (AN/TSQ-93) configuration?

443. State what the USAF Spacetrack system provides; identify the MEWS Spacetrack "eyes" for the North American continent and give the functions of BMEWS and OTH.

Space Tracking. Early space observation efforts in this country were directed primarily toward assuring success of the Vanguard (first U.S. space program) project. Procedures were based upon the expectation that satellites would emit cooperative radio transmissions. This would permit precise tracking by relatively simple ground tracking systems. Founded upon this premise, a global observation network called Minitrack was established. Also in existence at that time was a program called Moonwatch. In this program, amateur astronomers and other interested persons with appropriate equipment were urged to observe satellites and to report their observations. However, before Vanguard could be launched successfully, the Soviet Union launched Sputnik I. Although Sputnik I carried a transmitter, its operating frequencies did not correspond with those planned for Vanguard. This Soviet launching revealed the inadequacies of the existing methods of observation.

Today there are two major systems in use for the purpose of detecting and tracking missiles and satellites. They are the USAF Spacetrack System and the Missile Early Warning System (MEWS).

USAF Spacetrack System. This system provides a means for detecting, tracking, cataloging, and identifying man-made objects in space. In addition, the USAF Spacetrack System affords essential data to the USAF Space Defense Center (SDC) inside NORAD's Cheyenne Mountain Complex (NCMC) at Colorado Springs, Colorado. Radar, telemetric, and optical space sensors, located throughout the world, provide continuous observational data to the SDC. The Space Defense Center functions as the command control facility through which NORAD exercises operational supervision of the USAF Spacetrack System. Aerospace Defense Command (ADC) is responsible for carrying out the USAF Spacetrack mission. It does so through the 14th Aerospace Force, which has overall command supervision of ADC elements and managerial direction of other participating USAF agencies.

Missile Early Warning System (MEWS). The next major system that we shall discuss is the Missile Early Warning System. There are three systems within MEWS. They are the Ballistic Missile Early Warning System (BMEWS), the Sea-Launched Ballistic Missile (SLBM) System, and the Over-the-Horizon (OTH) System. These systems are the "eyes" watching for ICBM or intermediate range ballistic missile (IRBM) penetrations toward the North American continent.

a. Ballistic Missile Early Warning System *(BMEWS).* BMEWS was specifically designed for detecting and providing early, reliable warning of a mass ballistic missile attack against the United States, Southern Canada, and the United Kingdom. It has a sensor network, a communications network, a command and control center (central computer and display facility, CC&DF), and a central data processing facility.

Due to the increasing satellite population, all facilities that could contribute directly or indirectly to aerospace defense were integrated into the USAF Spacetrack System. This led to the second mission for BMEWS and started the planning for the integration of BMEWS into the Spacetrack System. Today, the Spacetrack mission of BMEWS is clearly defined.

The Spacetrack mission of the BMEWS sensors is to detect, track, and report positions of man-made orbiting objects in accordance with the Space Defense Center's tasking system. The value of BMEWS becomes apparent when you realize that the BMEWS sites collectively have the capability to detect 99 percent of the entire satellite population in earth orbit within an average 24-hour period. This support is given on a noninterference basis with the BMEWS primary mission.

b. Sea-Launched Ballistic Missile *(SLBM)* Detection and Warning System. This system supplements the missile radar coverage of the BMEWS that guards the northern approaches to North America. The SLBM system, comprised of seven sites on the Atlantic, Pacific, and Gulf coasts, has as its purpose the detection of any missile launched at sea and approaching our coastline.

c. Over-the-Horizon *(OTH)* System. OTH consists of a "family" of systems that bounce radar signals off the ionosphere and back to earth, far beyond the ionosphere and back to earth, far beyond the horizon. This system also adds to the BMEWS capability, and it substantially improves the warning time in the event of a ballistic missile attack.

Other supporting agencies. There are many other agencies that contribute to the space mission. USAF commands, other than ADC, are supporting the space efforts. Certain civilian agencies and universities are contributing significantly. In general, you will find that any agency having the capability to do so is contributing in some way to space surveillance.

Exercises (443):

1. What does the USAF Spacetrack System provide?

2. What MEWS systems function as the "eyes" watching for ICBM and IRBM penetrations toward the North American continent?

3. What is the operational Spacetrack mission of BMEWS?

4. Discuss briefly the operational function of OTH and what else it accomplishes.

CHAPTER 4

Corrosion Control

NOTE: For objectives 444 through 454, study objectives 001 through 011 in Module 10001, *Corrosion Control,* which accompanies this volume. When you complete Module 10001, return to the text.

Module 10001

CDC 30554-3 Objectives	*Module 10001 Objectives*
444	001
445	002
446	003
447	004
448	005
449	006
450	007
451	008
452	009
453	010
454	011

Corrective Maintenance

IN THE PREVIOUS chapters of this CDC, you gained an insight into the knowledges needed to perform the various duties associated with maintaining a computer system. As your trainer guides and directs you through the maintenance inspections and tasks associated with your particular system, this important fact should become apparent to you: Successful mission accomplishment of a computer or switching system is dependent upon a system of scheduled maintenance inspections performed by competent maintenance personnel. Wouldn't it be great if the effective performance of all scheduled maintenance guaranteed equipment infallibility? Of course, this is not the case, since equipment failures can occur at any time. However, effective accomplishment of the scheduled maintenance inspections minimizes equipment failure. When a failure does occur in your system, you will be responsible for troubleshooting—i.e., for isolating and correcting the problem as fast as you can in order to return the system to the performance of its primary mission.

Troubleshooting is not what we once knew. It has taken on a new dimension. With the advent of the computer came the necessary digital techniques information. Without this information being available to the technician, the facility to troubleshoot a system employing solid-state or integrated circuitry just was not available. In order to perform the troubleshooting function, the specialist had to learn the new techniques that were employed in the newer equipment. Digital and integrated circuitry has forced even the experienced maintenance specialist to learn new methods of troubleshooting, as well as the fundamentals which are associated with the new system concepts. With the advent of the computer, and all of its shortcuts and wonders, came a new age of troubleshooting. The computer figures our pay, works out mathematics problems, and makes our life as a maintenance specialist much easier than previously so. Yes, the computer can do all of these things—as long as it functions properly. But, efficient as it is, the computer (just like humans) still has its problems. This is where you come in. Picture this situation: Everything is working smoothly. Then, suddenly, the electronic brain (that has practically taken our jobs away and which has made us look ridiculous because of its superior ability and speed in working math problems compared to ours) has failed. Now *it* is at *your* mercy. How do you act? Answer: Responding as any good maintenance person dedicated to that person's profession should react, you "cure" its ills.

But isn't this situation ironic? Granted you may not be as speedy or may not possess the efficiency or reliability of the computer, still, without *you* it stands revealed as nothing more than several miles of wire and a maze of electronic hardware—all completely within your power. But, while you are savoring this great feeling of power and pride, keep in mind that you will maintain your superiority only as long as you are able to maintain proficiency in troubleshooting your system.

Each computer or switching system has troubleshooting aids designed to accompany it—skillfully planned to make your job of isolating failures within it easier. Some of the more important troubleshooting aids that you might use on the job are:

- Fault indicators.
- System and unit testers.
- Performance test standards.
- Diagnostic programs.
- Flow diagrams.
- Specialized test equipment.

The various troubleshooting techniques presented in this chapter are representative of those used in troubleshooting most of the systems maintained by personnel in the electronic computer and switching systems specialty. The computer system that you are maintaining, together with your personal abilities, will dictate the troubleshooting technique or techniques you adopt and whether you excel in using it and them.

5-1. Isolation of Equipment Malfunctions

Isolating equipment malfunctions may involve many unrelated tasks. In fact, sometimes it may become a confusing experience. This section is devoted to eliminating for you as much of the confusion involved in isolating equipment malfunctions as is humanly possible.

455. Isolating equipment malfunctions, give the reason for thinking before acting; list the steps of a general troubleshooting procedure; name the indicator which can speed up troubleshooting and how; and explain briefly the value of periodic performance checks to document troubleshooting.

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In this segment we will cover troubleshooting considerations, the setting up of a general troubleshooting procedure, analysis of malfunction symptoms, and locating the trouble by inspection. We will begin by discussing just what is involved in troubleshooting considerations.

Troubleshooting Considerations. The basic troubleshooting procedures used in computer maintenance are generally quite logical. A good specialist will attack a problem by asking and trying to answer some simple questions. Your first questions normally concern the causes of the trouble. As each question is answered, you eliminate some possible sources of trouble, thus decreasing step by step the different areas you must troubleshoot. How far you are able to proceed will depend upon your knowledge of the equipment and your ability to troubleshoot. Your knowledge may permit you to locate the exact component that is causing the trouble, or it may only permit you to isolate the trouble to a cabinet or rack. However, with only a limited knowledge of the equipment and by using the correct procedure, as the troubleshooter, you will probably find the more obvious troubles.

Know your equipment. Remember, there is no substitute for equipment familiarization to aid you in troubleshooting your system. Why is this such an important consideration in troubleshooting? That's a good question. The best way to answer it is to ask you this question: If you are not familiar with your equipment to the extent that you can analyze its operation, indicators, printouts, and programs, how can you isolate a failure within that equipment and take the proper corrective action?

THINK before you act. The most important step in any troubleshooting effort is to think before you act. Ask yourself, "What are the symptoms and, knowing these, what could most likely be causing the trouble?" By asking yourself and trying to answer these questions, you will be following a logical sequence of steps—which will probably lead you to the cause of the trouble much more quickly than you would reach it by a trial-and-error (acting first, thinking second) approach to it.

Establish a General Troubleshooting Procedure. The word "general" as used here means all-encompassing. Establish a troubleshooting procedure you can follow, regardless of the particular hardware failure. Figure 5-1 presents a general troubleshooting procedure that can be used for just about any hardware failure encountered within a computer or switching system. The directions given in blocks 1 through 5 are steps to be used in locating the trouble, and the directions in blocks 6 and 7 are steps to be used in repairing the unit. Steps 2, 3, 4, and 5 may sometimes be eliminated, but steps 6 and 7 must always be followed. In the next few paragraphs, we will expand this general troubleshooting procedure by incorporating specific troubleshooting techniques into steps 1 through 5. When thus incorporated into a troubleshooting procedure, the troubleshooting techniques presented will simplify the troubleshooting effort.

Analysis of Malfunction Symptoms. (See *step 1*, fig. 5-1.) Many times when you enter this phase of troubleshooting, you will find that your work has already been done for you. That is, if a malfunction has occurred which lit up a visual indicator, that lighted indicator tells you the part of the system that has failed. In this way, you will find step 1 in figure 5-1 already accomplished for you. We call this to your attention because it is not unusual for many of the system's cabinets to have visual indicators and these are designed to aid you as parts of a troubleshooting guide. Having this, your job is then made simpler for you. So if you find that this condition exists—i.e., an indicator has illuminated and identified one drawer as malfunctioning—your next step is to proceed to step 2.

Locate the Trouble by Inspection. (See *step 2*, fig. 5-1.) Here we wish to point out that inspections fall into two main categories. First, we have the regular *visual* inspection of the mechanical aspects of the equipment—an inspection which is conducted for the purpose of finding dirt, corrosion, loose connections, mechanical defects, and other sources of trouble. Second, we have the *functional* inspections—inspections accomplished through periodic tests and through less frequent bench tests. Of course, bench tests are accomplished only when someone has determined that some sort of failure, or the possibility of failure, exists in the suspect equipment. The periodic test sequences are more the norm than the exception.

It is particularly important when you perform these periodic inspections (PMIs) that you carefully document performance data on each piece of equipment. We can demonstrate the value of these records in a number of ways. For example, by comparing data taken on a particular piece of equipment at different times, you can discover slow, progressive "drifts"—drifts that may be too small to show up significantly in any one test. Secondly, while the week-to-week changes that show up may be slight, by following their progression carefully, you can make many necessary replacements or repairs *before* the margin of performance limits for that equipment is reached. In this way, you can often avoid a malfunction situation entirely. So investigate immediately any marked variations.

This progressive drift could be the situation in the example we mentioned earlier, the one which involved the indicator which illuminated, thereby indicating a malfunctioning drawer. So say that the indicator illuminated and told you to look at a malfunctioning unit. Checking your records, you find that they show that this particular unit has been drifting from acceptable standards for the past few inspections. Your linkage of these facts immediately allows you to determine that you should proceed to step 6 in the troubleshooting sequence. What now? Well, if it is possible to replace the entire malfunctioning unit, you may get back to an operational status rapidly. However, if this is not possible, you must remove the unit and repair the defective part. Note here that such an action might take you right back to step 1 of the troubleshooting sequence. Why? Because your doing this will allow you to find the individual part which has failed within the whole complex faulty unit.

Throughout the entire maintenance action, you will have the greatest success as a troubleshooting technician

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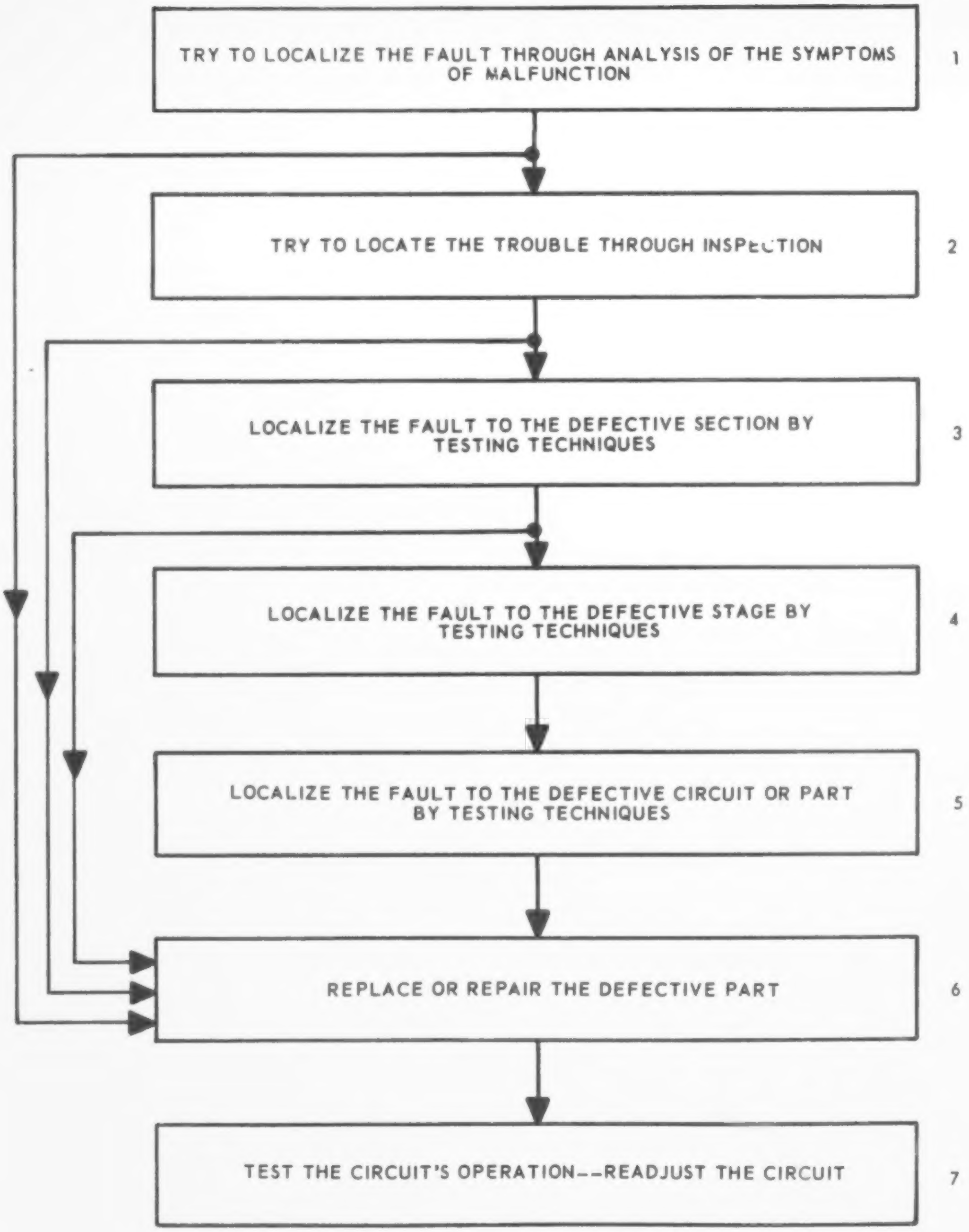
TRY TO LOCALIZE THE FAULT THROUGH ANALYSIS OF THE SYMPTOMS OF MALFUNCTION
1
TRY TO LOCATE THE TROUBLE THROUGH INSPECTION
2
LOCALIZE THE FAULT TO THE DEFECTIVE SECTION BY TESTING TECHNIQUES
3
LOCALIZE THE FAULT TO THE DEFECTIVE STAGE BY TESTING TECHNIQUES
4
LOCALIZE THE FAULT TO THE DEFECTIVE CIRCUIT OR PART BY TESTING TECHNIQUES
5
REPLACE OR REPAIR THE DEFECTIVE PART
6
TEST THE CIRCUIT'S OPERATION--READJUST THE CIRCUIT
7

Figure 5-1. Troubleshooting procedure.

if you follow a logical troubleshooting sequence like that we are discussing here. If you have a spare unit on hand, proceed to step 7 after you have removed and replaced the defective unit. Test the unit's operation and readjust the circuit as necessary.

Of course, our original assumption in this example—that an indicator has illuminated and told you that a fault condition exists in one of the units—might not allow you to proceed through the troubleshooting chart in figure 5-1 as quickly as we have just outlined. For instance, assume that there is no previous history of the unit in question having trouble—i.e., drifting—as our example assumes. Then, moving to step 2, the inspection phase, could reveal a burned component or a scorched wire to you. This discovery would then allow you to proceed to steps 6 and 7. But if your visual inspection reveals nothing, you have to proceed to step 3 next.

Exercise (455):

1. Discuss why, briefly, the most important step of any troubleshooting effort is to think before you act.

2. Cite in sequence the steps which comprise a general troubleshooting procedure.

3. What is the indicator which can often speed up your troubleshooting, and how can it accomplish this for you?

4. Why is it particularly important, when you make a periodic performance check, that you document the equipment performance data? Explain briefly.

456. Name and differentiate among the types of testing techniques which are employed in localizing a fault to a defective section.

Localize the Fault to the Defective Section. (See *step 3*, fig. 5-1.) This phase of troubleshooting is generally limited to some form of marginal checking, system checking, test routines and programs, or some form of diagnostic checks. Sometimes your type of equipment will even allow immediate waveform analysis or voltage sampling. These later two forms of checks will be discussed under another unit.

Marginal checking. This is a method of troubleshooting or periodic maintenance inspection in which certain operating conditions are varied from their normal values in order to detect deteriorating components. The amount of variation necessary before a component malfunctions indicates the margin of reliability. Since component values normally change with age, the marginal check is a valid indication of how soon a component will need to be replaced, and this is why it may be part of the periodic maintenance inspection. This does not eliminate the possibility that you may use the marginal check as a troubleshooting aid. In fact, when it is used in troubleshooting, the marginal check will point immediately to a defective unit because a component will have deteriorated past the allowable margin.

Two methods of marginal checking are used most: variation of vacuum-tube filament voltages and variation of circuit DC supply voltages. These types of checks are often used in power supplies.

Of the two methods just mentioned, the more popular one is probably the variation of the circuit DC supply voltages. Changing DC supply voltages can be used with nearly any type of circuit. For example, transistors and integrated circuits are made with a specified tolerance. The supply voltage to the unit may be lowered within the specified tolerance, and the unit will continue to function normally. If the voltage is lowered to the specific tolerance and the unit fails, it is a good indication that the unit is deteriorating and should be replaced.

System checking. As such, "system checking" is a broader term than "marginal checking." Whereas marginal checking is normally limited to the checking of a circuit, a stage, or a small section of an electronic system, system checking may check large sections or units in one operation. It is sometimes faster and more practical for use in preventive maintenance, although it is considered a practical aid in troubleshooting.

The first step in system checking is the operation of the system under the specific guidance of a test program or sequence, the results of which are known. If the results obtained from the test sequence are as expected, the system can be considered as operating correctly. Following this operational check, a second test sequence is applied to the unit under test. However, this time the test sequence contains instructions to vary certain supply voltages. This test sequence is designed to check the marginal operation of one complete section of the system, such as the demodulator unit, converter section, or some output section. If the results show that all sections are working within the specified limits, the marginal test reveals that the sections can be considered operational. If, however, errors appear, the operation of one or more components or circuits in the section under test are questionable. This procedure isolates a malfunction to a relatively small section, and individual circuits and components may then be tested by using test equipment to locate the doubtful components.

Diagnostic checks. Checks of this kind are used to localize the source of errors. However, modern day electronic systems often incorporate the individual diagnostic check into one big routine containing many such checks and call it a diagnostic program. This approach saves time, since one program exercises the entire system and will localize a trouble to one of the larger areas. Smaller more precise diagnostic programs or checks may then be used in localizing the source of malfunctions even further.

Diagnostic checks differ from other types of checks in that they are used to help technicians locate sources of errors. They may be combined in such detail as to cause

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the system to initiate an output that will indicate a faulty component, card, or section. The success of this particular feature lies in the ability of the visual indicators on your system to indicate the specific area of failure. You can look forward to seeing an increase in this area of fault indicators and diagnostic routines. They go hand in hand. This type of routine is a tremendous aid in troubleshooting and preventive maintenance.

Exercise (456):

1. Cite the types of testing techniques that are employed in localizing a fault to a defective stage.

2. What is marginal checking?

3. Contrast system checking with marginal checking.

4. Explain briefly the nature and value of diagnostic checking and diagnostic programs.

457. Specify the types of testing techniques and equipment employed to localize a fault to a defective stage.

Localize the Fault to the Defective Stage. (See *step 4*, fig. 5-1.) Once the unit which contains the malfunction has been isolated, you have to isolate the malfunction to a particular stage of the unit. The techniques you should employ in this phase of troubleshooting are similar to those you employed in the previous phase in that, in many cases, you may have some form of diagnostic check or test sequence available to assist you in locating the stage or circuit that contains the malfunction. The value of these diagnostic checks or test sequences is entirely dependent on the availability of peculiar test equipment. By "peculiar test equipment" we mean that test equipment which is especially designed for testing the unit that contains the malfunction. Examples of this type of test equipment are special drawer testers, power supply test sets, and specially designed unit test sets. All of these special sets are usually designed to exercise some unit to its fullest extent. Many have individual fault lamps that will indicate when some portion of the unit fails the self-test check. This last will assist you in rapidly isolating the malfunction to an individual circuit.

The other techniques available as troubleshooting aids in this phase of testing involve your using normal pieces of troubleshooting equipment to isolate the problem. Such equipment includes multimeters, oscilloscopes, VTVMs, special frequency meters, etc. You will use all of these at one time or another. One of the other valuable aids to troubleshooting which we should point out at this time is the specific technical order/technical manual (TO/TM) on the equipment under test.

If you are performing a test on an individual unit, not only is it imperative that you avail yourself of the service TO/TM on that unit of equipment, but also, if you are using a specialized piece of test equipment, you should have the specific TO/TM that has the test sequence published in it for the unit under test. You may then perform the test on that unit with all available information about it at your fingertips. WARNING: Any failure to use this cross-check technique of the specific TO/TM might invalidate your troubleshooting sequence. For instance, what if one of the TOs/TMs you use has a recent change in it that eliminates even just one step in a check? Answer: If you perform the check using the old method, either your check will be invalid or you may damage the test set or the equipment under test.

Exercise (457):

1. Cite the types of testing techniques that are employed in localizing a fault to a defective stage.

2. Why should you use the cross-check technique of the specific TO/TM for a specialized piece of test equipment you are working with?

458. Given typical circuits or parts and a text list of testing techniques, cite the technique best suited to specific units or circuits under test.

Localize the Fault to the Defective Circuit or Part. (See *step 5*, fig. 5-1.) In this phase of troubleshooting, as well as the previous one, you will be able to make use of some special test sets designed to test, not a unit, but sections within a unit. For instance, you might have used a power supply test set to locate a faulty card. In this phase of testing (step 5), you would follow on by using a specialized card tester to locate a faulty component on that card.

The types of test equipment that you will use in this phase of troubleshooting are printed circuit card test sets, integrated circuit card test sets, signal generators, frequency meters, VTVMs, multimeters, and oscilloscopes. The types of tests to be performed will be resistance measurements, voltage measurements, and waveform comparison.

Resistance measurements. When a malfunction develops, it could produce a change in the resistance values within the circuit. Thus, by measuring the DC resistance between various points in the circuit and reference points (usually ground is one reference point) and comparing it to the point-to-point resistance charts provided in the applicable TO/TM, you can locate malfunctions readily. The values given, unless otherwise stated, are measured between the indicated points and ground. CAUTION: Before making resistance measurements, make sure that the power to the equipment under test has been turned off, and discharge all filter capacitors.

Voltage measurements. Since most troubles encountered in equipment and systems either result from abnormal voltages or produce abnormal voltages, voltage measurements are considered an indispensable aid in the locating of a malfunction. Testing techniques that utilize voltage measurements also have the advantage that circuit operation is not interrupted. Point-to-point voltage measurement charts that contain the normal operating voltages encountered in the various stages of the equipment are available to maintenance personnel in the appropriate TO/TM. These voltages are usually measured between the indicated points and ground, unless otherwise stated. When voltage measurements are taken, it is considered good practice to set the voltmeter on the highest range initially so that any excessive voltages existing in a circuit will not cause overloading of the meter. To obtain increased accuracy, the voltmeter may then be set to the designated range for the proper comparison with the representative value given in the voltage charts. When you check voltages, it is important for you to remember that a voltage reading can be obtained across a resistance, even if that resistance is open. The resistance of the meter (and the multipliers) forms a circuit resistance when the meter test leads are placed across the open resistance. The voltage across the component may appear to be approximately normal, as read on the meter, but it may be abnormal when the meter is disconnected from the circuit. To avoid unnecessary delay in the troubleshooting procedure, it is good practice for you to make a resistance check on a "cold" circuit (before applying power) to determine whether the resistance values are normal.

If the internal resistance of the voltmeter and multiplier is approximately comparable in value to the resistance of the circuit under test, this comparability will indicate a considerably lower voltage than the actual voltage present when the meter is removed from the circuit. The sensitivity (in ohms per volt) of the voltmeter used to prepare the voltage charts for technical orders is always given on those charts. Therefore, if a meter of similar sensitivity is available, always use it so that the effects of loading will not have to be considered. If one is not available, then consider using another meter of the same type that you read an erroneous voltage with and try the same test with the new meter. If the results are the same, then you know that you have a condition of loading. Of course, you cannot rule out that part of the circuit as being the cause of your malfunction, because you are unable to perform a valid test on that portion of the circuit.

You should keep in mind constantly that all voltages are dangerous. Recognize that even low voltages or currents can be hazardous, and even lethal, if unusual conditions should exist. Thus, when it becomes necessary to measure high voltages, observe the following precautions:

a. Connect the ground lead of the voltmeter first. While making measurements, place one hand in a pocket or behind your back.

b. If the voltage to be measured is less than 600 volts, place the end of the test probe on the point to be tested. The point may be either positive or negative with respect to ground.

c. If the voltage to be measured is greater than 600 volts, proceed as follows: Shut off the circuit power, discharge any filter capacitors, and temporarily ground the point to be measured. Then connect (slip on) the proper test lead to the high potential point and move away from the voltmeter.

d. Do not come in contact with any part of the equipment while the power is on. This last is particularly important when the voltage under measurement is across two points, both of which are not ground potential.

If you intend to use an electronic voltmeter equipped with a polarity reversing switch, refer to the TO/TM as well as to the manufacturer's instructions for information on proper setup of the meter.

Waveform comparison. Both the measurement and the comparison of waveforms are most important. This technique is the most widely used in our system today. A whole CDC could probably be written on these techniques alone.

You will find that waveform analysis is indispensable in some circuits, such as those involved in pulse shaping or in analog or digital conversion. Waveforms may be observed at test points, shown in the waveform charts, or studied on schematic diagrams that are a part of the maintenance sections of the TOs/TMs for each item of equipment. You should know, however, that the waveforms given in instruction sections of this supplied literature are often idealized; therefore, the forms often do not show some of the details which are normally present when the actual waveform is displayed on an oscilloscope. An appreciable departure from the normal waveform indicates a malfunction that is located between the point where the waveform is last seen to be near normal and the point where it is observed to be abnormal. For example, if a waveform is observed to be normal at the collector circuit of the same stage, the trouble lies in that stage or at the input of the following stage.

Referring again to figure 5-1, you will verify that we have introduced many of the possible techniques and troubleshooting aids designed to help you isolate a possible malfunction right down to a failed component (step 6). Still, the most important part we have made in our entire discussion is for you to know your equipment. If you do not know it, your ability to troubleshoot will range from poor to nonexistent. Consequently, you should seek assistance if you just cannot handle a particular job. In the end, though embarrassing, this is the most expedient thing for you to do—the safest and most cost effective—rather than your attempting to troubleshoot or repair something you do not have the ability to handle.

The last technique of troubleshooting that we will discuss in this section is really a combination of steps 5 and 6 of figure 5-1, because it involves not only the troubleshooting phase but also the repair phase. Let us take a look next at one of the quickest solutions to keep

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our equipment or systems on the air with the highest possible degree of integrity.

Exercises (458):

1. What are the three tests performed with test equipment during troubleshooting?

2. You think you have an abnormal voltage in a circuit and decide to use a point-to-point voltage chart to check out your suspicion. What technique would you be using, and where can you get the right voltage chart (the one with the normal operating voltages)?

3. A voltage greater than 600 volts must be measured. Name the technique to use and tell how to proceed.

4. If you suspect that an incoming signal is not up to its proper level of performance or strength, which technique and type of test equipment would you use?

459. Describe briefly the group removal and replacement technique used and state the advantage of using this group technique.

Group Removal and Replacement Troubleshooting Techinque. Many of the systems within the Air Force inventory are built or operated in a mode which does not allow Maintenance much time for repair. In this case, an accepted method of troubleshooting is group removal and replacement of circuit cards. For instance, if you are called to repair a malfunction, your first action should be to analyze the symptoms by use of fault lamps, printouts, displays, facility lights, etc. Let us suppose that the fault indications showed a timing error. You now have one of two approaches to choose. First, with a schematic or block diagram, isolate the error to a certain area or group of cards. Second, use the troubleshooting charts that might identify the trouble symptom and list the cards to be removed or part to be replaced. Some TOs or TMs contain these troubleshooting aids. For systems designed to use the group removal and replacement technique, the second method is faster.

The group removal and replacement concept dictates that removal and replacement is restricted to one-half of the cards, not to exceed seven. If, after removal and replacement of the prescribed cards the trouble has been cleared, the cards are then taken to the card tester for checkout and location of the faulty component. If the trouble still exists within the group, removal and replacement of the second half of the cards is performed. Of course this technique will apply only if the system is designed for this type of troubleshooting; otherwise the spare cards will most likely not be on hand to perform the removal and replacement action.

Another type of removal and replacement technique is that which is used in conjunction with a programmed diagnostic test. In this operation, you load a diagnostic program into the applicable control unit and start it. The control unit will cycle through all of the diagnostic steps until the programmed test identifies the faulty unit and causes a printout of the suspect cards. Then you employ the group removal and replacement technique. After replacing the cards, start the diagnostic program again to check out the system. If the trouble has been cleared, the program will cycle completely through. It is possible to have more than one problem, of course, in which case the program will identify another individual card or group of cards which will have to be replaced.

There are many variations of the diagnostic program. Some programs will halt during their cycles until the operator selects or pushes certain designated buttons to continue the diagnostic check. After completing the entire diagnostic check and clearing the trouble, be sure to turn in or check the suspect cards. Do not return them to the shelf without checking them out, or the next time you have to troubleshoot the system you will be using faulty cards and most likely you will never be able to clear the problem.

We have looked at only two examples of the group removal and replacement technique of troubleshooting. There are other applications, but their techniques are the same in principle. It is probable that this technique of group removal and replacement will be the main technique employed in the newer electronic systems, especially where integrated circuits and modular units are involved. This technique provides for quick repair of systems; therefore, it is an effective technique that is often used on some equipment. Be on guard, though, since a card removed as faulty but not repaired creates a catastrophic situation. If you or your fellow workers fail to uphold the integrity of the quality of maintenance, the technique fails.

Exercises (459):

1. Give briefly the group removal and replacement technique used in conjunction with a programmed diagnostic test.

2. List the advantage of using the group removal and replacement technique.

460. Given a block diagram of a specific unit, cite the order in which test points should be checked to isolate a malfunctioning unit most efficiently.

Use of Test Points as a Troubleshooting Aid. One of the most valuable aids to the maintenance technician is the test point feature found in many of the systems and

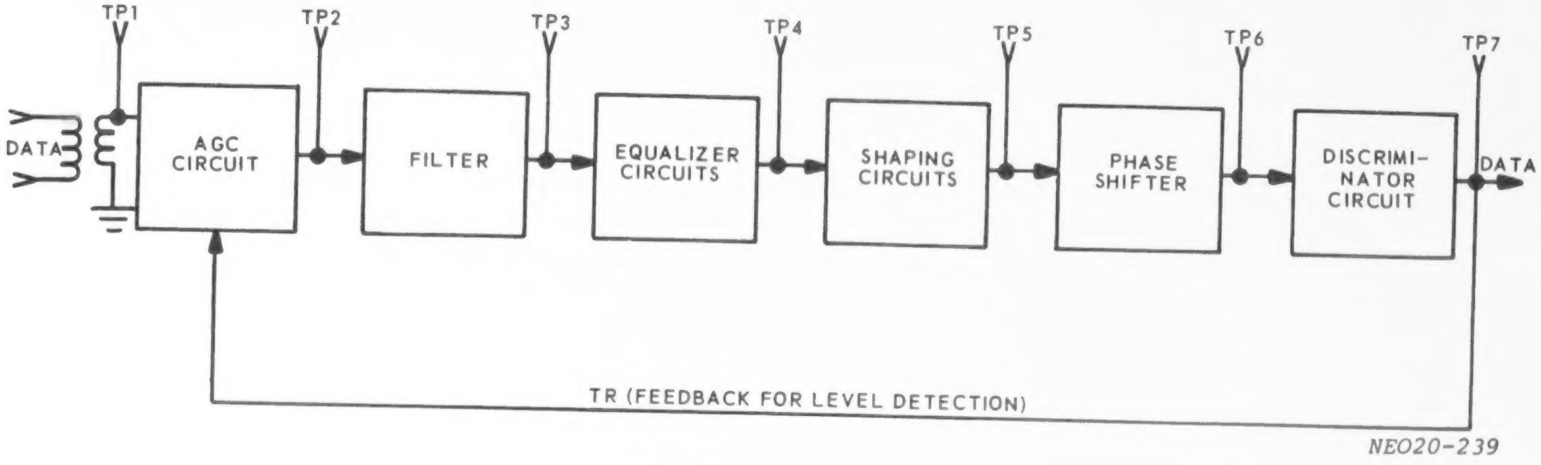
TP1
TP2
TP3
TP4
TP5
TP6
TP7
DATA
AGC CIRCUIT
FILTER
EQUALIZER CIRCUITS
SHAPING CIRCUITS
PHASE SHIFTER
DISCRIMINATOR CIRCUIT
DATA
TR (FEEDBACK FOR LEVEL DETECTION)
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Figure 5-2. Demodulator unit block diagram.

units in today's electronic equipment. The test point feature allows rapid isolation of a malfunctioning unit right down to a specific card in many cases. Isolation of individual malfunctioning components may also be possible by using the test point feature employed in individual units. Such is the case in many power supplies.

For an example of the test point feature and the associated techniques which should be employed for troubleshooting, refer to figure 5-2 and the troubleshooting approach. This figure is a block diagram of a demodulator unit representative of almost any of the equipment within our systems. Suppose that its output is absent and that you are attempting to isolate the failing section—i.e., AGC, filter, etc. What approach would you take in troubleshooting this demodulator unit? Look over the following steps (and figure 5-2) and compare them with the troubleshooting approach *you* would use:

(1) Check for the presence of the data input to the AGC circuit at test point 1 (TP1).

(2) Check the data output of the equalizer circuit at TP4. The results of this check will isolate the failure of the first or second half of the circuits in the demodulator.

(3) The first half of the circuits (i.e., the AGC, filter, and equalizer functions) would be suspect if no data appeared at the output of the equalizer at TP4. By checking the input and output test points of these first three blocks, you should be able to isolate the failure to one of them.

(4) The second half of the circuits (i.e., the shaping, phase shifter, and discriminator functions) would be suspect if data appeared at TP4, which is the output of the equalizer circuit. Then the trouble is known to exist in the second half of the remaining circuits. By checking the test points at the input and output of the remaining blocks, you should be able to isolate the failure to one of them.

The above method of troubleshooting is sometimes called the *split-half method*—i.e., once you determine the absence of an output, you split the circuits in half and check for an output at the halfway point. When you have determined that the failing circuit is in either the first or second half, you split these circuits in half for further isolation of the failure. Continue this process until you isolate the failure to one function. You can also continue this split-half method once you begin troubleshooting the circuits in the failing functional area.

Exercises (460):

1. Using figure 5-2 and the text, list the sequence of the test points that you would check to most efficiently isolate a malfunctioning unit.

2. What was the method of troubleshooting used in the text to diagnose the equipment malfunction?

5-2. Use of Logic Diagrams To Isolate Equipment Malfunctions

You have studied previously the operation of the various elements of logic, the symbology, and the necessary establishment of the truth table for analysis of functional operation of individual logic elements as well as integrated circuitry. Here these are related to Boolean Algebra.

461. Identify the standard for logic diagrams and from a list provided, construct the Boolean equation which describes the operation of the logic device.

In this segment, we will tell you how to use, instead of the individual logic elements, the entire logic diagram for analysis of circuit malfunctions. To do this, we will take up, first, logic symbols the DOD uses, where these are found, and certain variations of symbology. Then, second, we will look at troubleshooting with Boolean algebra, including a hypothetical problem.

Logic Symbols. In today's computer and electronic switching systems there is an increasing need for the individual maintenance person to be able to troubleshoot using logic diagrams. The circuits concerned in the various sections of a system are really no more than a combination of simple devices which perform a few basic operations. Each individual part of the system accomplishes an individual function, and each part can be broken down into subunits or further for analysis purposes. Consequently, one logic gate functions in the same way in every section of equipment; and considered along with the other logic elements within the section, it will perform a given function.

The analysis of logic operations is further complicated by the fact that the logic is not standardized but varies according to the manufacturer. As a consequence, in 1960, MIL-STD-806A, *Graphic Symbols for Logic Diagrams,* was developed and approved by the Department of Defense for preparation of logic diagrams. Unfortunately, many electronic systems were manufactured and in use before this data; many electronic systems and individual units which had employed nonstandard logic symbols are still quite commonly in use. Since 1962, variations of symbology used by the DOD have been developed from MIL-STD-806B, which replaced 806A in 1962. This means that there are still further variations in logic symbology in evidence today. For this reason, there is a move under way at present to replace the existent MIL-STD-806B with a more updated logic standard. In any case, the manufacturers who have adopted the military standard have merely adopted the symbology given there, but they do not fully use the basic concepts. To help you over these difficulties, we furnish in figure 5-3 some of the variations of symbology which have been developed from MIL-STD-806B.

A point for you to remember is that, although the symbol representation varies from manufacturer to manufacturer, the basic principle remains the same. Stated simply, no matter how it is disguised, an AND-gate

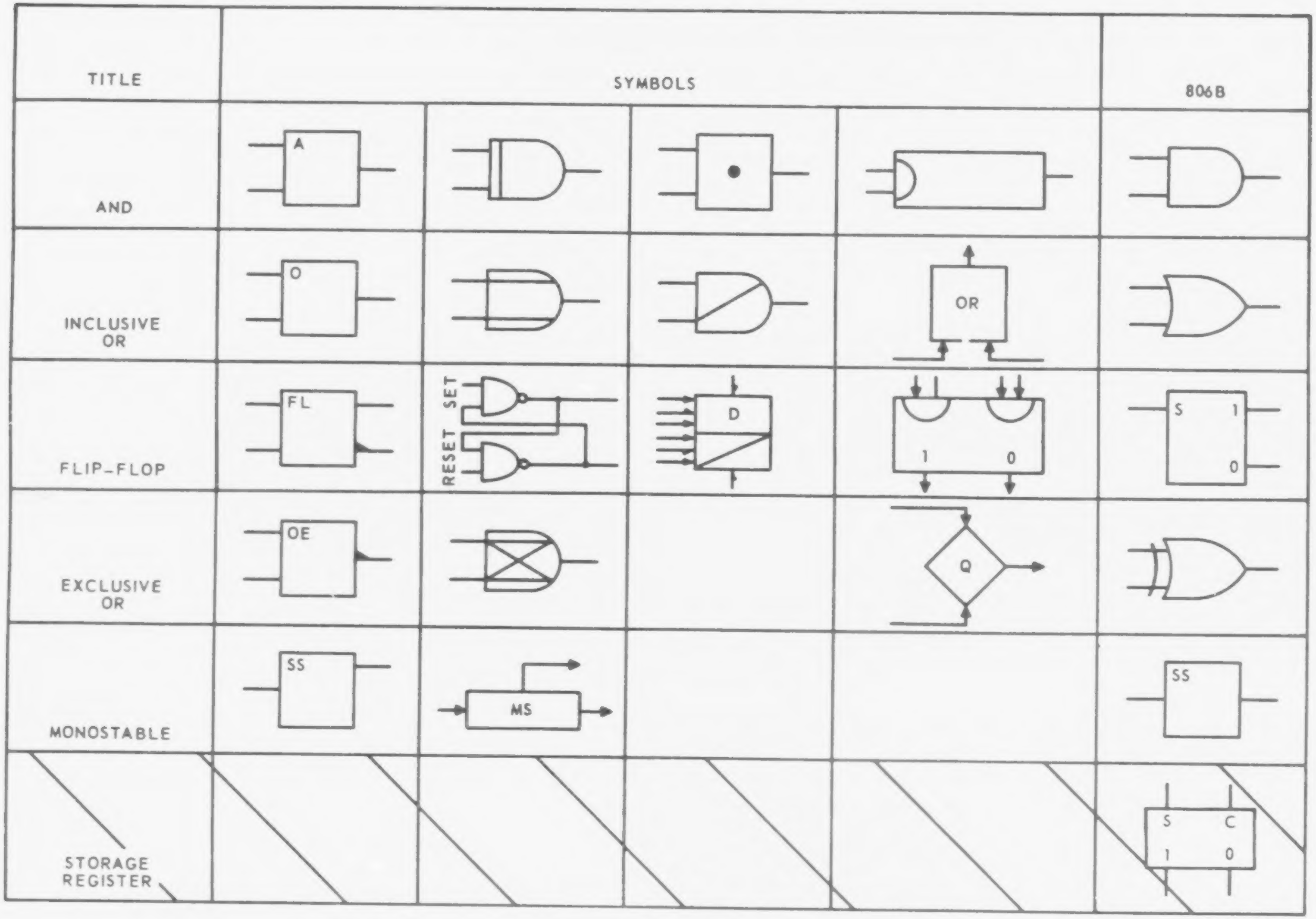
TITLE
SYMBOLS
806B
AND
A
INCLUSIVE OR
O
OR
FLIP-FLOP
FL
SET
RESET
D
1
0
S
1
0
EXCLUSIVE OR
OE
Q
MONOSTABLE
SS
MS
SS
STORAGE REGISTER
S
C
1
0

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Figure 5-3. Logic symbols

remains an AND-gate; and the principles involved in the functional operation of the particular logic device will remain the same, regardless of slight changes in the symbol used to represent the AND-gate.

It is your responsibility to know your system logic. The technical data for your equipment will include information concerning the logic symbols used by the equipment manufacturer.

In order to further broaden your knowledge, a list of manufacturers' logic symbols, as compared with the symbols given in 806B, is included in figure 5-3. The 806B symbol is shown in column 6, what it represents is shown in column 1, and a number of manufacturers' symbols for the symbols taken from 806B are provided in columns 2-5.

Troubleshooting with Boolean Algebra. You will recall that in volume 2 we reviewed the analysis of the development of the Boolean expression. We stated (in that volume) that it could be used to analyze the operation of a given section of logic combinations or individual logic elements. What is Boolean algebra? It is a form of logic that uses mathematical symbols to describe logic processes. Several advantages are obvious in having a mathematical technique for describing these circuits. For one, it is far more convenient to calculate with equations than it is with schematics or with logical diagrams. Just as an ordinary algebraic equation can be simplified using basic theories, so equations describing logical conclusions for arithmetic operations, logical decisions, and switching networks can also be simplified. Another reason is that such an approach enables you, the maintenance specialist, to understand and to troubleshoot better with the logic, thereby achieving greater efficiency of repair and maximum operational availability of equipment.

Normally, troubleshooting with Boolean algebra involves the development and use of a Boolean equation or truth table. But before we discuss the use of such an equation or table, we need to clarify what such an equation involves.

Boolean equations are developed from certain fundamental ideas encompassing logical conditions and operations. By "logical conditions" we mean *variables*; these are represented by letters. By "logical operations" we mean *functions*; these are represented by symbols. When a variable is used in a normal algebraic formula, the assumption is that the variable may take any numerical value. For example, in the equation "3A plus 6B equals C," the A, B, and C may range through the entire field of numbers. However, the variables used in Boolean equations have a unique characteristic in that they may only assume one of two possible values, high or low, 1 or 0; and these, in turn, may be represented by a true or a false condition. For review purposes, consider the development of a Boolean equation for the circuits shown in figure 5-4. Figure 5-4 illustrates two AND-gates feeding an OR-gate, thus becoming an overall OR-function. Note the lack of signs of grouping within the final equation.

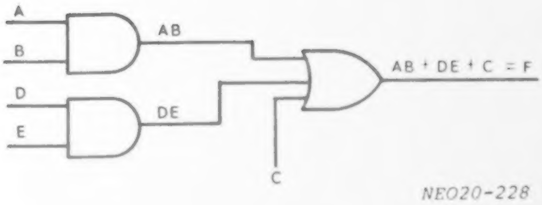


Figure 5-4. Logic OR-function.

In developing the Boolean equation for figure 5-4, we start at the input and work toward the output. This is a good rule to remember, especially when you attempt to develop a Boolean equation during a troubleshooting period. Based on your previous training, the Boolean equation just developed should not have seemed all that difficult to you. Although the example given is fairly simple, you should be able to see the value of this technique in the analysis of logic operation. When you use this technique in troubleshooting, you will find the analysis more difficult, but your understanding of the simple rules of Boolean algebra should aid you in developing the necessary expressions.

Another means of troubleshooting making use of the Boolean equation is to disregard the full equation and to develop instead what is known as a truth table. A table of this nature is nothing more than a means of determining an output by considering all inputs and their variables. Refer again to figure 5-4. The output AB + DE + C = F may be stated for all conditions. The example below will illustrate this technique.

$$(\bar{A}B) + (DE) + C = F$$
$$(A\bar{B}) + (DE) + C = F$$
$$(AB) + (\bar{D}E) + C = F$$
$$(AB) + (D\bar{E}) + C = F$$
$$(AB) + (DE) + \bar{C} = F$$
$$(\overline{AB}) + (DE) + C = F$$
$$(AB) + (\overline{DE}) + C = F$$
$$(\overline{AB}) + (\overline{DE}) + C = F$$
$$(\overline{AB}) + (DE) + \bar{C} = F$$
$$(AB) + (\overline{DE}) + \bar{C} = F$$

Although the above representation of the truth table does not follow the rules of Boolean algebra precisely, you can see that all possibilities are listed here that will result in an active output at point F. Of course, you could then proceed with the further development of the *remainder* of this truth table—i.e., to show the possibilities which would result in an inactive output at point F (or properly stated, for the condition of $\bar{F}$) so that the completed table would list all possible circuit conditions. The next question is, "How can a truth table help you in your troubleshooting efforts?"

When troubleshooting, the true value of a truth table is its identification of all input variables along with their outputs. The easiest way for you to see this basic relationship is by setting up a hypothetical troubleshooting problem. Let us suppose, then, that a failure occurs within a portion of your system which might employ circuitry very similar to that shown in figure 5-4. If you have had experience in the development of truth tables before, you will probably have already

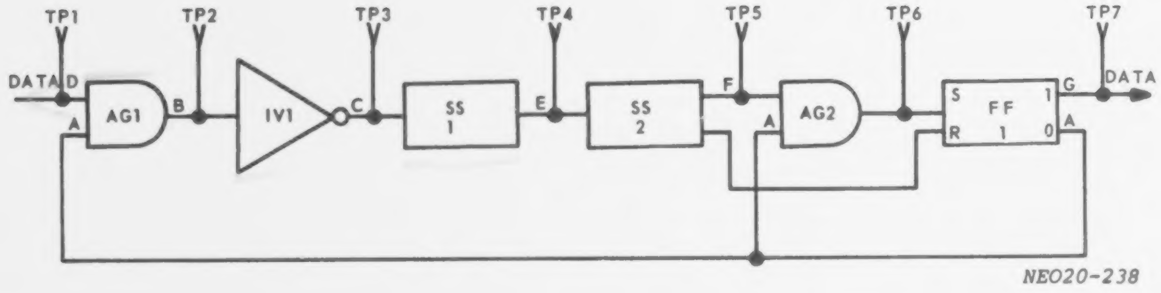


Figure 5-5. Logic circuit (objective 461, exercise 1).

memorized all of the possible combinations which would allow point F to have an active output. So you perform signal tracing using an oscilloscope, and check the test points which will allow you to prove just what the inputs to the OR-gate (whose output is point F) really are. Really, you are validating the input signals. You test inputs A, B, D, E, respectively, then the output AB, then the output DE, and then input leg C. If you find that all of the inputs are operational at the specific time they are supposed to function, the output point F must be present. But if point F is *never* present, then you can only assume that there is a failure within the OR-gate. At this point, it is in order for you to remove the printed circuit card and to check resistance measurements and front-to-back ratios for the circuit components. You may have a card tester or other device available to aid you in this phase of troubleshooting. From this sample problem analysis, the value of the establishment of and use of truth tables for circuit analysis should be evident.

Exercises (461):

1. Identify the presently approved Department of Defense source of logic symbols used in the preparation of logic diagrams.

2. What is the basic principle of symbol representation, no matter how it may be disguised?

3. The variable used in Boolean algebra can only assume one of two possible values. What are they?

4. Put simply, a truth table is nothing more than what?

5. In the hypothetical problem in troubleshooting given in the text involving a truth table, if point F is never present, what must you assume?

6. Using the text and the logic diagram shown in exercise figure 5-5, write here the Boolean expression which will allow a logic "1" to appear at point "G" of the diagram.

5-3. Soldering

A jump from Boolean algebra and its use in analyzing circuit problems to soldering may seem abrupt to you. Frankly, it *is* abrupt, but the linking key is that you will need to know both on your job and both relate to the corrective maintenance of circuit components.

Soldering is the process of joining two or more metals together by the application of heat and a low-melting point alloy. When heated, the alloy flows between and around the metals being joined; upon cooling, it solidifies and the metals are bonded together.

462. Point out particular procedures, purposes, factors, type tools, and material characteristics related to good, effective soldering.

Soldering. The soldering methods for conventionally wired equipment are essentially the same for both production soldering and repair work. For printed circuit assemblies, production methods and repair methods are different. In production, a dip-soldering method is used whereby several connections are made at the same time. Soldering repairs are made, however, individually by using techniques similar to those used for soldering conventional wiring. Special precautions are taken to prevent thermal damage to the heat-sensitive and closely packed circuit elements.

The preferred method of making electrical connections is to heat the terminal and connector to the temperature at which solder melts. Solder is then applied and flows over the joint in the presence of a rosin flux. The application of heat is maintained until the solder-flow process is completed. The heat source is then withdrawn to allow the soldered joint to cool and complete the connection.

Proper soldering and desoldering of connections in electronic equipment requires certain basic tools and equipment.

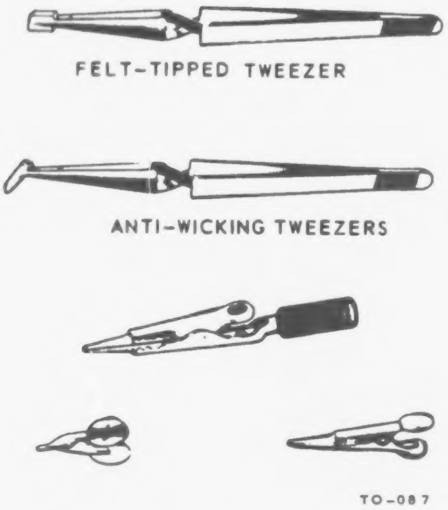


Figure 5-6. Typical thermal shunts.

Thermal shunts. When you perform a soldering operation, thermal shunts, or heat sinks, as shown in figure 5-6, should be used as necessary to protect heat-sensitive components, such as semiconductors, crystal devices, meter movements, and insulating materials. A thermal shunt should be of such material, size, shape, and design as to permit rapid application and removal with minimum interference to the soldering procedure, and to provide rapid heat removal from the area being soldered to prevent damage to heat-sensitive components. You should use thermal shunts that are of the clip-on type. An example is the alligator clip. This is the approved method and usually results in a minimum of damage to metal surface, insulation on the wires, and the component being soldered.

Cleanliness. Cleanliness is the key to reliable soldering. You must remove all dirt, grease, oxide, and scale from the surface to be soldered. Since necessary processing by the manufacturer often leaves an oxide formation on component leads, you must always clean the leads to brightness, regardless of their appearance.

For cleaning soldered areas, you can use a medium-stiff natural or synthetic bristle brush or a lint-free industrial cleansing tissue. Dip it into cleaning solvent approved for removing excess flux following solder solidification. You can use a pencil-type, white typewriter eraser for cleaning copper-clad unplated boards and for removing gold plating from printed circuits and some component leads.

Soldering and desoldering aids. Figure 5-7 illustrates three types of solder aids useful in the desoldering of soldered connections. The slotted ends of the soldering aids are used to lift the ends of wires and part leads from the terminals, while the pointed ends are used to remove solder from terminal holes and slots. The synthetic bristle brush aids in the removal of molten solder. Wire brushes are not recommended for this purpose.

You should not use soldering aids to exert force on wires or components for security testing. The quality of a properly bonded solder connection is determined by a visual inspection. Figures 5-8 and 5-9 show you examples of faulty and properly soldered connections.

Soldering irons. A typical soldering iron is shown in figure 5-10,A. Notice that it consists of a heating element, a tip, a handle, and a cord. Soldering irons come in

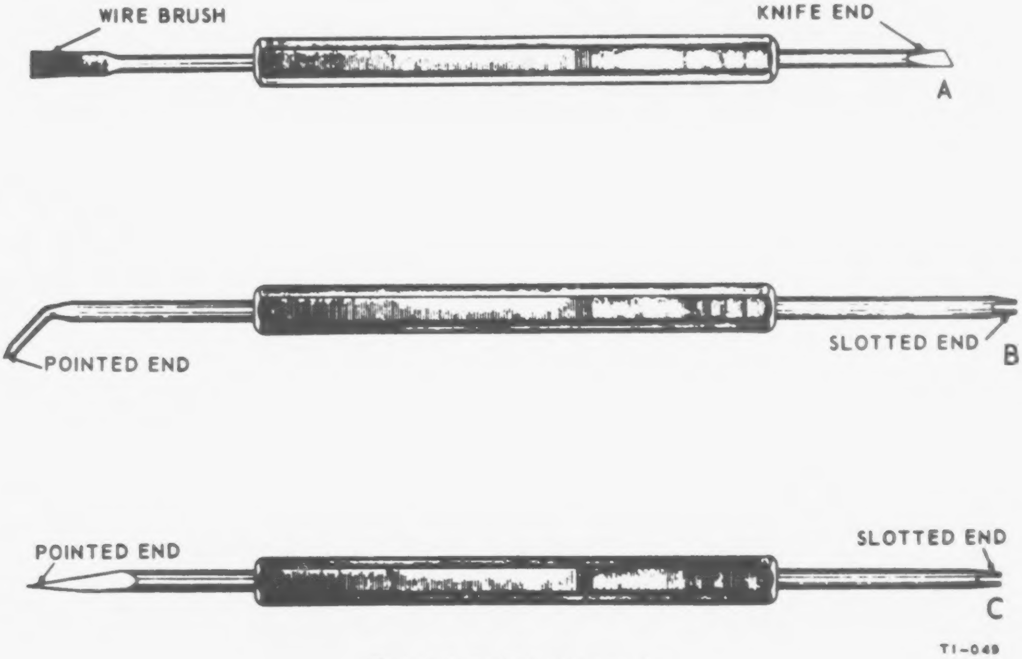
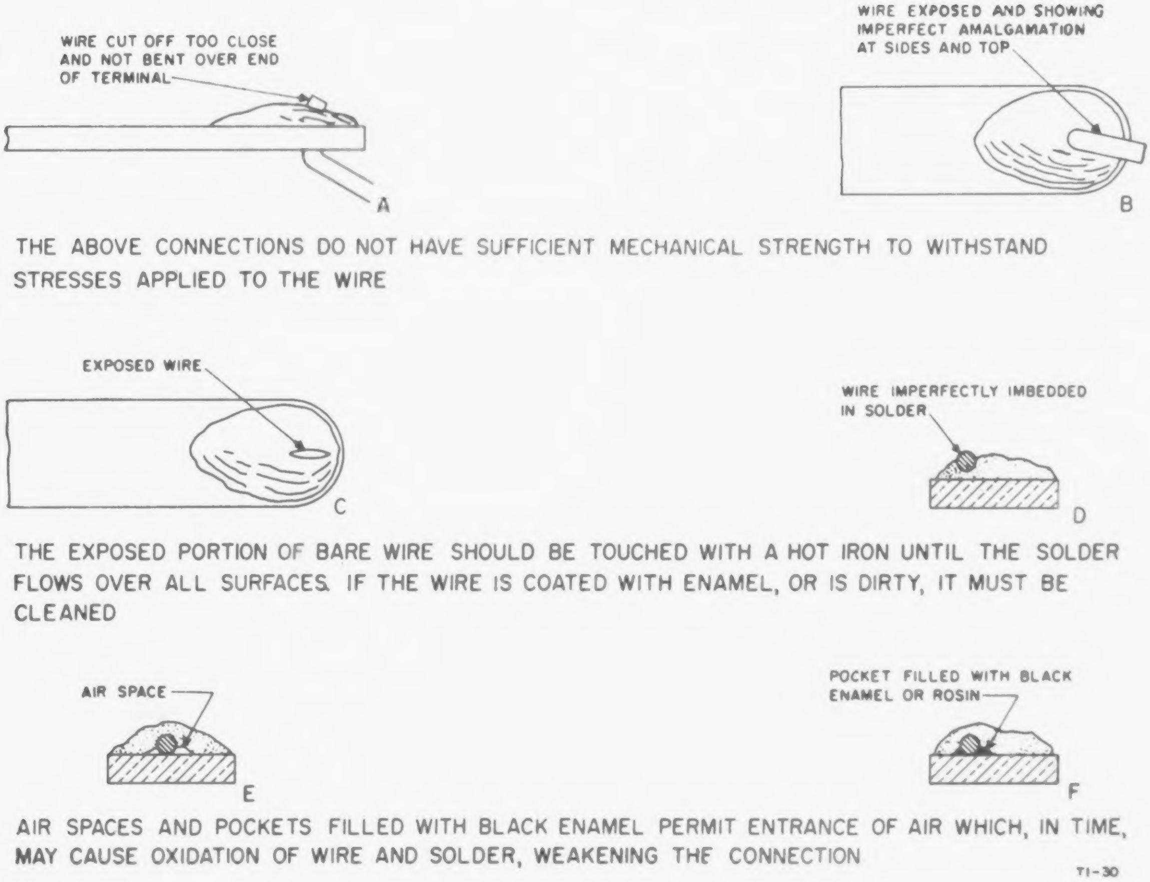


Figure 5-7. Typical soldering aids.


WIRE CUT OFF TOO CLOSE AND NOT BENT OVER END OF TERMINAL
A
WIRE EXPOSED AND SHOWING IMPERFECT AMALGAMATION AT SIDES AND TOP
B
EXPOSED WIRE
C
WIRE IMPERFECTLY IMBEDDED IN SOLDER
D
AIR SPACE
E
POCKET FILLED WITH BLACK ENAMEL OR ROSIN
F
TI-30

THE ABOVE CONNECTIONS DO NOT HAVE SUFFICIENT MECHANICAL STRENGTH TO WITHSTAND STRESSES APPLIED TO THE WIRE

THE EXPOSED PORTION OF BARE WIRE SHOULD BE TOUCHED WITH A HOT IRON UNTIL THE SOLDER FLOWS OVER ALL SURFACES. IF THE WIRE IS COATED WITH ENAMEL, OR IS DIRTY, IT MUST BE CLEANED

AIR SPACES AND POCKETS FILLED WITH BLACK ENAMEL PERMIT ENTRANCE OF AIR WHICH, IN TIME, MAY CAUSE OXIDATION OF WIRE AND SOLDER, WEAKENING THE CONNECTION

Figure 5-8. Faulty soldering connections.

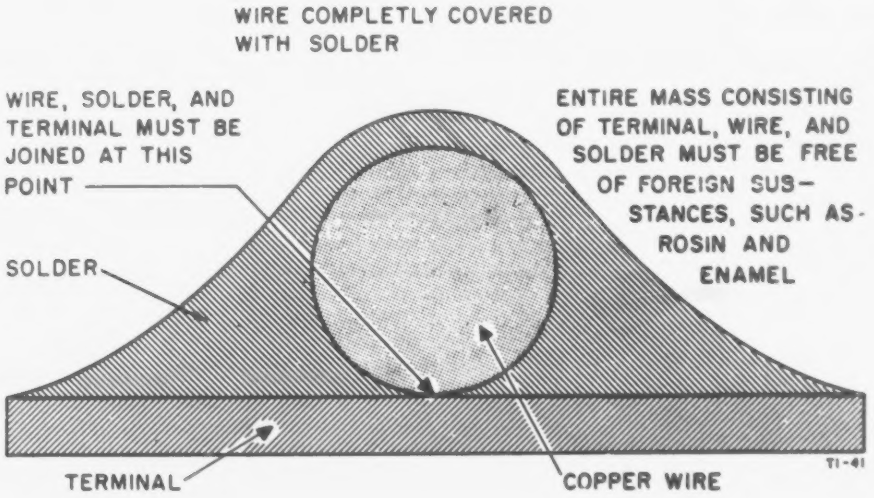

WIRE COMPLETLY COVERED WITH SOLDER
WIRE, SOLDER, AND TERMINAL MUST BE JOINED AT THIS POINT
ENTIRE MASS CONSISTING OF TERMINAL, WIRE, AND SOLDER MUST BE FREE OF FOREIGN SUBSTANCES, SUCH AS ROSIN AND ENAMEL
SOLDER
TERMINAL
COPPER WIRE
TI-41

Figure 5-9. Cross section of a properly soldered joint.

684

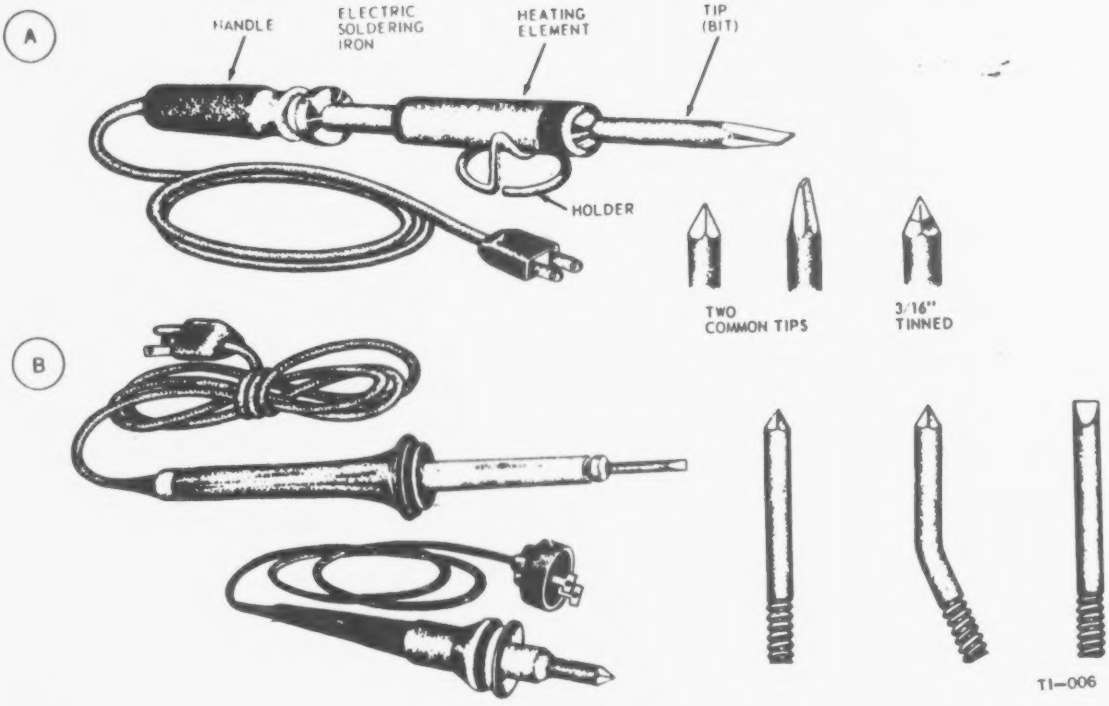


Figure 5-10. Soldering irons and tips.

different sizes, according to wattage rating and diameter of tip. The common tip sizes are 3/8, 5/8, and 7/8 inch.

You should usually use soldering irons which have a 44- to 52-watt rating, as shown in figure 5-10,A, for soldering on main distributing frames; whereas you should use soldering irons having a 100-watt rating or above for working on heavy grounding wire. We should point out here that the higher the watt rating of the iron, the slower it is to heat initially. Also, once an iron is heated, it has a tendency to overheat. However, you can compensate for overheating by using a temperature-regulating stand. Using a temperature-regulating stand allows you to leave the iron plugged in for considerable lengths of time.

Soldering irons having ratings in the 20- to 40-watt range, such as the one shown in figure 5-10,B, have distinct advantages over irons rated at larger wattages. For example, you can use them more effectively where space is limited. Also, this type of iron is excellent for repairing miniaturized parts, such as transistors or printed circuit cards.

Solders. Solders are usually classified into two general categories—hard and soft. Hard solders are usually made up of alloys of tin and lead. One of the most commonly used solders is the 60/40 tin-lead ratio (60 percent tin/40 percent lead), which has a relatively low melting temperature. A commonly used solder in electronics work comes in wire form. The wire is hollow, and the core is filled with rosin flux. Rosin-core solder is recommended for electronics repair, since it does not have the corrosive effects that acid-core solder has. You must remember to select the right type of solder for the soldering job you are doing.

Fluxes. The primary function of a soldering flux is to clean the metal surfaces of oxidation and other contamination just prior to applying the solder; however, you should not expect the fluxes to remove heavy surface oxides from metals. You must remove heavy surface oxides employing a mechanical or chemical cleaning process. Good workmanship practice dictates that the flux be applied at a point near the highest portion of the connection being soldered in order for the flux to precede the solder in its flow downward and to clean the surface properly. The flux attains its maximum activity and deoxidizing power at the soldering temperature. However, the formation of oxides is accelerated by heat. At unnecessarily high temperatures, the surfaces oxidize rapidly, and the flux, no longer a reducing agent at these temperatures, boils away.

Fluxes are available as solids, liquids, and pastes. Wire solder often contains an acid- or rosin-flux core for convenience in soldering. Soldering pastes are a mixture of flux plus wax, tallow, or grease, The flux and its residue can be either corrosive or noncorrosive. Thus, the flux must be selected to fit the soldering application.

Exercises (462):

1. What purpose does a thermal shunt serve?

2. What is the approved method of holding thermal shunts in place?

3. What is the key to reliable soldering?

4. What is the usual method of removing solder from terminal holes and slots?

5. What factors should you consider when you select a soldering iron?

6. What are the common sizes of soldering iron tips in use today?

7. If you were to replace a capacitor on a circuit card, what type of soldering iron would you use?

8. Solder is usually classified in what two categories?

9. What is a commonly used combination of tin-lead alloy solder that has a low melting termperature?

10. What purpose does flux serve in the soldering operation?

463. Explain briefly the procedure for preparing the soldering tips of soldering guns and soldering irons.

Preparation of Soldering Tips. Always check that a full insertion of the soldering tip into the heating element has been achieved, and that there is tight attachment to the soldering iron or gun. Periodically check that no oxidation scale has accumulated between the heating element and the soldering tip. Clean and dress unplated copper tips (while cold) with a flat, clean, single-cut, shear-tooth type file to produce a flat, clean, unpitted working surface. After cleaning and dressing the soldering tip, heat it and tin it with solder. Maintain a bright, continuous, tinned working surface on the soldering tip to insure maximum heat transfer and to avoid transfer of impurities to the solder connection. To do this, heat the iron, remove the old solder with a damp cloth, and clean and smooth the tip with an old file. Continue heating the tip until it turns a light mahogany hue; then apply a small amount of rosin-core solder to the tip. Remove the surplus solder with a damp cloth—the solder that cannot be removed has fused with the copper. A properly tinned iron is essential if you want neat, professional solder joints.

For soldering tips that are plated with an oxidation-resistive coating, clean them (while cold) with emery cloth or aluminum oxide cloth of approximately number 320-grit size. Use only sufficient pressure for proper cleaning and take care not to scratch or remove the plating. Do not use files for cleaning plated tips. After cleaning plated tips, heat and tin them to produce a bright, smooth, tinned working surface. Wipe hot soldering tips frequently with a wet, fine-textured sponge or cloth to maintain a bright, clean working surface.

Exercises (463):

1. What four things should be accomplished to insure proper preparation of soldering tips?

2. What type of soldering tip is cleaned with emery cloth?

464. Indicate the steps in the preparation of wires, cables, and terminals.

After examining the preparation of wires, we will discuss the preparation of terminals here.

Preparation of Wires. Wires should be cut to required lengths, stripped, cleaned, tinned, and inspected prior to attachment. Ordinarily, use the stranded-type of hookup wire. Wire size and insulation characteristics are designated by design requirements. Do not use the solid type of hookup wire unless it is required by design. When required, unsupported solid hookup wire should not exceed 1 inch in length between soldered connections. Wires that exceed this length must be rigidly secured or supported at 1-inch intervals.

Remove insulation from wires by use of an approved stripper. The length of stripped wire is determined by the type of terminal, whether maximum or minimum wrap is used, and the required amount of insulation clearance. Insulation clearance is the length of exposed bare wire between the insulation and the terminal after the connection is complete.

Wires having an outside diameter (including insulation) of $^1/_{32}$ inch or greater must have a minimum insulation clearance of $^1/_{32}$ inch and a maximum insulation clearance of the outside diameter plus $^1/_{32}$ inch.

Wires having an outside diameter (including insulation) of less than $^1/_{32}$ inch must have a minimum insulation clearance equal to the outside diameter and a maximum insulation clearance of $^1/_{32}$ inch. The reference point from which insulation clearance is determined for various types of terminals is illustrated in figures 5-15

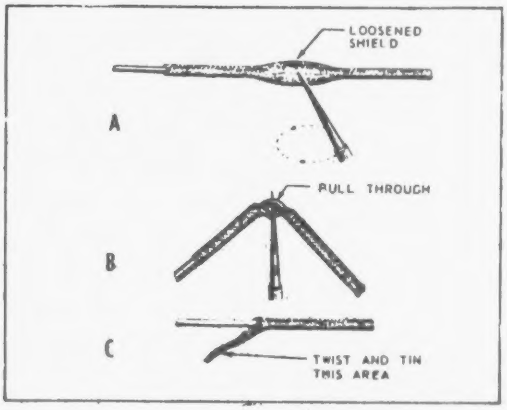


Figure 5-11. Preparation of shielded wire or cable.

through 5-21. When insulation is removed using a precision cutting-type stripper, check the cutter to insure that the correct stripping hole is used for the corresponding wire size. During the stripping operation, twist stranded wire in the direction of the lay in order to maintain the original form and prevent separation of the individual strands. The desired insulation clearance is the outside diameter of the insulation.

After stripping, examine the wire for insulation damage. Do not use wires with cut, split, or burnt insulation. However, slight discoloration from thermal stripping is acceptable. Examine wires to insure that outside strands have not been stretched, nicked, cut, scraped, or otherwise damaged. Damaged wires degrade connection reliability and are not used.

Preparation of Shielded Wire or Cable. Shielded wires or cables are used extensively in electronic equipment to reduce the possibility of introducing undesirable signals into low-level circuits. A typical shielded wire consists of an insulated stranded wire surrounded by a tinned braided shielding. Figure 5-11 illustrates the pigtail method of preparing a shielded wire or cable for a solder connection. CAUTION: Exercise extreme care to avoid damaging shielding or insulated wire while forming pigtail.

A pigtail is made as follows:

(1) Determine and mark the point where the shielding is to terminate. This point will depend upon the individual installation.

(2) Push the shielding braid to form a bubble (as shown in fig. 5-11,A) at the termination point.

(3) Insert the end of a soldering aid into the shielding braid at the termination point and work an open circular area in the shield.

(4) Bend the wire and insert the soldering aid between the shielding and the insulated wire (as shown in fig. 5-11,B). Pull the insulated wire through the open circular area in the shielding.

(5) Pull the empty part of the shielding taut and tin the end to prevent fraying.

(6) Strip the insulation from the center wire as described in earlier paragraphs.

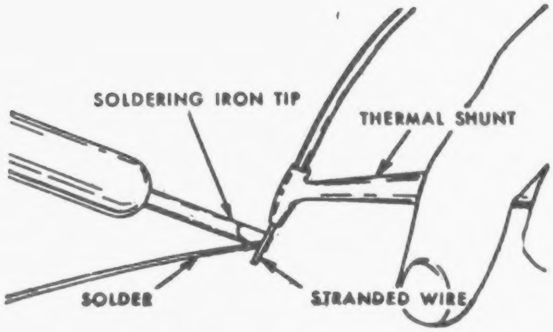


Figure 5-12. Correct method for tinning wire.

Tin all portions of stranded wire that come into contact with the area to be soldered. The wire should remain untinned for a distance equal to the insulation clearance from the point of insulation termination to permit inspection of the wire for nicks or cuts. The correct method for tinning wire is illustrated in figure 5-12. Wicking (distribution of solder along surface of heated wire) of the solder up to the point of insulation termination is prevented by the thermal shunt (antiwicking tweezers). An alternate method of tinning wires is as follows: Dip wire to be tinned in liquid flux to the desired depth; then dip it in a molten solder bath to correct the tinning depth.

Lightly clean pretinned leads with the lead cleaning tool until the tinned surface is bright and shiny. Clean untinned leads in the same manner prior to tinning as illustrated in figure 5-12. However, in this case place the thermal shunt between the part and the tinning operation to protect the part from heat damage.

After cleaning the leads, bend them to provide appropriate mounting form and stress relief in accordance with requirements of the terminal being used. Stress relief bends should be gradual, with the maximum acceptable bend having a radius no less than two times the

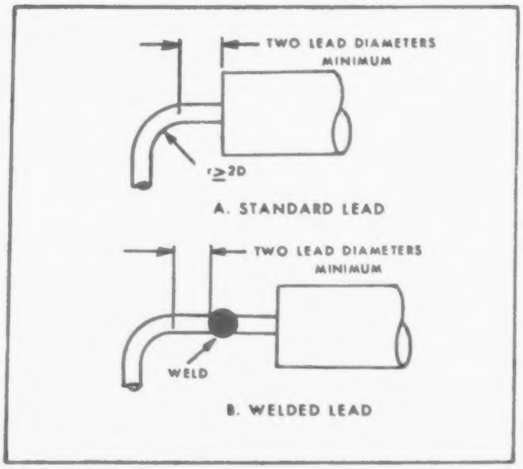


Figure 5-13. Maximum lead bend.

diameter of the lead. (See fig. 5-13,A.) Start lead bends at least two lead diameters from the part body for standard leads or from the weld for welded leads (as shown in fig. 5-13,B) such as those used for liquid electrolytic tantalum capacitors.

Preparation of Terminals. Clean terminals, using a pencil-style typewriter eraser until the tinned surfaces are bright and shiny. You should wash cleaned terminals with an approved solvent immediately prior to attaching any wire or part lead and soldering.

Exercises (464):

1. When are the different types of hookup wire used?

2. How is solid hookup wire supported?

3. Give the minimum and maximum insulation clearance of wires.

4. How is stranded wire twisted? Why?

5. Briefly explain how to prepare a cable.

6. Cite an alternate method for tinning wires.

7. Tell how to make stress relief bends on part leads.

8. How are terminals cleaned?

465. Supply the procedures for applying solder to connections, and describe an acceptable soldering connection and how to protect a soldered connection.

Soldering Procedures. Whenever practical, make connections mechanically secure prior to soldering. A connection should be done in such a manner as to aid the mechanical strength, increase the electrical conductivity, and provide an airtight covering to prevent corrosion from developing between the wire and the terminal.

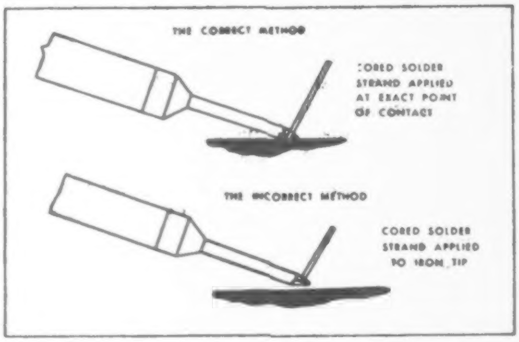

THE CORRECT METHOD
CORED SOLDER STRAND APPLIED AT EXACT POINT OF CONTACT
THE INCORRECT METHOD
CORED SOLDER STRAND APPLIED TO IRON TIP

Figure 5-14. The correct and incorrect methods of solder application.

Soldering operation. Attach wires and part leads to terminals and support them so that there is no movement during the soldering operation and cooling. Connect thermal shunts between heat-sensitive parts and the connections to be soldered. Clean the connection with an approved solvent. If solid wire solder is to be used, apply rosin-core flux to the connection. Maintain a clean, well-tinned soldering iron tip during soldering operation.

Apply the working surface of a heated soldering tip to the connection in such a manner as to transfer optimum heat to the surfaces being soldered. When the surfaces of the connection reach a temperature sufficient to melt solder, apply a proper amount of solder directly to the connection, as shown in figure 5-14. Do not melt the solder on the soldering tip and then allow the solder to flow onto the connection. Maintain contact of soldering tip with connection until all flux is boiled out and the solder has completely wetted (fused in a smooth continuous blend) with the wire and terminal surfaces. Do not overheat the connection. NOTE: Do not use any more solder than necessary. The core size and wire size of the solder should be the minimum required to complete a satisfactory connection or joint.

Do not subject the connection to stress at any time during the cooling and solidification of the solder. Disturbing the finished work will result in a joint that is mechanically weak and that has high electrical resistance. Use no liquid to cool a soldered connection. Allow solder joints to cool naturally at room temperature.

The soldering operation for hollow cylindrical terminals (solder cups) and connector pins differs from the soldering operation described for other types of

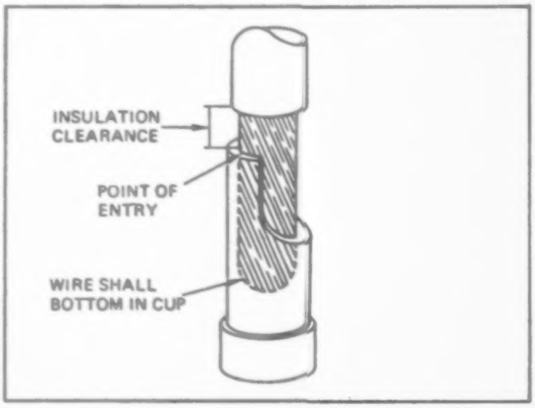


Figure 5-15. Wire placement in solder cup terminal.

terminals. Figure 5-15 illustrates wire placement and insulation clearance in a solder cup terminal. The solder cup terminal or connector pin is heated prior to insertion of tinned wire and a small amount of solder melted inside the terminal. Solder cup terminals should contain a sufficient amount of solder to completely fill the cup when the solder is melted and a tinned wire is fully inserted in the cup. Maintain contact of soldering tip with terminal until all flux is boiled out and the solder fuses smoothly into the conductor and terminal surfaces.

Use a medium-stiff bristle brush dipped in solvent to remove all flux and impurities from the soldered connection following solder solidification.

Solder connection inspection. Inspect each soldered connection after cleaning. Acceptable solder connections will have a shiny, bright appearance with no pits or holes, a good concave fillet between the wire and the terminal, and no excess solder. In all applications, except solder cups and connector pins, the contour of the wire should be visible and the end of the wire should not extend beyond terminal dimensions. In solder cup applications, the contour of the wire should be visible from the insulation termination to the point of entry into the cup.

Protection of completed connections. Solder connections requiring mechanical and electrical protection must have flexible insulation tubing of appropriate type and size installed over wires and part leads prior to attachment to terminals. Flexible insulation tubing is pushed back on the wire or part lead a sufficient distance from the terminal so that is does not interfere with the connection or soldering operation. After soldering, cooling, and cleaning the connection, push the flexible insulation tubing over the wire and terminal to protect the connection. Flexible insulation tubing should extend beyond the insulation termination point for a distance equal to or greater than the diameter of the tubing.

Exercises (465):

1. In addition to aiding the mechanical strength, how should a solder connection be done?

2. Tell briefly the procedures you must first perform before applying a soldering iron to a connection.

3. Explain briefly the procedure for applying solder to a connection.

4. Why must the connection *not* be subject to any stress during its cooling off?

5. How do you solder a hollow clindrical terminal?

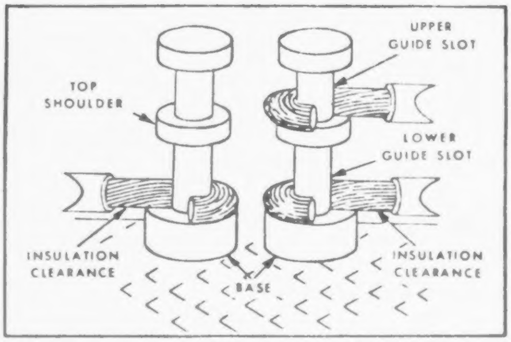


Figure 5-16. Turrent terminal connections.

6. Describe an acceptable solder connection.

7. How will completed connections be protected?

466. State the degree of wrap and where insulation clearance is measured for selected types of terminal connections.

Terminal Connections. The types of terminal connections that you will have to solder are turret, bifurcated, hook or pierced, flat perforated, and hollow cylindrical terminals (described in the preceding objective).

Turret terminal connections. Wires or part leads

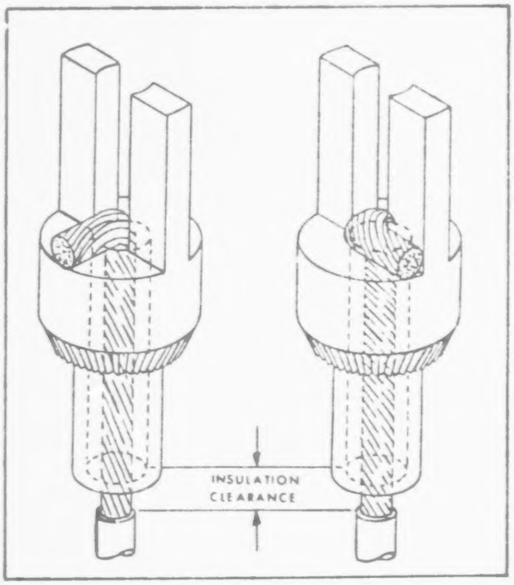


Figure 5-17. Bottom route connection on bifurcated terminal.

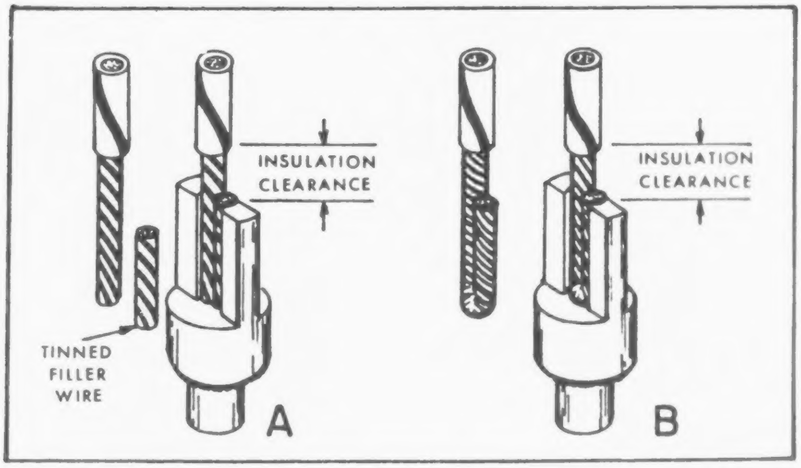


Figure 5-18. Top route connection on bifurcated terminal.

attached to a turret terminal must wrap around the terminal a minimum of 180° and a maximum of 270°. Figure 5-16 illustrates a 180° wrap. The wire should rest tightly against the top shoulder in the upper guide slot and should enter the terminal in a straight line. Insulation clearance is referenced from the base or top shoulder, as applicable.

Bifurcated terminal connection, bottom route. Wire routed through the bottom of a bifurcated terminal (fig. 5-17) must terminate with a 90° bend and rest tightly against the terminal shoulder. Insulation clearance is measured from the entry point of the wire into the terminal. Terminal fill is limited to a maximum of two wires when using a bottom route connection. When connecting two wires, use 90° bends to opposite sides of the terminal posts.

Bifurcated terminal connection, top route. A small diameter wire routed through the top of a bifurcated terminal (fig. 5-18.A) is inserted to fill any space remaining between the terminal posts. An alternate method of small wire connection, illustrated in fig. 5-18.B, is acceptable if the doubled diameter is sufficient to fill the space between the terminal posts. A large diameter wire, which fills space between the terminal posts, is inserted with no bend and requires only solder fillets for retention. The insulation clearance is measured from the entry point of the wire into the terminal.

Bifurcated terminal connection, side route. The wire must enter the mounting slot at a right angle and terminate with a 90° bend. When more than one wire is connected to the terminal, the direction of the 90° bend on each additional wire should alternate. The first wire is soldered to the base and the vertical post. Additional wires are soldered as close as possible to the preceeding wire, maintaining a clearance between the stranded wires equal to the thickness of the two insulations. The insulation on the first wire and all additional wires must be a uniform distance from the terminal posts. Insulation clearance is referenced from the base (see fig. 5-19).

Hook or pierced terminal connection. Wires attached to a hook or pierced terminal must wrap around the terminal a minimum of 90° and a maximum of 180°. Figure 5-20 illustrates a 180° wrap. Insulation clearance is measured from the top of the terminal.

Flat perforated terminal connection. Figure 5-21 illustrates typical flat perforated terminals. Wires are

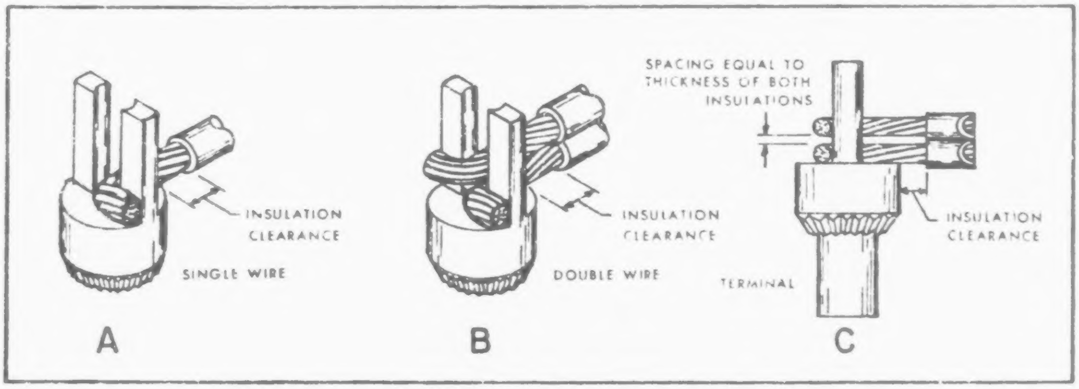


Figure 5-19. Side route connection on bifurcated terminal.

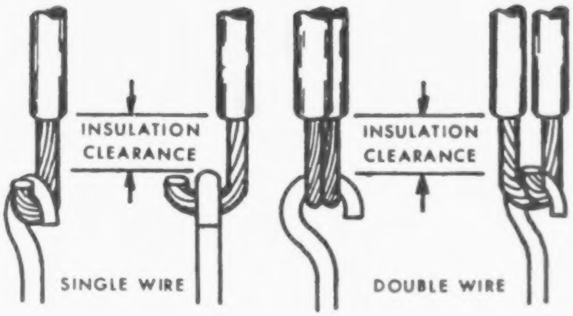


Figure 5-20. Hook terminal connection.

attached to perforated terminals using a 90° to 180° wrap. Figure 5-21 illustrates a 180° wrap. Measure the insulation clearance from the end of the terminal.

Exercises (466):

1. What degree of wrap is used for the following terminals?
   a. Turret terminal connection.

   b. Bifurcated terminal connection, bottom route.

   c. Bifurcated terminal connection, top route.

   d. Hook or pierced terminal connection.

2. Where is the insulation clearance measured from for the following terminals?
   a. Turret terminal connection.

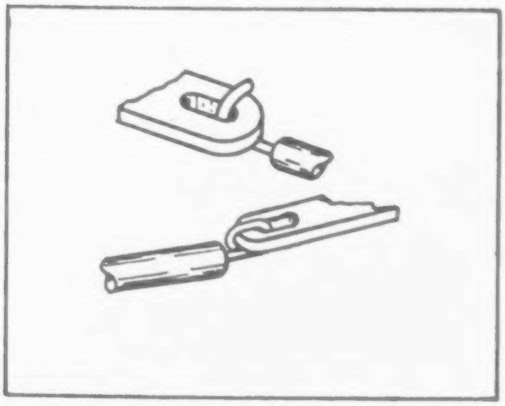


Figure 5-21. Correct wrap for flat perforated terminal.

   b. Bifurcated terminal connection, top route.

   c. Bifurcated terminal connection, side route.

   d. Flat perforated terminal connection.

467. Briefly outline and compare the basic desoldering techniques of wicking and sniffing.

Basic Desoldering Procedures. Since most of the soldering jobs you will encounter are the removal, replacement, and repair of components, you must know desoldering techniques as well as soldering techniques.

Although there are other techniques for desoldering, we will discuss only the *wicking* and *sniffing* techniques. Each of these techniques is very effective in removing the old solder from a previously soldered joint.

Wicking. Figure 5-22 shows some typical materials that can be used to make a wick. You can make an effective wick by stripping the braided shield from a piece of coaxial cable or by removing the insulation from a piece of multistrand wire.

This is the principle of wicking: If you apply heat to a well-saturated rosin wick, the solder will flow readily into the rosin area, leaving the terminal to which it was previously affixed. Almost as if by osmosis, the solder travels into the saturated wick.

In preparing your wick, use a wire size no larger in diameter than the pad size that you will be wicking solder from. This is important, because if you let the wick touch the board, it will "frogeye" the material on the board.

Refer to figure 5-22,A, and the list below for the procedures used in making an effective wick.

a. Remove 6 to 8 inches of shield from coaxial cable and flatten it with a bending tool.

b. Dip about 2 inches of the wick into liquid solder flux. Be sure the liquid flux rosin is the same as the rosin you intend to use in your repair work.

c. If you use multistrand wire, strip about 4 inches of insulaton from the wire.

d. Flatten the wire slightly, keeping the strands in place.

e. Dip the wire in liquid rosin and tin the end.

Now that you have an effective wick, see how to apply it. Refer to figure 5-23 for an illustration of wicking as we describe it.

a. Place the wick on top of the solder joint to be removed.

b. Place the iron tip on top of the wick. When the iron melts the solder, it will flow into the wick.

c. As the wick becomes saturated with solder, clip off the end of the wick, and repeat the operation until you have removed all the solder from the joint.

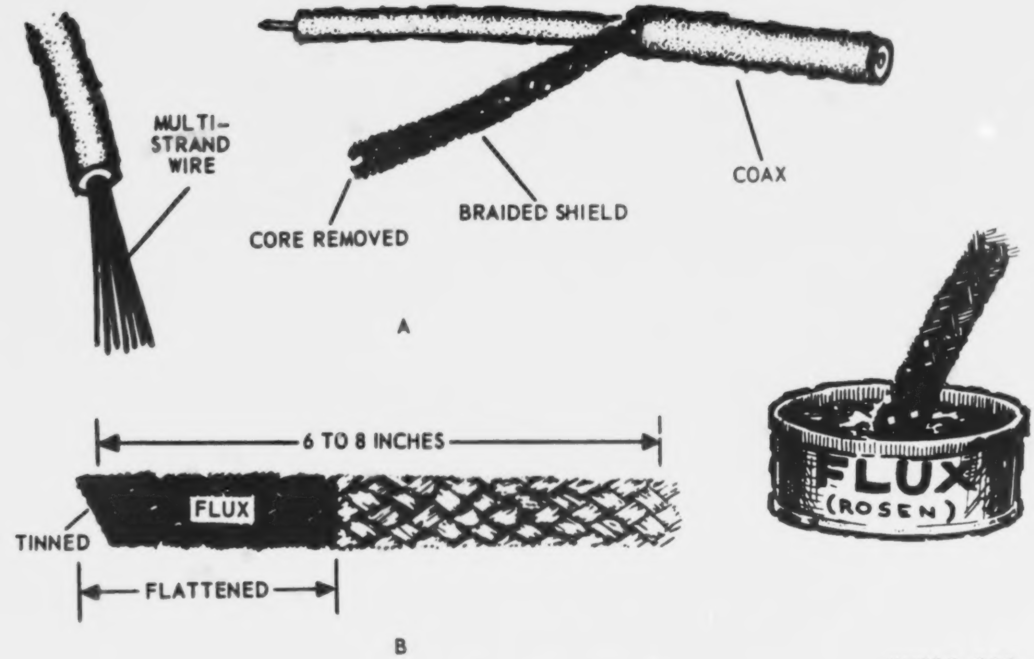

MULTI-
STRAND
WIRE
CORE REMOVED
BRAIDED SHIELD
COAX
A
6 TO 8 INCHES
FLUX
TINNED
FLATTENED
FLUX
(ROSEN)
B

Figure 5-22. Wicking tools.

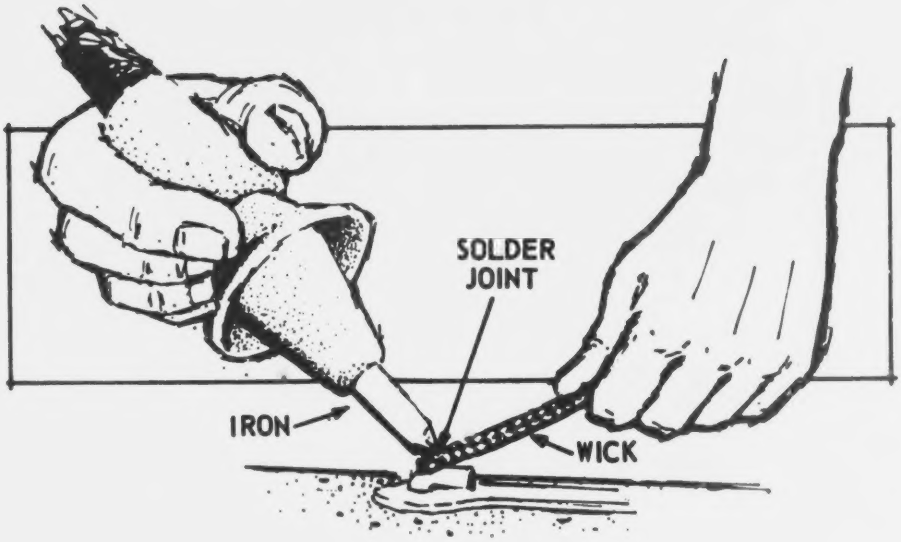

SOLDER
JOINT
IRON
WICK

Figure 5-23. Wicking application.

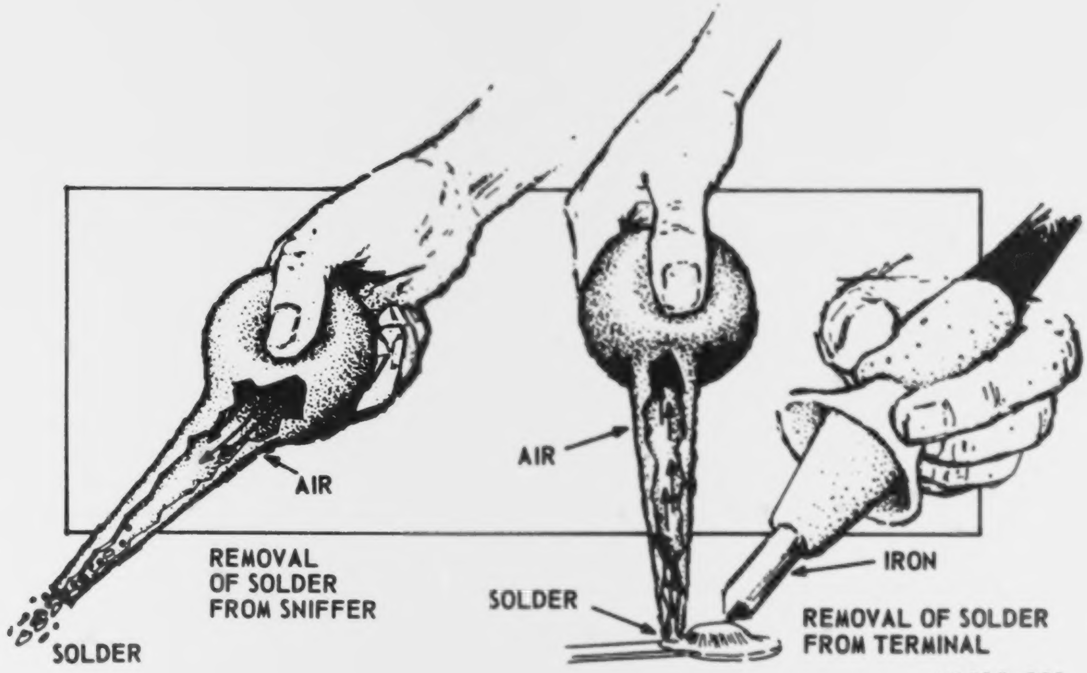


Figure 5-24. Sniffing Application.

Sniffing. In this method, you use a tool like a syringe. (Refer to fig. 5-24.) This tool is made from material that will not bond to solder. Although this method is not as highly recommended as wicking, it is effective.

The sniffer, sometimes called solder sucker, uses the force of air pressure to remove the molten solder. You use the sniffer as follows:

a. Squeeze the air out of the rubber ball at one end of the sniffer.

b. Keeping the ball depressed, place the pointed end of the sniffer next to the solder to be removed.

c. Heat the solder with a solder iron; keep the tip of the iron in the solder and *not* on the sniffer.

d. Slowly release the pressure on the sniffer ball. As the air enters the tube, it will pull the molten solder in with it.

e. After you have drawn the solder from the joint, remove the sniffer. Depress the tube again to remove the solder from the sniffer.

Some solder suckers are part of the heating tool and are referred to as desoldering tools, as shown in figure 5-25. This is often the case with soldering stations. Each of these methods removes solder from a joint. In each method, you must exercise caution because of the heat, component reaction to heat, and possible damage to base materials and adjacent components.

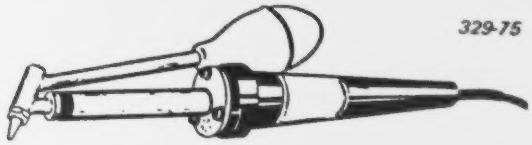


Figure 5-25. Desoldering tool.

Exercises (467):

1. Briefly explain the principle of wicking.

2. Outline the steps involved in the wicking process.

3. Briefly describe the principle of sniffing.

4. Of the two methods of solder removal, which is preferred?

468. State why some of the safety precautions you should observe while soldering are necessary.

Safety Precautions. Soldering is a safe process, if the hazards associated with soldering are recognized and normal safety precautions are observed. To help you keep soldering safe, we include *both* the following list of safety precautions for you to observe while soldering *and*, after each, the reason why it is a necessary precaution.

(1) Always handle soldering irons cautiously. There is always present the risk of receiving painful and dangerous burns during soldering operations. You can receive such burns easily from touching a soldering iron or from handling soldered connections or parts that have not cooled sufficiently.

(2) Support large workpieces securely while you are soldering. Otherwise, you may receive severe injuries or burns as you attempt to grasp a falling workpiece.

(3) Protect your eyes and skin with proper clothing and protective devices. Soldering fluxes spatter when heated.

(4) Do not rest a hot soldering iron on a wooden bench or chair. Use an appropriate soldering iron holder to avoid burned furniture or equipment or, worse still, a fire.

(5) Do not flip excess solder from the tip of a soldering iron. If you do this, bits of hot solder can hit you, causing serious skin and eye burns. Instead, use a clean, damp sponge or cloth for cleaning hot soldering tips.

(6) Do not wear rings or wrist watches while you are soldering. Even a small solder splatter caught under a ring or a watch can cause a severe burn.

(7) Disconnect electronic equipment from the supply circuit before you begin to solder. You can be seriously burned or be killed as a result of contacting energized circuits.

(8) Provide adequate room ventilation. Vapors from degreasing solvents and fluxes may contain toxic gases.

(9) Do not allow degreasing solvents or fluxes to touch or remain on your skin unnecessarily. Many materials used in these products can cause skin irritations. The remedy is to wash contact areas with cool water.

(10) Wash your hands thoroughly before you eat or smoke. Most fluxes contain materials that are hazardous to your health if you ingest them.

Exercise (468):

1. Why should each of the following rules be observed?
   a. Handle soldering irons cautiously.

   b. Protect eyes and skin.

   c. Clean tip with sponge or cloth.

   d. No rings or wrist watches.

   e. Ventilate room.

   f. Wash hands before eating or smoking.

5-4. Solderless Terminations

The wire-wrapped connection has become increasingly more popular in the construction and installation of electronic equipment. The wire-wrapped connection, if put on correctly, meets all requirements for a good electrical connection.

469. Describe certain prerequisites for a good wire-wrap connection; name parts of the wire-wrap tool, defining terms related to it; and clarify particular procedures, requirements, and advantages involved.

Wire Wrap. A wrapped connection must be put on with enough force so that it maintains sufficient pressure. A good pressure connection is one that has sufficient contact area and contact pressure, plus sufficient elastic energy to maintain that contact area and pressure throughout the desired life of the connection. There are millions of connections in existing telephone systems that have a desired life of 10 to 30 years. The wire-wrap method of connecting has this life expectancy (so does solder).

There are six basic requirements for an electrical connection. They are:

- Metal-to-metal contact.
- High-pressure contact.
- A gas-tight contact area.
- A large contact area.
- Mechanical stability.
- No localized stress concentration.

A connection made with a wire-wrap tool will have a large, gas-tight, metal-to-metal contact, with good mechanical stability and no localized stress connection. The tool will wrap the conductor around the terminal with an initial pressure of up to 100,000 pounds per square inch. The pull of the tool on the wire will cause the wire to expand. After the wire has cooled, it normally maintains a pressure of up to 29,000 pounds per square inch. This is well within the limits for a good, gas-tight, high-pressure connection.

In addition to meeting all of the requirements of a good electrical connection, the wire wrap also has the following advantages over the soldered connection.

- No solder disadvantages (heat, clippings, splashes, or operator burns).
- Savings in material and labor.
- Ease in disconnection from terminals.
- More compact connections.
- Uniformity of the connection with calibrated tools.
- More resistance to handling and vibration stress.
- More reliable connections.
- The possibility of being automated.

With the exception of the last of the above, all of the advantages are definitely applicable to your job within the computer and electronic switching field.

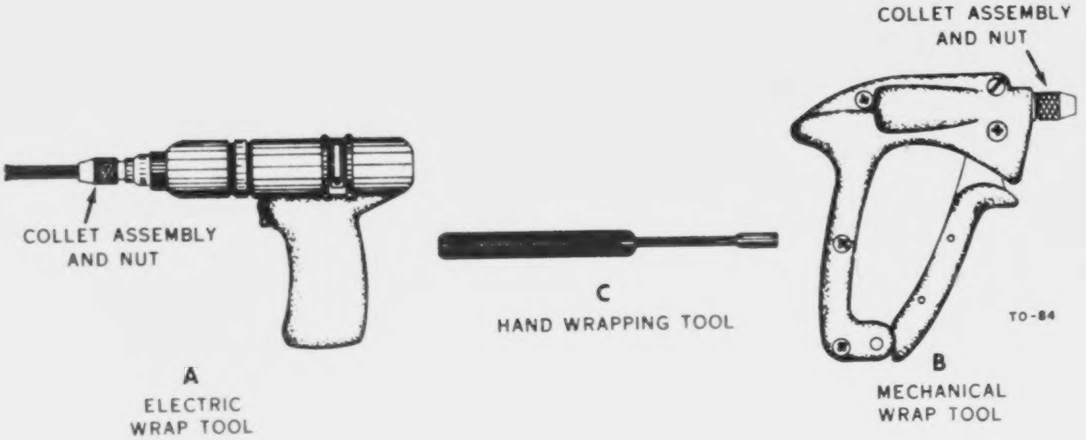


Figure 5-26. Types of wire-wrap tools.

The tool with which the wire is wrapped around the terminal consists of the basic tool plus the wrapping bit and sleeve. The wire-wrap tool is made in five different types: electric, battery, air, manual, or mechanical and hand. Three of these types are shown in figure 5-26.

The tool you would normally use is the hand-wrap tool. The electrical tools are used mostly for production work in factories, while the hand-wrap tool is used for the occasional connection.

The following general terms and their definition will help you better understand the instructions on the use of the wire-wrap tool given a little later.

Solderless Wrap. An electrical connection produced by wrapping a wire tightly around a pin-type terminal.

Wrapping Bit. The rotating member of the wrapping tool that wraps the wire around the terminal.

Sleeve. The stationary member of the wrapping tool which wraps the wire around the terminal.

Contact Area. The summation of all areas of contact between the wire and terminal edges.

Overwrap. The piling up of wraps, one on top of another.

Regardless of the type of power used to operate the wire-wrap tool, the actual business end of all types of tools will be very similar, consisting of two parts, the bit and the sleeve.

The bit rotates within the sleeve to do the actual wrapping. See figure 5-27 for a drawing of these parts. Fashioned out of hardened tool steel, the bit is made to fit a certain size of wire and terminal. The sleeve is made to fit the particular bit. You should always use them as a set to fit the particular wire and terminal on which the wrapping is being done. MAKE WIRE WRAP CONNECTIONS ONLY ON TERMINALS DESIGNED FOR THEIR USE.

Refer to figure 5-27 for the names of the various parts of the bit. We will use these names as we describe the operation here.

Inserting the wire. Insert the skinned portion of the wire $1^{1}/_{4}$ to $1^{3}/_{8}$ inches of bare wire for 22 gauge wire into the slot. The flare will help guide the wire into the slot. Notice that the slot is off-center. Be careful to insure that the wire has been inserted fully into the slot and is not pulled away when the operation of wrapping is started. For this see figure 5-27.

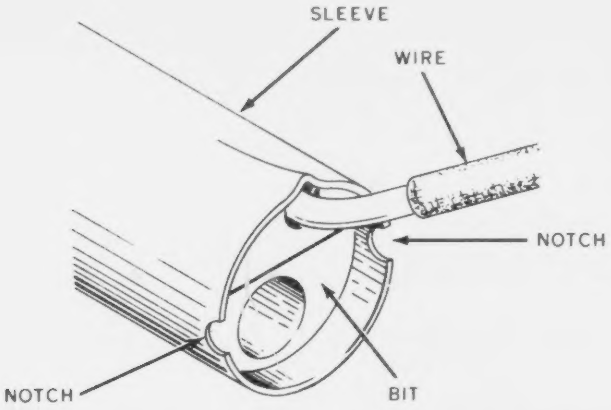


Figure 5-27. Inserting the wire.

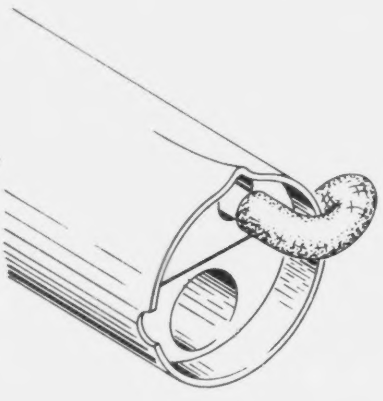


Figure 5-28. Anchoring process.

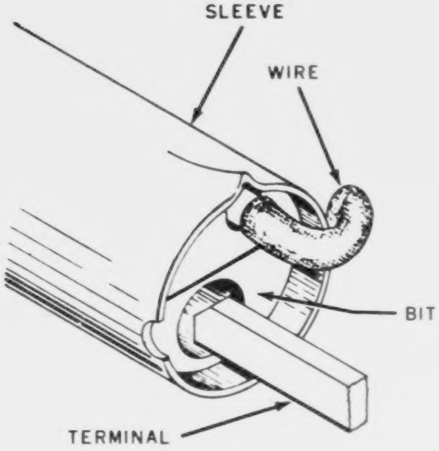

SLEEVE
WIRE
BIT
TERMINAL

Figure 5-29. Tool and terminal positions.

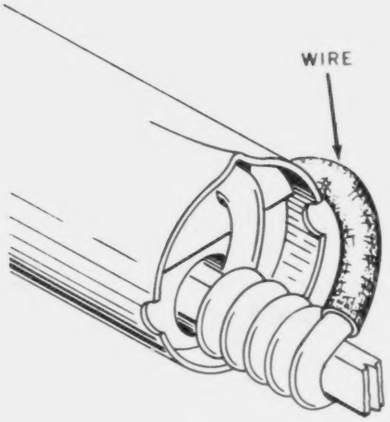


Figure 5-30. Wrapping cycle.

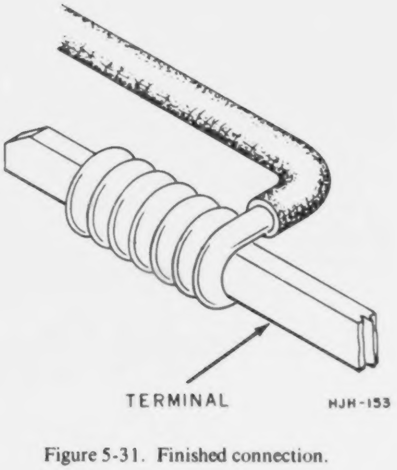
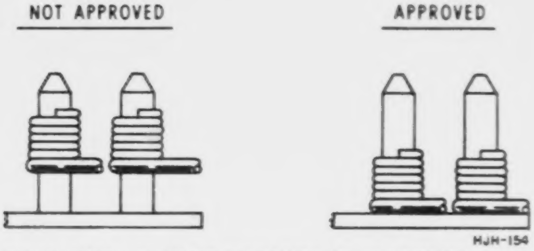
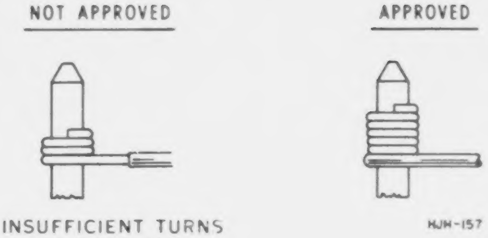

TERMINAL
HJH-153

Figure 5-31. Finished connection.


NOT APPROVED
APPROVED
HJH-154

FIRST TURN OF WIRE LOCATED AS CLOSE AS POSSIBLE TO TERMINAL BASE OR ANOTHER CONNECTION

Figure 5-32. Position of wire wrap.


NOT APPROVED
APPROVED
HJH-157

INSUFFICIENT TURNS OF BARE AND INSULATED WIRE

Figure 5-33. Number of turns.

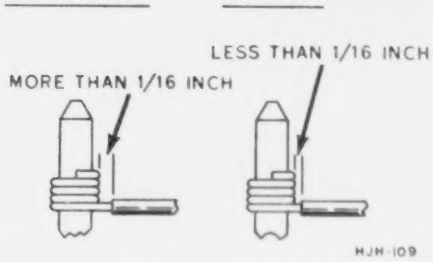

NOT APPROVED
APPROVED
LESS THAN 1/16 INCH
MORE THAN 1/16 INCH
HJH-109

Figure 5-34. Insulation position.

Anchoring process. Bend the wire back through the notch of the sleeve. Seat the insulation against the sleeve to complete the anchoring process. For this see figure 5-28.

Tool and terminal positions. Place the tool over the terminal, allowing space for a minimum of five or six complete wraps. Make the first connection on a terminal as close to the terminal base as possible. Line the bit up with the terminal so that it slips on without bending or damaging the terminal in any manner. For this see figure 5-29.

Wrapping cycle. Hold the wrapping tool firmly, twisting the handle to operate the bit and allowing the tool to back off from the terminal as the wire is wrapped. For this see figure 5-30.

Cycle completed. Carefully remove the wire-wrap tool from the terminal. The finished product should look like that in figure 5-31. Keep the wire wrap close to the base, as shown in figure 5-32. Make sure the wire wrap has sufficient turns on the terminal, as shown in figure 5-33 and that there is no wire insulation farther than $^1/_{16}$ inch from the terminal, as shown in figure 5-34.

You can unwrap any solderless wrapped connection, using any of the several methods available. For example:

a. You can unwrap the connection by hand, without any tools.

b. You may remove the connection using an available tool, such as longnose pliers.

c. You can unwrap the connection using the hand unwrapping tool.

CAUTION: A wire-wrap connection that has been removed from the terminal *must not* be rewrapped using the old wire, unless all of the wrapped wire can be cut off and new, skinned wire is used. Normally, a new wire is used.

If it is not possible for you to skin new wire and to completely rewrap the connection, it will be necessary for you to solder the connection. IF ANY CONNECTION ON A TERMINAL IS SOLDERED, SOLDER ALL CONNECTIONS ON THAT TERMINAL.

Here are a few practical suggestions to follow when you are wire-wrapping.

a. Use only 24- or 22-gauge, tinned, solid-copper wire.

b. Be sure there is a minimum of five full turns for 24- or 22-gauge wire. (NOTE: As a guide, skin wire 1" to 1'. Solder any deviations.)

c. Use only approved terminal made for wire-wrap terminations.

d. Do not use the skinned portion of a used wire for a terminal connection. If you use an old wire, you must wind it with pliers for a minimum one turn and solder it. Or, if you wish to make a wire wrap connection, cut off the skinned portion of the used wire and reskin it.

e. Solder the overlapping of any turns on a connection.

f. Solder the overlapping of any connection onto another.

g. Solder open spirals. Do not attempt to close an open spiral by reapplying the tool.

h. Solder all connections of a terminal if any connection on that terminal has been soldered.

i. Solder a minimum of two adjacent turns for wrapped connections requiring soldering.

j. Be sure that the axial pulling force on the wire will not tend to unwrap the connection. You should dress wires at right angles to the terminal axis.

k. Limit to $^1/_{16}$ inch the distance from the end of the wire insulation to the terminal shiner.

l. Provide a minimum clearance of $^1/_{64}$ inch between the wire end (pigtail) and adjacent components.

m. Do not nick, flatten, or bend the wire before using it.

n. Make certain that the terminal is not bent or scraped when you remove connections after wrapping. You must place the wrapping tool on the terminal and withdraw it in a direction parallel to the terminal. You cannot straighten bent terminals satisfactorily.

o. On most standard terminals, there are three wrapping areas or levels. If a strap is run from one terminal to another, strap both ends of the strap on the same level.

p. Take care of the wrap tool. Don't leave it on top of ladders or lying in high places, because it could fall off and be damaged. Also, it could hurt someone.

Exercises (469):

1. What are the requirements for a good pressure connection?

2. State the basic requirements for an electrical connection.

3. List five of the advantages of wire-wraps over soldered connections.

4. Name the parts of a wire-wrap tool.

5. Define (a) solderless wrap, (b) sleeve, and (c) overwrap.

6. In the operational description of wire wrapping, explain briefly that involving tool and terminal positions.

7. What is the minimum of turns of 24- or 22-gauge wire required for a good wire wrap connection?

8. What should be done to overlapping turns and open spirals?

5-5. Remove and Replace Defective Components

After you complete your troubleshooting action, you will need to remove and replace the malfunctioning system, subsystem, assembly, subassembly, unit, or component. Of course, this is the most expedient manner in which to return the equipment to operation, and the operational status is of paramount importance. However, there will be times when immediate removal and replacement of the malfunctioning item will not be possible. Then, you must determine whether repair of the malfunctioning item is possible.

470. List in proper sequence the steps to be followed in removing or replacing equipment.

Removal and Replacement of Defective Systems, Subsystems, Assemblies, or Subassemblies. Normally, we think of systems, subsystems, assemblies, or subassemblies as large items. They can be this, of course, and sometimes the removal of these large items, as well as the replacement of them, can be a large task. On the other hand, the items may be rather small. If so, then the task is easier. The first thing that you should think of, as a maintenance technician, when you are presented the task of removing and replacing a large item is this: "Where can I get the help that I need to perform such a task?" Answer: The help you need is as close as the nearest equipment service manual—the applicable technical order.

The applicable technical order for the removal and replacement action is, as we mentioned earlier in Volume 1 of this CDC, the -2 TO; specifically, Chapter 5 of the -2 service manual, *Maintenance*. The subjects included in this TO which are related to the task of removal and replacement are these: (1) disassembly, repair, and replacement, including general parts replacement; (2) reassembly and testing; and (3) performance tests. Yes you may have to use commercial publications or technical manuals for some references on equipment which you have to remove and replace. Usually, though, the applicable TO will have a section devoted to service or removal and replacement.

Another aid to the removal and replacement of items is the *Illustrated Parts Breakdown* (IPB) -4 TO. This provides a pictorial view of the item you have to remove and replace. The IPB also identifies the item by part number; and the category listing will tell you whether the item may be procured through normal supply channels, is expendable and must be thrown away, or must be manufactured locally.

Using the help that you get from the applicable publication, you are nearly ready to undertake the removal and replacement task. You have the service instructions for the task, but wait—have you reviewed mentally what steps you are going to take from start to finish? You should, because this step of preparation can save you time and eliminate many of the possible hazards which could face you or your fellow workers later. What techniques should you consider? Look over the list that follows to see whether or not you will agree that a well-thought-out technique will, in fact, pay dividends.

(1) Remove power (be safe).

(2) Label any and all wires to be removed.

(3) Disconnect any jacks or plugs which may be used on the item to be repaired.

(4) Unsolder any wires as required.

(5) Remove any assembly or subassembly to facilitate access to the defective unit as required.

(6) Follow prescribed directions as outlined in TOs or contractor manuals for removal, repair, and reinstallation.

(7) Remove the assembly or component and replace it with a serviceable assembly or component.

(8) Reinstall all wires, jacks, and accessories.

(9) Make a static check.

(10) Apply power and make the necessary dynamic checks, insuring that specifications, as stated, are measured.

Many of the steps just given will apply in one case but not in another. By using them to plan ahead of time for the task at hand, you will make your job much easier. If you are not experienced in the removal and replacement of an item, ask for help. It is better to get the help you need than to try to explain later why you did not. Many of the individual tasks we have listed will be pointed out later in this segment, for they are remove and replace tasks in themselves.

Exercise (470):

1. Arrange the following list of steps for the removal or replacement of equipment in the proper sequence.

____ a. Remove any assembly or subassembly to facilitate access to the defective unit as required.
____ b. Disconnect any jacks or plugs which may be used on the item to be repaired.
____ c. Make a static check.
____ d. Remove the assembly or component and replace it with a serviceable assembly or component.
____ e. Unsolder any wires as required.
____ f. Remove power.
____ g. Apply power and make the necessary dynamic checks.
____ h. Label any and all wires to be removed.
____ i. Follow prescribed directions as outlined in the applicable manuals.
____ j. Reinstall all wires, jacks, and accessories.

471. Identify types of lamps and fuses, briefly describe replacement procedures, and give the title of the TO cross referencing military and civilian fuse designation.

Replacing Lights and Fuses. In the system on which you are now working, lights, fuses, and switches are used

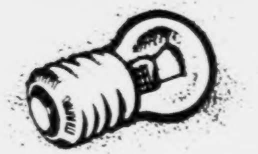
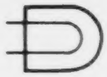
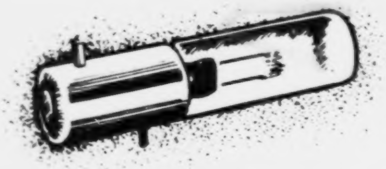
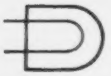
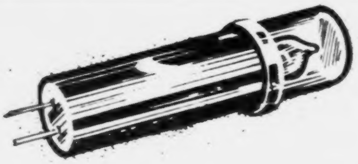
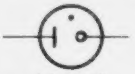
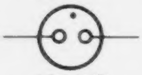
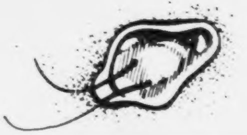
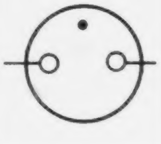
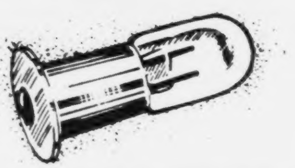
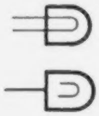
	DESCRIPTION	NUMBERS	SYMBOL	SCHEMATIC REF
1		GE 46 6-8V GE 112 1.2V		DS1
2		GE 47 6-8V GE 57 12-16V GE 313 28V GE 1819 28V GE 1820 28V GE 1929 28V GE 1847 6.3V		DS1
3		NE 2 65V START NE 51 65V START NE 2H 65V START	 DC LAMP  AC LAMP	NE DS1, 2
4		NE 2 65V START NE 2E 65V START NE 68 60V START NE 83 60V START		NE
5		GE 327 28V GE 328 6V GE 320 14V GE 381 6.3V GE 387 28V		DS1, 2

Figure 5-35. Lamps.

in abundance. This is true for all data processors, computers, and switching systems.

These lights and fuses are of vital importance to you, because they show you the operational capability of the data processor. As more of the systems are changed to solid-state and integrated circuits, quick reliable indicators, such as lights or fuses, are needed to speed the detection of failure. It then becomes necessary for you to understand how these indicators are built and installed. Physical features and principles of operation need to be analyzed. We will include the impact on the system during the repair of the unit as a part of the analysis to show the relationship to the task. Logical approaches and basic steps will be developed too.

The analysis of this subject includes a study of the types of lamps, their uses, and typical replacement procedures used to restore the circuits to normal operation; the types of fuses normally found; and the types of fuse holders plus typical replacement procedures.

Lamp and lamp sockets. Study figure 5-35 closely, because it includes a description of the most common lamps used in electronic equipment. These lamps come in various voltage ranges, sizes, and shapes. Common lamp nomenclatures are given in this figure as well as their voltage ratings. These are vital for you to understand in the event that you must replace lamps with substitute lamps. Some lamps even contain resistive and capacitive components internally.

By referring to figure 5-35 showing the lamps, it is easy to see why each lamp requires a special type of socket. Consider the first *lamp* shown, the *screw base*; its socket is as shown in figure 5-36. Since you use only two wires, your removal and installation of it are relatively simple. Observe the wire replacement to the terminals of the new socket when you are reinstalling a new lamp socket. Installing the wires on the wrong terminals is a modification of equipment and is not authorized unless directed.

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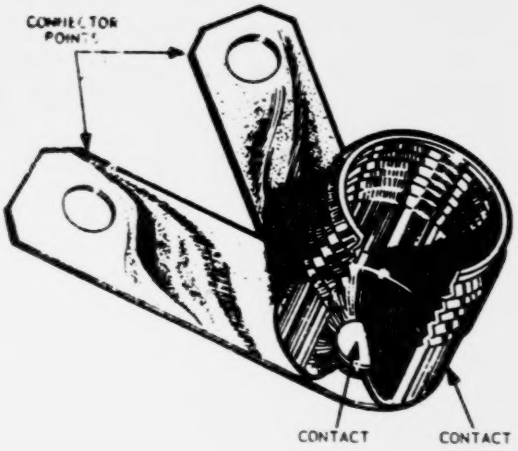


Figure 5-36. Screw base socket.

You must remove power, of course, before removing a defective socket and installing a new socket. You must always take precautions when you work on these units, because, although the lamp may be using only a low-voltage DC or AC source, a shorting of the source voltage to the chassis can result in complete loss of power to the equipment and in site downtime as well as injury to the personnel involved.

A typical removal, reinstallation procedure would be:

(1) Remove power.
(2) Label the wires to be removed.
(3) Unsolder the wires from the socket.
(4) Solder the new socket to the wires.
(5) Check continuity with a VOM.
(6) Secure the socket to the chassis with a washer and a retaining nut.
(7) Apply power and perform an operational check.

The offset prong plug-in lamp shown in figure 5-35 requires a socket like that shown in figure 5-37. Observe how one side of the socket has a cut higher than the other side to accommodate the prongs on the side of the lamp. Also, note that this socket usually contains a spring that pushes the base contact up to the lamp when the lamp is seated properly. The spring allows for insertion of the lamp to seat it properly.

Installation of a lamp (like the offset prong plug-in lamp) requires:

(1) Aligning the prongs on the lamp with the slots in the lamp socket according to the placement.
(2) Inserting lamp into socket, depressing the spring base.
(3) Twisting the lamp and releasing it , allowing the prongs on the lamp to seat in the slots.

Removal procedures are the reverse of the installation ones just given. Replacement of the lamp holder (socket) is the same as that for the screw type.

The *neon indicator*, shown in figure 5-35(3), is commonly used to display data processors where counter operations are shown, when error indicators are used, and when register operation shows cycling operations. Some of these lamps contain internal resistive and capacitive networks plus lamp filaments. Most of the sockets designed to accommodate this type of lamp are generally two- to four-wire connected units. Refer to figure 5-38 and observe a type of socket which is used. Your replacement of this socket requires your strict adherance to identification and your replacement of leads when you reinstall it.

An installation of this lamp is shown in the schematic in figure 5-39. The NE2 lamps (shown) are placed in series with the output of the flip-flops. On these flip-flops, internally the signal swing is from 0V to −30V, depending upon the state of the flip-flop. When the

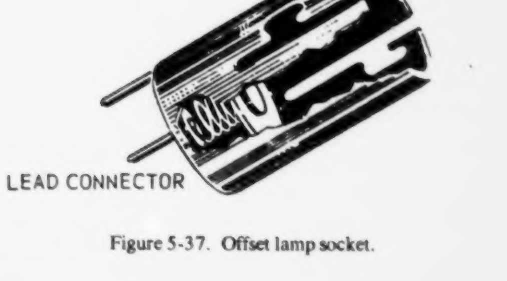


Figure 5-37. Offset lamp socket.

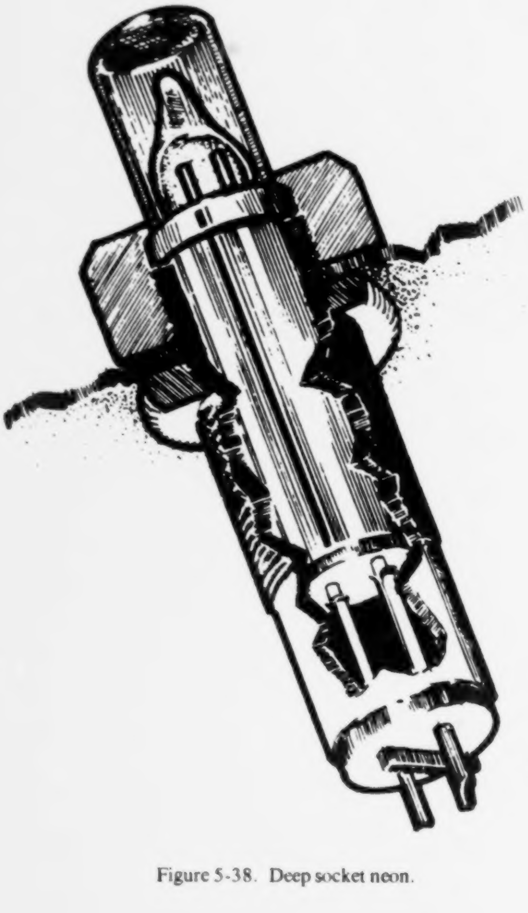


Figure 5-38. Deep socket neon.

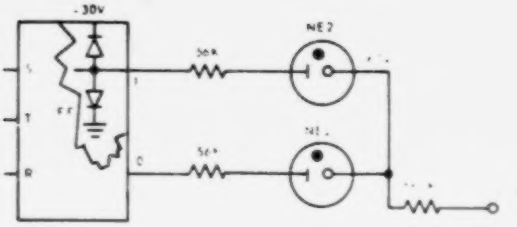


Figure 5-39. Indicator circuit.

output of the flip-flop is a logic 1 (0V), there is an approximate 67V difference of potential across the lamp, and it lights. In the zero state, the difference of potential is only approximately 37V, and ignition of the neon does not occur. Figure 5-35 shows that neons need 65V to start.

The neon lamp shown in figure 5-35(4) is usually found in a power supply. Quite often its purpose is for regulation of the power supply. It may be a plug-in lamp with stiff leads. More commonly, however, it is a lamp with no metal base, and it has flexible lead wires protruding from the glass envelope. (Refer here to fig. 5-40.) In power supplies using this lamp, two wells filled with solder are installed to secure the leads of the lamp. Installation and removal consists of your heating the envelope with a soldering iron, removing the lamp lead, and then inserting the new lamp lead in the molten solder. Again, any work you perform in this area *must* be done with all power removed.

The final lamp shown in figure 5-35 (5) is a *subminiature lamp*. This lamp is pushed into a glass lens, and the lens is then screwed into the socket, as shown in figure 5-41. This lamp unit usually contains a two-wire connection. It may, however, have multiple leads soldered to one of the two connector points. Your strict observance of wire placement is necessary when you remove or replace the lamp base. Use procedures outlined in the description of the basic screw lamp.

The tasks involved in the replacement of a lamp socket are basic and simple; yet a few specific practices do become important when analysis is applied. These are:

(1) Mark the wires to be removed and installed on the new socket.

(2) Exercise care in removing and replacing a lamp from the socket after first determining the type of lamp used.

(3) Remove power from the unit before starting any repair action.

(4) Use proper soldering techniques in all cases.

(5) Make a static check with a VOM for continuity prior to applying power.

(6) Apply power and make a dynamic check.

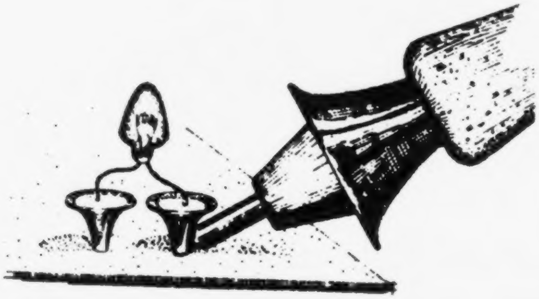


Figure 5-40. Neon in well socket.

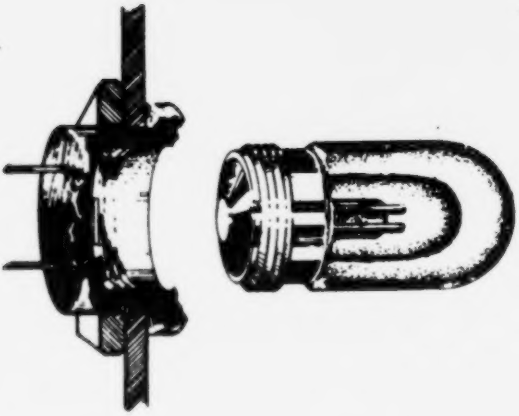


Figure 5-41. Subminiature socket with neon lamp.

Learn to recognize the various types of lamps from their appearance, size, use, description on a schematic or wiring diagram, and their voltage ratings. Above all, observe and practice safety to protect yourself and your equipment. A mistake could burn or kill you. A mistake could also destroy your equipment, cause unscheduled downtime, abort a mission, or cause a loss in the net.

Fuses and fuse holders. We have already identified a fuse as an indicator for the maintenance man which will alert him to a defect or malfunction in the system. The primary use of any fuse is, of course, to protect an electronic unit from destruction by excessive current or voltage. This fact then leads to the analysis of fuse applications in the following terms: (1) Where are fuses normally installed? (2) What are the principles of fuse operation? (3) What sizes and shapes are they, and what type holders are provided for them? (4) Finally, what comparisons are there between the removal and replacement of the holder to that of the lamp holder just discussed?

Refer to figure 5-42. Typically, you will find a fuse in an input power line whether it be an AC or DC source voltage. Fuses may be installed on a drawer, a rack, and a chassis, or in a cabinet. They may be remotely placed and still be wired to the circuits of a given unit. The important thing for you to know is where the fuse circuits are for your equipment. Air-conditioning systems, motors, and cabinet service lights are also examples of circuits that will be fused to prevent destruction by overload in these units. On a wiring diagram you will probably see a fuse as a symbol like the one shown in figure 5-43. The designation will usually be an "F" followed by a number.

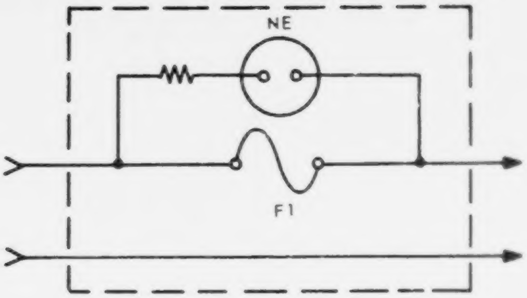


Figure 5-42. Fuse and fuse holders.

On the fuse itself will be a number. It will very likely look like this example:

Part
Number

Breakdown: F01 A 125V 2A

2-ampere rating

125V maximum voltage

Characteristic (normal-blow)

Style or dimension code (ferrule, glass, size)

The current-carrying element in a fuse melts when heated to temperatures in excess of about 170° and opens, thereby removing the source voltage from a unit. Two factors are important in this analysis: first, the type of material used for fusing and its melting properties and, second, the principles of Ohm's and Kirchoff's laws as applied to circuits using fuses. In the first instance, the current-carrying element used in fuses is engineered to specific thicknesses, lengths, and widths to carry specific voltage and current loads. This metal will heat and remain intact, provided the applied heat does not exceed the melting point of the metal. Second, basic laws of electronics apply to selection of fuses for specific circuits. You must consider the (1) total wattage dissipation, (2) total amperage needed to maintain circuit operation, and (3) total voltage requirements when you determine the size and type of fuse that you will use.

How does Ohm's law apply to fuses?

$$\text{Ohm's law: } I = \frac{E}{R}, \text{ or } R = \frac{E}{I}, \text{ or } E = IR, \text{ or } R = IE$$

Consider a unit using a 125V, 2A fuse. Consider, also, that the fuse will blow at exactly 2A. What effect can an increase in line voltage have on the fuse? Using the formula $I = \frac{E}{R}$:

$$I = 2A \quad E = 125V \quad R = \text{resistance of the fuse}$$

$$\uparrow 2A = \frac{125\uparrow}{R\rightarrow} = \text{blown fuse (arrows indicate a change)}$$

With the resistance of the fuse wire as a constant, an increase in line voltage causes an increase in current, and the fuse melts. Another problem: What effect can a decrease in resistance within the circuits cause? The power formula $P = E^2$ is used. A short circuit in the operating unit will very likely lower the total resistance of the unit to almost ground potential and increase the power requirements by increasing the current flow. Since power is related to heat, the fuse filament will develop more heat and burn through.

$$\uparrow P = \frac{E^2\rightarrow}{R\uparrow} \text{ blown fuse}$$

Another basic principle of electronics is Kirchoff's law. Looking at the schematic found in figure 5-42, observe how, when the fuse is intact, current will flow into the entire circuit through the fuse and not the NE2 lamp circuit, because current will always seek the easiest path. However, if the fuse blows, the current path is through the NE2 lamp. This lamp circuit will draw very little current and no damage will result to the circuit. This circuit is used where a visible indicator is used to show a blown fuse.

Fuse holders can become damaged and require replacement. The most common causes of damage are heat and mechanical abuse. If holders are corroded, dirty, or loosely hold the fuse, they will heat. The heat, in turn, can damage the insulating material in the holder. The heating condition will get worse with time, and the holder will have to be replaced.

By observing the fuse holders shown in figure 5-43, it should be easy for you to see that only two connectors will usually have to be unsoldered and resoldered when you replace a fuse holder. The tasks of replacing a fuse holder and the replacement of the lamp socket are so nearly alike that this restatement of the typical steps will apply to almost all work done on fuse holder replacement:

(1) Mark the wires to be removed.
(2) Remove power before starting any repair action.
(3) Exercise care in removing the unit.
(4) Employ proper soldering techniques in all cases.
(5) Make a static check with a VOM for continuity prior to applying power.
(6) Insert a new fuse of the proper voltage and amperage ratings, size, and type.
(7) Apply power and make a dynamic check.

Our analysis of fuses and their holders has shown that the task of fuse holder replacement is simple and basic and that it parallels the techniques used in the replacement of lamp sockets. This analysis has also shown that various types of fuses exist for specific purposes. Further, the fuse wire is designed to carry or handle a specific maximum voltage and current source. Exceeding these values causes the filament to melt, protecting the circuit. Also, this analysis pointed out what effect a short circuit in the equipment must have on the circuit fuse. Correct interpretation of these facts makes it paramount that exact replacement of fuses with both proper voltage and current ratings be installed, and exact types, such as fast blow or slow blow, be reinstalled.

If you should encounter an unfamiliar fuse designator,

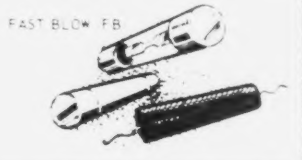
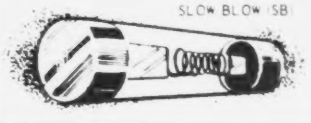
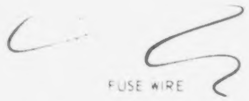
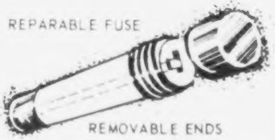
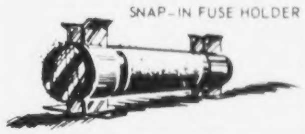
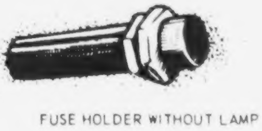
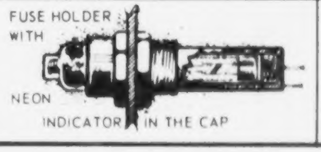
NO.	TYPE PICTORIAL	SIZE VOLT AMP RATING	DESCRIPTION USES APPLICATION
1		125V/250V .01/10A 1-1/4" L X 1/4" Dia. 1" L X 1/4" Dia. 5/8 X 5/64	Metal ends with a glass or ceramic cylinder between the ends. Blows instantly with input surges or shorts.
2		125V/250V .01/30A 1-1/4" X 1/4" Dia.	Similar to Fastblow in size, except this fuse is designed to withstand heavy surges for a short time period but will blow instantly on shorts.
3		125/250V Variable amps depending upon the diameter of the wire.	A strand of malleable wire designed to melt as any other fuse. However, this fuse is usually connected between terminals and not put in a fuse holder. This wire may also be used to repair reparable fuses.
4		125/440V Variable to 100 amps, sizes vary with amperage and voltage requirements.	This fuse has screw-type end connectors which, when removed from the center cylinder, allow for replacement of the fuse wire.
5.		Size and weight is determined by the size of fuse to be held.	Built to accommodate short and long FB and SB fuses as well as reparable fuses.
6		1-11/32" X 5/8" overall. Voltage ranges to 250V @ 15 amps. 1-5/8" X 5/8"	Fuse holder with a twist top. Top is removed by slight inward pressure and twisting the release. Internal contact is backed by a spring to allow for removal and installation of a fuse.
7	 FUSE HOLDER WITH NEON INDICATOR IN THE CAP	Approximately 2-3/8" L X 5/8" Dia. Voltage ranges 2.5V to 250V @ 20 amps.	Fuse holder with a neon indicator in the cap. This neon lights when the fuse blows (refer to text for description.)

Figure 5-43. Fuses and neon circuit.

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refer to your equipment technical data or to TO 00-25-234, *General Shop Practice Requirements for the Repair, Maintenance, and Test of Electronic Equipment.* Section V of this TO provides detailed information on the reading of fuse designations and a cross-reference of military and commercial designations for fuses.

Exercises (471):

1. Why is it important for you to remove power before you install a new lamp socket?

2. State the steps in a typical removal, installation procedure.

3. How is an offset prong plug-in lamp installed?

4. What are the two uses of the NE68 lamp?

5. Where are fuses normally found in a circuit?

6. What is the approximate melting temperature of the current-carrying element of a fuse?

7. What effect will a large decrease in resistance have on a circuit fuse?

8. What are the most common causes of fuse holder damage?

9. How is a fuse holder replaced?

10. What is the title of TO 00-25-234 that cross-references military and civilian designations for fuses?

472. Identify switch types by their description, or use, indicate signs of such defects, and briefly describe switch replacement procedures.

Identification and Replacement of Switches. We will review here the types of switches used in electronic equipment, since there might be some type which you are unfamiliar with. For the power-on and power-off functions, you will find that the types of switches used are very similar to those that you might have used in turning off your electronic equipment in your home. Of course, switches are designed for many other uses. Two broad uses of switches are (1) digital input and (2) command input devices. A switch designed to provide a digital input will provide the input source for either a static level logic 1 or a dynamic level 1, or a pulse train. It may even provide the source for an octal input. A switch designed to provide command input will provide preset, reset, advance, repeat cycle, and other short-duration machine command signals. Analysis will show how these switches are used and what types of switches are usually associated with these actions.

The identification of switches, their uses, and their defects also includes descriptions of their reference symbols, schematic symbols, coil operations, lamp circuits associated with these, and external circuits commonly employing switches. Since defects are common to almost all types of switches, the repair or replacement of the switches is explained as a common element instead of individually.

The most common switch known is the *toggle switch.* Refer to figure 5-44 for a pictorial description of this switch type. This switch may be designed as a single-pole single-throw (SPST) having two fixed conditions—ON and OFF—or it may be spring-loaded, as in the case of a reset switch, where it can be turned on and will spring back to OFF when released. The spring-loaded version is usually found in command or control circuitry. This is where a reset pulse must be used, a clear pulse is needed, or a preset pulse is needed. In any of the uses listed, a relatively short-duration pulse is required, and the spring-loaded toggle switch is effective.

Another switch used for the same purpose is the spring-loaded *pushbutton microswitch.* Its description (refer to fig. 5-44) is different, but its function is exactly the same as that of the spring-loaded toggle switch. The schematic symbols and reference designations for both types of switches are shown in figure 5-45.

Still another switch commonly found in data processors and display consoles is the pushbutton switch with a lamp indicator under the pushing surface. For this see figure 5-44. This switch comes in two types—the nonholding or spring-release return and the holding type. The holding type employs a holding coil that latches the switch in the ON position when depressed. The second pressing of the switch releases the voltage from the holding coil and returns the switch to its OFF condition. In some applications, the holding coil voltage may be removed by another switch remote from the original switch.

In both types of switches, the holding and nonholding, lamp circuits are employed to identify the condition of the switch as ON or OFF. Observe the schematic shown in figure 5-46 and analyze how two of the lights (DS1 and DS2) are lighted when the switch is off and how two different lights (DS3 and DS4) are lighted when the switch is on. Trace the paths for current flow to prove this analysis. Also, observe how the holding coil shown in the

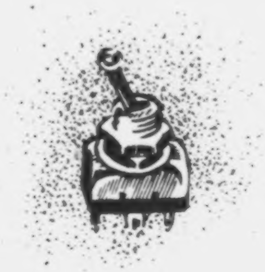
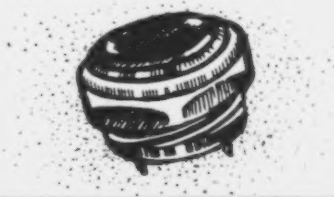
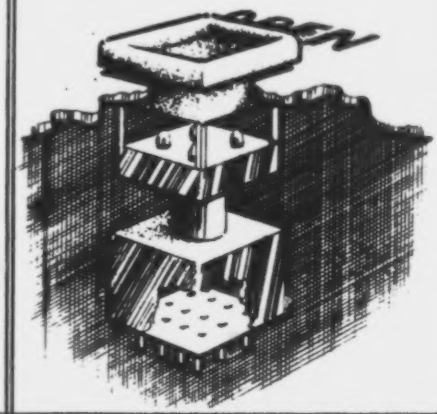
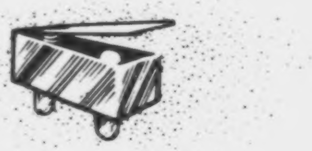
NO	TYPE AND ILLUSTRATION	DESCRIPTION/USE
1.	**Toggle** 	a. Two position OFF, ON, Normally Open (NO), Normally Closed (NC). b. Two position NO, NC and common (C). c. SPST, Single Pole Single Throw. d. DPDT, Double Pole Double Throw. (not shown) multiple connectors in series. e. Spring loaded in one direction. f. Primary uses. (1) Control of voltage and current--ON-OFF. (2) Reset, Preset, Command Control of digital circuits.
2.	Microswitch, circular 	a. Two position ON-OFF, spring loaded contactor. b. Command uses, Reset, Preset control of digit circuits.
3.	**Pushbutton Switch w/Lamp Indicators**  	a. Pushbutton switch with: (1) Lamp indicator for either OFF, or ON or both. (2) Contact connectors NO, NC, C. (3) Holding coil for locking in either NO or NC. b. Holding coil may not be used as lock, requiring independent release. c. Lamps may be OFF or ON or may contain dual lamp circuit where one or more lamps will always be on. d. Primary uses: (1) Digital input device, entering codes, bits, presetting wired configurations, advancing. (2) Command uses, transfer, clear, erase, reset.
4.	Microswitch, rectangular cased with Level Contactor 	a. A rectangular encased switch with 2 external connectors. b. Connector ball is usually depressed by a spring tension arm assembly. c. Uses--controlling operations of electromechanical devices.

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Figure 5-44. Switches.

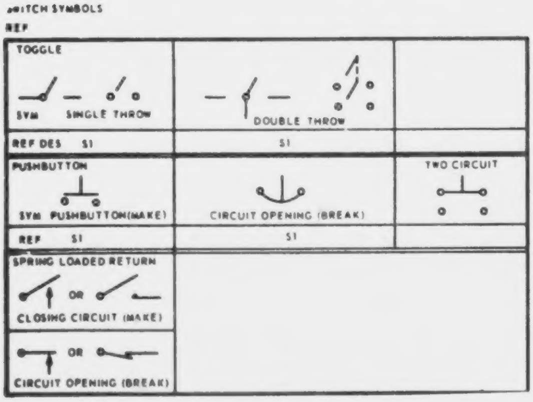
SWITCH SYMBOLS
REF
TOGGLE
SYM SINGLE THROW
DOUBLE THROW
REF DES S1
S1
PUSHBUTTON
TWO CIRCUIT
SYM PUSHBUTTON(MAKE)
CIRCUIT OPENING (BREAK)
REF S1
S1
SPRING LOADED RETURN
OR
CLOSING CIRCUIT (MAKE)
OR
CIRCUIT OPENING (BREAK)

Figure 5-45. Switch symbols.

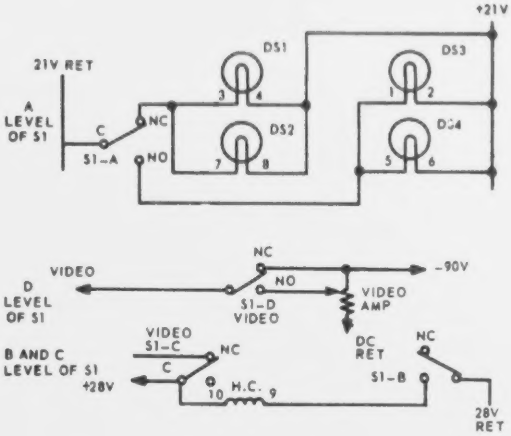
+21V
DS1
DS3
21V RET
A LEVEL OF S1
C
NC
NO
S1-A
DS2
D:4
3 4 1 2 7 8 5 6
NC
VIDEO
-90V
D LEVEL OF S1
NO
S1-D VIDEO
VIDEO AMP
VIDEO S1-C
B AND C LEVEL OF S1
+28V
NC
C
10 H.C. 9
DC RET
NC
S1-B
28V RET

Figure 5-46. Switch (with holding coil) circuit.

schematic is energized and deenergized as a result of the switch action. Your observation of the current path will illustrate this premise. Always remember that all circuits function only when the path for current flow is complete.

The type of switch shown in figure 5-47 is usually used in digital units. It may be used, as shown in section A of this figure, to enter a static level 1 to a register or counter each time it is depressed; or it may be connected, as shown in sections B and C, to relays to provide a pulse train in either binary, binary coded decimal, grey code, octal, or a special code prepared for specially designed circuitry.

The microswitch used in mechanical devices is another switch commonly found in many of our electronic devices, as is shown in figure 5-44. This switch is often placed in a drive unit, so that closing its contacts causes a cycle to repeat or stop. The illustration in figure 5-48 shows that when the switch is depressed by the pivoted arm of the cam, it breaks the cycle and causes a change in operation. These microswitches are spring-loaded; and, when the arm is removed, the switch is returned to its normal state.

We have discussed the various switches used in our equipment. Now, let us identify malfunctions which might be attributed to them, what repair actions are required, and what safety factors must be employed.

Defects which occur most often are these:

- A defective spring.
- A broken contact.
- A burned contact.
- Shorted contacts.
- A charred switch body.

Signs of defects are these:

- Sticking of the spring-loaded switch.
- No continuity when checked.
- A loose toggle.
- Improper placement of the microswitch unit.
- Improper solder connections.
- A nonoperating holding coil.

Since switches may have more than two connections, exact replacement of wires is an absolute *must*. Some

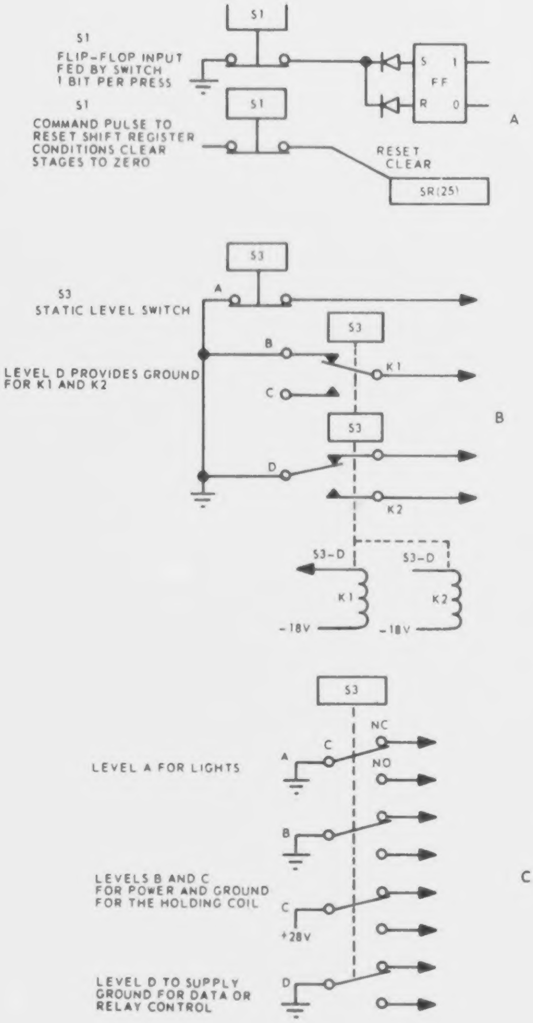
S1
S1
FLIP-FLOP INPUT FED BY SWITCH 1 BIT PER PRESS
S 1
FF
R 0
S1
COMMAND PULSE TO RESET SHIFT REGISTER CONDITIONS CLEAR STAGES TO ZERO
RESET CLEAR
SR(25)
A
S3
S3
STATIC LEVEL SWITCH
A
S3
B
K1
LEVEL D PROVIDES GROUND FOR K1 AND K2
C
B
S3
D
K2
S3-D
S3-D
K1
K2
-18V
-18V
S3
NC
C
LEVEL A FOR LIGHTS
A
NO
B
LEVELS B AND C FOR POWER AND GROUND FOR THE HOLDING COIL
C
C
+28V
LEVEL D TO SUPPLY GROUND FOR DATA OR RELAY CONTROL
D

Figure 5-47. Pushbutton switch circuit.

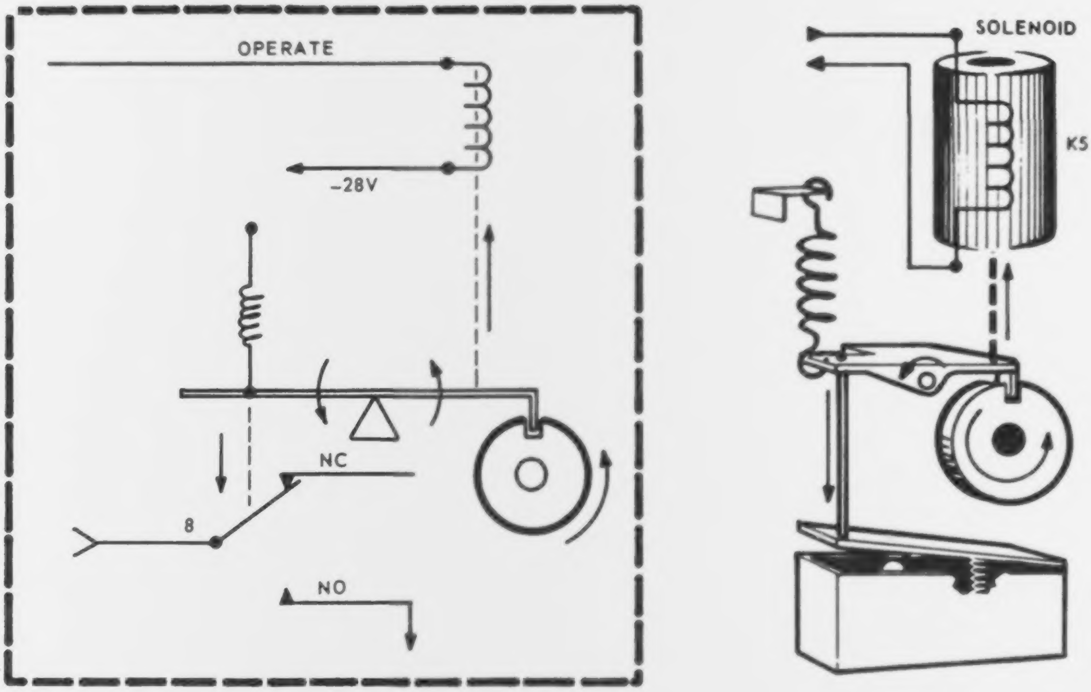

Figure 5-48. Microswitch operation.

switches, such as the push-and-hold with lamp circuits and holding coils, have as many as 12 or more pins. Since these are arranged in rows, they are often designated by A, B, C, D or 1, 2, 3, 4; and each row could have a normally open (NO), common (C), and normally closed (NC) connector. Identification of wires prior to their removal from the defective unit is a *must.*

To replace switches, follow these basic procedures:

a. Remove power to the switch (safety).
b. Carefully label all wires for exact replacement.
c. Remove wires by using proper unsoldering techniques (if soldered).
d. Position and solder the new switch to the leads.
e. Secure the switch to the cabinet.
f. Perform a static check with a VOM.
g. Perform a dynamic check with power applied to insure that:

(1) All lights, if any, work properly.
(2) Coil holds or spring releases properly.
(3) Switch is properly positioned.
(4) Mechanical operation is as specified in the applicable technical publication.

Exercises (472):

1. Contrast the uses of (a) digital input and (b) command input devices.

2. Identify the type of switch that best matches its description.
   a. A rectangular encased switch with two external connectors.
   b. Two-position OFF-ON.
   c. Lamp indicator for either OFF or ON or both. Contact connectors, NO. NC, C.
   d. Two-position ON-OFF, spring-loaded contactor.

3. What are the uses of the digital switch shown in figure 5-46?

4. By what signs do you know that a switch is defective?

5. Briefly list the steps to be followed when replacing a switch.

473. Identify the labeling methods used on and the basic sections of connector pins, and list the steps involved in repairing a connector.

Removal and Replacement of Electrical and Mechanical Connectors. The repair, removal, and replacement of electrical and mechanical connectors are similar to the tasks we have described previously. You were working with soldered connections in the case of switches. Now you will be working with solderless connectors as well as with soldered connections.

Refer to figure 5-49 as we proceed. Pictured here are two examples of connectors you will find in your equipment. Either connector, although they are used in different places in the equipment, will perform similar functions; that is, connecting circuits through electrical connections to transfer data, signals, or voltages. These two types of connectors are manufactured for as few as one wire connection to as many as 225 wire connections. Each pin connector is labeled (see the illustration). Lettering is usually used in preference to numbers, starting with A through Z and continuing with AA through ZZ, if necessary, except for the letters I, O, and Q, which are never used. There are some equipment areas in which the connector pins are labeled with numerals. Learn how the connectors are labeled in your equipment and where they are. Numbering on the units usually follows general reading rules. For example, the pins are designated A and B on row 1 across, C and D on row 2 across, etc., through to the end, or A, B, C, etc., clockwise in circular cable connectors.

Observe figure 5-50 next. On these multiple connector bodies, the solderless pins—both male and female—are designed to hold a single wire and are meant to be inserted into a connector body. Each pin has three basic sections: A—the wiring retaining section, which is crimped to hold the unit; B—the spring tension section, which is designed to lock the pin in place in the hole provided in the connector body; and C—the male or female mating unit. Looking at D of this figure, the cutaway cross-section of a typical connector body, observe how a ridge is employed to accept the spring tension clip, the "B" portion of the pin. When inserted in the connector body, the pin locks in place. Removal of this pin requires an extraction tool that is designed to slide over the spring tension clip, compress the spring, and allow removal of the pin.

Many companies manufacture crimping tools. However, each crimper is designed to perform the same function: To secure a wire to the pin by crimping a portion of the pin around the wire with enough pressure to retain the wire. Crimpers are designed to allow their function to be performed on all sizes of wire and pins. For instance, a crimper used to fasten a pin to #22 wire would have a very small opening, as shown in figure 5-51, whereas a size 12 wire would require a crimper with a

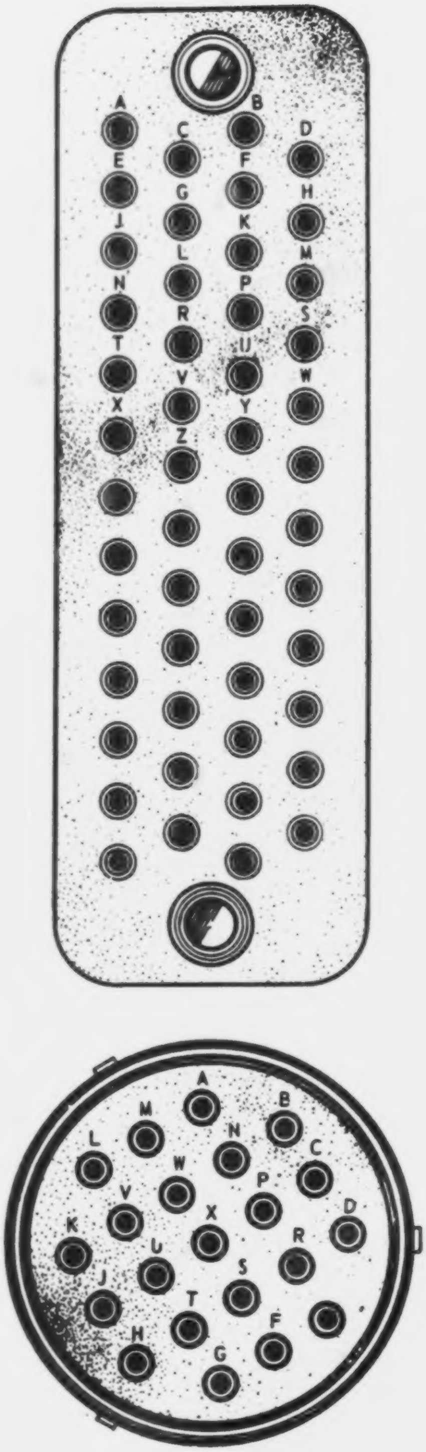

Figure 5-49. Connectors.

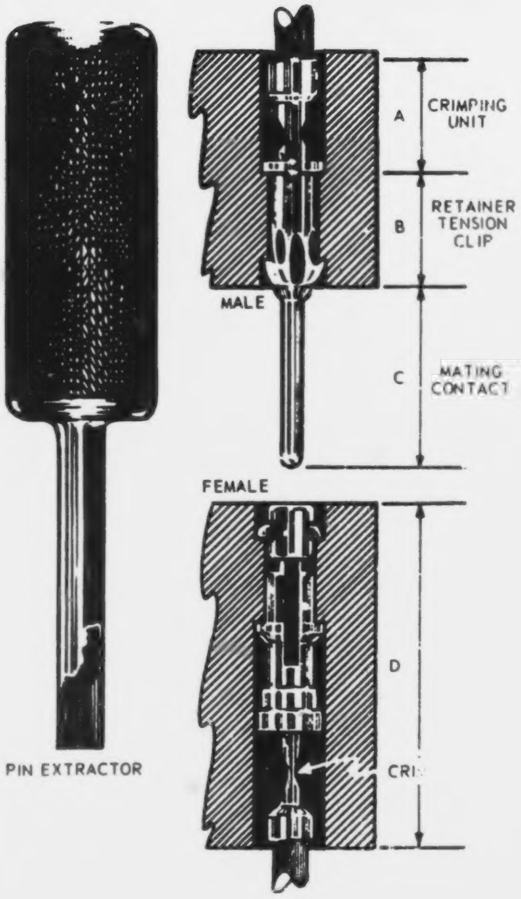

Figure 5-50. Solderless pin connector unit.

wider opening to accommodate the larger wire and pin.

When removing and replacing or repairing the jacks, plugs, or connectors on your equipment, learn (by studying the manufacturer's publication) which tool is used for each size wire and pin used in your system.

Some of the types of defects you might encounter with jacks, plugs, or connectors are these:

- Recessed pins.
- Loose-fitting pins.
- Cracked or broken plastic connectors.
- Bare wire contact with the metal casing in metal connectors.
- Defective threads or missing guide pins on metal connectors.

See figure 5-52 for an illustration of listed defects. Listed below are the typical steps involved in the replacement of multiple connectors. Bear in mind that one very helpful feature in the manufacture of multiple lead cables is that the cable strands are generally twist-paired and color-coded.

(1) Carefully mark each wire position and color code prior to starting any repair action.

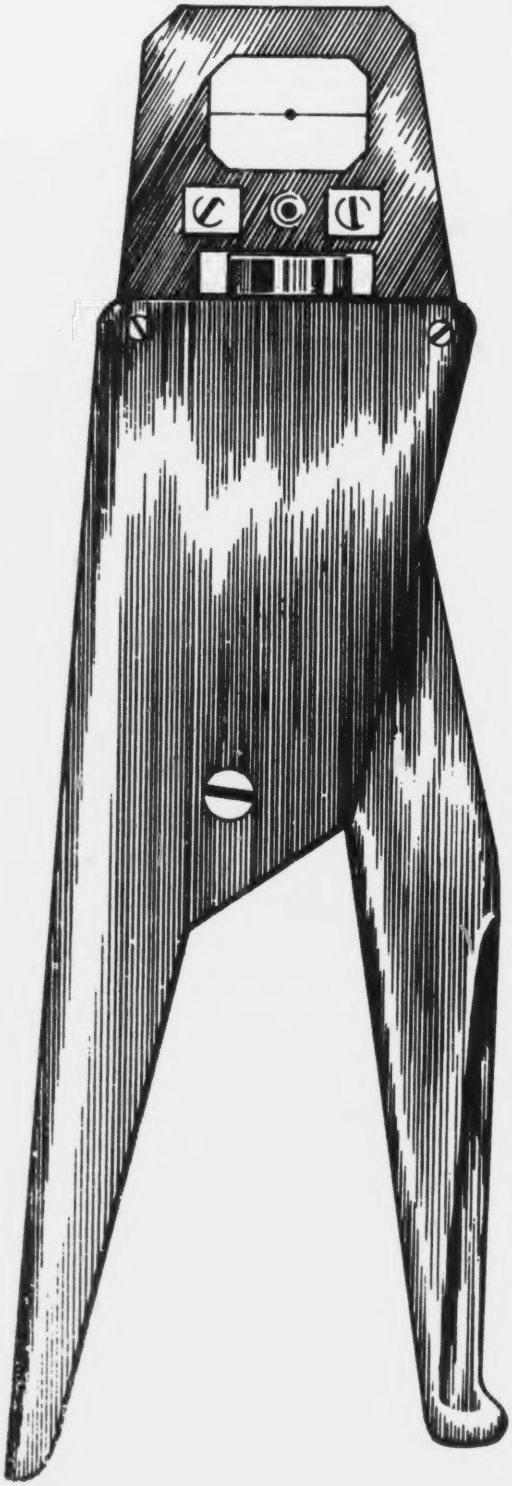

Figure 5-51. Crimper.

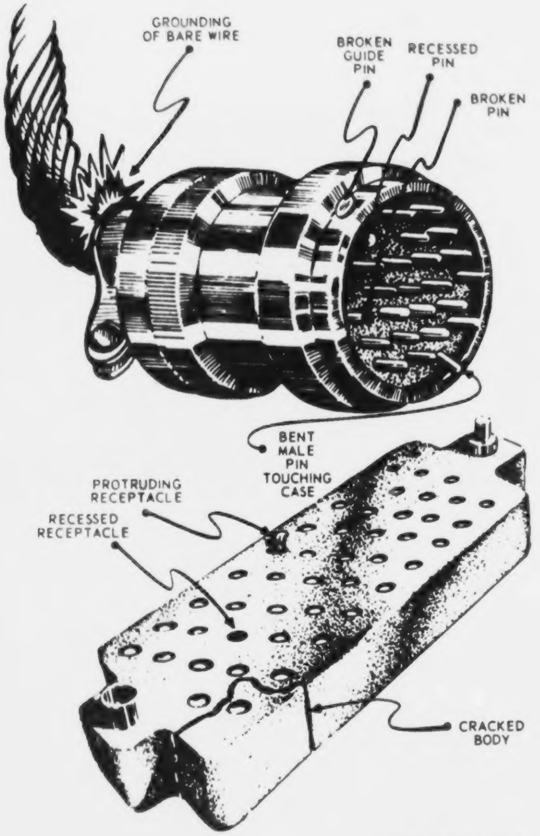

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Figure 5-52. Defective connector.

(2) Remove power before proceeding with any work (safety).

(3) Disconnect the connector from the panel (if applicable).

(4) Use the pin extractor to release the pins.

(5) Insert the pins in the new connector if all pins are in good condition.

(6) Replace any defective pin.

(7) Examine workmanship for properly seated pins, no cracks, and no frayed or loose wiring.

(8) Secure the connector to the frame (if applicable).

(9) Secure the mating unit to the repaired or replaced connector and carefully match the guide pin.

(10) Apply power and make dynamic checks (where applicable).

The removal and replacement of multiple connectors requires you to make a careful, conscientious effort. You must focus your attention on the elements listed in this text and on peculiar factors of your equipment that may be potential trouble spots. You must select a definite method for identifying wires before removing them from the connector to be changed, and you must insure 100-percent accuracy and quality when reinstalling the wires and pins. Further, you must use the correct crimping tool for the size wire and pin when replacement of pins is required. Finally, you must be able to recognize deficiencies and to relate them to possible trouble symptoms.

Exercises (473):

1. What two methods are used to identify connector pins?

2. Which of the methods identified in exercise 1 is preferred?

3. Which letters are not used to identify pin connectors?

4. What are the three basic sections of connector pins?

5. Briefly list the steps involved in repairing a connector.

5-6. Circuit Card Repair

Increased reliability, economical operation, increased packing density, and weight reduction have resulted from the ever-increasing use of printed circuit cards in the electronic switching equipment that you maintain.

474. Identify the types of printed circuits, defining one, and give certain precautions for reparable printed circuits.

First, the types of printed circuits; then second, general precautions to observe when repairing such circuits—these concern us in this BOF unit.

Types of Printed Circuits. Two basic types of printed circuit assemblies exist. The first, a true printed circuit, is a circuit comprised of printed wiring and printed parts, all arranged in a predetermined design on, or attached to, a flat insulating material surface that forms a common base. The second, those printed circuits more commonly used, includes those made up of conductive patterns (printed wiring) and miniaturized separable parts. Of the two types, only the printed circuit assembly using separate parts is readily reparable. The printed circuit assembly wiring pattern is formed in three basic ways: by painting, by chemical deposit, and by being stamped or etched on metal foil.

Painted-type printed circuits. The wiring pattern on the painted type of printed circuit board is formed by brushing or spraying a conductive paint through a stencil onto the nonconducting base. Repair of these painted printed circuit boards is not recommended, unless a specialized technique—one which will not degrade overall reliability—has been devised.

Chemically deposited printed circuits. The chemically deposited type is made by using a stencil and an appropriate chemical solution. When dipped into this solution, the wiring pattern—in the form of a metallic film—is precipitated on the nonconducting base. Repair of chemically deposited printed circuit boards is not recommended.

Metal-foil printed circuits. The wiring pattern on the metal-foil type of printed circuit board consists of thin metal foil bonded to the nonconductive base. The wiring pattern is produced by stamping or chemically etching to remove unwanted portions of the metal foil. The metal foil type is the most readily reparable. Consequently, it is the most commonly used type of printed circuit assembly. Therefore, repair techniques described in later objectives will apply primarily to metal-foil printed circuits.

General Precautions. Certain precautions are necessary in soldering printed circuit cards because of the delicate nature of the wiring material, wiring-to-card bonding, and the heat sensitivity of miniaturized parts. Thus, when you solder printed circuit cards, these are the general precautions you must observe:

(1) Reduce the amount of heat required for the soldering operation by using a small-diameter low-melting-point solder.

(2) Use a small, low-power soldering iron to permit access to cramped areas of the card.

(3) Use grounded soldering iron equipment or ground the soldering iron tip, preferably by using alligator clip leads. The leakage current of some soldering irons is enough to damage transistors and small semiconductor devices.

(4) Use enough thermal shunts or heat sinks to protect heat-sensitive devices sufficiently.

(5) Insure that the total time of heat application does not exceed the time required to melt the solder and provide proper fusion of solder with the terminal pad and component lead. When you make a solder connection, apply the minimum amount of heat required to produce a satisfactory connection.

(6) If you experience difficulty in soldering a connection, stop and allow the connection to cool completely before you attempt to resolder.

(7) Remove flux and flux residues from solder connections after the connection has cooled. Remove these by using isopropl alcohol or aliphatic naphtha.

Exercises (474):

1. State what a true printed circuit is.

2. What are the three basic printed circuit patterns?

3. How is a chemically deposited printed circuit made?

4. How is a metal-foil printed circuit made?

5. Of the two basic types of printed circuits, which one is reparable?

6. Supply certain precautions necessary for reparable printed circuits.

475. Give the procedures in troubleshooting a printed circuit, determining the extent of the trouble and repairing printed circuits.

Troubleshooting Printed Circuits. Although the troubleshooting procedures you should follow for printed circuits are similar to those you follow for conventional circuits, the repair of printed circuits requires considerably more skill and patience. The reason is that printed circuits are small and compact. Thus, you and your fellow personnel should become familiar with the special servicing techniques required.

In all instances, check the defective printed circuit before beginning work on it. Also, determine first whether any prior servicing has been done on it. Not all personnel having access to this type of equipment have the skill and dexterity required for its maintenance; hence, some preliminary service may be necessary. By observing this precaution, you may save a great deal of time and labor.

You should pinpoint the defective part by a study of the symptoms and by a careful and patient analysis of the circuit before attempting to trace trouble on a printed circuit board. Determine whether the conducting strips are coated with a protective lacquer, epoxy resin, or similar substance. If so, carefully scrape it away or, better still, use a needle or chuck-type needle probe, as shown in figure 5-53, that will easily penetrate the coating for a continuity check.

Breaks in the conducting strip (foil) can cause permanent or intermittent trouble. In many instances, these breaks are so small that you cannot detect them with your naked eye. You can only locate these almost invisible cracks (breaks) with the aid of a powerful hand- or stand-held magnifying glass, as illustrated in figure 5-54.

The most common cause of an intermittent condition is poorly soldered connections (cold solder joints). Other causes are broken boards, broken conducting strips, fused conducting strips, arc over, loose terminals, etc.

To check out and locate trouble in conducting strips of a printed circuit board, set up a multimeter for making

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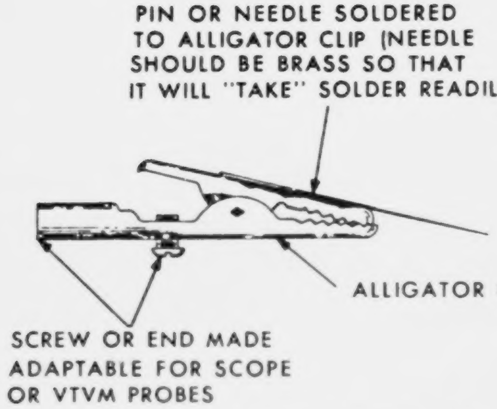
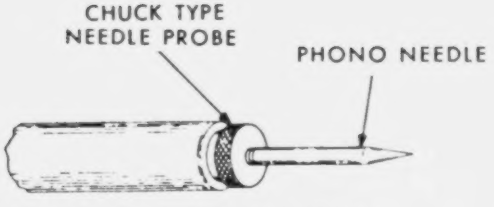

PIN OR NEEDLE SOLDERED TO ALLIGATOR CLIP (NEEDLE SHOULD BE BRASS SO THAT IT WILL "TAKE" SOLDER READILY.)
ALLIGATOR CLIP
SCREW OR END MADE ADAPTABLE FOR SCOPE OR VTVM PROBES

IMPROVISED NEEDLE POINT PROBE

(A)


CHUCK TYPE NEEDLE PROBE
PHONO NEEDLE

COMMERCIAL TYPE NEEDLE POINT PROBE

(B)

Figure 5-53. Needle probes.

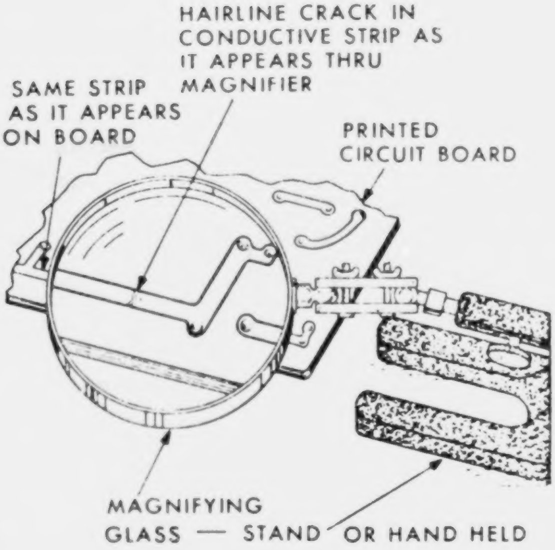

HAIRLINE CRACK IN CONDUCTIVE STRIP AS IT APPEARS THRU MAGNIFIER
SAME STRIP AS IT APPEARS ON BOARD
PRINTED CIRCUIT BOARD
MAGNIFYING GLASS — STAND OR HAND HELD

Figure 5-54. Using a magnifying glass to locate a hairline crack.

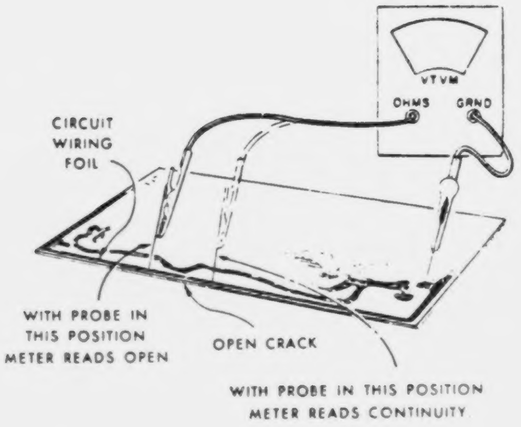

VTVM
OHMS
GRND
CIRCUIT WIRING FOIL
WITH PROBE IN THIS POSITION METER READS OPEN
OPEN CRACK
WITH PROBE IN THIS POSITION METER READS CONTINUITY

Figure 5-55. Using VTVM to locate a break in conductive strip.

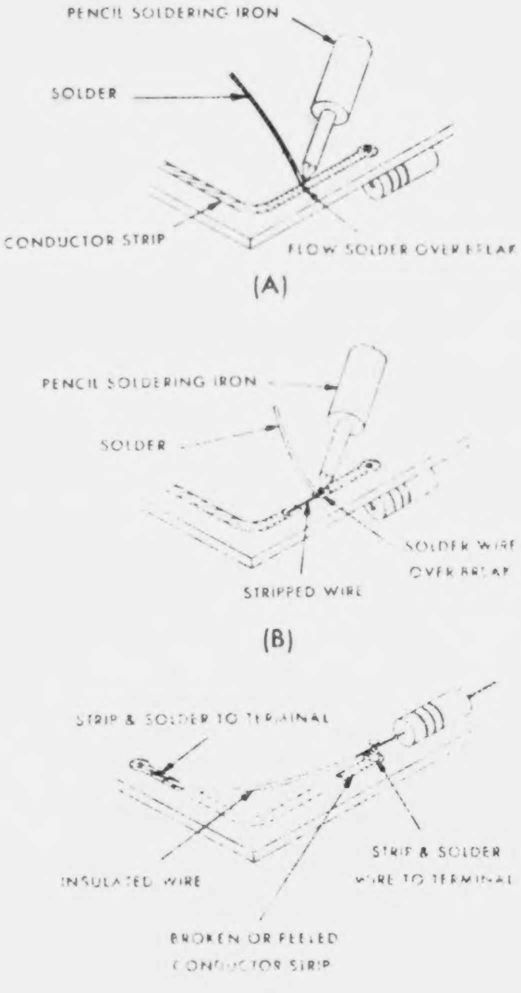

PENCIL SOLDERING IRON
SOLDER
CONDUCTOR STRIP
FLOW SOLDER OVER BREAK
(A)
PENCIL SOLDERING IRON
SOLDER
SOLDER WIRE OVER BREAK
STRIPPED WIRE
(B)
STRIP & SOLDER TO TERMINAL
INSULATED WIRE
STRIP & SOLDER WIRE TO TERMINAL
BROKEN OR PEELED CONDUCTOR STRIP
(C)

Figure 5-56. Three methods of repairing broken conducting strips.

point-to-point resistance tests, as shown in figure 5-55, using needlepoint probes. Insert one point into the conducting strip close to the end of the terminal, and place the other probe on the terminal or opposite end of the conducting strip. If the multimeter indicates an open circuit, drag the probe along the strip (or if the conducting strip is coated, puncture the coating at intervals) until the multimeter indicates continuity. Mark this area and then use a magnifying glass to locate the fault in the conductor (fig. 5-54).

CAUTION: Before using an ohmmeter for testing a circuit containing transistors or other voltage-sensitive semiconductors, check the current it passes under test on all ranges. Do not use a range that passes more than 1 mA.

If the break in the conducting strip is small, lightly scrape away any coating covering the area of the conducting strip to be repaired. Clean the area with a firm-bristle brush and approved solvent; then repair the cracked or broken area of the conducting strip by flowing solder over the break (fig. 5-56,A). If there is any indication that the strip might peel, bridge the break with a small section of bare wire by the method shown in figure 5-56,B. Apply solder along the entire length of the wire to bond it solidly to the conducting strip. You must use considerable care in applying the solder to prevent it from flowing onto or near an adjacent strip. Keep the solder within the limits of the strip that is being repaired. If a strip is burned out or fused, cut and remove the damaged strip. Connect a length of insulated wire across the breach or from solder point to solder point (fig. 5-56).

It is best for you not to glue or bond a conducting strip that has been lifted or peeled from the board at a terminal or solder point. Instead, clip off the raised section and replace it with insulated hookup wire from solder point to solder point. Printed circuit boards are frequently subject to leakage and shorts, especially if the spacing between conductors is very close or because of the careless formation of a solder bridge between the conducting strips during soldering. (NOTE: After repairs, always scrutinize the board for solder droppings that may cause possible shorts.)

Frequently a low-resistance leakage path is created by moisture and/or dirt that has carbonized onto the phenolic board. You can detect this leakage by measuring the suspected circuit with a multimeter. To overcome this condition, clean the carbonized area thoroughly with solvent and a stiff brush. If this does not remove it, use a scraping tool (spade end of a solder aid tool or its equivalent) to remove the carbon, or drill a hole through the leakage path to break the continuity of the leakage. When you use the drilling method, be careful not to drill into a part mounted on the other side.

Occasionally a conductor will rupture or fuse, usually because of a current overload. Generally the rupture, or fusing, is the result of limited spacing and narrow conductors. Do not try to repair this type of damage, other than to bridge the rupture or fused area with a length of insulated wire, as shown in figure 5-56,C.

Most printed circuit boards have areas of conduction, known as grounding conductors, at each edge of the board or on the parts-mounted side of the board. These grounding conductors are conducting strips used for grounding parts and as a mounting contact for the chassis or common ground. Sometimes an intermittent conduction will result if the grounding screws or mounting screws become loose. If this occurs, tighten the screws and then solder a good bond directly from the grounding strip to the chassis or equipment ground. If this is not practical, bond the screws (after tightening) with epoxy resin or similar compound.

The most common cause of broken boards is droppage. Some boards are broken because of careless handling by service personnel while the equipment is under repair. Be extremely careful at all times while handling a board. Do not flex the board indiscriminately; be especially careful when removing the board or replacing parts; do not force anything associated with the board.

A printed circuit can be flexed to a certain extent; however, flexing may break the board, which must then be replaced at a considerable loss of time. To prevent this possibility, it is always a good policy to use a chassis-holding jig or vise when servicing printed boards.

Before repairing a broken printed circuit board, assess the damage. Inspect the condition of the board and the extent of the break. If the board is not too complicated or the damage not too extensive, you can probably repair it.

After completing the repairs, clean the repaired area with a stiff brush and solvent. Allow the board to dry thoroughly, and then coat the repaired area with an epoxy resin or similar compound. This coating not only will protect the repaired area but will also help to strengthen it.

NOTE: When a board is broken, it is much better for you to replace the entire board. The repair techniques given above are only for temporary repairs.

Exercises (475):

1. What is the first thing a maintenance man should check before performing maintenance on a printed circuit?

2. How should a defective part on a printed circuit be pinpointed?

3. What is the most common cause of intermitttent conditions in printed circuits?

4. What is the correct procedure in locating a trouble in a conducting strip?

5. What precaution should you always observe when

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you are testing a circuit containing transistors or other voltage-sensitive semiconductors?

6. If the break in a conducting strip is small, what are the correct repair procedures?

7. What is the correct procedure for repairing a conducting strip that has lifted or peeled from the board?

8. What is the most common cause of broken circuit boards?

476. Specify the correct procedures for checking printed circuit card components and indicate the grouping of integrated circuits for testing and ways to identify transistor loads.

Testing Printed Circuit Card Components. Reactive components can become open or shorted. In either case, the component is useless, because it cannot store energy. Coils and capacitors can also become partially efficient because of partial shorting or leaking. The following discussion covers some of the common procedures for checking reactive components.

Covered in this unit are, in sequence, capacitor troubles, inductor troubles, and diode troubles.

Capacitor troubles. A leaky capacitor is equivalent to a partial short. The dielectric gradually loses its insulating properties under the stress of applied voltages. A good capacitor has very high resistance (in megohms). A shorted capacitor shows zero resistance, while a leaky capacitor indicates less than normal resistance.

When you are checking a capacitor with an ohmmeter, be very sure the component is disconnected from the circuit to avoid parallel circuit paths. Discharge the capacitor before checking with the ohmmeter. When you connect the ohmmeter across a capacitor, the ohmmeter pointer should move quickly toward a low resistance reading, and then slowly recede toward infinity (always use the ohms × 1 meg range). Paper, mica, and ceramic capacitors should have an insulation resistance in the 500 MΩ to 1000 MΩ area, which is virtually infinite resistance. Electrolytic capacitors are somewhat lower—in the 0.5 MΩ range.

When you connect the ohmmeter initially, its battery charges the capacitor. Maximum current flows at the first instant of charge, and the meter indicates low resistance. As the capacitor charge slows, less current flows, and the meter indicates more resistance. When the capacitor has charged to the meter potential, the charging current is zero, and the ohmmeter reads only a small leakage current through the dielectric. This capacitor action shows that the capacitor can store a charge and is normal.

Troubles in a capacitor are indicated as follows:

a. When the ohmmeter reading is immediately zero and stays there, the capacitor is shorted.

b. When the capacitor shows a charging action but the final ohmmeter reading is less than normal, the capacitor is leaking. The electrolytic capacitor must be checked by taking a normal reading, then reversing the ohmmeter leads and taking another reading. The higher reading indicates the true condition of the component.

c. If the capacitor shows no charging action and immediately indicates a high resistance, it is open.

However, you should reverse the ohmmeter leads to fully discharge the capacitor, and then take another reading. Also, very small capacitors of 100 pF or less have very little charging action, and you should use a smaller ohmmeter range when you are checking these smaller capacitors.

Inductor troubles. You should make inductor checks with the component disconnected from the circuit if you want to set a true indication. The most common trouble in coils is an open, which is indicated by an infinite reading on the ohmmeter.

Less common troubles are a short between turns (which reduces the inductance), a short between primary and secondary turns in a transformer, and a short to an iron core.

A coil has a DC resistance equal to the resistance of the wire used in the winding. For RF coils with inductance values up to several millihenrys, the 10 to 100 turns in the coil have a DC resistance of 1 to 20 ohms. Inductors for lower frequencies have several hundred turns and a range in resistance from 10 to 500 ohms, depending upon the wire size.

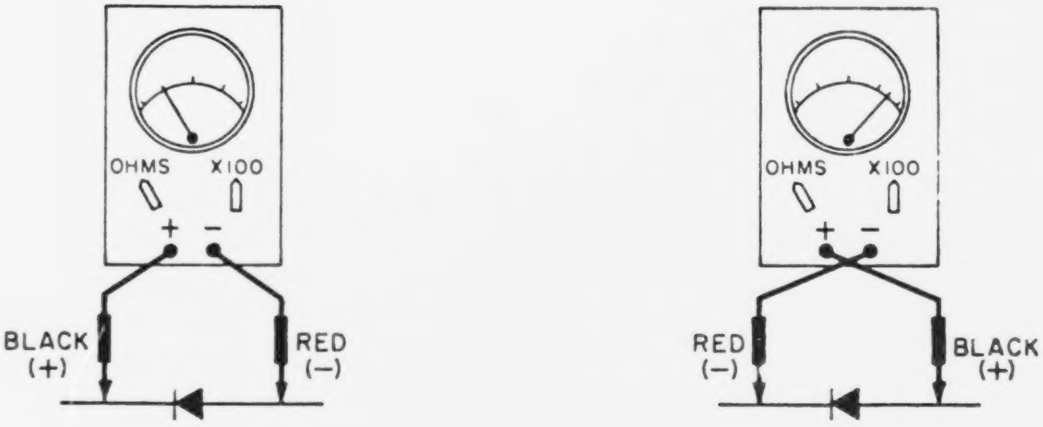
When checking a transformer with four or more leads, check the resistance across the two primary leads, across the two secondary leads, and across any other pairs of leads for additional secondary windings.

For an autotransformer with three leads, check the one lead to each of the other two. When an open is indicated in a coil, you should check the connection from the external terminals to the coil. Often these can be resoldered to make the coil reusable.

Shorted turns cannot be checked definitely with the ohmmeter, because a few shorted turns only slightly reduce the DC resistance. When you suspect shorted turns because of reduced resistance, replace the unit. Excess heat across the short can eventually create an open in the coil.

The resistance between separate windings in a transformer is normally infinite. If the ohmmeter is connected between the primary and secondary windings and reads a low resistance, this indicates a short between the primary and the secondary. Similarly, the resistance between the winding and the core or frame should be infinite. If a low reading is shown between these points, this indicates a short.

Diode troubles. The solid-state diode may be thought of as a resistor that has a high resistance in one direction and a very low resistance in the other direction. As you remember, the end of a diode which current can most



CATHODE ANODE
REVERSE BIAS

CATHODE ANODE
FORWARD BIAS

Figure 5-57. Forward-bias and reverse-bias diode.

easily enter is the cathode, while the end through which current leaves is the anode. A diode may become open or shorted. In either case, the diode is useless. The following discussion covers some of the common procedures for checking a diode.

There are several physical differences in diodes, but even if we know these differences, we may still be unable to discern between a diode and a resistor. One sure way for you to tell the difference is to check with an ohmmeter. A resistor has the same resistance to current in both directions, while a diode shows more resistance to current in one direction than the other. As shown in figure 5-57, a diode exhibits a different resistance when reversing lead positions.

The markings on a diode case often become illegible, and it is impossible for you to tell from visual inspection which lead is the cathode and which is the anode. In a situation such as this, it is possible for you to determine the cathode and anode of a diode by using an ohmmeter. To forward bias a diode, you must place a negative potential on the cathode. Therefore, when you check a diode for its resistance ratio, if you know what lead is negative and which is positive, you can determine which lead is the cathode and which is the anode.

CAUTION: Ohmmeter circuits, which pass a current of more than 1 milliampere through the circuit under test, cannot be used safely in testing diode or transistor circuits. Many ohmmeter circuits exceed this safe value of 1 milliampere. Insure that you are using the test meter and range settings specified by the technical data. When in doubt about current ratings do not use a range setting below R × 100.

Transistor Troubleshooting. A transistor may have two, three, or four leads, depending upon its function. Each lead connects to an element (base, emitter, or collector) inside the transistor. A transistor used as a power amplifier may have only two leads, but the case serves as the third lead. A transistor used for amplifying high frequencies may have four leads.

Identifying transistor types. Before making measurements or replacing a transistor, you must know where each lead is connected in the circuit. You must know how to identify the leads of a replacement transistor so that you can connect it into the circuit properly. You must also know how to identify the leads to a transistor already connected into a circuit before making measurements in the circuit.

One way for you to identify the leads of a transistor is to compare the transistor with reference charts, such as those shown in figure 5-58. Another way for you to identify the leads of a transistor in a circuit is to locate and identify the parts connected to the transistor. This process requires the use of the circuit schematic and the parts layout diagram. For example, to locate the collector lead of a transistor in an oscillator circuit, you need the schematic diagram, the parts layout diagram, and the circuit board on which the transistor is connected (A, B, and C, respectively, fig. 5-59).

First, refer to the schematic and identify a few of the parts connected to the transistor collector. As shown by the schematic in A, some of these parts in the oscillator circuit are capacitors C1401, C1405, and C1406, and coils L1401 and L1402.

Next, locate the transistor and all other parts on the parts layout diagram. Compare the selected parts on the diagram with the parts on the circuit board. Turn the circuit board over so that you are looking at the circuit pattern, and locate the conductor that connects the parts to one of the transistor leads. This is the collector leads (C, fig. 5-59).

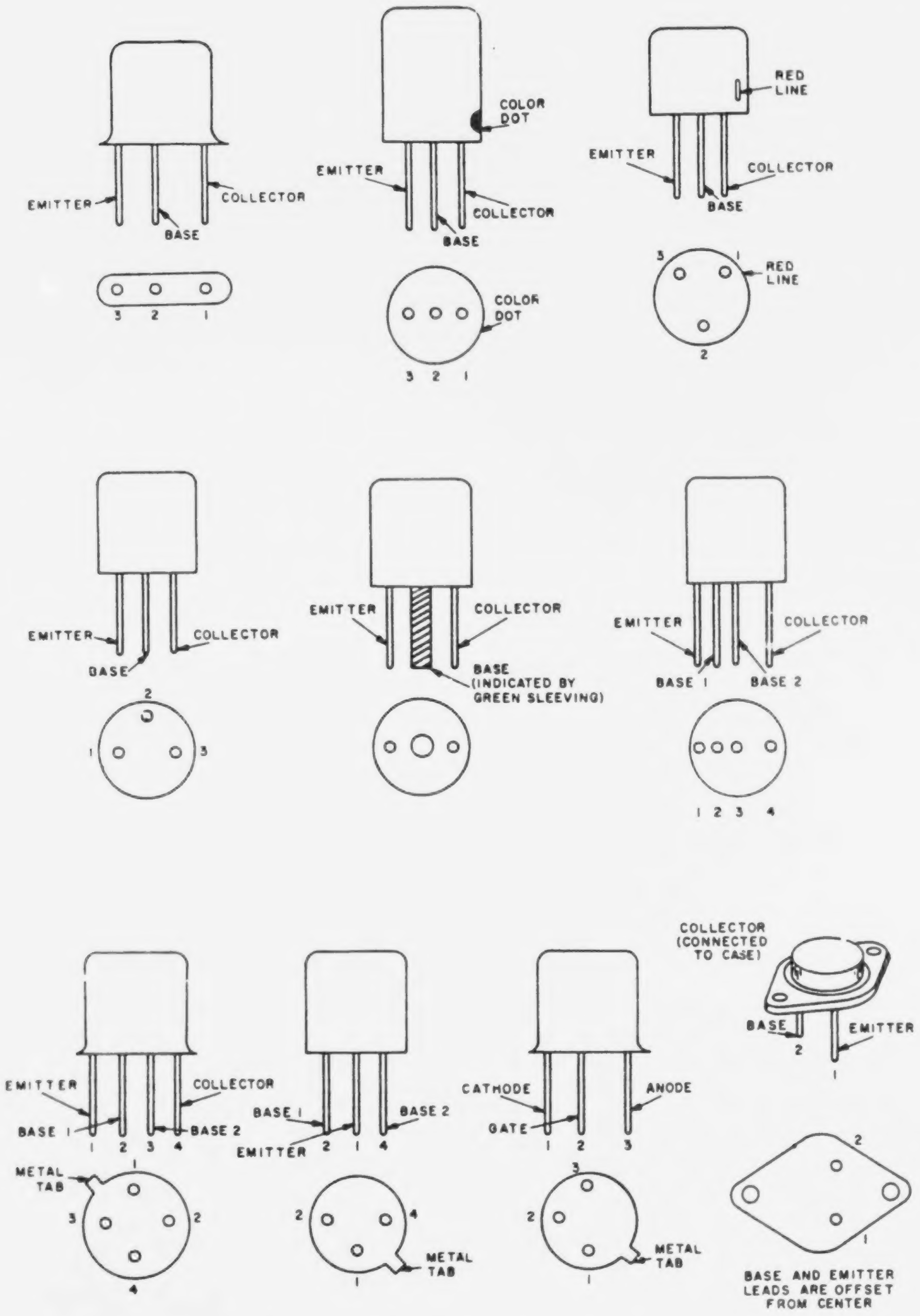

EMITTER
BASE
COLLECTOR
3 2 1
EMITTER
COLOR DOT
BASE
COLLECTOR
COLOR DOT
3 2 1
RED LINE
EMITTER
BASE
COLLECTOR
3
1
RED LINE
2
EMITTER
BASE
COLLECTOR
2
1
3
EMITTER
COLLECTOR
BASE (INDICATED BY GREEN SLEEVING)
EMITTER
COLLECTOR
BASE 1
BASE 2
1 2 3 4
EMITTER
BASE 1
COLLECTOR
BASE 2
1 2 3 4
METAL TAB
1
3
2
4
BASE 1
BASE 2
EMITTER
2 1 4
2
4
1
METAL TAB
CATHODE
ANODE
GATE
1 2 3
3
2
1
METAL TAB
COLLECTOR (CONNECTED TO CASE)
BASE
EMITTER
2
1
2
1
BASE AND EMITTER LEADS ARE OFFSET FROM CENTER

Figure 5-58. Transistor reference chart.

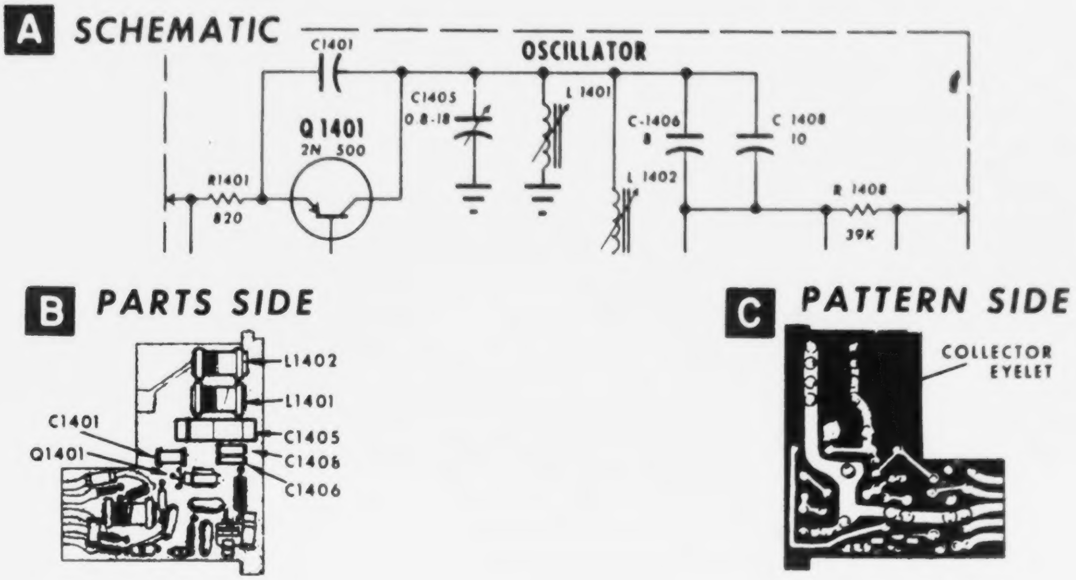


Figure 5-59. Schematic, parts layout, and circuit board.

When looking at the circuit pattern, it may be difficult to determine to which parts the conductors are connected. A helpful technique is to place the board in front of a strong light to get an X-ray view of the parts on the opposite side.

To find the correct troubles in transistor circuits, you must have a definite procedure and you must follow it. Let's look at troubleshooting transistors.

Transistor testing. Transistors may be thought of essentially as two diodes mounted back to back. In this procedure you will use the ohmmeter to check the condition of transistors and determine their type. A transistor may become open or shorted. In either case, it is useless. There are many transistor testers available. However, the multimeter may be used to check the condition of the transistor, and it is probably more frequently used for this purpose. The following discussion will acquaint you with some of the common procedures for checking a transistor.

While you are using an ohmmeter to check the condition of a transistor, it is also possible for you to determine its type (PNP or NPN). Since a transistor is essentially two diodes mounted back to back, to check its condition you must measure the resistance ratio (about 10 to 1) of each junction (E-B and C-B) and then measure the resistance between the emitter and the collector. (NOTE: Be familiar with your multimeter. Know which lead is positive and negative during ohmmeter operation. For example, when using the PSM-6 as an ohmmeter, the meter leads reverse polarity according to the way the internal power source is connected. The red lead becomes the negative lead, and the black lead becomes the positive lead.)

Also, a transistor must be isolated from its related circuit before you can check its type or condition with an ohmmeter. In many cases, this requires the transistor to be desoldered from the circuit. But if the transistor is not removed from the circuit, it is possible for you to obtain an erroneous ohmmeter indication.

NOTE: There must be a ratio (at least 500 to 1) between the two resistance measurements, if the junction under test is to be considered good.

Connections for these tests are shown in figure 5-60. With the positive ohmmeter lead connected to the base of a PNP transistor (figure 5-60,A), a high-resistance reading (50,000 ohms or higher) should be obtained between the base and the emitter, and between the base and the collector. With the negative ohmmeter lead connected to the base of a PNP transistor (figure 5-60,B), the resistance between the base and the emitter should be 500 ohms or less. If you make the same ohmmeter tests on an NPN transistor, the results will be reversed; that is, the high-resistance reading will be obtained with the negative ohmmeter lead connected to the base, and the low-resistance reading with the positive ohmmeter lead connected to the base. If you obtain open or shorted readings from the ohmmeter test, replace the integrated circuit or use another transistor on the array if there is an unused one.

The type of test depicted in figure 5-60 may also be used for determining the type of transistor, PNP or NPN, when its type is unknown. With the test connection as in figure 5-60,A, a high-resistance reading (50,000 ohms or

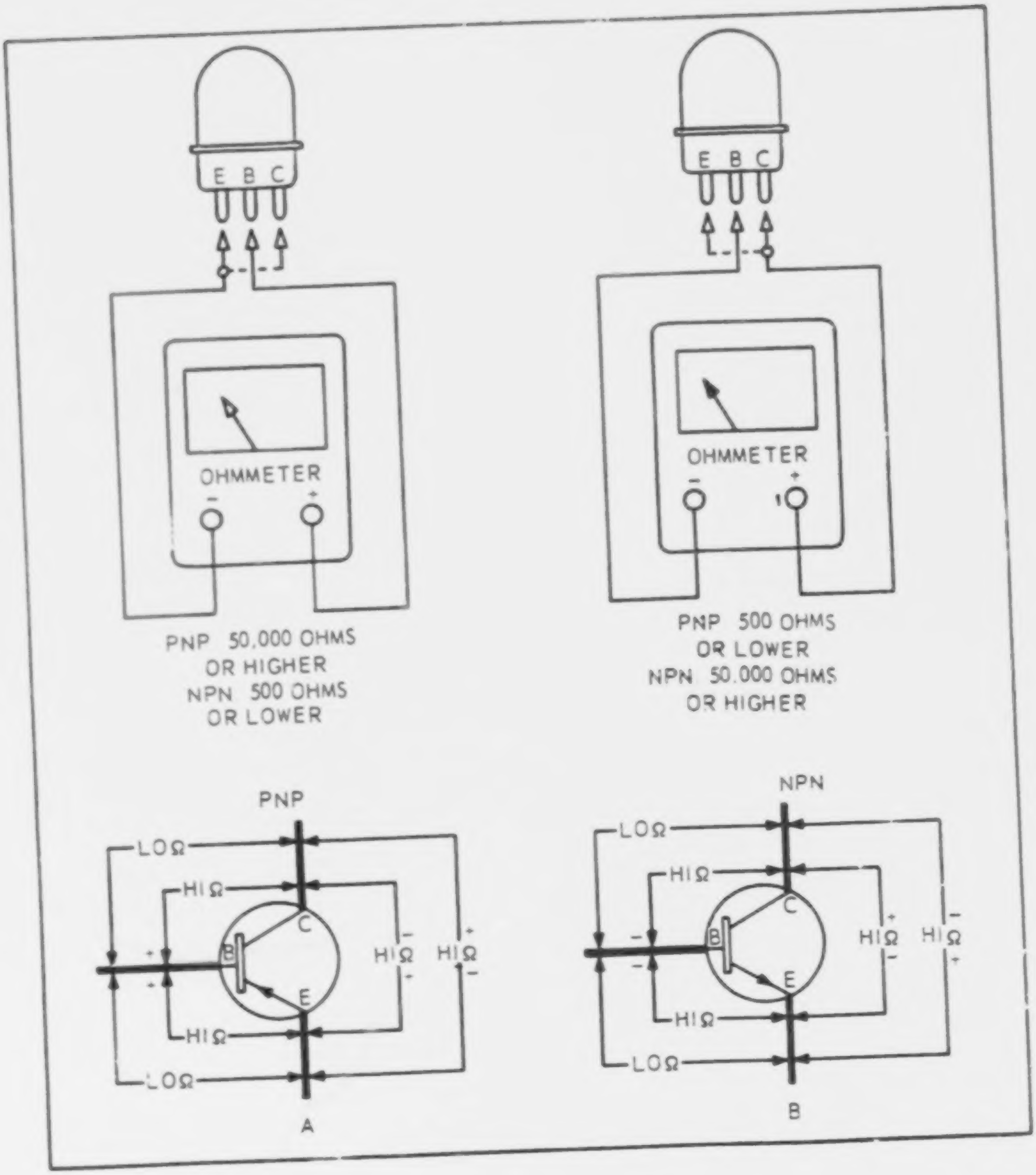

E B C
OHMMETER
PNP 50,000 OHMS OR HIGHER
NPN 500 OHMS OR LOWER
PNP 500 OHMS OR LOWER
NPN 50,000 OHMS OR HIGHER
PNP
NPN
LO Ω
HI Ω
B
C
E
A
B

Figure 5-60. Transistor resistance testing.

higher) shows that it is a PNP type; a low-resistance reading (500 ohms or less) shows that it is a NPN type. Make a check between emitter and collector in both directions by reversing leads of the ohmmeter. These should be high-resistance values (generally 50,000 ohms or higher). Power transistors may have a low resistance between emitter and collector, but not less than the lowest previously measured value. This check will eliminate the possibility of a short/open between emitter and collector.

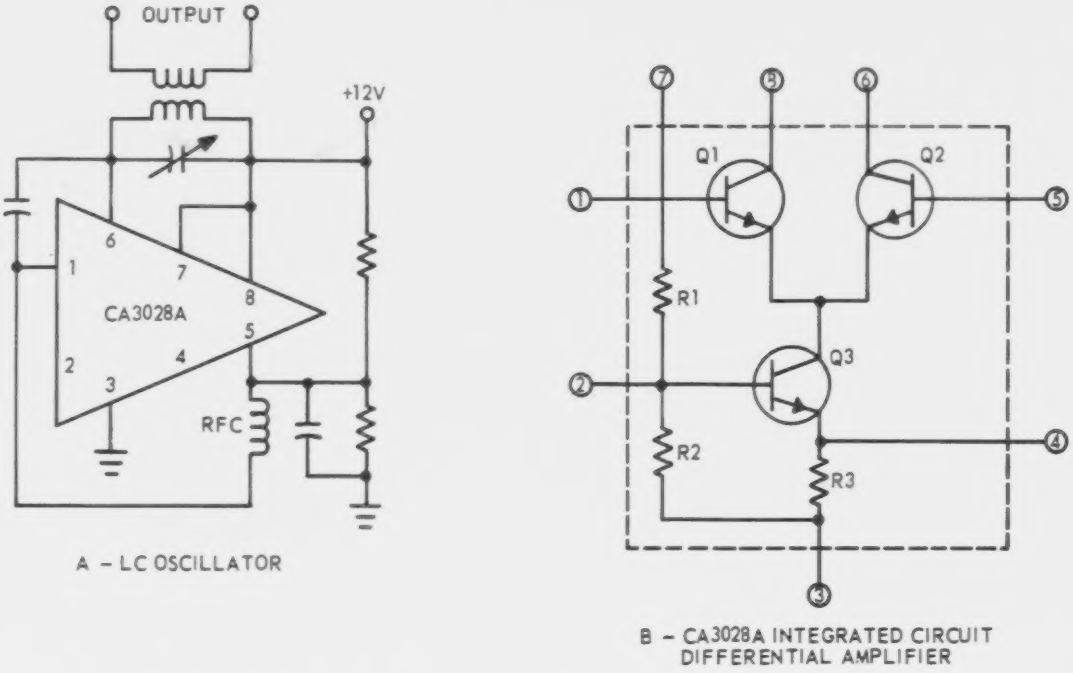
Integrated Circuit Testing. Troubleshooting and maintenance of ICs are based on a throwaway policy. When an IC is defective, it is thrown away. The only problem that you may face is determining which IC is bad. In some cases, the equipment itself automatically pinpoints the defective IC for you. But if you don't have such sophisticated equipment, you must troubleshoot the circuit.

Troubleshooting circuits having integrated circuits is more involved than for those systems which do not have ICs. Simple discrete solid-state devices, such as diodes, transistors, and field-effect transistors permit direct access to each terminal lead. A given circuit will then be readily identifiable, permitting the maintenance person to perform all troubleshooting required to isolate a defect to an individual component.

The testing of integrated circuits is made more difficult because of the large number of active and passive components that are present in these highly compact units. You can expect that the methods used for testing ICs will differ considerably from those used in testing discrete components.

An IC which is not installed in a circuit may be checked with an IC tester. The IC tester applies voltages and signals to selected terminals to make it act as a given circuit. The outputs of this circuit are expected to obtain given standards. For testing in this manner, integrated circuits are divided into three groupings. They are linear ICs, nonlinear ICs, and uncommitted transistor (array) ICs. Each of these groups has established procedures, as applicable, for static and/or dynamic tests. This works well for an IC out of circuit. However, in your equipment using an IC tester to check the IC in circuit may not be possible and often integrated circuit stages are not readily identifiable. In the schematic shown in figure 5-61,A, it is not obvious that this is an LC-type oscillator. Even when the circuit has been identified, it is still not possible for you to perform troubleshooting analysis upon it. One possibility in troubleshooting, however, is to test the integrated circuit on an IC tester. If it is good, the trouble will be indicated as being in the discrete components. But suppose that it has tested bad? The obvious thing to do is to replace it with a new one. So if there is no IC tester available, a maintenance procedure would be to replace the suspected bad IC with a new one. In either case, a new IC would be in the circuit. If the oscillator now produces the normal output, the defect has been eliminated. But, suppose that the trouble is not in the IC but in one of the discrete components. It is possible that the external problem could destroy the new IC, and you, as the maintenance person, would still not have located the defect. Deductive reasoning in either case should lead you to believe the trouble to be in the IC and not in the discrete component.

The only way that you can perform detailed circuit analysis of a circuit using integrated circuits is to know



A – LC OSCILLATOR

B – CA3028A INTEGRATED CIRCUIT DIFFERENTIAL AMPLIFIER

Figure 5-61. LC oscillator using CA3028A IC.

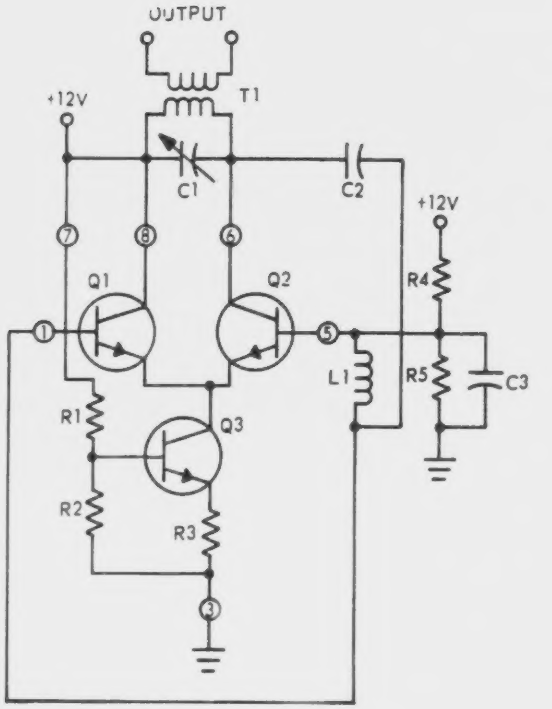


Figure 5-62. Butler LC oscillator.

exactly what circuitry is inside the IC package (fig. 5-61,B). You can get this information from your technical manual or an IC data book. With this knowledge, your troubleshooting techniques become basically the same as those used when all discrete components are used. However, you should observe certain precautions when testing integrated circuits. Basically, the IC is a small, delicate, low-power device that can be easily destroyed if improper parameters are applied to it. Any of the following can ruin a perfectly good IC:

- Overvoltages—from too large a power source.
- Transients—noise spikes.
- Ohmmeter—internal power source giving overvoltages.
- Heat-soldering in or out of a circuit.

The only difference here is that in multistage ICs all connections cannot be reached. Careful planning will permit most necessary checks to be made. Having all information in figure 5-61 available will produce the circuit in figure 5-62, which is little different from an LC oscillator built entirely from discrete components.

Exercises (476):

1. When you check a capacitor with an ohmmeter, what procedure should you follow?

2. Match each condition of a component in column B with the given ohmmeter indication in column A.

NOTE: Each item in column B may be used only once.

Column A

____ (1) An ohmmeter across the windings shows a slight decrease in DC resistance.
____ (2) The ohmmeter immediately shows low resistance, then gradually recedes to infinity.
____ (3) The ohmmeter shows infinity across the coils.
____ (4) The ohmmeter indicates infinity across the capacitor both ways.
____ (5) The ohmmeter shows low resistance between primary and secondary windings.
____ (6) The ohmmeter shows low resistance across the capacitor.

Column B

a. Open coil.
b. Open capacitor.
c. Shorted windings.
d. Shorted primary and secondary.
e. Leaky capacitor.
f. Normal capacitor.

3. When a diode is forward-biased, what potential is placed on the cathode and on the anode?

4. What are some of the ways you can identify the leads of a transistor?

5. What procedure can help you determine the parts to which the conductors are connected?

6. With the red lead on the base and the black lead on the emitter of an NPN transistor, the PSM-6 reads infinity. Explain briefly whether this is a good or a bad indication and why.

7. When checking diodes with a PSM-6, the red lead is ________ and the black lead is ________ .

8. When using a PSM-6 to check a diode, you should never use a range setting below ohms times 100. True or false?

10. What three groups are integrated circuits divided into for testing purposes?

11. Suppose you have identified the circuit (an LC-type circuit) in figure 5-60,A. What troubleshooting procedure would you use if you had no IC tester to locate the problem?

12. Give four ways in which a perfectly good IC can be ruined.

477. Supply details of the correct procedure for removing and replacing components on printed circuit boards.

Component Removal and Replacement. It is always desirable for you to replace parts on a printed circuit board without applying heat directly to the conducting strip. Why? Because this procedure prevents damage to the printed circuit conductors, feed-through devices, eyelets, or terminals, and saves time in repair. It also prevents damage to semiconductors and other heat-sensitive parts that may be in proximity to the part being repaired.

Replacing parts requires that you consider each type of part mounting individually to determine the best method of removing it.

For example, a part to be removed may be too close to a heat-sensitive semiconductor or another part to allow you to apply the hot pencil soldering iron. A quick test to determine this safe distance is to place your finger between the semiconductor (or heat-sensitive part) and the part to be removed. Then place the hot soldering iron in the position to be used. If the heat is too great for your finger, it is too hot for the semiconductor. After determining that the heat-sensitive part is too close, place a shield (asbestos or like substance) between the parts before applying the hot soldering iron and place heat sink clamps on all leads from the heat-sensitive part. Solid-state parts and their associated circuitry are extremely sensitive to thermal changes. Therefore, you must be particularly careful to prevent exposing them to heat. Heat sinks and shunts must be applied with shields inserted to protect the associated parts any time repair or removal of a part requires the use of a hot soldering iron. Solid-state parts and associated assemblies require the same care in handling and skill in repairing that are applied to assemblies in equipment of unitized or modular construction containing transistors, capacitors, crystals, etc.

Axial-lead parts. You can remove an axial-lead part that has been bonded to a printed circuit board (with an epoxy resin or similar compound) by breaking the defective part or by applying heat to the bonding compound. The method to be used depends upon the part itself and its location.

If the defective axial-lead part cannot be removed by heat, cut or break the part away from the bonding compound. Figure 5-63 illustrates different methods of breaking the part away from the bonding compound where the part is too close to other parts to use cutting pliers. In some instances, the part to be replaced is so closely positioned between other parts that one lead must be cut close to the body of the defective part to permit application of the prying tool. Wherever possible, cutting the defective part with end-cutting pliers or diagonals, as shown in figure 5-63,C, is the preferred method to use.

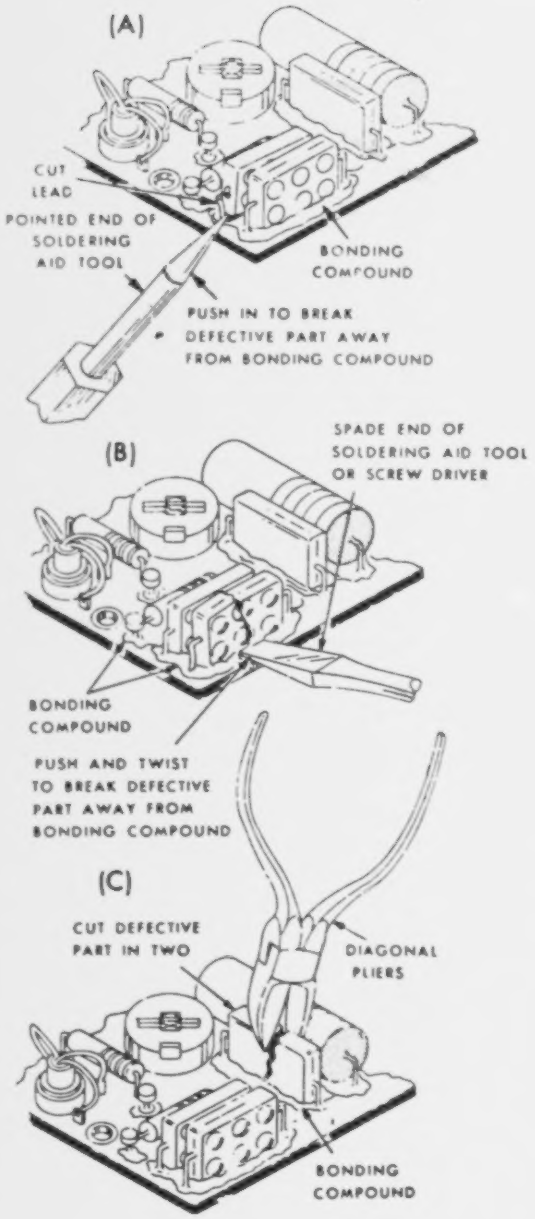

(A)
CUT LEAD
POINTED END OF SOLDERING AID TOOL
BONDING COMPOUND
PUSH IN TO BREAK DEFECTIVE PART AWAY FROM BONDING COMPOUND
(B)
SPADE END OF SOLDERING AID TOOL OR SCREW DRIVER
BONDING COMPOUND
PUSH AND TWIST TO BREAK DEFECTIVE PART AWAY FROM BONDING COMPOUND
(C)
CUT DEFECTIVE PART IN TWO
DIAGONAL PLIERS
BONDING COMPOUND

Figure 5-63. Removing defective part from bonding compound.

Regardless of which tool you employ (round, pointed, or spade type), use it carefully to prevent damage or breakage to the printed board or other parts. Apply the point of the tool against the bonding compound between the part and the printed circuit board. Use the tool in such a manner that it works away the bonding compound from the part to be broken away until enough has been removed for the tool to exert pressure against the part. Keep the leverage surface area of the tool flat against the surface of the printed circuit board; this helps to keep the tool from gouging or breaking the board. (CAUTION: Never apply much pressure against a printed circuit board.)

After you have removed the defective part from the bonding compound, remove the leads or tabs from their terminals on the printed circuit board. Clean the area thoroughly before installing the new part. Do not remove the compound left on the board under the removed part unless its condition requires it. Why? Because the mold left in the compound should be of the same kind as the part; thus, inserting the new part into the mold helps to secure it from vibration. After you have finished the repairs and tested the circuit, spray the newly soldered area with an insulating varnish or equivalent. Coat the new part or parts with a bonding compound.

Transistors. To replace a proven defective transistor, first cut all of its leads and then remove it from the assembly. Transistors are mounted on circuit boards in many different ways; thus, it is necessary for you to study how a particular transistor is secured before attempting to remove it. For example, to remove a transistor with a clamp-type mounting, you need only a pointed tool between the clamp and the transistor. However, a transistor mounted in a socket may have a wire or spring clamp around it. If so, remove this clamp before pulling the transistor out of the socket. In some instances you will find the transistor bolted through the board. Here, remove the nut and washer and then remove the transistor. Where vibration is a prime factor, the manufacturer mounts the transistor through the circuit board and bonds it. For this type, you need a flat-ended, round-rod type tool (drift punch) of a diameter less than that of the transistor case. Be sure that the printed circuit board on which the transistor is mounted is secured in a proper device and in such a way that pressure exerted against the board is relieved by a proper support on the other side (fig. 5-64). Apply a hot pencil soldering iron to the bonding compound while simultaneously applying the drift punch against the top of the transistor. Exert enough pressure to remove the transistor from the softened compound, and then go on through and out the other side of the board (fig. 5-64).

Before installing the new transistor, prepare it carefully for installation. Also, test it in a transistor tester. This precaution will assure you that the transistor is good before you install it. For several reasons transistors can and do become defective in storage. Therefore, always check them before installation. Preshape and cut the new transistor leads to the shape and length required for easy replacement. Use sharp cutters and do not place undue stress on any lead entering the transistor. The reason for this is that the leads are fragile and can be damaged by excessive bending or by too sharp a bend. So shape the bend into a gradual curve, and make the bend at least 1/4 inch to 3/8 inch from the base of the transistor. A safety measure that you can take to insure that the lead will not break off at the base is to use two pairs of needle-nose

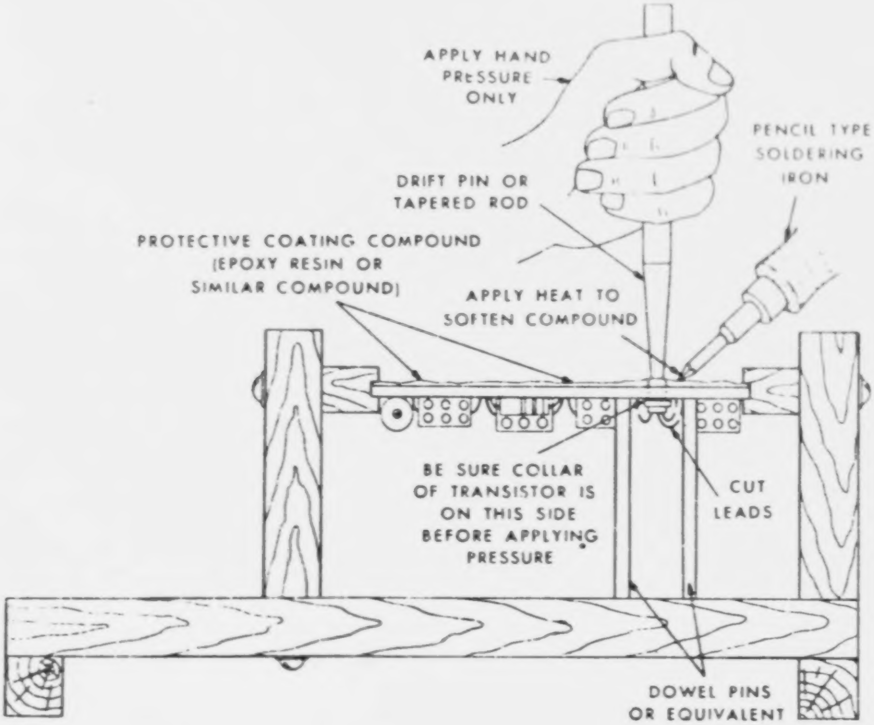

APPLY HAND PRESSURE ONLY
PENCIL TYPE SOLDERING IRON
DRIFT PIN OR TAPERED ROD
PROTECTIVE COATING COMPOUND (EPOXY RESIN OR SIMILAR COMPOUND)
APPLY HEAT TO SOFTEN COMPOUND
BE SURE COLLAR OF TRANSISTOR IS ON THIS SIDE BEFORE APPLYING PRESSURE
CUT LEADS
DOWEL PINS OR EQUIVALENT

Figure 5-64. Removing a transistor that has been through-board mounted.

pliers. With one pair grasp the lead close to the transistor base while shaping the rest of the lead with the other pair.

NOTE: Apply the above procedure and precaution to any and all semiconductors, capacitors, and other miniaturized parts in equipment of modular or unitized construction.

After removing the remaining pieces of the defective transistor terminal leads and cleaning and preparing the terminals on the board, connect the new transistor to its proper terminals.

REMEMBER: Handle any semiconductor or miniaturized part carefully; be gentle and be precise.

When the defective transistor is to be removed from a bonded through-board mounting, be sure that the new transistor clears the hold before you connect it to its terminals. If the hole is too large, shim it with a thin plastic sleeve. If the hole is too small, ream it to accept the new transistor. Rebond the fitted transistor after testing the repaired circuit and proving it to be operative. (CAUTION: Do not use heat to rebond replaced semiconductors.)

Multilug parts. To remove and replace a multilug part—such as a transformer, choke, filter, or other similar potted, canned, or molded part—release the part from its mounting before disconnecting or cutting its conductors. Before applying pressure to remove such a part, inspect it carefully to be sure that the part is completely free of all of its connections to the printed circuit board and that all bent or twisted mounting lugs have been straightened; otherwise, you may break the board.

Never wrench or twist a multilug part to free it. Why? Because this will cause the conducting strip to become unbonded from the board. Work this type of part in and out in line with its lugs while applying a hot pencil soldering iron (fig. 5-65,A) and using a bar-type triplet adapter or similar desoldering tool.

Whenever possible, cut the conducting or mounting leads and lugs of the defective multilug part on the mounting side of the board (fig. 5-65,B). Heat and straighten the clipped leads with a hot pencil soldering iron and a slotted soldering aid tool applied to the circuit side of the board; pull the leads or tabs through with pliers, as shown in figure 5-65,C.

To replace the new multilug part, make sure that all of the lead holes or slots are free and clean, allowing easy insertion of the multilug part. Do not force any part into position on a printed circuit board, because the board might break or the printed circuit strip and eyelet terminal lift. If the part does not position easily, check and rework the terminals and holes until it does seat freely; then proceed to solder.

Be very careful when replacing defective parts that have leads terminating on standoffs, feed-through terminals, etc. In most instances standoffs and feed-through terminals are very small and mounted on a thin phenolic board; thus, they are vulnerable to damage by heat and undue pressure.

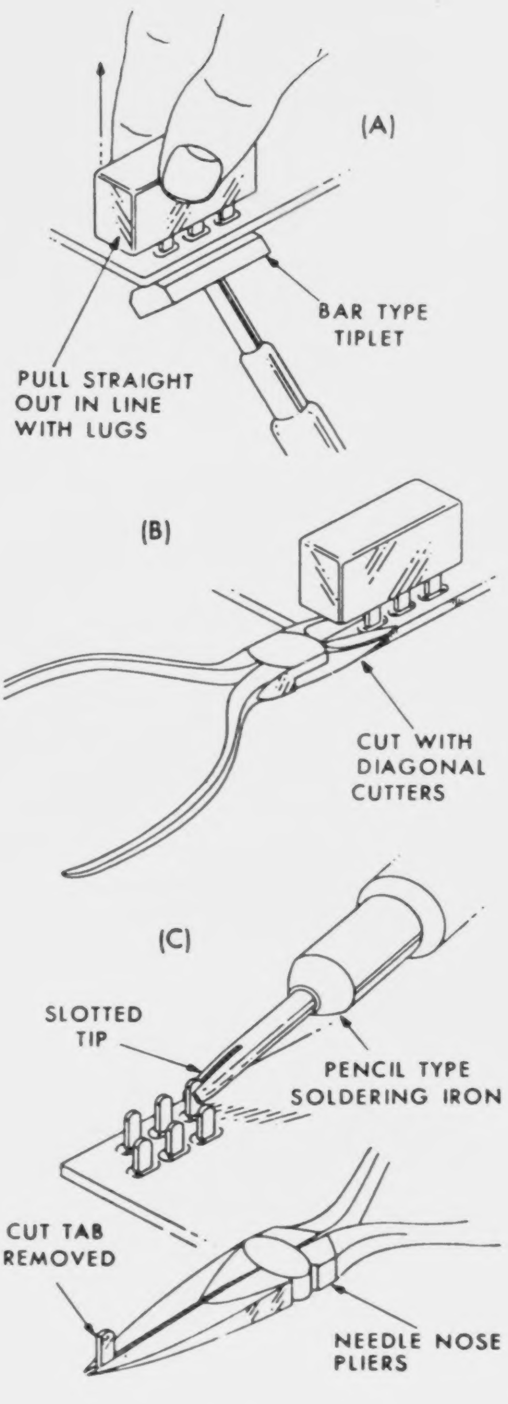

(A)
BAR TYPE TIPLET
PULL STRAIGHT OUT IN LINE WITH LUGS
(B)
CUT WITH DIAGONAL CUTTERS
(C)
SLOTTED TIP
PENCIL TYPE SOLDERING IRON
CUT TAB REMOVED
NEEDLE NOSE PLIERS

Figure 5-65. Removing a defective multilug part.

Exercises (477):

1. Why is it desirable not to apply heat directly to a conducting strip?

2. What method can you use to test to see if a heat-sensitive part is too close to the connection?

3. What is the purpose of a heat sink?

4. What are the two methods of removing bonded parts?

5. If the part is inaccessible, what method is preferred to remove it?

6. When breaking the bonding, how should you use the prying tool?

7. Why should the old compound be left under the removed part?

8. What method is used to remove a transistor that has been mounted through the board and bonded?

9. What is the first step you should take before installing a transistor?

10. What safety measure can you take when bending transistor leads?

11. If the new transistor does not fit into the hole, what should you do?

12. Before applying pressure to remove a multilug part, what should you look for?

13. Space permitting, what is the best method for removing multilug parts?

14. Why should you be careful when replacing defective parts that have leads terminating on standoffs?

CHAPTER 6

Power Supplies

THE POWER SUPPLY is an electronic unit used to convert one form of electrical power. A power supply can be constructed to convert AC power to DC power or a small DC to a large DC. The amount of power produced by the power supply must meet the load requirements of the circuit it serves.

6-1. Theory and Operation of Power Supplies

Alternating current source power supplies are by far the largest class of power supplies used to operate electronic equipment; and, within this class, the majority of power supplies operate from a power line frequency of 60 Hz. Further subdivisions can be made by considering the number of phases involved; single-phase power supplies comprise a larger class than the three-phase power supplies.

478. Name the parts of a power supply and state their purposes.

Power Supply. Figure 6-1 is a block diagram of a power supply. The blocks represent the individual circuits within the power supply, and the arrows show the path the current takes through the circuits. The input voltage is applied to the transformer, which is capable of stepping up or stepping down the voltage to the required level for the circuit being supplied. The amount of voltage from the transformer is determined by the voltage input to it and the type transformer being used. Thus, the transformer in a power supply is used to provide the correct amplitude of voltage needed for the particular circuit being used. The voltage output from the transformer is then applied to a rectifier.

The purpose of the rectifier is to change the AC voltage to DC voltage. The DC output fom the rectifier is constantly changing in amplitude, being in the form of pulses; this output voltage is referred to as a pulsating DC voltage. The pulsating DC cannot be applied to the amplifiers and obtain satisfactory operation. This output voltage must be changed to a constant amplitude DC. This is done by the next circuit in the block diagram, the filter. However, even the output from the filter can change, due to changes in input voltage or in the amount of current drawn from the power supply. To compensate for these variations, we use a voltage regulator to maintain or regulate the output voltage to the critical level needed. We will discuss methods of regulating this voltage later in this chapter. The last circuit in the power supply is the voltage divider. Its function is to provide the output voltages which are required for the amplifier's bias and collector supply voltage.

Exercises (478):

1. What are the basic parts of a power supply?

2. What is the purpose of the transformer?

3. What is the purpose of the rectifier?

4. What is used to insure that the output is a constant amplitude DC?

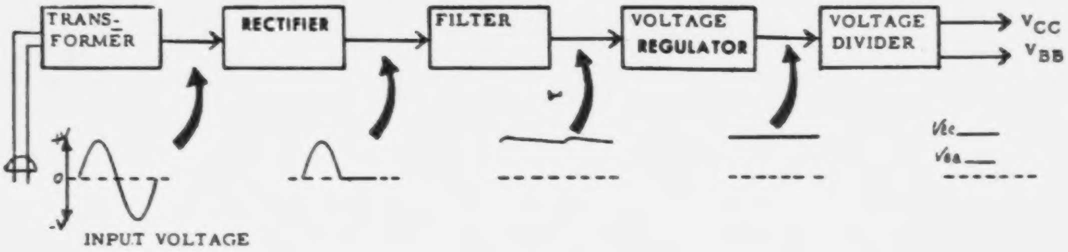


Figure 6-1. AC to DC power supply block diagrams.

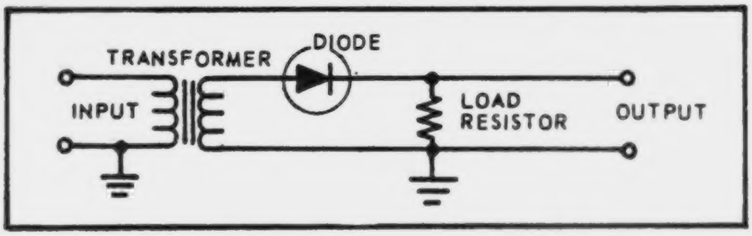


Figure 6-2. Simple half-wave rectifier.

5. Why is a voltage regulator used?

6. What is the purpose of a voltage divider?

479. Associate various operational characteristics with their appropriate types of rectifiers.

Rectifier. You probably have replaced the battery in a transistor radio at some time. The battery provides a DC voltage to the transistors so that they will operate properly. What about a transistor radio that gets its power from the 120-volt AC wall socket? Where does the required DC voltage come from?

By definition, a rectifier is a device which changes AC to DC. It does this by permitting current to flow more easily in one direction than it does in the other. An ideal rectifier is one that offers 0 impedance to the flow of current in one direction and an infinite impedance to the flow of current in the opposite direction.

Once the alternating current has been rectified, a low-pass filter can be used to create a relatively smooth DC voltage. This chapter deals with rectifiers and filters that are used to produce DC voltages. The rectifying device is the PN junction diode.

Half-wave rectifier. You have studied the structure of a PN junction diode. You have learned how the application of reverse bias increases the depletion region and reduces the current flow through a diode. You have also learned that forward bias decreases the width of the depletion region and allows a large amount of current to flow through the diode. A diode placed in series with a source of AC power and a load resistor has reverse bias and forward bias applied with every cycle. Thus, since current flows more easily in one direction than the other, rectification is accomplished.

Figure 6-2 shows a simple rectifier circuit with a diode, a source of AC power, and a load resistor. The transformer provides the AC input to the circuit; the diode provides the rectification; and the load resistor serves two purposes: (1) It limits the amount of current flow in the circuit to a safe level, and (2) it develops an output signal due to the current flow through it.

In this field "load" is defined as any device that draws current. A device that draws little current is a "light" load, and a device that draws a large amount of current is a "heavy" load. Remember, though, that when we speak of "load," we are talking about the device that draws current from the power source.

Assume the polarity shown in figure 6-3, with the top of the transformer positive with respect to ground. With this polarity, the diode is forward biased, the depletion region is narrow, the resistance of the diode is low, and current flows through the circuit in the direction of the arrows. Current flow through the load resistor develops the voltage drop, shown as the positive half of the AC input signal.

When the AC input goes in a negative direction, as shown in figure 6-4, the top of the transformer becomes negative (with respect to ground) and the diode becomes

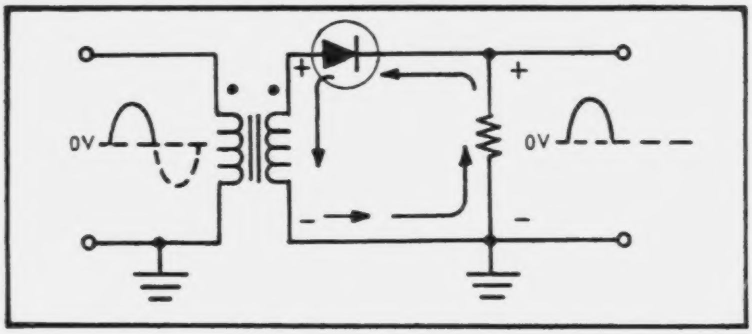


Figure 6-3. Half-wave rectifier, positive polarity, forward-biased diode, positive output.

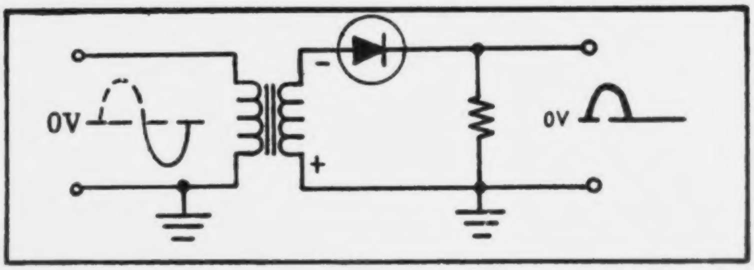


Figure 6-4. Half-wave rectifier, negative polarity, reverse-biased diode, zero output.

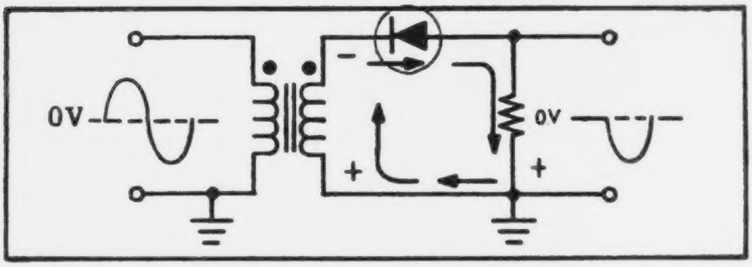


Figure 6-5. Half-wave rectifier, diode reversed, negative output.

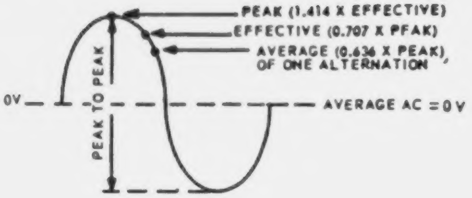

PEAK (1.414 X EFFECTIVE)
EFFECTIVE (0.707 X PFAK)
AVERAGE (0.636 X PEAK), OF ONE ALTERNATION
0V
PEAK TO PEAK
AVERAGE AC = 0 V

Figure 6-6. Sine wave.

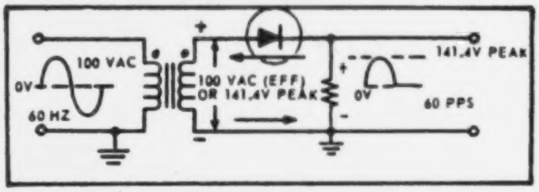

100 VAC
0V
60 HZ
+
100 VAC (EFF) OR 141.4V PEAK
−
141.4V PEAK
+
0V
60 PPS
−

Figure 6-7. Half-wave rectifier.

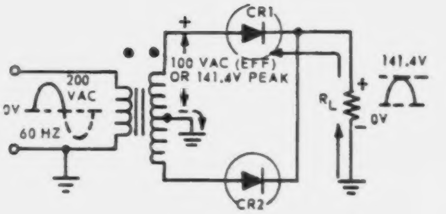

200 VAC
0V
60 HZ
+
100 VAC (EFF) OR 141.4V PEAK
CR1
CR2
R_L
+
141.4V
0V

Figure 6-8. Full-wave rectifier (positive half cycle).

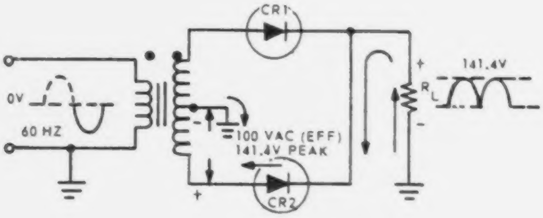

0V
60 HZ
CR1
−
100 VAC (EFF) 141.4V PEAK
+
CR2
+
R_L
−
141.4V

Figure 6-9. Full-wave rectifier (negative half cycle).

reverse biased. With reverse bias applied to the diode, the depletion region increases, the resistance of the diode is high, and minimum current flows through the diode. For all practical purposes, there is no output developed across the load resistor during the negative alternation of the input signal. This circuit is a half-wave rectifier because current flows during half of the input wave. If the diode is reversed, as shown in figure 6-5, a negative output voltage can be obtained.

Now that you have seen how current flows and how an output is developed in the half-wave rectifier, you can determine the peak output voltage, inverse peak voltage, and the average output voltage when you are given the effective voltage developed by the secondary of the input transformer.

For a short review, refer to figure 6-6. Each alternation of the AC sine wave has peak, effective, and average values. If the effective voltage of the waveshape is 100 volts, the peak value can be determined by multiplying 100V × 1.414. The average voltage of one alternation can be determined by multiplying 141.4V × .636. If the peak value is given, the effective voltage can be determined by multiplying by .707:

Peak voltage = 100V (effective) × 1.414 = 141.4 volts
Average voltage = 141.4V(peak) × .636 = 90 volts
Effective voltage = 141.4V(peak) × .707 = 100 volts

Now let's analyze the voltage values of the half-wave rectifier shown in figure 6-7. With the voltage applied, the output developed across the load resistor is as shown. (NOTE: Disregard the voltage drop across the diode. The peak voltage in the output is equal to the peak voltage applied to the diode. The peak output is 141.4 volts (100V effective × 1.414).)

On the negative alternation, the diode is reverse-biased and does not conduct. During the negative alternation, the peak inverse voltage (PIV) across the diode is equal to the peak voltage across the secondary of the transformer, or 141.4 volts. As you will recall, a diode can stand only so much voltage in the reverse direction before it will break down. So by knowing the value of the peak inverse voltage, you can select a diode that has a breakdown rating which exceeds this value.

The average output voltage during one half cycle is .636 times the peak value. With 0 volts output during the second half cycle, the average output voltage becomes only one-half of the average for one alternation. The average output voltage from this circuit is:

$$\frac{414.4\text{V} \times .636}{2}$$

or 45 volts.

The last item of concern to you with regard to the half-wave rectifier is the output ripple frequency. That is, how many pulses or periodic fluctuations take place in 1 second. As you can see by the output signal provided in figure 6-7, the output ripple frequency will be equal to the frequency of the applied AC signal, because you get one pulse output for each cycle of the input. Therefore, if the input frequency is 60 hertz, the output ripple frequency is 60 pulses per second (pps).

Full-wave rectifier. A full-wave rectifier permits current to flow in the same direction through the load during both alternations of an AC input. Looking at the schematic of a full-wave rectifier supplied in figure 6-8, you can see that it is two half-wave rectifiers combined into one circuit.

The identifying features of a full-wave rectifier are two diodes (CR1 and CR2), a center-tapped transformer, and a load resistor (R_L). To understand how the full-wave rectifier operates, refer to figure 6-8. The polarity shown on the transformer applies forward bias to CR1, and current will flow from the center tap through the load resistor, through CR1, and back to the transformer. The output voltage is developed across R_L.

When the input voltage changes direction, the transformer will have the polarity shown in figure 6-9. This applies forward bias to CR2, and current will flow in the direction shown by the arrows. The output voltage is again developed across R_L.

Note that when one diode is forward-biased, the other is reverse-biased. Therefore, current will flow through the load resistor in the same direction on each alternation. The output is a series of one-polarity pulses. By reversing both diodes, the output polarity can be changed. Therefore, a positive or negative voltage may be obtained from the circuit.

In the half-wave rectifier, the ripple frequency is equal to the input frequency. In the full-wave rectifier, you get a pulse in the output for each alternation of the input; therefore, the ripple frequency in the full-wave rectifier is twice the input frequency.

What is the ripple frequency of a full-wave rectifier if the input frequency is 60 hertz?

Ripple frequency = 2 × input frequency
= 2 × 60
= 120 pulses per second

Now, find peak inverse voltage of the circuit shown in figure 6-8. When the CR1 is forward-biased, CR2 is reverse-biased. Consider that the conducting diode CR1 has no voltage drop across it. (Remember that some voltage is dropped across a conducting diode; (still, this result is so small in comparison to the voltage dropped across the load resistor that you can ignore it.) Since CR1 drops no voltage, and since each half of the center-tapped transformer has 141 volts, CR2 has a total of 282 volts across it in the reverse direction. Figure 6-9 shows CR2 conducting and CR1 reverse-biased. Now, CR1 has 282 volts across it in the reverse direction. This means that in a full-wave rectifier, each diode must withstand an inverse voltage twice the value of the output peak voltage.

If a full-wave rectifier has an output peak voltage of 75 volts, what is the inverse peak voltage of the circuit?

Inverse peak voltage = output peak voltage × 2
= 75 × 2
= 150 volts

The diodes used in the full-wave rectifier must have a breakdown rating twice as great as that of the half-wave diode. For example, to get 120 volts peak output from a half-wave rectifier, the diode must have a breakdown

708

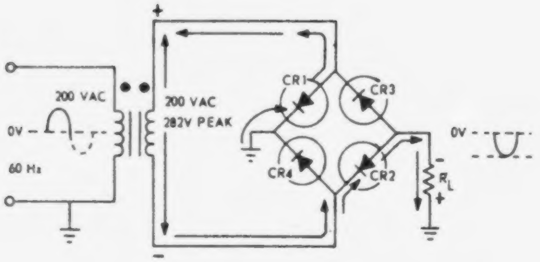


Figure 6-10. Bridge rectifier (positive half cycle).

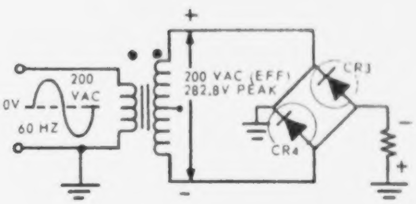


Figure 6-12. Bridge rectifier PIV.

rating of 120 volts or more. To get 120 volts peak output from a full-wave rectifier, the diodes must have a breakdown rating of 240 volts or more. Half-wave: Peak inverse voltage = peak output voltage. Full-wave: Peak inverse voltage = 2 × peak output voltage.

The last voltage solved for here is average output voltage. For every alternation that is applied to the full-wave rectifier, there is a pulse developed in the output. To find the average voltage for one alternation of a sine wave, use average voltage = peak voltage × .636. Since the second alternation of the input sine wave is also used to produce the output, the formula for a complete cycle is the same:

$$\text{Average voltage} = \text{peak voltage} \times .636$$

What is the average voltage output from a full-wave rectifier if the peak output is 141 volts?

$$\begin{aligned} \text{Average voltage} &= \text{peak voltage} \times .636 \\ &= 141 \times .636 \\ &= 90 \text{ volts} \end{aligned}$$

Observe that, with the same peak output, the average output voltage from a half-wave rectifier is only half as much as that from the full-wave rectifier. The fact that a full-wave rectifier has twice the average output voltage for the same peak output voltage is an advantage that will be retained in the bridge rectifier.

Bridge rectifier. The bridge rectifier is a modification of the full-wave rectifier. However, the bridge rectifier does not require a center-tapped transformer, although it does require two additional diodes.

To understand how the bridge rectifier operates, refer to figure 6-10. With the transformer polarity as shown, CR1 and CR2 will be forward-biased, and current will flow from the bottom of the transformer, through CR2, R_L, and CR1, and back to the top of the transformer. The rectified output is developed across R_L, and the polarity, in this case, is negative.

When the input voltage changes direction, the transformer will have the polarity shown in figure 6-11. Now CR3 and CR4 are forward-biased. Therefore, current will flow in the direction shown by the arrows, and the output is another negative pulse, developed across the load resistor.

The bridge rectifier is a full-wave device, because current flows through the load resistor during both alternations of the input signal. Therefore, the output ripple frequency will be two times the input frequency or 120 pulses per second with a 60-hertz input.

To illustrate peak inverse voltage, refer to figure 6-12. When CR1 and CR2 are conducting, they have a low resistance and can be considered shorts. Therefore, CR3 and CR4 are effectively connected across the secondary of the transformer, and the PIV is equal to the peak of the secondary or equal to the peak of the output voltage.

The last voltage of concern to you here is the average output voltage. Refer to figure 6-13. For every alternation that is applied to the bridge rectifier, there is a pulse developed in the output. Since both alternations of the input sine wave are being used, the average output voltage is equal to peak voltage × .636, or in this case, 180 volts.

For a summary of the three rectifiers, refer to figure 6-14. Notice that the peak output from each circuit is the peak voltage applied to a single diode.

Because a center-tapped transformer is required for the full-wave rectifier, the total number of turns in the secondary have been doubled. Nevertheless, the voltage applied to each diode is the same as the half-wave. This will provide the same peak output from the full-wave rectifier as from the half-wave rectifier. Also, the peak output voltage from the bridge is twice that of the full-wave, since it does not have a center-tapped transformer.

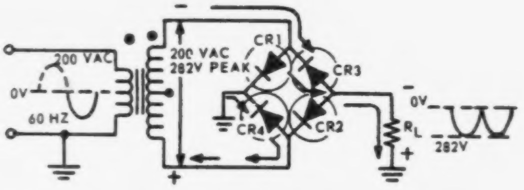


Figure 6-11. Bridge rectifier (negative half cycle).

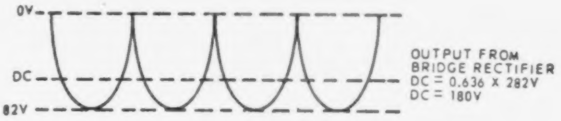


Figure 6-13. Bridge rectifier output.

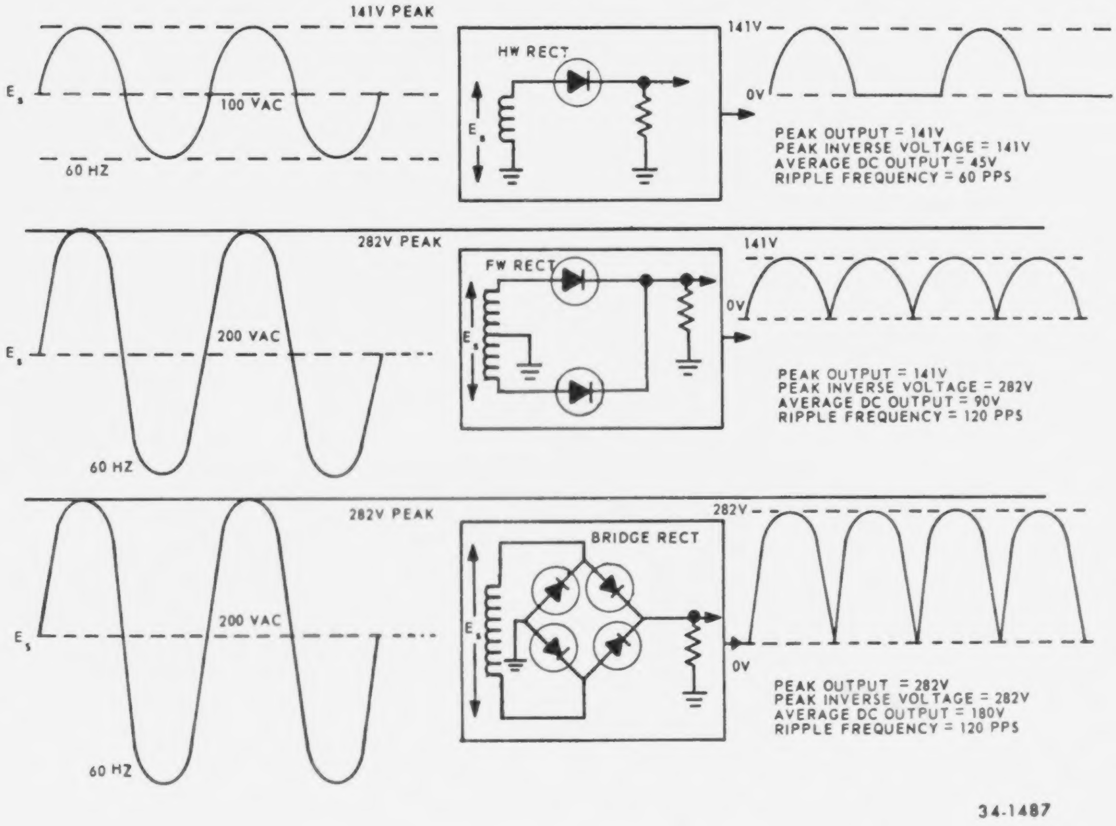
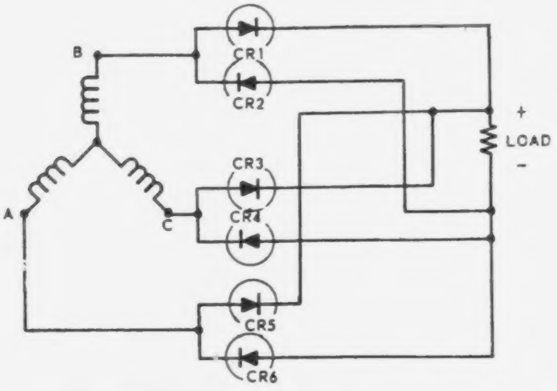
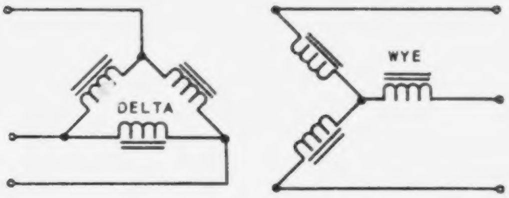
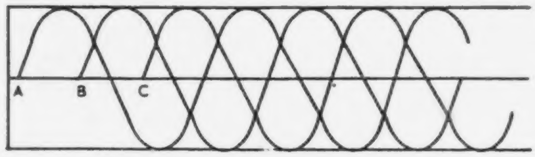

141V PEAK
Es
100 VAC
60 HZ
HW RECT
Es
141V
0V
PEAK OUTPUT = 141V
PEAK INVERSE VOLTAGE = 141V
AVERAGE DC OUTPUT = 45V
RIPPLE FREQUENCY = 60 PPS
282V PEAK
Es
200 VAC
60 HZ
FW RECT
Es
141V
0V
PEAK OUTPUT = 141V
PEAK INVERSE VOLTAGE = 282V
AVERAGE DC OUTPUT = 90V
RIPPLE FREQUENCY = 120 PPS
282V PEAK
Es
200 VAC
60 HZ
BRIDGE RECT
Es
282V
0V
PEAK OUTPUT = 282V
PEAK INVERSE VOLTAGE = 282V
AVERAGE DC OUTPUT = 180V
RIPPLE FREQUENCY = 120 PPS
34-1487

Figure 6-14. Summary of half-wave, full-wave, and bridge rectifiers.


B
A
C
CR1
CR2
CR3
CR4
CR5
CR6
+
LOAD
−

A. THREE-PHASE FULL-WAVE RECTIFIER

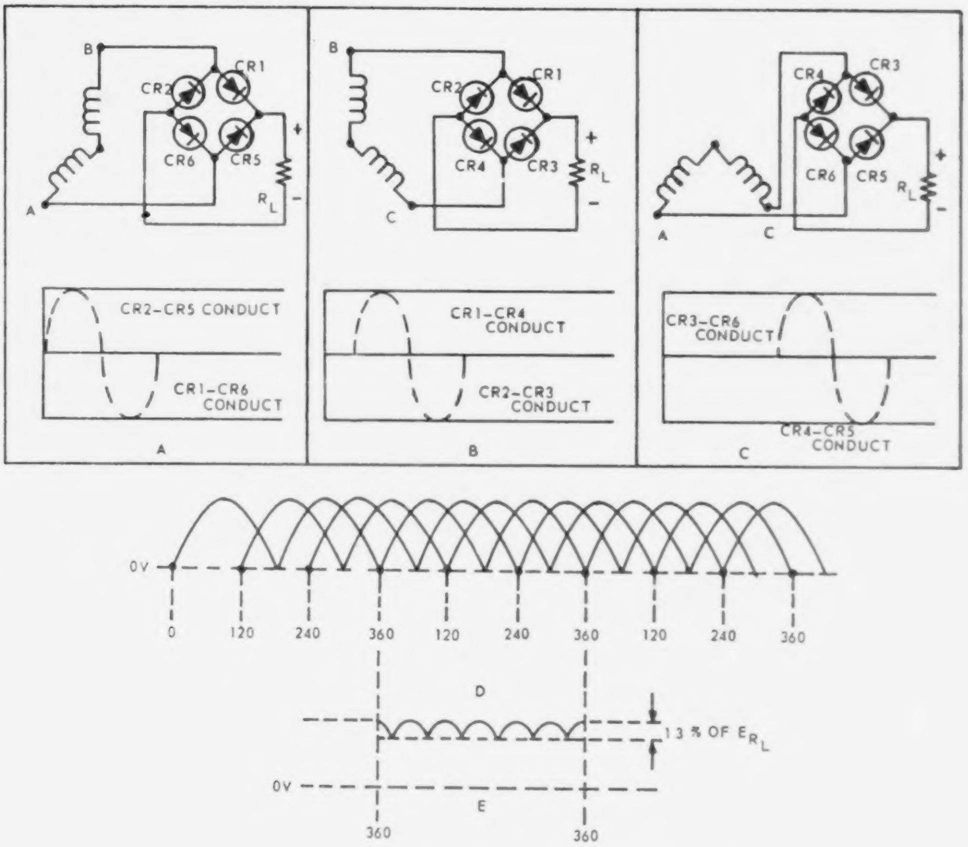




B. THREE-PHASE WAVESHAPES

Figure 6-15. Three-phase transformer windings.

Figure 6-16. Three-phase full-wave rectifier and waveforms.



34-1490

Figure 6-17. Three-phase rectifier analysis and waveforms.

Because the half-wave develops an output on only one-half of the input signal, its average output is one-half that of the full-wave. Also, because the bridge does not use the center tap of the transformer, its output is double that of the full-wave. The ripple frequency of the full-wave and bridge is twice that of the half-wave, since they use both alternations of the input signal.

The last item of concern to you here is peak voltage applied across the entire secondary of the input transformer.

Three-phase rectifier. When large amounts of power are needed, a three-phase input may be used in preference to a single-phase input. Many Air Force systems require three-phase power. The unfiltered output voltage of a three-phase rectifier is smoother than that of a single-phase rectifier.

A three-phase generator provides three equal single-phase voltages that have a phase angle between them of 120°. Three-phase current flows from the generator to a transformer, which will have either wye-connected or delta-connected windings, as shown in figure 6-15.

Assuming equal turns with primary and secondary windings, a delta-wound primary with a wye-wound secondary steps up the voltage. With equal windings, a wye primary with a delta secondary steps up the current. Three-phase voltages can be rectified by a three-phase bridge-type rectifier. Figure 6-16 shows the rectifier and the three-phase input voltage waveforms.

Three-phase voltages and currents have a phase displacement of 120 electrical degrees. In respect to time, this displacement is one-third the period of a cycle. The voltage waveforms in figure 6-16 show the three-phase voltages present at A, B, and C. Note that phase A is the reference phase, that phase B lags phase A by 120°, and that phase C lags phase B by 120°. In the three-phase bridge circuit shown, current flow through the load produces the output polarity shown. A reverse polarity is produced simply by reversing each diode.

Disregarding leg C of the transformer, let us trace an input voltage to determine the resulting output from the rectifier. Use transformer legs A and B of the wye-wound secondary of figure 6-16,A.

Phase A and phase B form a series circuit in figure 6-17,A. On the positive alternation of phase A voltage, assume that point A is positive with respect to point B through CR2, R_L, and CR5 to point A. On the negative alternation of the cycle, current will flow from point A through CR6, R_L, and CR1 to point B. The polarity of the voltage across R_L is negative at the bottom and positive at the top for both alternations of the input cycle.

Now disregard transformer leg B, and you have a series circuit with legs A and C (as shown in figure 6-17,C).

Assume that point C is positive with respect to point A. Current will flow from point A through CR6, R_L, and CR3 to point C to complete the circuit. On the next alternation, current flows from point C through CR4, R_L, and CR5 to point A to complete the circuit. Once again you will find that R_L has the same output polarity.

Figure 6-17,E, illustrates the resulting waveform that appears across R_L, combining all three phases of rectification as shown in figure 6-17,D. Observe that the ripple frequency is six times the input frequency. With a 60-hertz input, the three-phase, full-wave rectified output ripple frequency is 360 pps. The amplitude of ripple in the output is approximately 13 percent of the amplitude of the output voltage. With this low-amplitude ripple voltage, very little filtering is necessary in order to have a smooth DC output.

Exercises (479):

1. What will the output ripple frequency of the half-wave rectifier be, and why?

2. Match each characteristic in column B with its related term in column A. NOTE: Each item in column B may be used once or more than once.

Column A	*Column B*
___ (1) Half-wave rectifier.	a. Current flows during half of the input wave.
___ (2) Three-phase rectifier.	b. Ripple frequency is twice the input frequency.
___ (3) Full-wave rectifier.	c. Average voltage = peak voltage × .636.
___ (4) Bridge rectifier.	d. Breakdown rating of its diode must be twice as great as that of the half-wave diode.
	e. Requires a center-tapped transformer.
	f. Very little filtering is necessary to have a smooth DC output.
	g. Requires a three-phase bridge-type rectifier.
	h. Ripple frequency is six times the input frequency.

480. Indicate various significant uses and operations of voltage multiplier circuits.

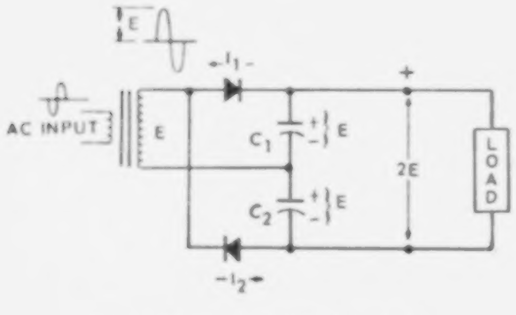
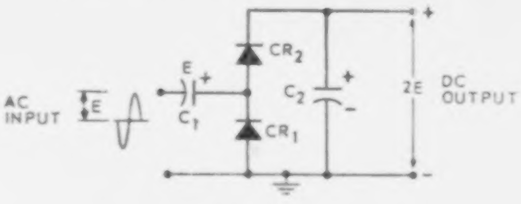


Figure 6-18. Conventional voltage doubler.

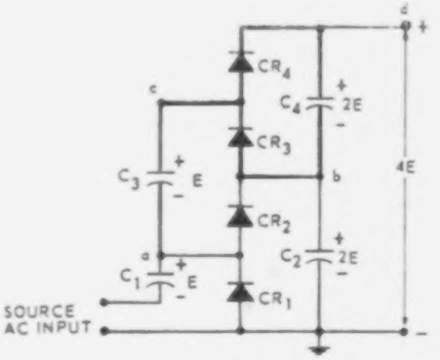
Voltage Multipliers. As a specialist, you know that one way of obtaining a DC output voltage is to use a multiple of the peak AC source voltage as a step-up transformer. There are other ways to do this, however, which do not require an increase in the secondary voltage of the transformer. In fact, voltage multiplication can be achieved without a transformer at all. Let's consider two types of rectifying circuits that produce a DC output voltage that is about twice the peak AC input voltage; then we will explain to you how higher multiples of voltage can be developed from a given source.

Conventional voltage doubler. Referring to figure 6-18, you will find a voltage doubler circuit that is essentially a full-wave rectifier; both the positive and negative alternations feed power to the load. During the positive alternations of the secondary voltage, CR1 conducts I_1 and capacitor C1 charges to the peak secondary voltage, E. During the negative alternations of the secondary voltage, CR2 conducts I_2 and C2 also charges to the peak secondary voltage, E. Since the polarity of the charge on C2 is series-aiding to the charge on C1, the voltage across the output terminals is twice the value of the peak secondary voltage (2E). Inasmuch as both the charging (via the rectifier) and discharging (via the load) of C1 and C2 constitute the ripple, the ripple frequency of this circuit is twice the frequency of the input AC.

Cascade voltage multipliers. A cascade voltage doubler circuit is illustrated in part A of figure 6-19. You can obtain any desired multiple of voltage by adding sections, as illustrated in part B of the figure. After analyzing the operation of the cascade doubler with us, you should be able to explain readily how higher degrees of multiplication are acquired.



A. DOUBLER



B. QUADRUPLER

Figure 6-19. Cascade voltage multiplier.

First, consider the negative alternation of the input. During these alternations, you can see that CR1 keeps C1 charged to E with a polarity as indicated. On the positive alternations, C2 is kept charged by the conduction of CR2. When CR2 conducts in the forward direction, C2 feels the peak AC input voltage, which is series-aiding the voltage across C1; therefore, the input peak E plus the voltage E on C1 charges C2 to 2E. Although full-wave rectification occurs, the output capacitor C2 is charged only during the positive half cycle. Consequently, the ripple frequency of this circuit is that of a half-wave rectifier, equal to the AC input frequency. This means that, like the half-wave rectifier, the cascade doubler is not suited for heavy current loads. Regulation is poor, and filtering is difficult.

For light loads that require a high DC voltage, the cascade circuit is quite popular, since it can be built up to provide the desired level of output. Refer to part B of figure 6-19, and note that the heavily lined circuitry is a replica of the cascade doubler. It is, therefore, possible to increase the DC voltage in multiples of two by adding doubler circuits.

The lightly lined circuit is identical to that in part A of the figure. The heavily lined circuit differs only in that the voltage across the input capacitor C3 is 2E rather than E. Capacitor C3 is kept charged to 2E by the action of CR1 and CR3. These two rectifiers effectively place C3 in parallel with C2. Whenever the charge on C3 is less than that of C2, CR3 is forward-biased. So when CR1 becomes forward-biased during the negative half cycle of the source AC input, C3 is charged by C2. You can see, therefore, that the output capacitor C2 feeds the input capacitor C3. Note that the DC voltage with respect to ground (or common) at point a is E; at point b, it is 2E; and at point d, it is 4E. Additional sections could give 5E and 6E, etc.

The cascade voltage multiplier is particularly useful as a transformerless high-voltage low-current supply. Each rectifier must withstand twice the peak input AC in the reverse direction; therefore, regardless of the amount of multiplication, the maximum PIV on any single rectifier is 2E.

You have now seen that the primary function of a rectifier circuit within an AC to DC power supply is to change AC voltage to DC voltage. However, as we discussed the different types of rectifier circuits, it was pointed out to you that the output voltage was pulsating DC; that is, it has pulses or ripples. We have also pointed out and briefly discussed that removing or reducing the output ripple of the rectifier circuit is accomplished by filters. Now, let's find out about some of the different methods of filtering.

Exercises (480):

1. Can voltage multiplication be achieved without using a transformer? If so, how can it be accomplished?

2. Refer to text figure 6-18. How is the ripple frequency doubled in this circuit?

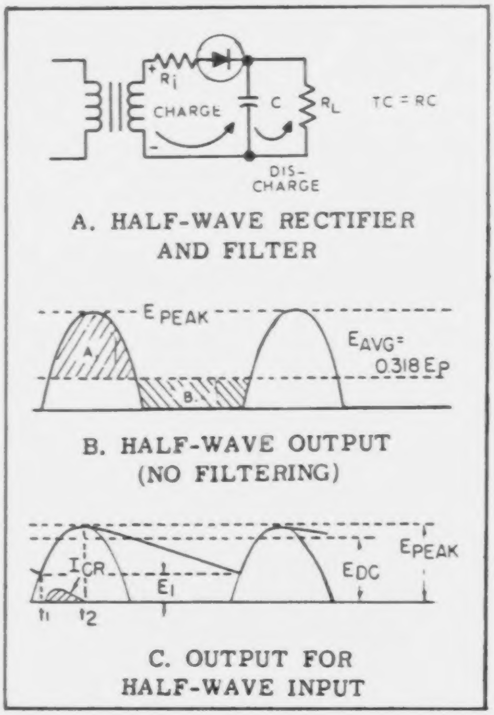
3. Refer to text figure 6-19. How can any desired multiple of voltage be produced?

4. What is the main use of a cascade voltage multiplier?

481. Associate selected operational characteristics with their appropriate types of filters.

Filters. We have discussed methods of converting AC to pulsating DC by use of various rectifier circuits. Most electronic equipment requires smooth DC supply that approaches the ripple-free output of a battery. Properly designed filters are used to convert pulsating DC to smooth DC. The filter reduces the amplitude of the ripple in the output of a rectifier. This is also described as decreasing the amplitude of the AC component in the rectified output, leaving the average DC component.

The unfiltered output of a half-wave rectifier is shown in figure 6-20,B. The polarity of the output voltage does not reverse, but its magnitude fluctuates above and below an average value as pulses of energy are delivered to the load. Note that the average voltage is shown as the line that divides the waveform so that area A equals area B. The fluctuation of the voltage above and below this average value is called *ripple,* or the AC component of the rectified output.



A. HALF-WAVE RECTIFIER AND FILTER

B. HALF-WAVE OUTPUT (NO FILTERING)

C. OUTPUT FOR HALF-WAVE INPUT

Figure 6-20. Capacitive filter and waveforms.

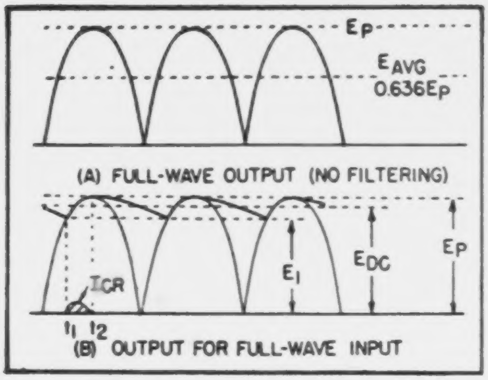


Figure 6-21. Waveforms for full-wave rectifier capacitive filter.

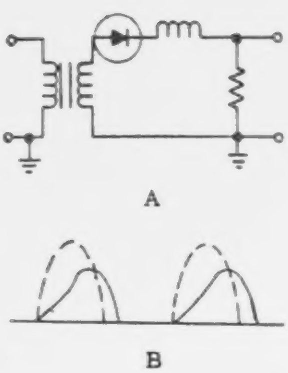


Figure 6-22. Inductive filter and waveforms.

The output of any rectifier, therefore, is composed of a direct voltage and an alternating or ripple voltage. For most applications, the ripple voltage amplitude must be decreased to a very low value. The circuit that decreases ripple voltage from the rectifier output is called a *filter*.

Capacitive filter. Ripple voltage exists because the rectifier supplies energy to the load in pulses. The fluctuations can be reduced considerably if some of the energy is stored in a capacitor while the rectifier is delivering its pulse.

Figure 6-20,B, shows the output of a half-wave rectifier. This pulsating DC voltage is the output of figure 6-20,A, before connecting filter capacitor C. C charges rapidly through current-limiting resistor R_i. The rate of charge of C is limited by the reactance of the transformer secondary, resistance of R_i, and the forward resistance of the diode. The voltage across the capacitor rises nearly as fast as the sine-wave voltage input to the rectifier. In other words, the RC charge time is short. The charge on the capacitor represents a storage of energy. When the rectifier input decreases, the energy stored in the capacitor discharges through load resistor R_L. The voltage across the capacitor (and the load) falls off slowly if the capacitor and load resistance form a relatively long time constant (R_LC). Current thus continues flowing through the resistor, and the amplitude of the ripple is greatly decreased, as may be seen in figure 6-20,C. Figure 6-20,A, shows the unfiltered voltage of a full-wave rectifier, while figure 6-21,B, shows the capacitive-filtered output-voltage waveform.

After the capacitor has been charged, it acts as a DC power source, and the rectifier does not conduct until the input voltage to the rectifier exceeds the voltage across the capacitor. Thus, in figures 6-20,C, and 6-21,B, current flows through the diode when the rectifier input reaches a voltage greater than the capacitor voltage. This occurs at time t_1 when the rectifier output voltage has a magnitude of E_1. Current continues to flow through the diode until slightly after the peak of the sine wave at time t_2. At this time, the sine-wave voltage is falling faster than the capacitor can discharge. A short pulse of current, beginning at t_1 and ending at t_2, is therefore supplied to the capacitor by the power source.

The average voltage of the unfiltered rectifier output is shown in figures 6-20,B (half-wave) and 6-21,A (full-wave). Because the capacitor stores energy during the pulse and delivers this energy to the load between pulses, the output voltage does not fall to zero. Hence, the average voltage of the filtered output is greater than that of the unfiltered output.

If the resistance of the load is small, the heavy current drawn by the load discharges the capacitor before the next pulse arrives and the average output voltage decreases. For this reason, a simple capacitive filter is not sufficient for rectifiers that supply a low-resistance load.

Inductive filter. Another device that is important as a filter is the inductor. Both the inductor and capacitor are reactive devices—that is, they both store energy on part of an alternation and return energy on the other part. Figure 6-22,A, shows an inductive filter. Filter indicators are placed in series with the load.

Figure 6-22,B, shows waveshapes of the half-wave rectifier with and without an inductive filter. The dotted lines represent the output current without the inductor, and the solid lines represent the output with the inductor.

The inductive filter uses inductive reactance properties of the coil only. The magnetic field created when current increases through a coil opposes the increase in current. A decrease in current allows the magnetic field to collapse, creating a force which opposes further reduction in current. The coil thus opposes any change in current. Study the solid line waveshape of figure 6-22,B, with this in mind.

Thus far, you have considered the capacitor and inductor separately as filters. You have been shown that the effect of both series inductance and parallel capacitance in a filter is to cause a steady flow of current through the load by storing energy during part of the cycle and returning energy to the circuit during the other

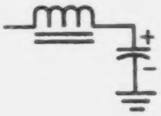


Figure 6-23. L-type inductive input filter.

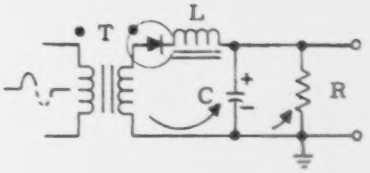


Figure 6-24. Rectifier and L-type inductive input filter (positive half cycle).

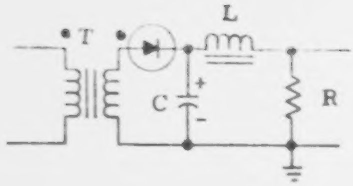


Figure 6-26. Rectifier and L-type capacitive input filter (no input).

part. The two types of reactance are much more effective when used together.

Remember that all inductors are connected in series with the load and that all capacitors are connected in parallel with the load. Filters which use these properties of a reactance develop a regulated output voltage. Regulation is defined as maintaining a constant voltage, current, or power in a circuit.

L-type filter. Now consider two different types of L-type filters as they are connected to rectifiers. One is an L-type inductor input filter, and the other is an L-type capacitor input filter. Two components that comprise the filter are the inductor (L) and the capacitor (C). Figure 6-23 shows an L-section inductor input filter.

Figure 6-24 connects this filter to the half-wave rectifier circuit. But what happens when you apply an AC signal? The diode conducts when the positive half of the incoming sine wave is applied to the transformer. The arrows show the current flow. As current begins to flow, capacitor C begins to charge, and a magnetic field (resisting this increase in current flow) builds up around L.

Since the diode is forward-biased, it will offer very little resistance, but the charging path for capacitor C now contains the impedance offered by the coil. For this reason, the capacitor will not charge to as high a value as it could if L were removed. It follows, also, that the voltage across R is lower with the inductive input filter.

As the positive half cycle begins to decrease (going in a negative direction), the diode approaches cutoff and capacitor C discharges through the load resistor, as shown in figure 6-25. The collapsing field of the inductor will make the diode conduct longer, and the energy stored by the coil is returned to the circuit. This provides a relatively constant output voltage. The other L-type filter arrangement is the capacitive input, shown in figure 6-26, using capacitor C and inductor L.

Now apply sine-wave input to the half-wave rectifier circuit and analyze the circuit operation, using figure 6-27. With the positive half of the sine-wave input applied, the polarity across the secondary of transformer T forward-biases the diode. As the diode conducts, current flows through two paths, L and R in series and capacitor C, as shown. Notice that the charge path for capacitor C contains only the extremely small resistance of a forward-biased diode. This means that the capacitor can quickly charge to a higher voltage than it could with the inductive input filter.

When the negative half of the input sine wave appears across the secondary of T, the energy in the coil and capacitor is delivered to the load as shown by the arrow in figure 6-28. Since the capacitor charges to the peak value, the output voltage across the load resistor is high (with high load resistance). As load resistance decreases, however, output decreases.

Summarizing, we can state that an inductive (choke) input filter gives a lower output voltage and good voltage regulation. On the other hand, a capacitive input LC filter gives a higher output voltage but less voltage regulation.

Pi-type filter. Now, consider the pi-type filter with a half-wave rectifier. Two arrangements are shown in figure 6-29: one type uses an inductor, while the other type uses a resistor, but both have two capacitors to ground.

To begin your study of pi-type filters, consider the pi-type filter that contains an inductor, figure 6-30. The components which make up the filter are C1, L, and C2. With a sine wave applied to the rectifier circuit, the positive half-cycle on the secondary of T forward-biases the diode, which begins to conduct. Simultaneously, C1 and C2 begin to charge. C1 charges to peak voltage, but C2 charges through L to a lower voltage. The negative half cycle on the secondary of T reverse-biases the diode, and capacitors C1 and C2 discharge through the load resistor (see fig. 6-31). This type of arrangement will give a fairly high output voltage and good voltage regulation.

A somewhat less effective pi-type filter is the RC type. Figure 6-32 shows this filter using a resistor in place of the inductor. When the positive half of the sine wave appears across the secondary of T, the diode conducts

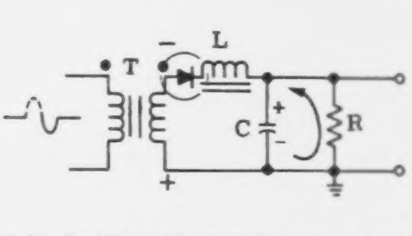


Figure 6-25. Rectifier and L-type inductive input filter (negative half cycle).

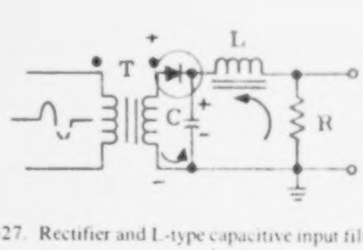


Figure 6-27. Rectifier and L-type capacitive input filter (positive half cycle).

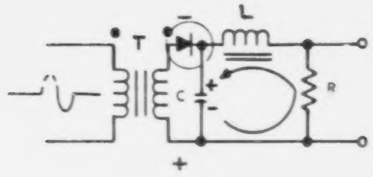


Figure 6-28. Rectifier and L-type capacitive input filter (negative half cycle).

and capacitors C1 and C2 charge. With the negative half of the input sine wave applied, the reverse-biased condition on the diode allows C1 and C2 to discharge, as shown in figure 6-33.

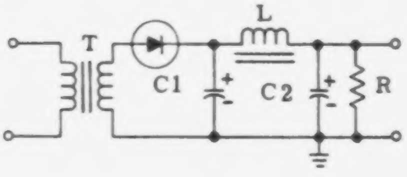
Since R1 is replacing an inductor, the DC output voltage is lower, and voltage reduction is not as good as you found in the LC pi-type. Since R1 is in series with R_L, the voltage dropped across R1 represents loss as far as the load is concerned.

In conclusion, we can say that a pi-type LC filter will yield a high output voltage and better voltage regulation than the RC pi-type filter. It is easy to explain the reasons for the above statements. First, the inductor is a reactive device which represents a high impedance to AC but very little resistance to DC. Second, the inductor opposes any change in current, and thus it reduces or smooths out any current surges.

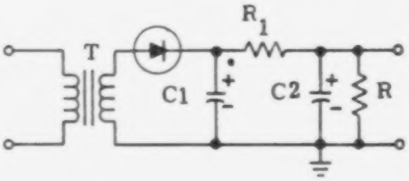
When you use a resistor instead of an inductor, the voltage regulation provided by the inductor is not present. But when current changes through the load, the voltage drop across the filter resistor also changes.

Exercises (481):

1. We say the filter reduces the ripple amplitude in a rectifier output. How else can this action be described?



A. L-C PI FILTERS



B. R-C PI FILTERS

Figure 6-29. Pi filters.

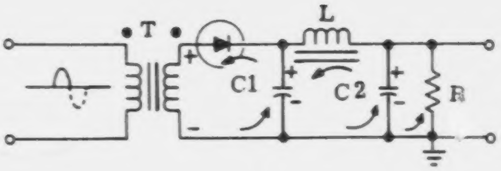


Figure 6-30. LC-pi filter (positive half cycle).

2. Match each characteristic in column B with its related appropriate filter in colume A. NOTE: Each item in column B may be used once or more than once.

Column A	*Column B*
___ (1) Pi-type filter.	a. Has two capacitors connected to ground.
___ (2) Inductive filter.	b. Gives a low output voltage and good voltage regulation.
___ (3) L-type filter.	c. Average voltage of the filtered output is greater than that of the unfiltered output.
___ (4) Capacitive filter.	d. Not sufficient for rectifiers that supply a low-resistance load.
	e. Two components comprise the filter circuit, an inductor and capacitor connected in an L.
	f. Uses inductive reactance properties of the coil only.

3. After the capacitive filter produces a capacitor charge which represents a storage of energy, what kind of power source does the charged capacitor act as?

4. What kind of output voltage and voltage regulation will the negative half cycle on the secondary of T, which reverse-biases the diode, and the discharge of capacitors C1 and C2 through the load resistor (shown in fig. 6-31) yield?

482. Associate various operational characteristics with their appropriate types of regulators.

Voltage Regulators. The output voltage developed by a source of power changes (1) with a change in input and

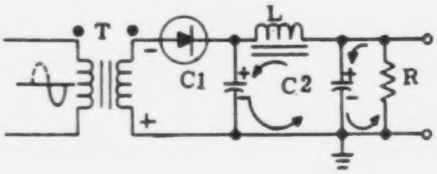


Figure 6-31. LC-pi filter (negative half cycle).

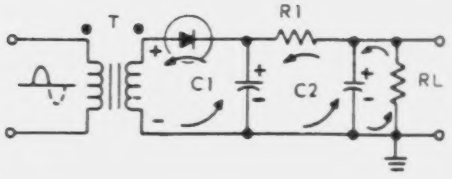


Figure 6-32. RC-pi filter (positive half cycle).

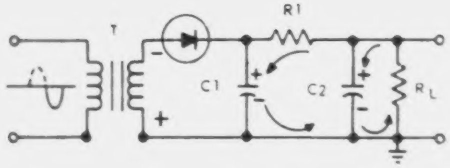


Figure 6-33. RC-pi filter (negative half cycle).

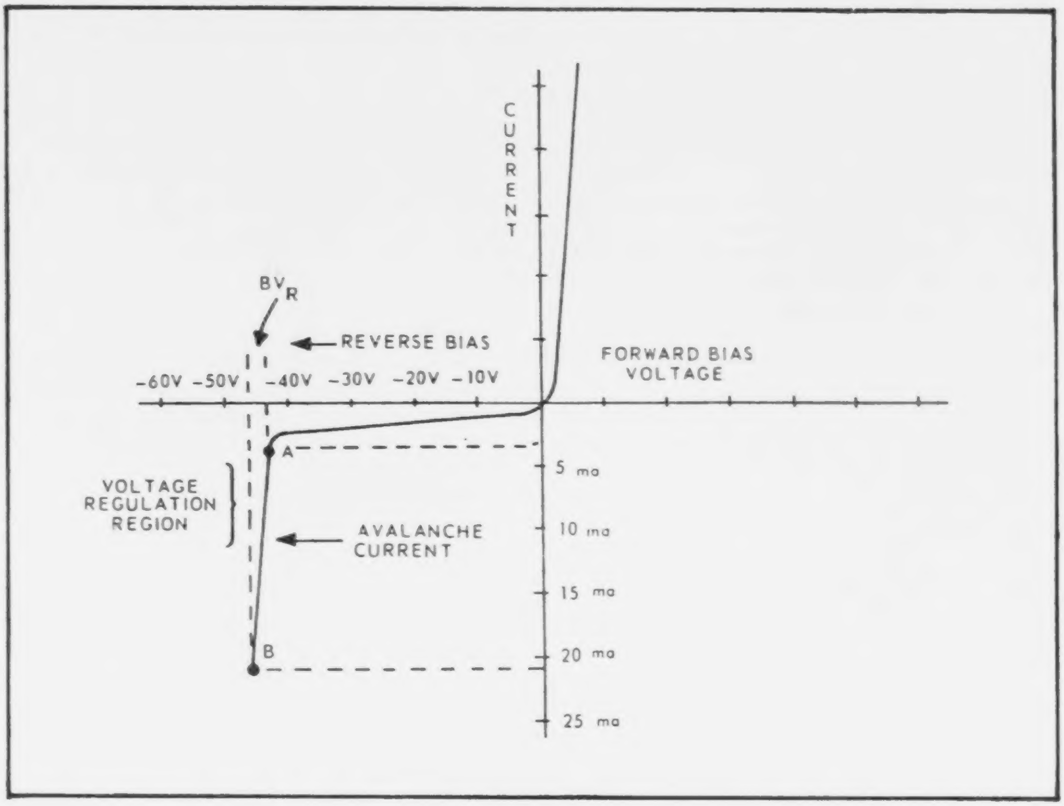


Figure 6-34. Zener diode characteristics curve.

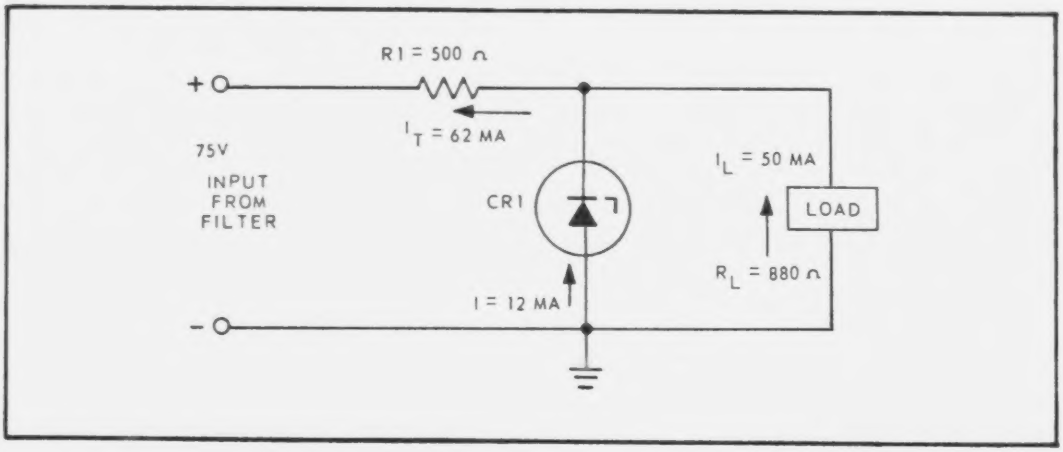

R1 = 500 Ω
+
-
IT = 62 MA
75V
INPUT FROM FILTER
CR1
I = 12 MA
IL = 50 MA
LOAD
RL = 880 Ω

Figure 6-35. Zener voltage regulator circuit.

(2) when current is drawn from the source. Many electronic circuits operate satisfactorily with a moderate amount of variation in the supply voltage without suffering a severe operational deficiency. Some circuits are very critical, and even a slight deviation from the normal supply voltage will cause unsatisfactory operation. These circuits require the use of a voltage-regulating device. Crystal diodes manufactured for this purpose are called *zener diodes.* Sometimes referred to as *avalanche diodes* or *breakdown diodes,* these diodes use the breakdown voltage and the avalanche current region of the PN junction. This objective discusses zener diodes, electronic voltage regulators, and silicon-controlled rectifiers (SCRs).

Zener diode. "Zener" is a name given to a family of diodes designed to operate with reverse breakdown voltage. Zener diodes operate in the avalanche region of their characteristic curves without damage.

The voltage-current characteristics of a typical zener diode are shown in figure 6-34. With forward bias, the zener diode operates the same as a regular PN junction. With a small reverse bias across the PN junction, the barrier potential is increased. This action increases the depletion region at the junction. Only a small leakage current will flow due to minority carriers.

Increasing the reverse voltage increases the velocity of the minority carriers. Some of these carriers collide with covalent-bond electrons, and the collision releases them as carriers. This action has a cumulative effect called *avalanche ionization.* It comprises a rapid increase in reverse current that, unless checked by a series-limiting resistor, may destroy the semiconductor. The reverse voltage at which avalanche effect occurs is called the *reverse breakdown voltage* and is abbreviated BV_R.

The zener diode voltage regulator is operated between point A (fig. 6-34) and point B. At point A, the current is about 3 mA, and the voltage across the zener is about 43 volts. At point B, the current is about 22 mA, and the voltage across the zener is about 45 volts. Between points A and B, the current changes 19 mA as the voltage changes 2 volts.

A zener voltage regulator circuit is shown in figure 6-35, along with the schematic symbol of zener diode CR1. The zener diode is placed in parallel with the load and in series with the current-limiting resistor R1. The voltage delivered to the load is controlled by the BV_R value of CR1. If the supply voltage (input from filter) decreases, the reverse voltage across CR1 will decrease. Therefore, the speed of the carriers in the crystal will decrease, and reverse current will decrease. The current through R1 decreases with a proportionate decrease in voltage drop across R1. The decreased drop across R1 cancels some of the original drop in the supply voltage and keeps the voltage across the load fairly constant.

Zener diodes are designed to operate at various voltages. When a regulated voltage in excess of the rating of one zener diode is required, two or more diodes may be connected in series. Several regulated voltages can be obtained from a single rectifier power supply.

To illustrate the operation of a zener diode, we must use both figures 6-34 and 6-35. Figure 6-34 indicates that the current midway between points A and B is about 12 mA and that the voltage across the zener is about 44 volts. Thus, the voltage across the load is also 44 volts. Current through the 880-ohm load resistance (fig. 6-35) is 50 mA. The current through R1, therefore, is the sum of the load current and the zener current, or 62 mA. The voltage drop across the 500-ohm R1 is 31 volts. The input voltage from the filter network is the sum of E_{R1} and E_{CR1}, or 75 volts.

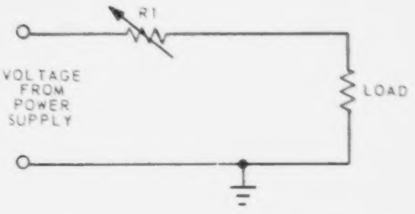


Figure 6-36. Equivalent EVR circuit.

If the voltage from the filter were to decrease to 69 volts, the voltage across the zener and the load would change to 43 volts. Figure 6-34 shows that with 43 volts across CR1, current through CR1 is 3 mA. The decrease of 9 mA through R1 and the decrease of 1 mA through the 880-ohm load decreases E_{R1} by 5 volts. So, for a change in input voltage (from the filter) of 6 volts (75 to 69 volts), the load voltage changed only 1 volt (44 to 43 volts). Checking:

$$E_{R1} + E_{load} = 69V;\ 26V + 43V = 69V$$

If the voltage from the filter were to increase to 81.5 volts, the voltage across the load would go to 45 volts. The increase of 10 milliamperes through CR1 (22 mA at 45 volts, fig. 6-34) and the 1 mA increase through the load increases the voltage drop across R1 to 36.5 volts (36.5V + 45V = 81.5V). The results are as follows: The voltage from the filter could have a change in amplitude of 12.5 volts (69 to 81.5 volts), but the voltage across the load would change only 2 volts (43 to 45 volts).

Even though a zener diode does regulate voltage, it has certain limitations. The current operating range (maximum to minimum) is limited; there is a voltage change between the minimum current and maximum current conditions; and the amplitude of the regulated voltage is fixed by the type of zener used. Electronic voltage regulators use amplifier circuits along with the zener diode to overcome the limitations of the zener diode alone.

Electronic voltage regulator (EVR). An electronic voltage regulator is a circuit designed to maintain the output voltage nearly constant regardless of input voltage or load changes. An electronic voltage regulator can be likened to the series resistive circuit shown in figure 6-36. The load resistance is connected in series with variable resistor R1 across the output terminals of the power supply. The voltage from the power supply has ripple and is not regulated. Further, the resistance of the load may change. Due to input voltage and load resistance changes, the voltage across the load cannot remain constant.

However, if the size of R1 is increased as the input

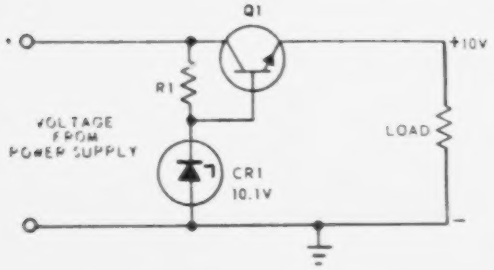


Figure 6-37. Simplified EVR circuit.

voltage goes up, the voltage across the load can be made to remain constant. An increase in E applied to a series circuit increases I total. A corresponding increase in R total will decrease I total back to its original value. Further, if the size of R1 is decreased as the input voltage decreases, the output voltage remains constant. Likewise, if the load resistance is decreased and if R1 is decreased a proportional amount, the load voltage remains constant. If the load resistance increases and if R1 is increased a proportional amount, the load voltage remains.

A simplified electronic voltage regulator circuit is shown in figure 6-37. A transistor has been inserted in place of the variable resistor. Recall that a transistor is a variable resistance, and its resistance can be controlled by electronic means. Zener diode regulator CR1 with current-limiting resistor R1 develops forward bias for Q1. The zener is rated at 10.1 volts and, during normal operation, holds the voltage on the base of Q1 constant at this value. With Q1 conducting, a voltage of approximately 10 volts is developed across the load resistance. Therefore, the bias on Q1 during normal operation is the difference between the base-emitter voltages, or .1 volt. With the base voltage of Q1 held constant by CR1, the only way the bias of Q1 can be changed is for the voltage on the emitter to change. Thus, the voltage on the emitter, which is also the load voltage, determines the resistance of Q1.

If, for any reason, the load voltage decreases, the bias on Q1 increases. With an increase in forward bias, the resistance of Q1 decreases and more current flows, bringing the load voltage back toward its original value.

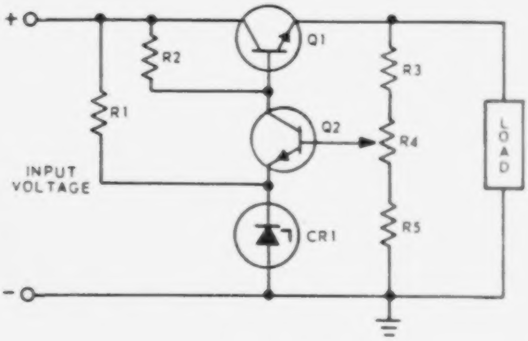


Figure 6-38. Electronic voltage regulator.

Or, if the load voltage increases, the bias on Q1 decreases. A decrease in forward bias of Q1 causes resistance of Q1 to increase. This causes less current to flow and the voltage across the load returns to the regulated value. The circuit is designed so that the resistance change in Q1 is proportional to a change in load voltage. This operation holds the voltage across the load relatively constant in case either the input voltage of the load resistance changes.

Although this is an improvement over the simple zener diode regulator, the simplified electronic voltage regulator still has limitations. Figure 6-38 shows a schematic of a complete electronic voltage regulator circuit. Now, two class A amplifiers, Q1 in series and Q2 in shunt, detect and compensate for variations in source voltage or load. With the addition of Q2 and the voltage divider network (R3, R4, and R5), this circuit regulates the voltage across the load to a smoother, more constant value.

Transistor Q1 is in series with the load. The action of Q1 changing its resistance to hold the output voltage constant is still present. Notice that the base current of Q1 is not controlled by Q2. R2 is the collector-load resistor for Q2 and the forward-bias resistor of Q1. Resistor R1 is the current-limiting resistor for CR1.

The bias for transistor Q2 is determined by the voltages on its emitter and base. The zener diode sets the emitter voltage, which is called the *Q2 reference voltage.* The voltage on the base of Q2 is developed by the voltage divider network (R3, R4, and R5) connected across the load. This arrangement continuously samples the output voltage. In other words, if the output voltage were to increase, the voltage on the movable arm of R4 would increase. So, with the emitter voltage of Q2 being held constant at all times, the conduction of Q2 is controlled by the voltage at the arm of R4.

To illustrate the operation of the electronic voltage regulator, let's discuss (1) an increase of input voltage and (2) an increase in the load on the circuit.

An increase in input voltage is felt across voltage dividers R3, R4, and R5. The voltage at the arm of R4 will go in a positive direction. This increase in voltage at the base of Q2 increases its forward bias. Transistor Q2 conducts harder and increases the voltage drop across R2. This makes the voltage on the base of Q1 less positive. A less positive voltage on the base of Q1 decreases the forward bias of Q1, which increases its resistance. When the resistance of Q1 increases, more voltage is dropped across Q1 (collector to emitter). The increase in voltage drop across Q1 nearly equals the increase in input voltage (from the filter), and the load voltage remains relatively constant. This action is instantaneous, and the EVR circuit maintains a regulated output voltage any time the input voltage increases. A decrease in input voltage results in just the opposite action within the circuit, and the output voltage remains at the regulated value.

An increase in load on the circuit means that the resistance of the load has decreased. When this occurs, load voltage decreases. Any change in load voltage causes the voltage at the arm of R4 to decrease. The decrease in voltage at the base of Q2 reduces its forward bias.

Transistor Q2 then conducts less, and the current through the load resistor decreases. This causes the voltage on the base of Q1 to increase (become more positive). The increase in voltage on the base of Q1 increases forward bias and causes the resistance of Q1 to decrease. The decrease in resistance of Q1 (emitter to collector) causes the voltage across Q1 to decrease, leaving more voltage across the load. The decrease in voltage across Q1 nearly equals the decrease in load voltage and, for all practical purposes, the load voltage remains constant.

Transistor Q1 is referred to as the series regulator. The voltage on the arm of R4 is called the *error signal,* and Q2 is the differential or error amplifier, since it amplifies the error signal. The zener diode provides the reference voltage for error amplifier Q2. This regulator circuit provides very close regulation of the output voltage.

Another characteristic of the electronic voltage regulator circuit is the fact that the output voltage can be adjusted to a specific value. Resistor R4 is the output voltage adjuster. If the arm of R4 is moved up, the forward bias on Q2 increases and Q2 conducts harder. The voltage across R2 increases, and the voltage on the base of Q1 decreases. The forward bias of Q1 is thus decreased, so the resistance of Q1 increases. This action will reduce the output voltage.

If the arm of R4 is moved down, the forward bias of Q2 decreases. Q2 conducts less, and the voltage across R2 decreases. The voltage on the base of Q1 increases, which decreases the resistance of Q1. This action will cause the output voltage to increase to a higher value.

As with any electronic circuit, the EVR is subject to failure. Knowing the correct operation and the symptoms of malfunction, a technician can repair an electronic voltage regulator circuit very rapidly.

You can make two quick checks to determine the possible trouble. First, check the DC (load) output voltage, and second, check to see if the circuit still regulates the output voltage.

Assume that the output voltage is higher than normal and that there is no regulation. This could be caused by an open zener diode. With CR1 open, Q2 cannot conduct, and the voltage on the base of Q1 may be very high. The resistance of Q1 will be very low; therefore, the output voltage will be higher than normal. The circuit cannot regulate, because the reference voltage for Q2 is no longer present. Another possibility is that R3 is open. With R3 open, the voltage on the base of Q2 will be near 0 volts, and Q2 cannot conduct. Again, the voltage on the base of Q1 will be a high positive, and the output voltage will rise to a value higher than normal. The circuit cannot regulate because the sample voltage is no longer present. If transistor Q1 were to short, the same symptoms would be present.

A symptom of no output voltage could be caused by an open Q1 or an open R2. With Q1 open, the series circuit is broken. With R2 open, there is no forward bias for Q1, so the only output voltage will be due to minority current.

Silicon-controlled rectifier (SCR). The silicon-controlled rectifier is basically a four-layer (PNPN) semiconductor device having three electrodes: a cathode, an anode, and a control electrode called a gate. Like all rectifiers, the SCR conducts current primarily in one direction. It differs, however, from conventional rectifiers in that it will not conduct a substantial amount of current in the forward direction until the anode-to-cathode voltage exceeds a certain minimum voltage called the forward breakover potential. The value of this potential can be varied or controlled by the use of an external signal at the control electrode (gate) of the SCR. This unique control characteristic makes the SCR particularly useful in power-controlling devices, especially in high-power circuits. Figure 6-39 shows the schematic symbols of the SCR.

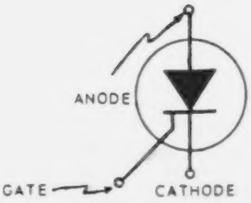


Figure 6-39. Silicon-controlled rectifier schematic symbols.

Figure 6-40 shows the SCR properly connected in a circuit that can be used to determine its forward breakover potential. Since the supply voltage causes the anode to be positive with respect to the cathode, the resulting electrostatic field through the device causes electron carriers to be attracted toward the anode and causes hole carriers to be attracted toward the cathode. This electrostatic field and the resultant movement of carriers form forward bias at junctions J1 and J3 Conduction from cathode to anode would occur if J2 were not reverse biased. Examinations will show that the electrostatic field through the SCR causes the majority carriers to be drawn away from J2, and a reverse-bias condition results. The movement of carriers, then, is a momentary condition that will cease when the reverse-biasing potential across J2 equals the anode-to-cathode

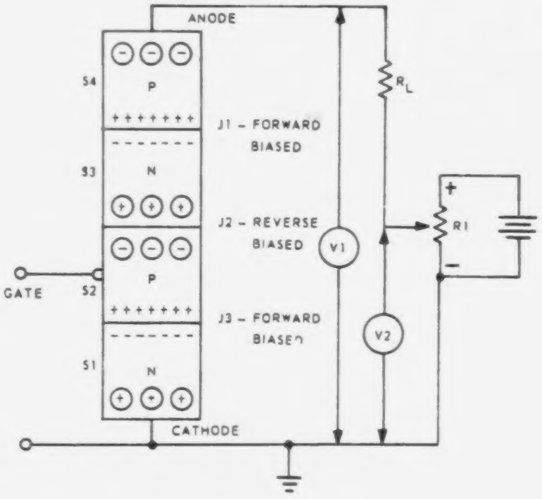


Figure 6-40. Bias on SCR junctions.

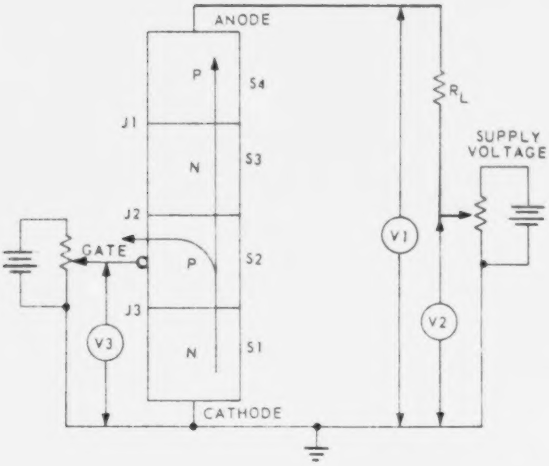


Figure 6-41. Achieving conduction by gating.

potential. The SCR is now in its nonconducting or OFF state.

Conduction can be achieved by one of two means. The first means is to increase the anode-to-cathode potential until the reverse-biased junction, J2, breaks down. The potential at which this breakdown occurs is called the *forward breakover potential.* Once breakdown occurs and conduction results, the anode-to-cathode voltage (V1 in fig. 6-40) decreases due to the increased voltage drop across RL. At first glance, it would appear that there is no longer enough potential across J2 to maintain the breakdown condition. However, this breakdown condition continues. Recall that a junction is said to be reverse-biased when majority carriers are attracted away from the junction. Recall also that reverse bias for majority carriers is forward bias for minority carriers (holes in N-type material, free electrons in P-type material). The method of maintaining conduction with a potential across J2 that is less than the forward breakover potential is based on the following concept: Once the breakdown of J2 has occurred, electrons from section S1 cross J3. If S1 is more heavily doped than S2, some of the electrons crossing J3 will *not* meet holes and combine. This condition is called *saturation.* Those that do not combine act like minority carriers, since they are electrons in P-type material. These electrons then see J2 as being forward-biased for them, and they cross on over J2 into the N-type section S3. J1 is also forward-biased for them, and they move on to the anode and out into the circuit. The important aspect, then, is to have S1 more heavily doped than S2 so that electrons continue in excess in S2. When this occurs, sections S1, S2, and S3 act like a single piece of N-type material, since electron current moves through them. Since the anode is P-type material, the overall effect is as if we now have a single PN junction at J1. The SCR remains in this high-conducting condition until the current drops to a value below that necessary to supply more than enough electrons from S1 and S2 to combine with and cancel out all the holes in S2. This minimum current is called *holding current.* When the holes in S2 outnumber the free electrons arriving from S1, the number of these electrons reaching J2 is insufficient to maintain conduction and conduction stops. J2 reverts to a simple reverse-biased junction until the forward breakover potential is again exceeded.

The second means of achieving conduction involves the use of a gate electrode. A positive potential on the gate is used to cause conduction. This potential is less than the anode-to-cathode breakover potential. To understand the operation of the gate electrode, study figure 6-41. You will notice that the gate is tied to the P-type section S2. If the gate is made positive with respect to the cathode, an external path for current flow is provided, and current flows across J3. If the gate potential is

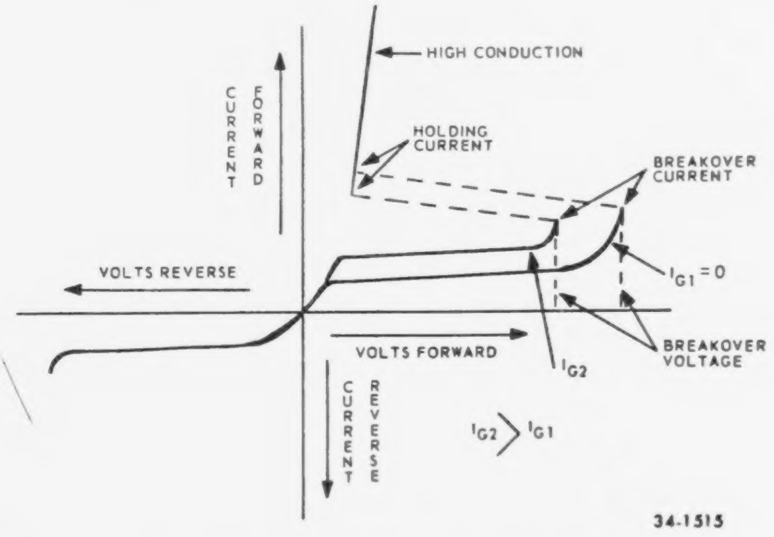


Figure 6-42. E-I curves for different values of gate current.

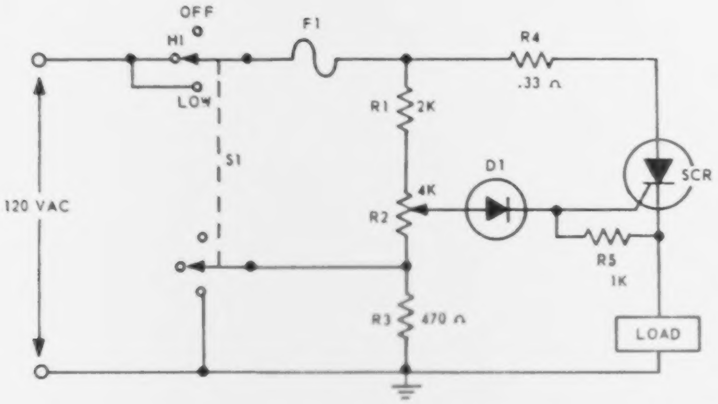


Figure 6-43. SCR power control circuit.

sufficiently positive to cause saturation of section S2, the excess electrons in S2 will see J2 as being forward-biased for them, and conduction will begin through the device to the anode. The more positive the gate potential is made, the greater will be the saturation of S2 and the lower the anode-to-cathode voltage required to attract electrons across J2.

Figure 6-42 shows two curves, one with zero gate current ($I_{G1} = 0$) and one with gate current (I_{G2}), which is greater than zero ($I_{G2} > I_{G1}$). Observe that the breakover voltage point with I_{G2} is lower than with I_{G1}. The voltage forward represents the anode-to-cathode voltage measured by V_1 in figure 6-41. If the gate current is increased sufficiently to saturate section S2, current flows through the SCR even with no anode-to-cathode voltage applied.

After the silicon-controlled rectifier is triggered by the gate signal, the current flow through the device is independent of gate voltage or gate current. It remains in the high-conduction state until the anode current is reduced to a level below that required to sustain conduction. The device can be turned off in minimum time by application of a reverse bias from anode to cathode.

If an AC signal is applied to the anode, the SCR can be made to conduct during any portion of the positive alternation by applying a signal to the gate. For example, if the triggering signal is applied at the positive peak of the anode voltage waveform, the SCR conducts only a quarter of a cycle. This flexibility of control distinguishes the silicon-controlled rectifier from all other types of semiconductor devices.

Figure 6-43 illustrates a typical circuit for a practical application of the SCR. Here, a variable potential may be applied through D1 to the gate of SCR. Gate current controls the conduction time of the SCR, which, in turn, controls the amount of current through the load. The current passed by the SCR may control the speed of a motor, the heat of a soldering iron, or operation of certain small home appliances.

Basically, the circuit is of the phase-control type. The gate circuit of the SCR is supplied with the positive half of the AC input, the negative half being blocked by D1 to protect the SCR gate from reverse voltage. As this positive voltage increases to some value determined by the setting of S1 and R2, sufficient voltage is applied to the gate to turn on the SCR. Resistor R5 serves as part of the voltage divider to assure proper triggering of the SCR. It also serves to limit reverse voltage between gate and cathode when the SCR is not conducting. R4 is a surge-limiting resistor. It is important to protect the SCR, since even very short transients can cause serious damage.

The SCR is turned on for some portion of the positive half cycle, and it supplies pulsating DC to the load. Switch S1 selects either a HI or LO speed function by determining how late in the half cycle the gate firing can be set. With R3 out of the circuit, gate firing can be completely prevented by setting R2 to its minimum position.

Exercises (482):

1. Match each characteristic in column B with its related term in column A. NOTE: Each item in column B may be used only once.

Column A

____ (1) Silicon-controlled rectifier (SCR).
____ (2) Zener diode.
____ (3) Electronic voltage regulator (EVR).

Column B

a. Placed in parallel with the load and in series with the current-limiting resistor.
b. A four-layer, three-junction device that has three electrodes.
c. Potential on the gate controls the potential at which breakover takes place and the diode conducts.
d. Exhibits voltage-regulating characteristics when operated at specific reverse voltage.
e. A sample of the output voltage is applied to the error amplifier.
f. Conducts easily in the forward direction when the forward breakover potential is exceeded.
g. A potentiometer is used to adjust the output voltage.

Column B

h. Operates in the avalanche region of its characteristic curve without damage.

i. In this basically phase-control-type circuit, the gate circuit is supplied with the positive half of AC input, with the negative half being blocked by D1 to protect the gate of this type from reverse voltage.

j. With this device, though the power supply voltage has ripple and is not regulated, if the size of R1 is increased as the input voltage increases, the voltage across the load can be made to stay constant (see fig. 6-36).

k. Because these operate at various voltages, when two or more are connected in series, several regulated voltages can be gotten from a single rectified power supply.

2. Cite the three limiting characteristics of the zener diode.

3. With the EVR, it is characteristic that a symptom of no output voltage can be a product of two conditions. Name and briefly describe each.

4. What characteristic of the SCR makes it important for you to protect the SCR?

483. Given a voltage divider network determine the correct component parameters when the designated voltage is applied.

Voltage Dividers. A resistor that is used as a load resistor may also serve as a voltage divider and as a bleeder. A simple voltage divider composed of three similar resistors in series is shown in figure 6-44. As long as no load current is drawn from any terminal except the top, the voltage across the resistors will divide in proportion to the resistance values of the various resistors. It is common practice to ground one end of a voltage divider. Therefore, ground potential is normally used as a reference point. If a rectifier and its filter are connected so that no part of the circuit is grounded, the voltage divider can be grounded at any point without affecting the operation of the rectifier, provided that the insulation of all parts in the circuit can withstand the voltage involved.

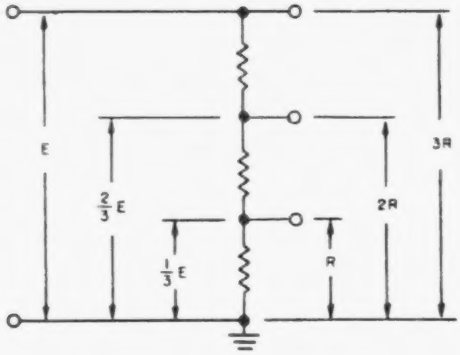


Figure 6-44. Simple voltage divider.

As soon as a load is connected across the divider at any of the intermediate terminals, the voltage division shown in figure 6-44 is no longer applicable. Suppose that a voltage divider is required across a power supply with a maximum output of 10 milliamperes at 300 volts. Suppose further that two voltage taps are required in addition to the full output voltage across the divider circuits; these taps are to provide the following:

- 50 volts at 1 milliampere for load 3.
- 150 volts at 1 milliampere for load 2.
- 300 volts at 7 milliamperes for load 1 (main load).

These requirements are shown in part A of figure 6-45.

Your first step in solving this problem is to calculate the value of the bleeder current, I_b. You can calculate this value as follows:

$$\begin{aligned} I_{\text{total load}} &= I_{\text{load 1}} + I_{\text{load 2}} + I_{\text{load 3}} + I_b \\ &= 7 + 1 + 1 + I_b = 9 + I_b \end{aligned}$$

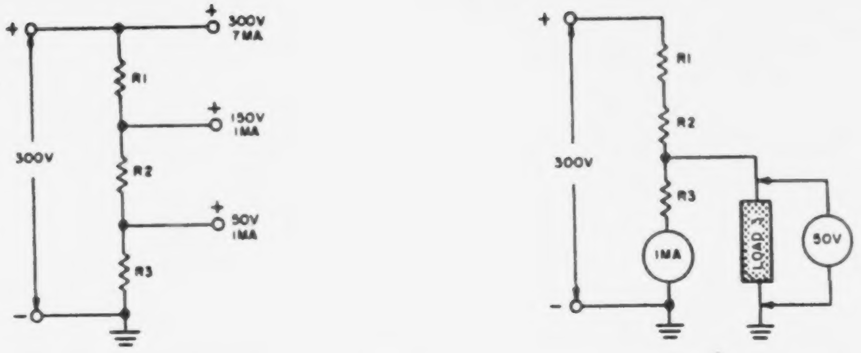
However, the bleeder current is one-tenth of the full-load current, or $I_b = I_{\text{total load}/10}$; so algebraic substitution will result in this:

$$\begin{aligned} I_b &= \frac{9 + I_b}{10} \\ 10I_b &= 9 + I_b \\ 10I_b - I_b &= 9 \\ 9I_b &= 9 \\ I_b &= 1 \text{ milliampere} \end{aligned}$$

Your next step is to calculate the value of voltage divider resistor R3. In this connection, refer to part B of figure 6-45. You can determine this value very simply by means of Ohm's law, since the voltage across this resistor is known to be the voltage across load 3. Here is the calculation:

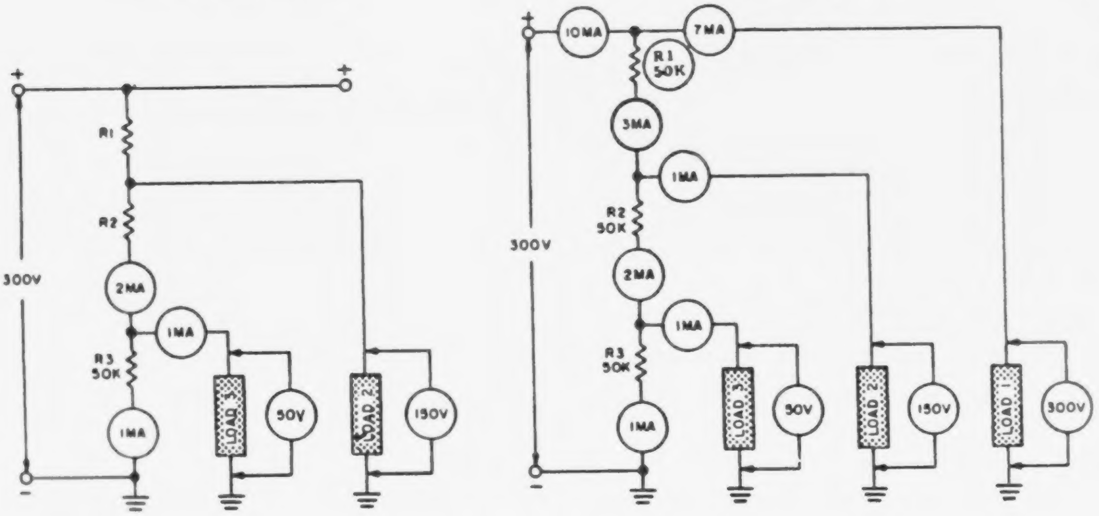
$$R3 = \frac{E_{\text{load 3}}}{I_b} = \frac{50 \text{ volts}}{0.001 \text{ ampere}} = 50{,}000 \text{ ohms}$$

The next resistor in the voltage divider is R2, the value of which you calculate on the basis of the voltage drop across R2 and the total current through R2. The voltage across this resistor is the desired voltage at this tap less the voltage dropped across resistor R3. This means that $E_{R2} = E_{\text{load 2}} - E_{\text{load 3}}$, which equals 150 − 50, or 100 volts. A consideration of the current through the resistor (refer to part C of fig. 6-45) will show you that the bleeder current, in conjunction with the current through load 3, is going to flow through R2. The total current through R2



A
DESIRED VOLTAGE DIVIDER

B
CALCULATION OF R3



C
CALCULATION OF R2

D
CALCULATION OF R3

Figure 6-45. Individual steps in the calculation of a voltage divider.

will therefore be $I_b + I_{load\ 3}$, which is 2 milliamperes. Thus, your calculation of the resistance value of R2 is this:

$$R2 = \frac{E_{R2}}{I_{R2}} = \frac{100 \text{ volts}}{0.002 \text{ amperes}} = 50{,}000 \text{ ohms}$$

You can find the value of resistor R1 by a process similar to the one you used to find the value of R2. Part C of figure 6-45 shows that the current through R3 will consist of the currents through load 3 and load 2, plus the bleeder current, I_b, or a total of 3 milliamperes. The voltage across this resistor will be the total power supply voltage − the voltage across load 2; that is $E_{R1} = E_{total} - E_{load\ 2}$, which equals 150 volts. Calculate the resistance value of R1 by means of Ohm's law like this:

$$R1 = \frac{R_{R1}}{I_{R1}} = \frac{150 \text{ volts}}{0.003 \text{ ampere}} = 50{,}000 \text{ ohms}$$

You can make a check confirming the total circuit current by observing that 3 milliamperes flow through the voltage divider to merge with 7 milliamperes flowing through load 1, giving a total of 10 milliamperes, the original specified current; refer here to part D of figure 6-45.

A voltage divider will operate satisfactorily as long as the load currents through the individual circuit branches are constant. If a load that is placed in a voltage divider is keyed, such as by an oscillator, or if the load current changes by any means whatever, all the voltages and currents of every other load placed on the voltage divider circuit will be changed, possibly enough to produce faulty operation within other circuits that are connected to the voltage divider.

Exercise (483):

1. Suppose you have a simple voltage divider with three similar resistors in series. What will happen in the

operation of the rectifier if a rectifier and its filter are so connected that no part of the circuit is grounded and the voltage divider is grounded at not more than one point at a time? What other provision must necessarily by present for this result to take place?

2. Refer to figure 6-45. If load 3 is 60 volts at 2 milliamperes, load 2 is 150 volts at 1 milliampere, and load 1 is 300 volts at 6 milliamperes, what are the values of the following circuit parameters?
   a. I_b.

   b. R_3.

   c. R_2.

   d. R_1.

484. Give selected aspects of the operation of a typical solid-state power supply.

Typical Solid-State Power Supply. One of the advantages of solid-state power supplies is compactness, which is chiefly important in computers today. As a rule, you will find that a computer module containing a solid-state supply is compact and readily accessible to facilitate maintenance. You will find a schematic of a typical power supply module illustrated in figure 6-46. This particular module produces these three DC voltages: −12, −3, and + 3 volts. These voltages are utilized within the solid-state logic circuits of the computer. Section A of the schematic contains the circuitry of the −12-volt supply; section B, the +3-volt supply; and section C, the −3-volt supply. Input power is 115 volts ± 10 percent, 60-Hz, single-phase AC.

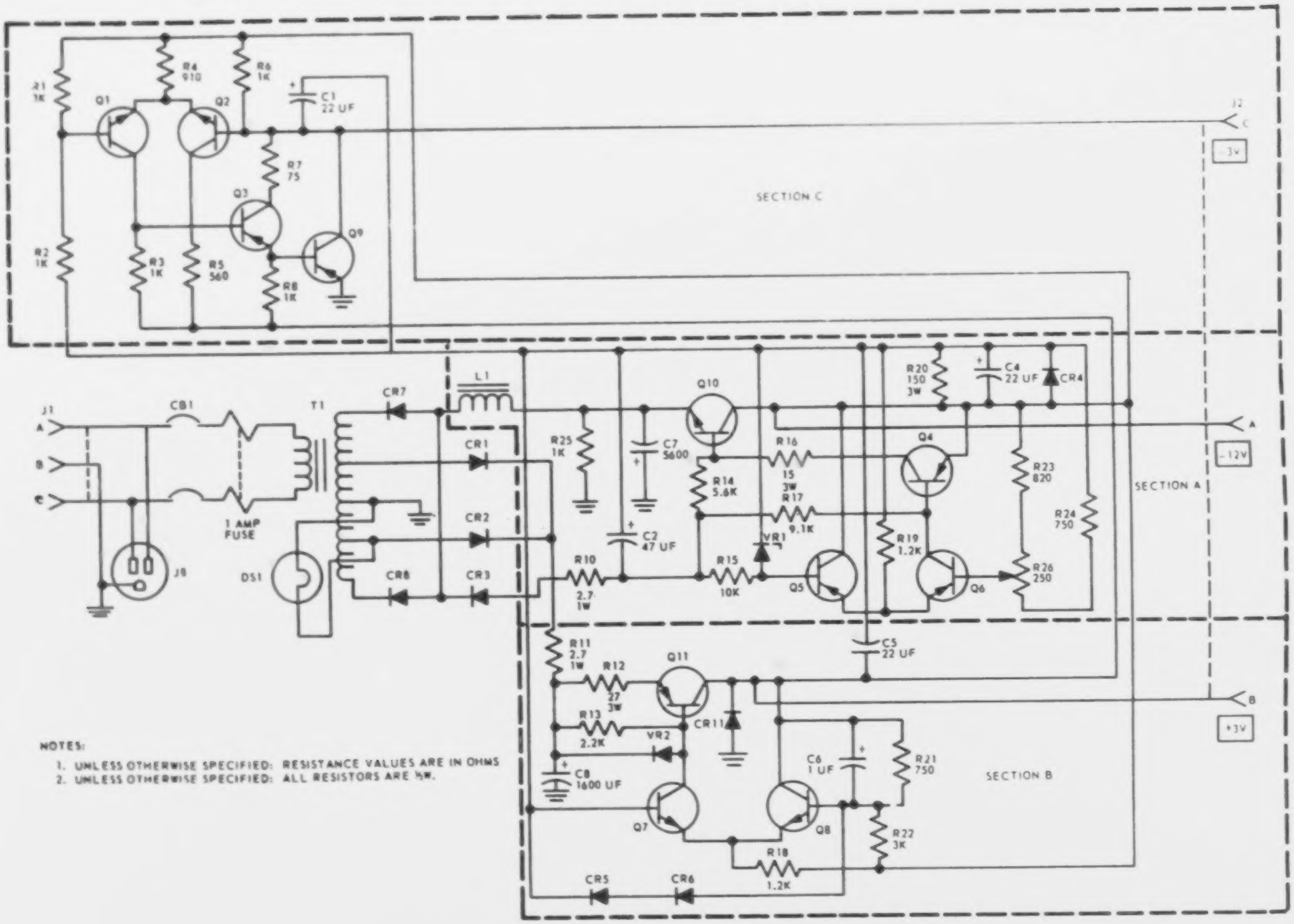
The −12-volt portion of the power supply (shown in section A of fig. 6-46) is a series-regulated supply. With circuit breaker CB1 turned on, AC power is applied to transformer T1 and power-on light DS1 lights. The AC voltage at the secondary of T1 is full-wave rectified by diodes CR7 and CR8 and filtered by an LC filter circuit consisting of inductor L1 and capacitor C7. Resistor R25 serves mainly to discharge the filter capacitor when power is turned off. A negative DC voltage is also developed by an RC filter circuit consisting of resistor R10, diode CR3, and capacitor C2. This voltage is more negative than that developed by the LC filter; it insures proper biasing within the −12-volt supply. Transistors Q10 and Q4, the series regulator transistors, may be considered as a single equivalent transistor with a current gain equal to the product of the current gains of both transistors. Transistors Q5 and Q6 form a differential amplifier circuit that compares a sample of the output voltage with a reference voltage set by zener diode VR1 to provide feedback control of series transistors Q10 and Q4 in order to insure regulation of the −12-volt output. In other words, if the output voltage increases or decreases, the differential amplifier senses this change and provides feedback to the series-regulating transistors.

To investigate how the circuit regulates the −12-volt output, assume that the voltage changes. If the voltage of the −12-volt line were to go more positive, the base voltage of transistor Q6 would go more positive, since it is derived from the −12 volts through the voltage divider consisting of resistors R23, R26, and R24. (The potentiometer R26 is initially adjusted to set the output voltage at the desired −12 volts.) The base voltage of transistor Q5 is fixed at −5.6 volts by zener diode VR1, which then fixes the common-emitter voltage of Q5 and Q6 at about −5 volts. Since the base voltage of Q6 went positive for an assumed rise in voltage at the input line and with the emitter voltage of Q6 fixed, the collector voltage of Q6 will go more negative. Transistor Q4 will conduct more heavily due to the increased negative voltage at its base, and the voltage at the emitter of Q4 will go more negative, since it must follow the base voltage. Therefore, the effect of the positive-going voltage change is compensated for by an increase in conduction of Q4. Since the base voltage of Q4 went more negative, the collector voltage of Q4 will go more positive, causing Q10 to also conduct more heavily. The voltage drop across Q10 will decrease, thereby bringing the −12-volt line more negative to compensate for the assumed positive increase in voltage.

The function of diode CR4 is to prevent the −12-volt line from going positive. Capacitor C4 provides filtering of high-frequency line noise. Resistor R20 provides a minimum load for the choke filter when the external load is light so that current is always flowing through the choke.

A second series regulator circuit which provides +3 volts is shown in section B of figure 6-46. Transistor Q11 is the series regulator transistor, while transistors Q7 and Q8 form a differential amplifier. A full-wave rectifier consisting of diodes CR1 and CR2 feeds into a capacitor filter, C8. Resistor R11 limits the current to protect diodes CR1 and CR2. The base of Q7 is connected to ground. The base voltage of Q8 is set at 0 volts by the voltage dividers R21 and R22, which are between +3 and −12 volts. To analyze the circuit operation under changing output conditions, assume that the output voltage goes more positive. The base voltage of Q8 increases, and this increases the current through the common-emitter resistor R18, causing Q7 to conduct less. The voltage at the collector of Q7 increases, causing series regulator transistor Q11 to conduct less. The voltage across Q11 increases, causing the output line voltage to go more negative in order to compensate for the initial positive voltage rise.

The function of capacitor C6 is to provide greater circuit response to high-frequency line variations. Diodes CR5 and CR6 prevent the base of transistor Q8 from going more positive than about 1 volt; this insures


SECTION C
SECTION A
SECTION B
R1 1K
R2 1K
R3 1K
R4 910
R5 560
R6 1K
R7 75
R8 1K
Q1
Q2
Q3
Q9
C1 22 UF
J2
C
-3V
J1
A
B
C
CB1
1 AMP FUSE
T1
J8
DS1
CR7
CR1
CR2
CR8
CR3
L1
R25 1K
C7 5600
C2 47 UF
R10 2.7 1W
Q10
R14 5.6K
R16 15 3W
R17 9.1K
VR1
R15 10K
Q5
Q4
R19 1.2K
Q6
R20 150 3W
C4 22 UF
CR4
R23 820
R24 750
R26 250
A
-12V
C5 22 UF
R11 2.7 1W
R12 27 3W
Q11
R13 2.2K
VR2
CR11
C8 1600 UF
C6 1 UF
R21 750
R22 3K
Q7
Q8
R18 1.2K
CR5
CR6
B
+3V

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE ½W.

Figure 6-46. Typical solid-state power supply.

adequate circuit operation when it is initially turned on. Diode CR11 prevents the +3-volt output line from going negative. Capacitor C5 provides filtering of high-frequency noise on the +3-volt line. Resistor R12 provides a short-circuit current limit if the output +3-volt line is shorted. Zener diode VR2 provides the reference voltage for the regulator circuit.

The third power supply (shown in section C of fig. 6-46) provides −3 volts. This circuit employs a shunt regulator circuit consisting of transistors Q3 and Q9. This particular circuit arrangement does not need a filter circuit, because it derives voltage from the −12-volt and +3-volt supplies. The base voltage of transistor Q1 is set at −3 volts by the voltage dividers R1 and R2, which are between −12 volts and ground. Transistors Q1 and Q2 form a differential amplifier. With the emitter voltage of Q1 and Q2 at the same potential, the base voltage of Q2 will be −3 volts, which is the same potential as the base of Q1. If the −3-volt line voltage were to go more positive, transistor Q2 would conduct more, and the voltage at the common emitter of Q1 and Q2 would rise, causing Q1 to conduct less and its collector voltage to increase. This increase in Q1's collector voltage would be detected at the base of Q3; therefore, Q3 would conduct less, and the voltage drop across it would increase. The increase in voltage across Q3 would cause the output line voltage to become more negative. The voltage at the base of Q9 would also go more positive, causing it to conduct less. This would allow the −3-volt line to go more negative, thereby compensating for the initial increase in voltage.

The function of capacitor C1 is to filter the high-frequency noise on the −3-volt line. Resistor R6 provides a light load between the −3-volt and −12-volt lines. The current capacity of this −3-volt supply is adequate, because it is the type of supply that is normally used to supply a bias or reference voltage for clamping logic circuit outputs (in this case, negative logic). In this particular circuit, the clamp current actually flows from the −3-volt line through the clamping diode and resistor of the load to the −12-volt supply; therefore, the −12-volt supply msut handle the current.

Exercises (484):

For exercises 1-4, refer to figure 6-46 if necessary.

1. What is the purpose of R10, CR3, and C2?

2. If the voltage of the −12-volt line goes more positive, what will happen to the voltage drop across Q10?

3. What is the purpose of R12?

4. What type of regulating circuit is used in the −3-volt portion of the power supply?

485. Specify the causes of certain power supply malfunctions, state testing procedures, and give the intent of a cited circuit malfunction.

Power Supply Malfunctions. Regardless of whether you are troubleshooting a solid-state or electron-tube power supply, the troubleshooting procedures are practically the same with regard to circuitry. We will confine our analysis here to several common troubles and symptoms that may be caused by defective solid-state devices. We will also briefly discuss the checking of these devices and consider some matters pertinent to their replacement—including circuit modifications and the reason for them.

Symptoms and troubles. Often, the malfunction of a power supply is the fault of the rectifying device. Crystal and metallic rectifier diodes fail, as do electron-tube diodes. Also, certain faults can be attributed directly to the solid-state rectifier. They are (1) open-circuited rectifier, (2) short-circuited rectifier, (3) high forward-voltage drop, (4) high leakage current, and (5) overheated rectifier. You can readily detect the symptoms associated with these faults, since they cause obvious and sometimes serious trouble.

Fault 1, an open-circuited rectifier, causes a lower DC output. If the rectifir nnuiinit is a full-wave or polyphase thpn the DC output would be reduced when one rectifier is open circuited. If it is a single-phase half-wave rectifier, there will be no DC output.

The symptoms just mentioned for the open-circuited rectifier (fault 1) are also the same for fault 2, a short-circuited rectifier. In addition, there will be excessive heating and AC will appear at the output. Unless short-circuit protection is built into the power supply, other circuit components can be permanently damaged.

Either fault 3, a high-forward-voltage drop, or fault 4, a high-leakage current, will cause lowered DC output and increase heating. A high forward-voltage drop is caused by an increased forward resistance; whereas a high leakage current is caused by a decreased reverse resistance. Whichever of these faults occurs, the rectification ratio is reduced accordingly and so is the efficiency of the rectifier.

Fault 5, an overheated rectifier may be caused by faults 2, 3, or 4, which we have mentioned previously, but it also can be caused by excessive loading or inadequate cooling. Regardless of the cause, however, the rectifier that is heated beyond its safe limits will either be short-lived or be completely destroyed. When the source of the trouble is the rectifier itself, your replacement of the rectifier will return the circuit to normal operation. However, when the overheating is the result of loading or improper heat dissipation, the trouble will persist after you have replaced the rectifier unless you take corrective measures to insure proper loading and cooling.

Looking at another area of possible malfunction, when a power supply has a regulator unit, a defective solid-state device (thermistor, zener diode, transistor, etc.) may be the source of trouble. The symptoms here can range from an increased or reduced DC output (regulated or not) to no DC output. Why? Because these symptoms and troubles are not only dependent upon the complexity of the circuitry, they are dependent upon the type of regulator unit employed as well. We cannot, therefore, say much on this subject in general. Consequently, for any particular faulty unit you must deal with, you will have to depend upon your basic knowledges and reasoning ability to determine whether or not a solid-state device could be at fault. If you think that is where the fault is, you will have to test the suspected device.

Checking and testing. You can detect symptoms in a number of ways. For example, you will discover much overheating readily by the smoke or odor it produces. A faulty selenium rectifier, for instance, smells like rotten eggs. You can find abnormal voltages and currents quickly by taking voltmeter and ammeter readings. You can see ripple in the output using an oscilloscope; perhaps you will even *hear* it in an audio system. The frequency of the ripple may reveal the trouble; for example, a 60-Hz ripple from a single-phase full-wave unit indicates that you are getting only half-wave rectification. If so, more likely than not, a rectifier is defective.

You can also detect some circuit troubles by making a visual inspection. To begin with, broken connections and damaged components are usually very obvious. So is the discoloration of circuit components often caused by overheating. You may, for example, see dark spots on the plates of a faulty metallic rectifier. Such a dark spot indicates a physical rupture of the barrier layer caused by high temperature. If you find that the spot is small, probably no permanent damage has occurred, because the plates of the metallic rectifier are self-healing. Nevertheless, the effective rectifying area is reduced, and overheating will ultimately cause failure. Therefore, although a spot covering less than 20 percent of the plate area is considered within allowable limits, replacement of the rectifier is recommended whenever spotting appears. But what if you find a faulty metallic rectifier showing burned spots around its contact washer and the surrounding area? Answer: This is likely a result of poor contact with the front electrode. Suppose, too, that you see solder-like blotches beneath a rectifier stack. These are also caused by excessive heating. In this case, the alloy of which the rectifier is made has melted and run off the bottom edge of the cells. From all of these examples, it is clear that you can frequently detect faulty metallic rectifiers by visual means. But you cannot do this for crystal rectifiers; you have to test to check their electrical characteristics.

You will find checking with an ohmmeter is an easy and practical way to test a crystal or metallic rectifier to determine whether it is open or shorted. A high resistance (several thousand ohms) measured in both directions indicates that the rectifier is open; whereas a relatively low resistance (a few hundred ohms) measured in both directions indicates that it is shorted. A good rectifier has a low forward resistance and a high reverse resistance. Since, however, an ohmmeter applies voltage to the rectifier under test, it is not a reliable instrument for testing quality. Remember that the forward resistance of a solid-state rectifier is not linear but varies as a function of the applied voltage. Therefore, you must check the rectifier under rated conditions to obtain a conclusive indication of its quality.

Many test sets are available to test solid-state devices. Each set has instructions provided with it to enable you to test properly. Solid-state devices are identified by prefix letter(s) and a number on the device. Common prefixes are as follows: IN for crystal diodes, MR or SR for metallic rectifiers, Z (also HZ or MZ) for zener diodes, and 2N for transistors. Once you've identified the device, you can find its specifications in an applicable TO or TM. Then, knowing the rated parameters, you can tell from the readings of the test set whether the device is substandard.

Be warned: It is quite possible that the solid-state device may test good and yet still be the source of trouble. What should you do then? Answer: The only sure way to find out, is for you to replace it. As for electron tubes, you can use an identical device—one that is known to operate properly—in place of the questionable one. Note this, too: Normally, the time required to change a tube is small when compared to the time required to replace a defective solid-state device.

Replacements. You should always replace a faulty circuit component with one exactly like it. When this is not possible, *and you have been authorized to substitute an unlike item*, it might be necessary for you to make some circuit modifications to protect the circuit or device itself.

Since solid-state devices can be damaged instantly and are affected adversely by overheating, a casual approach to the replacement of circuit components can be costly. So give particular attention to inserting limiting resistors when you find this necessary in order to prevent excess current flow or surges. For example, if you use a large input-filter capacitor in place of a defective one, turn-on and recurrent surge currents may increase beyond rated limits.

This is where stacking and paralleling solid-state rectifiers is a common practice—one which makes it possible to rectify high voltages and high currents, respectively. You should understand that rectifiers can be series-connected in all of the rectifier circuits discussed and illustrated in this chapter. The rated PIV of the stack is the sum of the rated PIVs of the individual rectifiers. To get a desired current-handling capacity, you can use crystal or metallic rectifiers in parallel. You can use a combination of series or parallel rectifiers to replace a rectifier of almost any rating.

Exercises (485):

1. Situation: The output of a DC power supply is low and the temperature of the power supply is normal. What is the most probable cause?

2. Two faults attributed directly to the solid-state rectifier are (a) high forward-voltage drop and (b) high leakage current. What is the cause of each?

3. Concerning dark spots on the plates of a faulty metallic rectifier, (a) what does such a spot indicate, (b) what is the allowable limit for such a spot, and (c) what is recommended when spotting occurs?

4. Situation: A very high resistance is measured in both directions across a metallic rectifier. What is the trouble?

5. What is the rated peak-inverse voltage of a stack of rectifiers?

CHAPTER 7

Oscilloscope Measurements

HAVE YOU OBSERVED a senior technician or maintenance specialist troubleshooting a stubborn system problem? What is the first thing they did? They started by checking all the indications provided by the built-in test equipment. They then grabbed an oscilloscope and headed toward an equipment rack or cabinet. The oscilloscope is probably the most used, most versatile piece of test equipment.

7-1. Basic Voltage Measurements

You can measure almost anything with the two-dimensional display of an oscilloscope. In most applications, voltage is displayed on the vertical axis in reference to time on the horizontal axis. Using special probes or transducers, you can measure current or nonelectrical conditions such as sound, pressure, light, or heat.

A scope display presents more information faster than other test equipment. For example, from the display you can determine if the signal is AC or DC, how much noise is on the signal, the voltage level and frequency of the signal, and other characteristics in relation to voltage and time. Making oscilloscope measurements becomes second nature to the trained technician, and it can be for you too.

485a. (497—for CE feedback reference only). State the factors involved in measuring AC peak-to-peak voltage with an oscilloscope and solve a given problem concerning peak-to-peak voltage measurements.

Peak-to-Peak AC Voltage Measurements. The following procedure is used to measure peak-to-peak voltage. After determining the peak-to-peak value, you can use a mathematical process to determine the peak-to-peak value, you can use a mathematical process to determine peak or RMS values. (Peak-to-peak divided by 2 equals the peak value, and peak value multiplied by 0.707 will equal the RMS value.) To find the peak-to-peak signal with an oscilloscope:

(1) Connect the signal to be measured to either input connector.

(2) Set the MODE switch to display the channel selected in step 1.

(3) Set the volts/div switch to display about 5 divisions of waveform.

(4) Set the AC–GND–DC switch to AC if the signal is above 16 Hz or to DC if the signal is below 16 Hz.

(5) Set the triggering controls to obtain a stable sweep and the time/div switch to obtain several cycles of waveform.

(6) Turn the vertical and horizontal position controls so that the waveform lower extremity coincides with the lowest horizontal graticule line and that one of the peaks is on or near the vertical centerline, as shown in figure 7-1.

(7) Measure the divisions of vertical deflection.

NOTE: Make sure that the variable volts/div control is in the CAL position.

From this point on the measurement becomes a mathematical problem.

The formula to use is:

$$\frac{\text{volts}}{\text{peak-to-peak}} = \frac{\text{vertical}}{\text{deflection}} \times \frac{\text{volts/div}}{\text{setting}} \times \text{probe attenuation factor}$$

Assuming that the 10X probe is used, that the volts/div switch is set to .5, and reading the waveform illustrated in figure 7-1 vertical divisions, we would have the following solution:

$$\frac{\text{Volts}}{\text{Peak-to-peak}} = 4.6 \times 0.5 \times 10 = 23 \text{ volts}$$

Exercises (485a):

1. What are the factors involved in measuring AC peak-to-peak voltage?

2. If the vertical deflection is 4.8 divisions, the volts/div switch is set in the 0.2 position, and a 10X probe is being used, what is the peak-to-peak value of the AC signal being measured?

485b. (498—for CE feedback reference only). State the factors involved when measuring instantaneous DC voltage and solve a given problem using these factors.

Instantaneous DC Voltage Measurements. With an

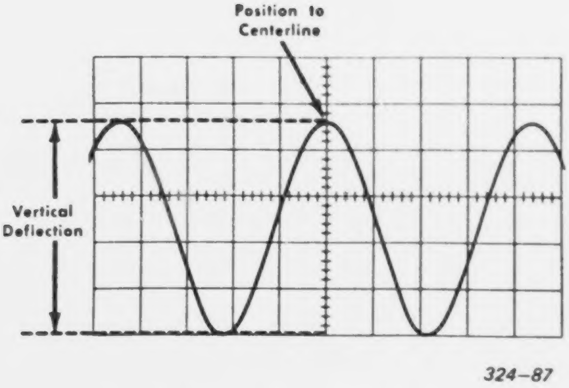


Figure 7–1. Peak-to-peak voltage measurements.

oscilloscope you can measure instantaneous voltages with respect to ground or some other reference level. The reference level chosen is determined by the setting of the AC–GND–DC switch. A second factor concerns the polarity of the signal with regard to the reference level. A negative-going signal is measured from the top of the graticule. The procedure for measuring instantaneous DC voltage is as follows:

(1) Connect the signal to be measured to either input connector.

(2) Set the MODE switch to display the channel selected in step 1.

(3) Set the volts/div switch to display about 5 divisions of waveform.

(4) Set the AC–GND–DC switch to GND.

(5) Set the A sweep mode to AUTO TRIG.

(6) Using the vertical position control, position the trace to the bottom of the graticule for a positive-going signal or the top of the graticule for a negative-going signal. For example, the reference line of the graticule illustrated in figure 7-2 is the bottom line. Once you establish the reference line, do not move the vertical position control.

(7) Set the AC–GND–DC switch to DC.

(8) Set the A triggering controls to obtain a stable sweep.

(9) Set the time/div switch to display the desired waveform.

(10) Measure the distance from the reference line to that point of the display that is to be measured. On figure 7-2 the point we have chosen to measure is called point A. The number of divisions indicated is 4.6. Since the signal was measured from the bottom of the graticule, the polarity is positive. If the reference line were at the top of the graticule, the polarity would be negative (−1).

As in the first measurement, the rest of the measurement is a mathematical problem. This measurement deals with vertical deflection, polarity, volts/div setting, and probe attenuation factor. Note that in both measurements we have mentioned probe attenuation factor. In some measurements which have no attenuation factor, plain leads are used. In this case the probe attenuation factor is not included in the voltage calculation formulas. The formula for the computation of the instantaneous voltage is:

$$\begin{array}{c}\text{volts}\\\text{peak-to-peak}\end{array} = \begin{array}{c}\text{vertical}\\\text{deflection}\end{array} \times \begin{array}{c}\text{volts/div}\\\text{setting}\end{array} \times \begin{array}{c}\text{probe}\\\text{attenuation}\\\text{factor}\end{array}$$

Assuming that we have a vertical measurement of 4.6 divisions of point A in figure 7-2, a volts/div setting of 2, and are not using an attenuation-type probe (polarity is positive), the formula is:

$$\begin{array}{l}\text{instantaneous}\\\text{voltage at point A}\end{array} = 4.6 \times (+1) \times 2 = +9.2 \text{ volts}$$

Exercises (485b):

1. State the factors involved in measuring instantaneous DC voltage.

2. When measuring instantaneous DC voltage, the following values are noted:

Vertical deflection	4.2 divisions
Polarity	negative
volts/div	0.1
Probe attenuation	10X

What is the value of the instantaneous voltage measured?

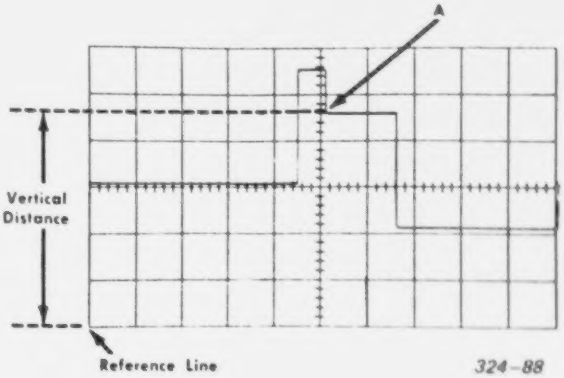


Figure 7–2. Instantaneous DC voltage measurements.

7-2. Basic Techniques of Waveform Measurement Using an Oscilloscope

NOTE: For objectives 486 through 496, study objectives 001 through 011 in Module, *Basic Techniques of Waveform Measurement Using an Oscilloscope*, which accompanies this volume. When you complete Module 10012, return to the text.

MODULE 10012

CDC 30554-3 Objectives	*Module 10012 Objectives*
486	001
487	002
488	003
489	004
490	005
491	006
492	007
493	008
494	009
495	010
496	011

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TO 31-1-141-6, *Basic Electronics Technology and Testing Practices, Basic Computer Programming Techniques.*

TO 31-1-141-9, *Basic Electronics Technology and Testing Practices, Testing Techniques and Practices.*

NOTE: None of the items listed in the bibliography are available through ECI. If you cannot borrow them from local sources, such as your base library or local library, you may request one item at a time on a loan basis from the AU Library, Maxwell AFB, AL 36112, ATTN: ECI Bibliographic Assistant. However, the AU Library generally lends only *books* and a limited number of AFMs. TOs, classified publications, and other types of publications are *not* available. Refer to current indexes for the latest revisions of and changes to the official publications listed in the bibliography.

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Answers for Exercises

CHAPTER 1

Reference:

400 - 1. They are computer programs used in both preventive and corrective maintenance tests to detect circuit failures rapidly and to discover failures that may occur only under particular operating conditions.

400 - 2. First-order reliability programs check the operation of assemblies or circuit groups, such as registers and counters. Second-order programs are designed to check basic circuits and components.

400 - 3. Increasing area, decreasing area, overlapping area, and large area checks.

400 - 4. A check that initially tests a small number of circuits. If all tested circuits are operating properly, successive checks are run in which progressively greater numbers of circuits are added.

400 - 5. A decreasing area check.

400 - 6. Overlapping area.

400 - 7. A printed record of the contents of various computer registers to let you follow maintenance program operations.

401 - 1. A specified number of bits within a computer representing an instruction, operation, or other data.

401 - 2. It contains the data used in a computation by the computer.

401 - 3. The address portion and the command portion.

401 - 4. The capacity of the computer memory.

402 - 1. A simplified code representing a computer instruction used by the programmer, and one which is later changed to the binary form to be used by the computer.

402 - 2. The mnemonic code is more convenient and efficient for the people using computer instructions.

402 - 3. Jump, conditional jump, and unconditional jump.

402 - 4. The transfer instruction is used to duplicate a word in another section of the computer.

402 - 5. The shift instruction establishes the position of the binary point.

403 - 1. The process of representing any number by selecting an appropriate binary point.

403 - 2. The number of positions between the computer's binary point and the assumed binary point.

403 - 3. That the assumed binary point and the computer's binary point are in the same location.

403 - 4. A fractional number.

403 - 5. When the number of operands required is very large or the range of the operands is not predictable.

404 - 1. An instruction in the program that causes a section of that program to be repeated with its modifying elements.

404 - 2. By performing such tasks as sorting or tabulating, using repeated program steps through the use of program loops.

404 - 3. The modified address of a program loop.

405 - 1. The symbol with "step address counter" printed within it.

405 - 2. Symbols *c* and *f*.

405 - 3. The circle symbols with 1 and 2 within them.

405 - 4. A description or statement of the function to be performed.

406 - 1. Top-level and detailed.

406 - 2. High-level; low-level.

406 - 3. Symbols and instructions.

406 - 4. Low-level.

406 - 5. They should be available at levels low enough to implement all the levels used.

407 - 1. A program designed to be operated in conjunction with (or by) some type of control program.

407 - 2. A package of control and helper routines that facilitates the loading and operation of the maintenance program routines.

407 - 3. Interrupts, manual intervention, and printouts.

407 - 4. Program heading, results of program run, error information, and indicated repair statement.

407 - 5. Because the uniformity of the data format found in each of the four essential items required on the error printout varies from system to system.

CHAPTER 2

408 - 1. The accomplishment or preliminary procedures which are not normally repeated once the system is operating.

408 - 2. In the appropriate service manual or -2 technical order.

408 - 3. Insure proper grounding of the equipment.

408 - 4. In the appropriate service manual or -2 technical order.

409 - 1. a. To identify a failing function or subfunction.
b. To identify correct or incorrect data flow.

409 - 2. Operation or failure of the circuits must be related directly to the remote indicator.

409 - 3. By grouping its lamps to provide a display which, when read, reveals that data is stored.

409 - 4. They portray operations of counters, information in memory, fault indications, status of each part of a system, and status of an entire system.

409 - 5. Service manuals (-2 series) and circuits and diagrams manuals (-3 series).

409 - 6. By the use of metering circuits and alarm lamps.

409 - 7. Batteries and battery charging systems.

409 - 8. Any three of these: (1) sudden, total failure; (2) shortened life; (3) temporary change in value; and (4) permanent physical or chemical change leading to total failure prematurely.

409 - 9. As a good conductor, it can act as a low resistance path, can cause insulator breakdown or circuit shorts, and can lead to the growth of fungus and corrosion.

409 - 10. A device used to measure humidity.

410 - 1. It provides a permanent termination of wires for a

communications system and temporary cross-connections for equipment inputs and outputs.
410 - 2. Also a frame positioned between the MDF and the technical control patching facilities, it is described as a distributing frame on which subscriber line multiples appear on one side and the subscriber line circuit on the other for interconnection.
410 - 3. Wire connections for the unencrypted side of cryptographic devices, battery isolation relays, red circuit control, switching, and monitoring devices are made on this same portion.
410 - 4. (a) "tie points," (b) toward the rear, and (c) to make wiring and soldering easier.
410 - 5. Permanent wiring that connects such equipment as outside cables; multiplexing, teletyping, and COMSEC equipment; and patch panels, battery, and ground taps, which do not change, to the frame or the bottom of the horizontal boards.
410 - 6. Temporary wiring cross-connects between outside cables and equipment that is subject to reconfiguration or change.

411 - 1. (1) 45A2A1XA22-7
(2) 45A2A1XA13-16/4
(3) 45A2A1XA12-17/6
(4) 45A2A1XA14-19/6
(5) 45A2J2/A1P202-J
(6) 45A1J17-6
(7) W6060
(8) 46A1A14J2-6
(9) 46A2A1P3/A2J2-G
(10) 46A2A2XA2-16/6
(11) 46A2A2XA1-8/6
(12) 46A1A10TB2-6
(13) 46A1A10
(14) 46A1A10TB1-1
(15) V1-3
411 - 2. Chassis
(1) 45A2J2/A1P202-J
(2) 46A2A2J2-G
(3) 46A1A10TB2-3
(4) 46A1A10TB1-1
Cabinets
(1) 45A1A1J17-6
(2) 46A1A14J2-6

412 - 1. RM3 to RM6:
J611015 - J629018/015
412 - 2. RM3 to TP1:
J611015 - J613014/018 - J623017
412 - 3. RM3 to SIF:
in out
J611015 - J613005/004 - J614002/010 - J622014/013 - J/P602101 - J/P800119 - cable 5622 - J/P403703007 - J/P503405001 - J50332053/050 - J503103004 (HFF-1).
412 - 4. RM3 to SM-137:
J611015 - J616005/004 - J/P602119 - J/P980112 - Cable 5623 - J/P4960 - J/P4682117 - J4693018.
412 - 5. RM3 to assemblies in bay 600:
J611015 - J611002/003 - J/P602113 - CP642; branch A: J/P701109 - A701; branch B: CP682; branch A: J/P641109 - A641; branch B: J/P681109 - A681.
412 - 6. RM3 to bay 800/900:
J611015 - J611002/003 - J/P602114 - CP841; branch A: J/P842104 - J844018 and J846016; branch B: J/P902105 - J884002 and 018, and J886016, and J904002 and 018, and J096016.

413 - 1. a. J6, jack 6 at console.
b. Pin FF in J6.
c. Cable W59.
d. A2-A3-J3-9 (MDF).
e. A2-A2-J6-19 (MDF).
f. Cable W11.
g. Pin W on J1.
h. Jack J1 at memory unit.
413 - 2. a. J5 at memory unit.
b. Pin HH on J5.
c. Cable W13.
d. A2-A2-J5-20 (MDF).
e. A3-A3-J3-11 (MDF).
f. Cable W64.
g. Pin A on J6.
h. J6 at the console.

414 - 1. To clean and service equipment to insure that optimum operation is obtained at all times.
414 - 2. A 28-day routine cycle.
414 - 3. The tasks related to equipment moving or repositioning, corrosion control, painting, lettering, and equipment or facility cleaning.
414 - 4. a. The test equipment required.
b. The materials required.
c. The procedure to follow.
414 - 5. The PMI schedule from Maintenance Control identifies the equipment and from this information the workcard set and cards.
414 - 6. The inspection cycle, the power requirements, the equipment serviceability during PMI, the number of people required to perform the routine, the average time required, and the specialist requirements.

415 - 1. Discolored, burned, or cracked resistors and capacitors; loose connections; loose mounting; faulty tubes; sluggish or dirty relays; overheated transformers and motor housings; and defective insulators.
415 - 2. By the temperature of the element after it has been operating for a while.
415 - 3. First, remove dust, dirt, and foreign particles with a vacuum cleaner or compressed air. Next, use a lintless cloth and an *approved* cleaning solvent to remove any remaining dirt and grease spots.
415 - 4. Only use trichloroethylene in a well-ventilated area. Do *not* use it on thermoplastics, "doped" coils, or natural rubber.
415 - 5. In the applicable equipment technical orders.

416 - 1. Meters; the oscilloscope; CTR display equipment, printouts, lamps, audio alarms, and internal tests; and visual examinations of mechanical assemblies.
416 - 2. Line data, power supplies, and reference voltages.
416 - 3. An oscilloscope.
416 - 4. Pulse width, signal amplitude, linearity of ramp signals and sine waves, proper operating voltage levels, PRT, phase, polarity, proper waveforms (such as ramps, timing, deflection intensity, and generator outputs), ringing (noise), and data content.
416 - 5. To do this: Identify the points to measure and the controls to adjust, measure the input level of the radar returns at various ranges, and measure and adjust the circuit output for a desired level and phase of polarity.
416 - 6. To verify signal amplitude.
416 - 7. With an oscilloscope.
416 - 8. Include here: The use of CRT voltage controls for intensity, focus, positioning, and astigmatism; the symmetry and linearity of range marks; the callup operations of the console; and the printing capability of the digital display by the use of the test pattern. If complete, this test also exercises all character generators.
416 - 9. Meters or lamps.
416 - 10. Busy bit, sync group, or no message characters.
416 - 11. Proper (or improper) orientation of tapes, operation of servos, takeup reel tension, and photolamp illumination or vacuum pump operation.

417 - 1. By inclusion of high-gain amplifiers inserted at repeater stations every 6 or 7 miles.
417 - 2. The degree of interference or absence of interference in a transmission line.
417 - 3. A unit of power ratio.
417 - 4. At +6 to −25 dB.

418 - 1. Your answer should include any three of these purposes:
  a. To alter the bias voltage to a circuit.
  b. To alter the frequency of a circuit.
  c. To shift a frequency.
  d. To attenuate or amplify a signal.
  e. To limit or eliminate distortion.
418 - 2. The tabular-type, with an adjustable core, and the button-type, with a variable rotor.
418 - 3. Ceramic, mica, glass, piston, polystyrene, teflon, and air.
418 - 4. Linear.
418 - 5. The mechanical nature of each component limits its life cycle.
418 - 6. Rheostats and potentiometers.
418 - 7. Rheostat.
418 - 8. The contact attached to the pickoff terminal usually rests on a carbon resistance element. Each end of the element is in series with the source voltage or current. The position of the contact on the carbon resistance dictates the pickoff voltage or current.
418 - 9. An audible click and a pin to stop rotation.
418 - 10. Linear deposits and nonlinear (logarithmic) deposits.

419 - 1. Balancing.
419 - 2. By disassemblying the meter and repositioning weights. This is accomplished by the PME laboratory.
419 - 3. Zeroing or centering.
419 - 4. By adjusting a potentiometer in the meter circuit.
419 - 5. Equal to the balancing or applied voltage.

420 - 1. To (1) alter the gain ratio of the circuit, (2) control the pulse duration, or (3) act as a phase-shifting device.
420 - 2. By incorporating a high-gain amplifier.
420 - 3. By removing the feedback resistor and installing a variable capacitor or a resistor.
420 - 4. That waveform will become a sawtooth.
420 - 5. By control of the RC time constant with a variable capacitor or resistor.
420 - 6. It (a) controls the conduction time of this circuit and (b) delays the completion of the rectangular output waveform.

421 - 1. By using an adjustment potentiometer on the power supply.
421 - 2. Silicon-controlled rectifiers, zener diodes thermistors, and thyratron semiconductor devices.
421 - 3. By installing it remote for the power supply, with one leg of the resistance (carbon or wire) tied to ground and the other leg left untied (infinity). The wiper is tied to the power supply.

422 - 1. The CMC.
422 - 2. Free-running oscillators, one-shot MVs, blocking oscillators, time-sharing generators, and AGL generators.
422 - 3. Frequency adjustment and duty cycle adjustment.

423 - 1. Drums, tapes, disks, and delay line (magnetrorestrictive).
423 - 2. The heads are placed a specified distance above the recording surface on drums and disks. The tape heads are installed as per TO instructions and the tape tension and position are controlled by variable components.
423 - 3. A typical adjustment requires that an output voltage be measured at 125 to 150 millivolts peak to peak. The steps to arrive at this voltage output are such that the head is lowered to the stopped drum surface and then raised until 75 percent of the voltage waveform is displayed on the scope.
423 - 4. The driven capstan, vacuum pump motors, and rewind motors.
423 - 5. First, an oscilloscope using two traces may be used. On one trace the input pulse is shown; on the other trace the output pulse is shown. Since these are the same pulse, the measurement of time between input and output reveals the delay storage time.
423 - 6. Read/write amplifiers.
423 - 7. On the read/write amplifier units.
423 - 8. Horizontal and vertical width of each character, horizontal and vertical position of all the characters, and horizontal and vertical height of each character.
423 - 9. (a) The character height pot. (b) By the allowable parameter of the decoder.

424 - 1. Gate amplitudes, gate shaping (no overshoot or undershoot), and video levels.
424 - 2. Voltage output and ripple filtering.

425 - 1. Electronic and mechanical actions working together to produce a product.
425 - 2. To have all circuitry so function that a change voltage input causes a rotation to a new null. Further, once at the null, the unit rests and does not hunt.
425 - 3. In the input circuitry (transformer).
425 - 4. Yes. A change voltage is derived from some source and, after adjustment, must be fed to the servo for repositioning.
425 - 5. These are: the input transformer, the amplifier chain, the drive motor, the three pots, reference voltages, and the GAMI and LDRI boards.
425 - 6. An ohmmeter, a DC meter, an AC (RMS) meter, and an oscilloscope.
425 - 7. Digital-to-analog conversion.
425 - 8. (a) The alignment is performed in the off-line test mode.
  (b) Selected switch settings are used to provide X and Y range data to the D/A converters.
  (c) Gain ratios of related functional amplifier chains are to be found in unity.
  (d) Resolver B2 (part of the azimuth servo) must be properly oriented.
425 - 9. *Step 1:* Verification of digital data.
  Step 2: Verification of unity gain from the amplifier chain for both X and Y measured at AZA4XA7-6 and XA8-6 of the drive boards, respectively.
  Step 3: Verification that the output from R3 measured A2A2XA8-4 is equal to the output from the amplifier chain.
425 - 10 First, to adjust the clearance between the space pawl and the carriage rack teeth when the armature is energized. Second, to position the space magnet and armature when the armature is energized. Third, to adjust the clearance between the stop plate and the space pawl when the armature is energized.
425 - 11. All three require an energized coil.
425 - 12. a. Depressing space on the keyboard.
  b. Automatic sensing of the end-of-print cycle.
425 - 13. Alignment of interrelated assemblies is as follows:
  a. Space armature and shaft end play (parallel).
  b. Space bail (serial).
  c. Space pawl rack clearance (serial).
  d. Space pawl stop plate (serial).
  e. Space magnet (serial).
  f. Space pawl clearance (serial).
425 - 14. This is: (a) verification of input data, completion of prerequisite spacing alignments, and power; and (b) alignment instructions which identify each screw to be turned, loosened, and tightened, and the final securing of screws.

CHAPTER 3

426 - 1. Because the unit numbering method uses only one basic reference symbol for each single element in an entire system.
426 - 2. The 102d resistor in the assembly.
426 - 3. Unit 2, assembly A1, tube V2.
426 - 4. (a) In PMIs (TO series -6WC), and (b) when specifying a task to be performed on a piece of equipment.
426 - 5. Areas that are not assemblies.
426 - 6. Left to right, top to bottom, front to back.
426 - 7. 12A9.
426 - 8. Your answer should include any two of these: (1) It will help you in signal tracing and in locating the defective part in troubleshooting. (2) It will tell you exactly which control to turn or to adjust when you perform preventive maintenance routines. (3) It will further help you analyze a problem in logic, because the reference designation is

included on the logic sheet and clearly identifies the area you are examining.

427 - 1. -4.
427 - 2. 39A6TB1 through 39A6TB6.
427 - 3. 39-203859-01.

428 - 1. Resistance in series is increased and resistance in the shunt (parallel) is decreased.
428 - 2. Series must be increased.
428 - 3. It blocks any DC that may be present when reading AC voltage through preventing erroneous readings and possible damage to the meter.
428 - 4. In the ohmmeter and milliameter circuits.
428 - 5. Series-type ohmmeter.

429 - 1. True.
429 - 2. It is portable, versatile, free from calibration errors, and does not need external power.
429 - 3. Its loading characteristics, short scale, and danger of damage to meter movement as a result of negligence.
429 - 4. The movement might be damaged by the relatively high current of ohm meter operation.

430 - 1. The current drain on the internal battery is heaviest on this range.
430 - 2. By keeping your fingers away from the tips of the test probe and away from the pigtails or terminal lugs of the resistance being measured.
430 - 3. False.
430 - 4. Your answer should be one of these advantages of the TRVM over the VTVM: Because transistors require no heater current and draw so little collector current that battery operation is very practical, the TRVM is free of AC pickup, requires no warmup time. and is very compact.

431 - 1. On the potentiometric principle.
431 - 2. In the VTVM position.
431 - 3. The highest range for the range switch and VTVM for the null switch.
431 - 4. The range of voltages to be measured.
431 - 5. The input voltage.
431 - 6. Its ability to be used as a megohmmeter for rapidly measuring high resistance. They range from 1 to 250,000 megohms.
431 - 7. Increase the setting on the null switch.
431 - 8. 100.

432 - 1. A compact, accurate, multifunctional device with a rapid response.
432 - 2. A blocking capacitor probe tip and a tee-connector probe tip for coaxial line measurement.

433 - 1. To compare an unknown frequency or unknown time interval with a known frequency or known time interval.
433 - 2. The signal gate.
433 - 3. The time-base selector.
433 - 4. The pulses received during the interval between manual START and manual STOP.
433 - 5. A ratio measurement.
433 - 6. The amount of time between one point on a waveform to another point on the same waveform. The output is displayed in time (seconds, milliseconds, etc.).
433 - 7. To extend the range of the counter by a factor of 10.
433 - 8. By adding the reference frequency (from the harmonic selector) to the counter display.
433 - 9. Instantaneous direct readings of unknown microwave inputs.

434 - 1. According to frequency.
434 - 2. Audiofrequency and radiofrequency.
434 - 3. The shape of the output wave: i.e., sine-wave or square-wave generators.

435 - 1. Connect the probe clip to the power supply of the circuit under test. Then place the probe tip at the point to be tested.
435 - 2. The ability to monitor all pins of an IC clip and to provide indications faster than a logic probe when checking static or slowly changing signals.
435 - 3. Connect the pulser leads to the power supply of the circuit under test. Then touch the pulser probe to the point of the circuit to be activated and depress the pulse button.

436 - 1. The analyzer generates a signal or binary word, which is then processed by the equipment and returned to the analyzer. There it is compared to the original signal or binary word bit for bit.
436 - 2. To perform a bench test of a suspected malfunctioning equipment drawer or shelf assembly.
436 - 3. The test set control circuits provide the required control and timing signals that cause the signal generator to activate the drawer under test. The drawer outputs are then checked at the test points with auxiliary test equipment and compared with prescribed performance standards.
436 - 4. The use of variations in external wiring to connect various components on the card to form the required circuits.
436 - 5. By simulating operating conditions for the card under test and comparing circuit operation to a good card or standards specified by the test procedure.

437 - 1.
  a. Avoid mechanical shock.
  b. Avoid exposure to strong magnetic fields.
  c. Avoid excessive current.
437 - 2.
  a. Avoid contacting the coils of wattmeters, frequency meters, and power meters, because they may carry excessive current even when the meter point is on scale.
  b. Never short-circuit the secondaries of current transformers when the primary is energized.
  c. Never short-circuit the secondaries of potential transformers when the primary is energized.
  d. Insure that meters in motor circuits can handle the motor starting current, which may be as high as six or eight times normal running currents.
  e. Never leave an instrument connected with its pointer off scale or deflected in the wrong direction.
  f. Never attempt to measure the internal resistance of a meter movement with an ohmmeter, as the movement may be damaged by the current required to operate the ohmmeter.
  g. Never advance the intensity control of an oscilloscope to a position which causes an excessively bright spot on the screen or permits a sharply focused spot to remain stationary for any length of time.
  h. When checking electron tubes with a tube tester, always perform the interelement short test first. If the tube is shorted, make no further tests.
  i. Before measuring resistance, always discharge capacitors in the circuit to be tested. Note and record any points not having bleeder resistors or discharge paths for capacitors.
  j. Always disconnect voltmeters from field circuits or other highly inductive circuits before opening the circuit.
437 - 3. Coming into contact with live terminals or test leads or accidentally throwing the equipment to the deck, thereby perhaps entangling personnel in leads or cords and causing severe or fatal shocks. Also, if the situation is such that a potential difference exists between the metal cases of two or more instruments, this potential may be enough to produce harmful shocks.

438 - 1. Rough handling, moisture, and dust.
438 - 2. By using the build-in heaters.

439 - 1. To anticipate and to seek out possible troubles which can lead to test equipment breakdown.
439 - 2. It has the tools, standards, parts, and equipment to do this work.
439 - 3. Only to the extent that the maintenance you perform will

still permit that equipment to function accurately and reliably.

439 - 4. Normally, it is a PMEL responsibility.

439 - 5. The using organization and the base PMEL.

439 - 6. In TO 33K-1-01.

440 - 1. These are: TO 33-1-14, *Calibration and Certification of PME,* and TO 33K-1-100, *Calibration Technical Orders—Responsibilities and Calibration Measurement Areas.*

440 - 2. AFTO Form 108.

440 - 3. AFTO Form 256, No Calibration Required.

441 - 1. A circuit-switched telephone switching center which enables subscribers to dial telephones on a worldwide basis.

441 - 2.
a. Operates as a four-wire automatic switching center.
b. Functions as a common control, space-divided switching system, employing a solid-state memory array for programming traffic handling in the switching equipment.
c. Is capable of handling all voice and analog signals that can be passed over wideband voice circuits.
d. Accepts addressing signals from four-wire subscriber subsets arranged for DTMF signaling.
e. Accepts DP signals from private branch exchange (PBX) trunks and sends DP signals to PBX installations equipped for direct inward dialing.
f. Performs all tandem switching functions with other AUTOVON switching centers on a four-wire basis, using MF confirmation address signaling.
g. Is equipped with two or more DSA operator positions if the switch facilities have DSA. Here the operator gives special services for completing calls, placing delayed calls, arranging random conference calls, etc. Calls requiring operator service from switch facilities without DSA equipment are routed to the nearest DSA-equipped switch facility on general-purpose interswitch trunks.

441 - 3. A highly complex computerized communications system which is designed to transmit and receive narrative messages and data traffic from originators to addressees quickly and securely.

441 - 4. Five-level code, International Teletypewriter Alphabet Number 2 (ITA#2); and eight-level codes, Fieldata and American Standard Code for Information Interchange (ASCII). The latter two codes are superior because they have the capability of maintaining character integrity through assignment of parity and control characters, while the former has no such capability.

441 - 5. From 75 baud (94-100 wpm) to 4800 baud (6000 wpm).

441 - 6. Link.

441 - 7. The two identical computers are periodically reversed.

442 - 1. The Hughes 4118 computer.

442 - 2.
a. AN/TTC-30 central offices; the AN/TTC-32, a 40-line manual switchboard; communications patch bays; and various end instruments.
b. In the same order as for a, this equipment is located, respectively, at the TAB, TACC, CRCs, and CRPs; in the DASC; at each operations module; and throughout the TACS.

442 - 3. The AN/TTC-30 electronic switching system.

442 - 4. Your answer should include any four of these seven functions:
a. Checks the status of each line every 10 milliseconds.
b. Detects lines requesting service during the line status check and orders appropriate processing to satisfy the request.
c. Accepts keyed office code and/or directory number digits from the calling line and performs appropriate processing to establish a connection to the called line represented by the keyed digits.
d. Generated supervision tones (dial tone, preliminary ring tone, answer tone, warning tone, seizure tone, and release tone) for signaling to the calling and called lines.
e. Controls the activation of the electronic switches in the transmission network on a time-shared basis to establish and maintain a connection between terminals.
f. Updates the status of each line during the line check to reflect the present conditions for the line.
g. Initiates processing for disconnect when a call is completed.

442 - 5. Air Force component command post, control reporting/air traffic regulation center, control and reporting post, direct air support center, and the tactical air base communications/terminal air traffic control facility.

442 - 6. It coordinates and controls the 407L system's AC&W radar, and it functions as the focal point of the AC&W capability to display, evaluate, and distribute information on air activity within its sphere of influence.

442 - 7. Two functioning operating modules—the communications module and the operations module.

443 - 1. A means for detecting, tracking, cataloging, and identifying manmade objects in space.

443 - 2. The Ballistic Missile Early Warning System (BMEWS), the Sea-Launched Ballistic Missile (SLBM), and the Over-the-Horizon (OTH) System.

443 - 3. To detect, track, and report positions of manmade orbiting objects in accordance with the Space Defense Center's tasking system.

443 - 4. Operating as a "family" of systems, to bounce radar signals off the ionosphere and back to earth, far beyond the ionosphere and back to earth, far beyond the horizon. It also adds to the BMEWS capability and substantially improves the warning time in the event of a ballistic missile attack.

CHAPTER 4

See Module 1001 for answers to objectives 444-454.

CHAPTER 5

455 - 1. Because, by asking yourself before you act (start trying to find the trouble) the questions, "What are the trouble symptoms, and knowing this, what could most likely be causing the trouble," you will be following a logical sequence of steps that will probably lead you to the problem's cause much more quickly than you would reach it by a trial-and-error (acting first, thinking second) approach to it.

455 - 2.
Step 1: Localize the faulty by analysis of symptoms of malfunction.
Step 2: Locate the trouble through inspection.
Step 3: Localize fault to defective section by testing techniques.
Step 4: Localize fault to defective stage by testing techniques.
Step 5: Localize fault to defective circuit or part by testing techniques.
Step 6: Replace or repair the defective part.
Step 7: Test circuit operation; readjust circuit.

455 - 3. A visual indicator that many of the system's cabinets often have (in fact, several). If a trouble occurs and then an indicator light comes on, that light tells you what part of the system has failed. If you find this true of the problem you are trying to solve, then you can move to step 2 of the general troubleshooting procedure (referred to in exercise 2).

455 - 4. Because, having such performance check data documentation, you can spot slow, progressive drifts toward trouble and make necessary replacements or repairs before the margin of performance limits for a particular piece of equipment is reached. In this way, you can often avoid a malfunction situation entirely.

456 - 1. Marginal checking, system checking, test routines and programs, or diagnostic checks.
456 - 2. A method of troubleshooting or periodic maintenance inspection in which certain operating conditions are varied from their normal values in order to detect deteriorating components.
456 - 3. "System checking" is the broader term. Whereas "marginal checking" is normally limited to the checking of a circuit, a stage, or a small section of an electronic system, system checking may check large sections or units in one operation. While marginal checking is used in troubleshooting or periodic maintenance inspection, system checking, though considered a practical aid in troubleshooting, is sometimes faster and more practical for use in preventive maintenance.
456 - 4. Unlike other types of checks, diagnostic checks are used to help technicians locate sources of errors. They may be combined in such detail as to cause the system to initiate an output that will indicate a faulty component, card, or section. So used, their success lies in the ability of your system's visual indicators indicating the specific area of failure. A tremendous aid in troubleshooting and preventive maintenance, the individual diagnostic check may be incorporated into one big routine containing many such checks and called a diagnostic program.

457 - 1. Programs, diagnostic checks, or test sequences used in conjunction with test equipment peculiar to the system or unit under test, such as special drawer testers, power supply test sets, and specially designed unit test sets. Also, normal test equipment, such as multimeters, oscilloscopes, VTVMs, special frequency meters, etc.
457 - 2. Because you may then perform the test on the unit with all available information about it at your fingertips. Then, if there has been a recent change in the specific TO/TM which, for example, eliminates a step in a check, you will not perform that check using the old method, and your check will be both valid and not liable to damage the test set or equipment under test.

458 - 1. Resistance measurement, voltage measurement, and waveform comparison.
458 - 2. Voltage measurement. In the appropriate TO/TM.
458 - 3. Voltage measurement. If the voltage to be measured is greater than 600 volts, proceed as follows: Shut off the circuit power, discharge any filter capacitors, and temporarily ground the point to be measured. Then connect (slip on) the proper test lead to the high potential point and move away from the voltmeter.
458 - 4. Compare waveforms to the specifications listed in the applicable TO, using an oscilloscope.

459 - 1. First, load a diagnostic program into the applicable control unit and start it. The control unit will cycle through all of the diagnostic steps until the programmed test identifies the faulty unit and causes a printout of the suspect cards. Then, second, you employ the ground removal and replacement technique. After replacing the cards, start the diagnostic program again to check out the system. If the trouble has been cleared, the program will cycle completely through. Yes, you could possibly have more than one problem. In that case, the program will identify another individual card or group of cards which must be replaced.
459 - 2. Provides for quick restoration of equipment.

460 - 1. Check at TP1, TP4, and then between TP1 and TP4 if data did not show up at TP4. If it did, then go to TP7 and check between TP4 and TP7, etc.
460 - 2. The split half method.

461 - 1. MIL-STD-806B, *Graphic Symbols for Logic Diagrams.*
461 - 2. An AND-gate remains an AND-gate, and the principles involved in the functional operation of that particular logic device will remain the same, regardless of slight changes in the symbol used to represent the AND-gate.
461 - 3. 1 or 0.
461 - 4. A means of determining an output by considering all inputs and their variables.
461 - 5. That there is a failure within the OR-gate.
461 - 6. $\overline{D}a = G$.

462 - 1. To absorb heat to prevent damage to heat-sensitive components.
462 - 2. Thermal shunts should be the clip-on type, held in place by spring tension.
462 - 3. Cleanliness of the surface to be soldered.
462 - 4. Use of the pointed end of a soldering aid.
462 - 5. a. Size.
b. Shape.
c. Wattage.
d. Tip.
462 - 6. 3/8, 5/8, and 7/8 inch.
462 - 7. A small soldering iron in the 20- to 40-watt range.
462 - 8. Hard and soft.
462 - 9. 60/40 (60 percent tin/40 percent lead).
462 - 10. To clean the surface to be soldered.

463 - 1. Check that a full insertion of the heating element has been achieved, oxidation scale has accumulated, that proper thinning has taken place, and that there is no excess solder.
463 - 2. Tips plated with an oxidation-resistive coating.

464 - 1. Use the stranded type of hookup wire unless a solid type of hookup wire is required by design.
464 - 2. It is rigidly secured and supported at 1-inch intervals.
464 - 3. For wires having an outside diameter of 1/32 inch or greater, the minimum is 1/32 inch and the maximum is 1/32 inch plus the outside diameter of the wire. For wires having an outside diameter of less than 1/32 inch, the minimum equals the outside diameter of the wire and the maximum is 1/32 inch.
464 - 4. In the direction of the lay in order to maintain the original form and to prevent separation of the individual strands.
464 - 5. After determining and marking the termination point, push back the shielding braid to form a bubble at that point. Insert a soldering aid end into the braid and open a circular hole in the shield. Pull the insulated wire through the hole, strip it, and tin it to prevent fraying. Also, tin the shielding.
464 - 6. Dip the wire in liquid flux to the desired depth; then dip it in molten solder to correct the tinning depth.
464 - 7. Make a gradual bend with a radius of no less than two times the diameter of the lead. Start bends at least two lead diameters from the part body or weld, as applicable.
464 - 8. Use a typewriter eraser to clean the part until the tinned surfaces are bright and shiny. Wash the cleaned terminal with an approved solvent just before making a wire or part lead attachment and soldering.

465 - 1. To increase the electrical conductivity and to provide an airtight covering to prevent corrosion from developing between the wire and the terminal.
465 - 2. Attach the wire so that there is no movement. Use a thermal shunt if needed. Clean the connection and apply flux if needed. Clean and tin the soldering tip.
465 - 3. Apply the heated soldering tip for maximum heat transfer. When it is hot, apply solder directly to the connection. Heat until flux is boiled out and connection is wetted.
465 - 4. Because the connection would be mechanically weak and have high resistance.
465 - 5. After the terminal is heated, apply a small amount of solder inside it. Insert the wire and maintain heat until the flux is boiled out and the solder fuses into the conductor and terminal surfaces.
465 - 6. It will have a shiny, bright appearance with no pits or holes, a good concave fillet between the wire and terminal, and have no excess solder.
465 - 7. When required for mechanical and electrical protection, flexible insulating tubing is installed over the connection.

466 - 1. a. 180° to 270°.

b. 90° bend.
c. No bend.
d. 90° to 180°.

466 - 2. a. From the base or top shoulder, as applicable.
b. From the entry point of the wire into the terminal.
c. From the base.
d. From the end of the terminal.

467 - 1. If you apply heat to a rosin wick, the solder will flow readily into the rosin area, leaving the terminal to which it was previously affixed.

467 - 2. Place the wick on top of the solder joint to be removed; place the iron tip on top of the wick and when the iron melts the solder, it will flow into the wick; as the wick becomes saturated, clip off the end of the wick. Repeat these steps until you remove all the solder from the joint.

467 - 3. Sniffing removes the molten solder by suction.

467 - 4. The wicking method.

468 - 1. a. Burns can be received from soldering irons or from handling soldered connections that have not sufficiently cooled.
b. Soldering fluxes spatter when heated.
c. Flipping excess solder from tip can cause serious skin or eye burns.
d. A solder splatter caught under a ring can cause a severe burn.
e. Vapors from degreasing solvents and fluxes may contain toxic gases.
f. Most fluxes contain materials that are a health hazard when ingested.

469 - 1. Sufficient contact area and contact pressure, and sufficient elastic energy to maintain correct pressure.

469 - 2. Metal-to-metal contact, high-pressure contact, a gas-tight contact area, a large contact area, mechanical stability, and no localized stress concentration.

469 - 3. Your answer should contain any five of these advantages: no solder disadvantages, savings in material and labor, ease in disconnection from terminals, more compact connections, a uniformity of the connection with calibrated tools, more resistance to handling and vibration stress, more reliable connections, and the possibility of being automated.

469 - 4. Basic tool plus the wrapping bit and sleeve.

469 - 5 a. An electrical connection produced by wrapping a wire tightly around a pin-type terminal.
b. The stationary member of the wrapping tool which wraps the wire around the terminal.
c. The piling up of wraps, one on top of another.

469 - 6. Place the tool over the terminal, allowing space for a minimum of five or six complete wraps. Make the first connection on a terminal as close to the terminal base as possible. Line the bit up with the terminal so that it slips on without bending or damaging the terminal in any way.

469 - 7. Five full turns.

469 - 8. Solder them.

470 - 1. a. 5.
b. 3.
c. 9.
d. 7.
e. 4.
f. 1.
g. 10.
h. 2.
i. 6.
j. 8.

471 - 1. To prevent loss of power to the equipment or injury to the personnel involved.

471 - 2. Remove power, label the wires to be removed, unsolder the wires from the socket, solder a new socket to the wires, check continuity with a VOM, secure the socket to the chassis with a washer and a retaining nut, and apply power and perform an operational check.

471 - 3. You must align the prongs on the lamp with the slots in the lamp socket; insert the lamp into the socket and depress the spring base; twist and release the lamp, allowing the prongs of the lamp to seat in the slots.

471 - 4. (1) Display and (2) as a voltage regulator.

471 - 5. Usually in an input power line.

471 - 6. About 170°.

471 - 7. The fuse for the circuit will blow.

471 - 8. (1) Heat and (2) mechanical abuse.

471 - 9. Mark the wires to be removed, remove power before starting repair, remove the unit carefully, use proper soldering techniques, make a static check before applying power, insert the proper fuse and apply power, and make a dynamic check.

471 - 10. *General Shop Practice Requirements for the Repair, Maintenance, and Test of Electronic Equipment.*

472 - 1. Whereas (a) the digital input switch will provide the input source for either a static level logic 1 or a dynamic level 1, or a pulse train, and may even provide the source for an octal input, (b) a command input switch will provide preset, reset, advance, repeat cycle, and other short-duration machine command signals.

472 - 2. a. Microswitch, rectangular.
b. Toggle, microswitch circular.
c. Pushbutton switch with lamp indicators.
d. Microswitch, circular.

472 - 3. As shown in A, figure 5-46, it may be used to enter a static level 1 to a register or counter each time it is depressed; or as shown in B and C of figure 5-46, it may be connected to relays to provide a pulse train in either binary, binary coded decimal, grey code, octal, or a special code prepared for specially designed circuitry.

472 - 4. There is sticking of the spring-loaded switch, no continuity when checked, a loose toggle, improper placement of the microswitch unit, improper solder connections, or a nonoperating holding coil.

472 - 5. (1) Remove power to the switch.
(2) Label all wires carefully for exact replacement.
(3) Remove wires properly.
(4) Position and solder the new switch to the leads.
(5) Secure the switch to the cabinet.
(6) Perform a static check with a VOM.
(7) Perform a dynamic check with power applied.

473 - 1. Lettering and numbering.

473 - 2. Lettering.

473 - 3. I, O, and Q.

473 - 4. A—the wiring retaining section, which is crimped to hold the unit; B—the spring tension section, which is designed to lock the pin in place in the hole provided in the connector body; and C—the male or female mating unit.

473 - 5. (1) Mark each wire position and color-code.
(2) Remove power.
(3) If necessary disconnect the connector from the panel.
(4) Use the pin extractor to release the pins.
(5) Insert the good pins into the new connector.
(6) Replace any defective pins.
(7) Insure that pins are seated and there are no cracks, frays, or loose wiring.
(8) Secure the connector to the frame (if applicable).
(9) Secure the mating unit to the repaired or replaced connector and carefully match the guide pin.
(10) Apply power and perform dynamic checks (where applicable).

474 - 1. A pattern comprised of printed wiring and printed parts, all formed in a predetermined design on, or attached to, the surface of a common base.

474 - 2. (1) Painted, (2) chemically deposited, and (3) stamped or etched metal foil.

474 - 3. By dipping a stencil-covered nonconducting base into an appropriate chemical solution. The resulting metallic film forms the wiring pattern.

474 - 4. A nonconductive base is covered with metal foil. The

wiring pattern is formed by stamping or etching to remove unwanted portions of the foil.

474 - 5. The type made up of conductive patterns and miniaturized separable parts.

474 - 6. (1) Reduce the amount of heat required for soldering by using a small-diameter low-melting-point solder.
(2) Use a small, low-power soldering iron to permit access to cramped areas of the card.
(3) Use grounded soldering iron equipment or ground the soldering iron tip, preferably by using alligator clip leads.
(4) Use enough thermal shunts or heat sinks to protect heat-sensitive devices sufficiently.
(5) Insure that the total time of heat application does not exceed the time required to melt the solder and provide proper fusion of solder with the terminal pad and component lead.
(6) If you experience difficulty sodering a connection, stop and allow the connection to cool completely before you attempt to resolder.
(7) Remove flux and flux residues from solder connections after the connection has cooled.

475 - 1. Whether or not any prior servicing has been performed on the printed circuit.
475 - 2. By studying the symptoms and by carefully and patiently analyzing the printed circuit.
475 - 3. Poorly soldered connections.
475 - 4. Set up a multimeter for making point-to-point resistance tests, using needlepoint probes.
475 - 5. Never use a range that passes more than 1 mA.
475 - 6. Lightly scrape away any coating covering the area of the conducting strip to be repaired, clean the area with a firm-bristle brush and approved solvent, and then repair the cracked or broken area by flowing solder over the break.
475 - 7. Clip off the raised section and replace it with insulated hookup wire from solder point to solder point.
475 - 8. Droppage.

476 - 1. Be sure the component is disconnected from the circuit to avoid parallel circuit paths. Discharge the capacitor before checking the ohmmeter. When you connect the ohmmeter across a capacitor, the ohmmeter pointer should move quickly toward a low resistance reading, then slowly recede toward infinity (always use the ohms × 1 meg range).
476 - 2. (1) c.
(2) f.
(3) a.
(4) b.
(5) d.
(6) e.
476 - 3. The cathode has a negative potential, and the anode has a positive potential.
476 - 4. a. Compare the transistor to a reference chart.
476 - 5. Place the circuit board in front of a strong light to get an X-ray view of the parts on the opposite side.
476 - 6. Bad; the E-B is open.
476 - 7. Negative; positive.
476 - 8. True.
476 - 9. Connect the ohmmeter positive lead to the base of a PNP transistor (as shown in fig. 5-59,A).
476 - 10. Linear integrated circuits, nonlinear integrated circuits, and uncommitted transistor (array) integrated circuits.
476 - 11. Replace the suspected bad IC with a new one.
476 - 12. (1) Overvoltages—from too large a power source.
(2) Transients—noise spikes.
(3) Ohmmeter—internal power source giving overvoltages.
(4) Heat-soldering in or out of a circuit.

477 - 1. To prevent damage to the printed circuit, feed-through devices, eyelets, or terminals, and to save time in repair.
477 - 2. Place your finger between the heat-sensitive part and the connection. If it is too hot for your finger, it is too hot for the heat-sensitive part.
477 - 3. To protect the associated parts any time repair or removal of a part requires the use of a hot soldering iron.
477 - 4. Heating the bonding or breaking the part.
477 - 5. Cutting the part with diagonal pliers.
477 - 6. Use it so that the leverage surface of the tool is flat against the surface of the printed circuit board.
477 - 7. Because it will help secure the new part from vibration.
477 - 8. First, cut the leads. Then secure the board in a proper device and support the board on the other side to prevent its breaking. Simultaneously heat the bonding and drive the transistor through the board with a drift punch.
477 - 9. Test the transistor first, because it could be defective.
477 - 10. Use two pair of needle-nose pliers. With one pair grasp the lead close to the transistor base while shaping the rest of the lead with the other pair.
477 - 11. If the hole is too large, shim the transistor with a plastic sleeve. If the hole is too small, ream it out.
477 - 12. To see that the part is free of all of its connections and that all mounting lugs are straightened.
477 - 13. Cut the multilug part from the circuit on the mounting side of the board; then remove the lugs one at a time with soldering pencil and slotted soldering aid tool.
477 - 14. Because they are small and mounted on a thin phenolic board and could be damaged easily by heat or undue pressure.

CHAPTER 6

478 - 1. Transformer, rectifier, filter, voltage regulator, and voltage divider.
478 - 2. To step up or step down the voltage.
478 - 3. To change AC voltage to DC voltage.
478 - 4. Filter.
478 - 5. To maintain or regulate the output voltage to the critical level needed.
478 - 6. To provide the output voltages that are required for the amplifier's bias and collector supply voltages.

479 - 1. Equal to the frequency of the applied AC signal because you get one pulse output per input cycle.
479 - 2. (1) a.
(2) f, g, h.
(3) b, c, d, e.
(4) b, c, d.

480 - 1. Yes. By using a rectifying circuit.
480 - 2. The charge on C2 is series-aiding to the charge on C1.
480 - 3. By adding sections in cascade.
480 - 4. As a transformerless high-voltage low-current supply.

481 - 1. As decreasing the amplitude of the AC component in the rectified output leaving the average DC component.
481 - 2. (1) a.
(2) f.
(3) b; e.
(4) c; d.
481 - 3. A DC power source.
481 - 4. A fairly high output voltage and good voltage regulation.

482 - 1. (1) b; c; f; i.
(2) a; d; h; k.
(3) e; g; j.
482 - 2. The current operating range (maximum to minimum) is limited; there is a voltage change between the minimum current and maximum current conditions; and the amplitude of the regulated voltage is fixed by the type of zener used.
482 - 3. An open Q1 or an open R2. With Q1 open, the series circuit is broken. With R2 open, there is no forward bias for Q1, so the only output voltage will be due to minority current.
482 - 4. Even very short transients can cause serious damage.

483 - 1. The operation of the rectifier will not be affected in these

circumstances, provided that the insulation of all parts in the circuit can withstand the voltage involved.

483 - 2. a. I_b = 1 milliampere.
b. R_3 = 60,000 ohms.
c. R_2 = 30,000 ohms.
d. R_t = 37,500 ohms.

484 - 1. To form a filter network which develops a negative DC voltage.
484 - 2. It will decrease.
484 - 3. To provide current limiting for the +3-volt output line.
484 - 4. A shunt regulator circuit.

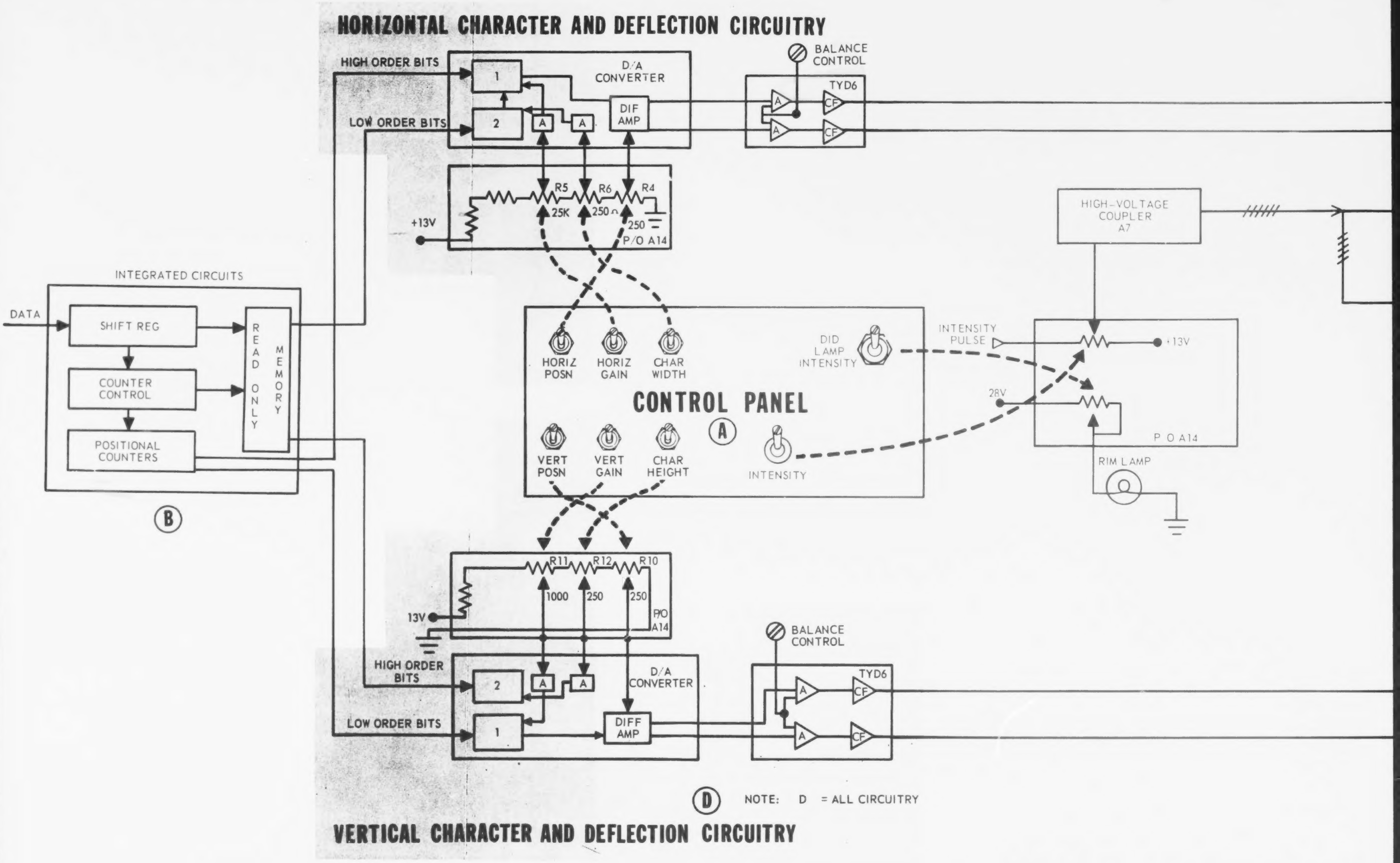
485 - 1. An open-circuited rectifier.
485 - 2. (a) An increased forward resistance; (b) a decreased reverse resistance.
485 - 3. (a) A physical rupture of the barrier layer caused by high temperature, (b) 20 percent of the plate area, and (c) replacement of the rectifier.
485 - 4. The rectifier is open.
485 - 5. It is the sum of the rated PIVs of the individual rectifiers.

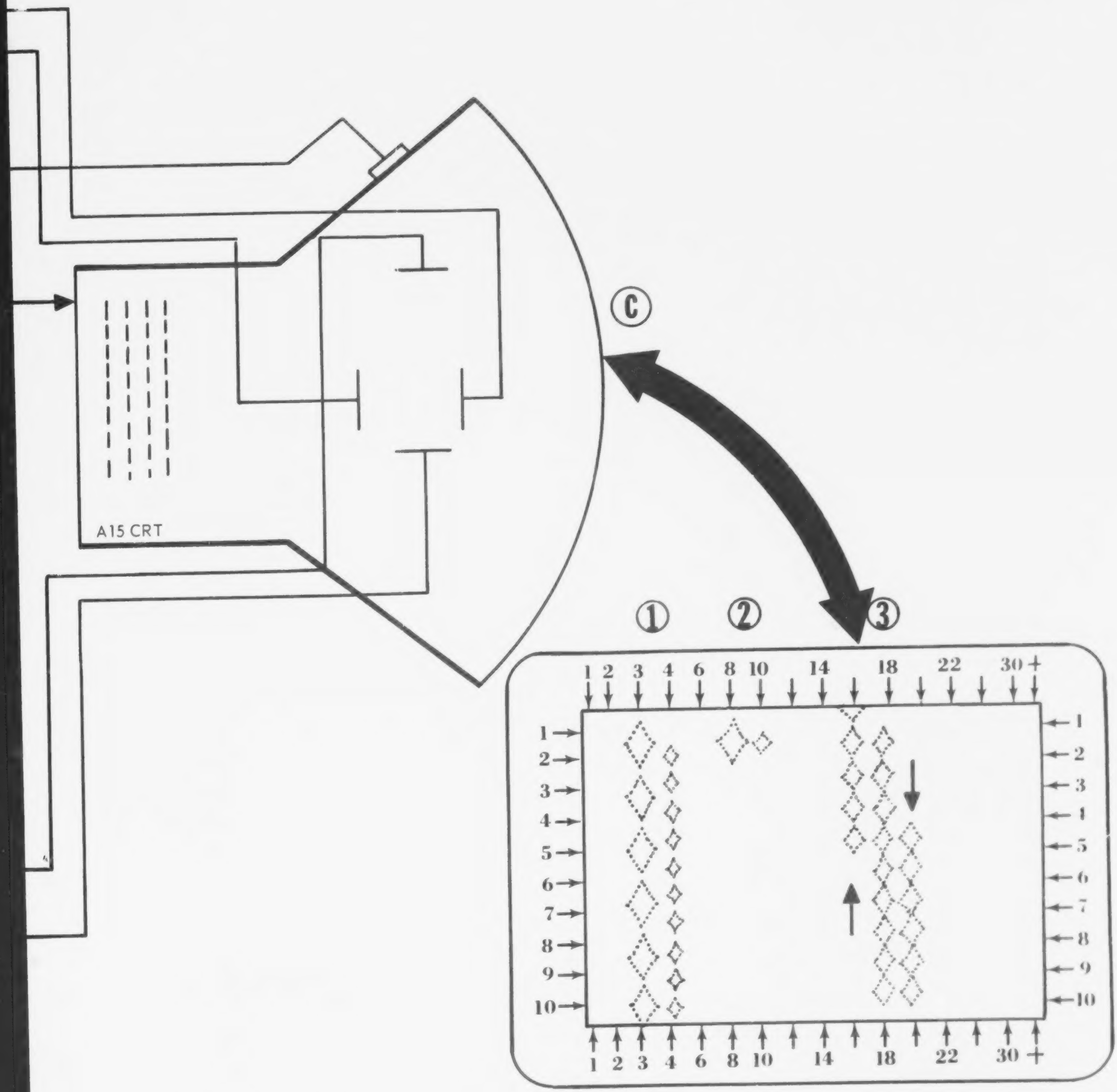
CHAPTER 7

485a - 1. Vertical deflection, volts/div setting, and probe attenuation factor.
485a - 2. Volts peak-to-peak 4.8 × 0.2 × 10 = 9.6 volts.

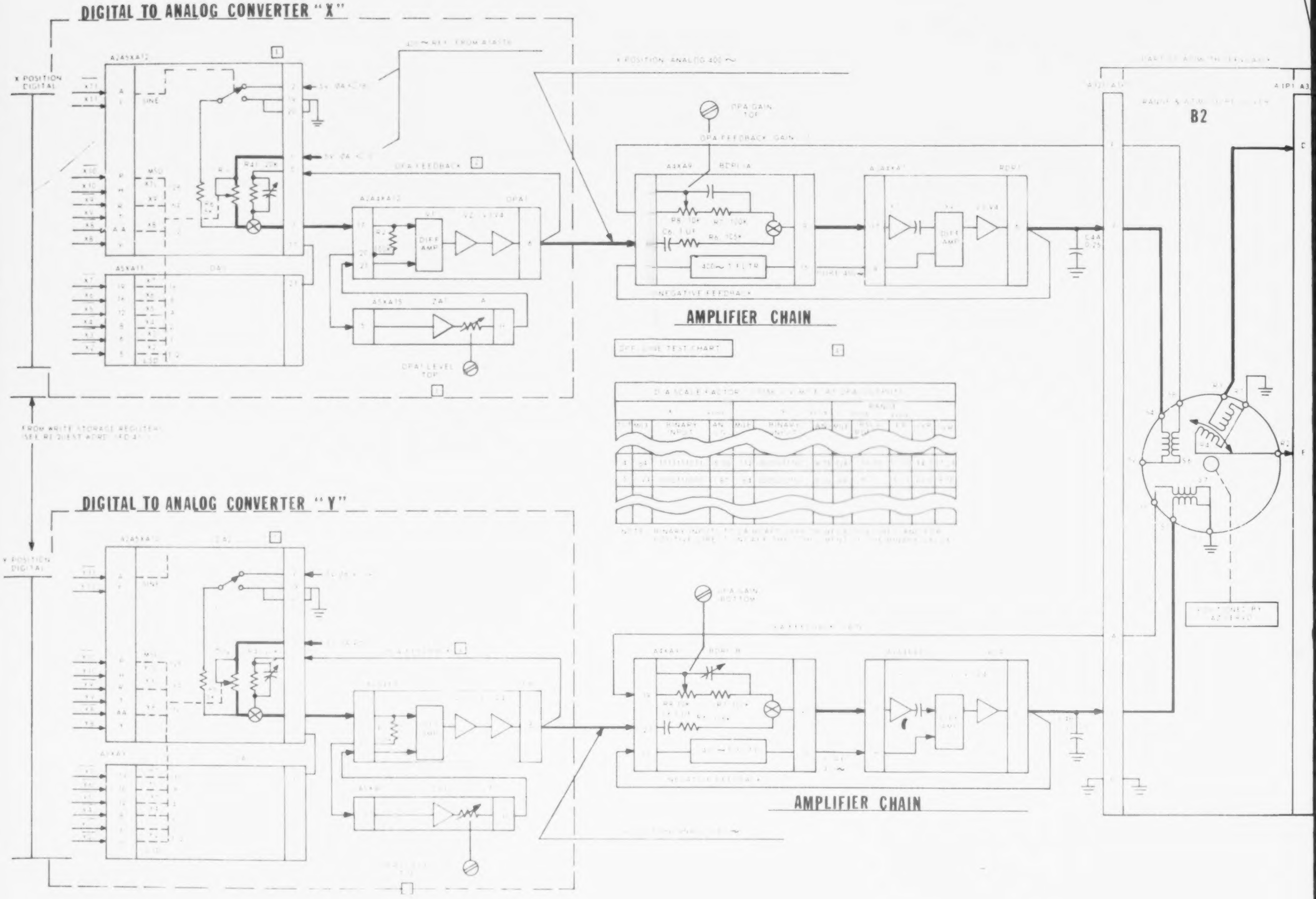
485b - 1. Vertical deflection, polarity, volts/div setting, and probe attenuation factor.
485b - 2. Instantaneous voltage 4.2 × (−1) × 0.1 × 10 = −4.2 volts.

See Module 10012 for answers to objectives 486–496.


HORIZONTAL CHARACTER AND DEFLECTION CIRCUITRY
HIGH ORDER BITS
LOW ORDER BITS
1
2
A
A
D/A CONVERTER
DIF AMP
BALANCE CONTROL
TYD6
A
A
CF
CF
R5
R6
R4
25K
250 Ω
250
+13V
P/O A14
HIGH-VOLTAGE COUPLER A7
INTEGRATED CIRCUITS
DATA
SHIFT REG
COUNTER CONTROL
POSITIONAL COUNTERS
READ ONLY MEMORY
B
HORIZ POSN
HORIZ GAIN
CHAR WIDTH
DID LAMP INTENSITY
CONTROL PANEL
A
VERT POSN
VERT GAIN
CHAR HEIGHT
INTENSITY
INTENSITY PULSE
+13V
28V
P O A14
RIM LAMP
R11
R12
R10
1000
250
250
13V
P/O A14
HIGH ORDER BITS
LOW ORDER BITS
2
1
A
A
D/A CONVERTER
DIFF AMP
BALANCE CONTROL
TYD6
A
A
CF
CF
D
NOTE: D = ALL CIRCUITRY
VERTICAL CHARACTER AND DEFLECTION CIRCUITRY


A15 CRT
Ⓒ
①
②
③
1 2 3 4 6 8 10 14 18 22 30 +
1 2 3 4 5 6 7 8 9 10
1 2 3 4 5 6 7 8 9 10
1 2 3 4 6 8 10 14 18 22 30 +

Foldout 1. DID IC unit.


DIGITAL TO ANALOG CONVERTER "X"
X POSITION DIGITAL
A2A5XA12
400 ~ REF FROM A1A1T6
X POSITION ANALOG 400 ~
SINE
R41 20K
DPA FEEDBACK
A2A4XA12
OPA1
DIFF AMP
A5XA11
DA1
A5XA15
ZA1
OPA1 LEVEL TOP
OPA GAIN TOP
OPA FEEDBACK GAIN
A3XA9
BDPL1A
R8 10K
R7 100K
C6 1 UF
R6 105K
400 ~ T FLTR
NEGATIVE FEEDBACK
A3A4XA7
DIFF AMP
C4A 0.25
AMPLIFIER CHAIN
OFF LINE TEST CHART
D/A SCALE FACTOR
BINARY INPUT
RANGE
B2
R1
R2
R3
R4
S1
S2
S3
S4
S5
S6
S7
FROM WRITE STORAGE REGISTERS
DIGITAL TO ANALOG CONVERTER "Y"
Y POSITION DIGITAL
A2A5XA12
SINE
DIFF AMP
OPA GAIN BOTTOM
NEGATIVE FEEDBACK
DIFF AMP
AMPLIFIER CHAIN
POSITIONED BY AZ SERVO

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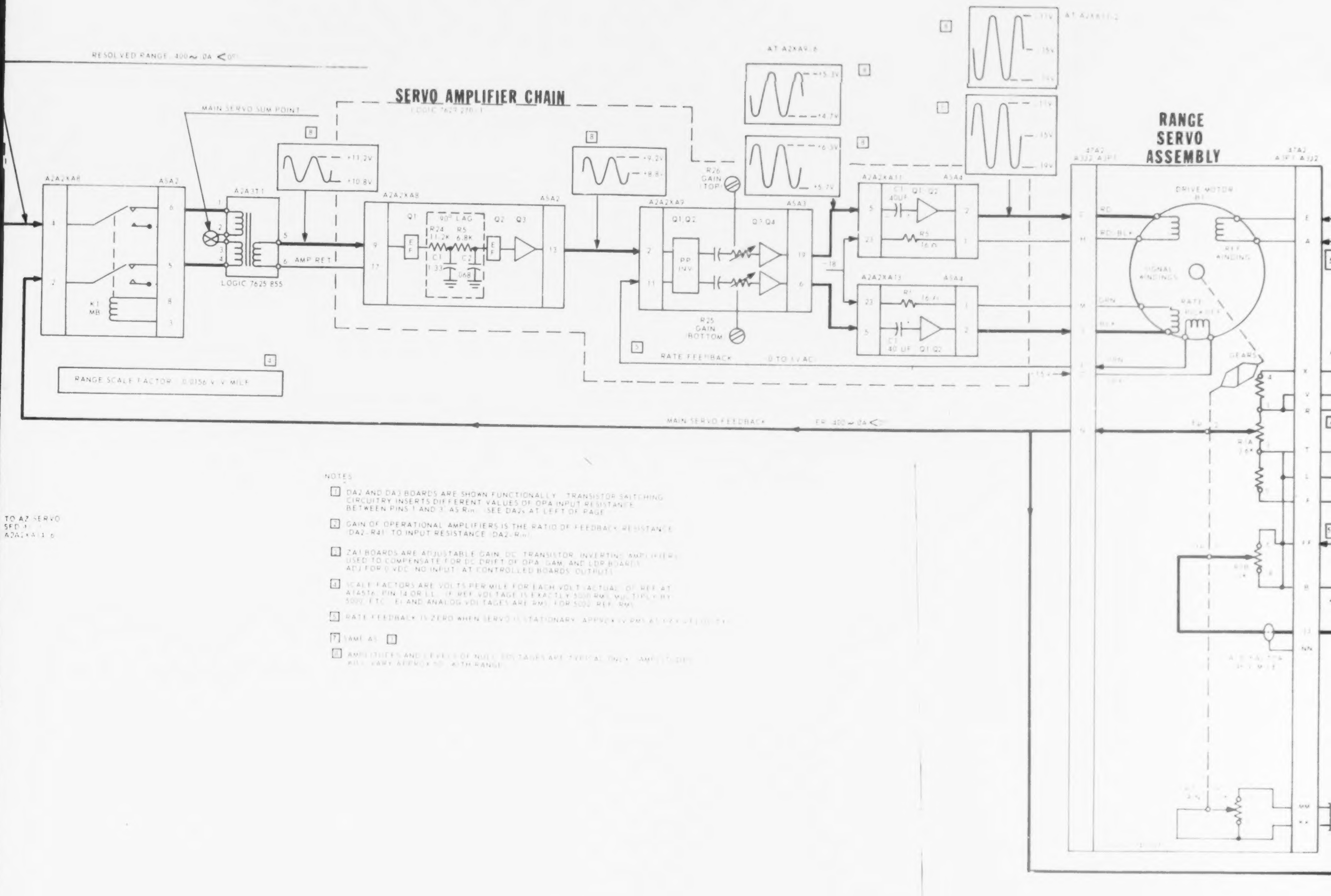
RESOLVED RANGE 400~ 0A <0°
MAIN SERVO SUM POINT
SERVO AMPLIFIER CHAIN
LOGIC 7625 278-1
A2A2XA8
A5A2
A2A3T1
LOGIC 7625 855
K1 MB
+11.2V
+10.8V
AMP RET
90° LAG
R24 11.2K
R5 6.8K
C1 .33
C2 .068
Q1
Q2
Q3
E F
+9.2V
+8.8V
A2A2XA9
A5A3
Q1,Q2
Q3,Q4
PP INV
R26 GAIN (TOP)
R25 GAIN (BOTTOM)
AT A2XA9-8
+5.3V
+4.7V
+6.3V
+5.7V
A2A2XA11
A2A2XA13
A5A4
C1 40UF
R5 16 Ω
C1 40 UF
RATE FEEDBACK
0 TO 1 V AC
AT A2XA11-2
11V
15V
19V
RANGE SERVO ASSEMBLY
DRIVE MOTOR B1
REF WINDING
SIGNAL WINDINGS
RATE PICKOFF
RD
RD-BLK
GRN
BLK
GEARS
R1A
R1B
MAIN SERVO FEEDBACK
ER 400~ 0A <0°
RANGE SCALE FACTOR 0.0156 V/V/MILE
TO AZ SERVO SED A2A2XA13-6

NOTES

1. DA2 AND DA3 BOARDS ARE SHOWN FUNCTIONALLY. TRANSISTOR SWITCHING CIRCUITRY INSERTS DIFFERENT VALUES OF OPA INPUT RESISTANCE BETWEEN PINS 1 AND 3, AS R_{in}. (SEE DA2s AT LEFT OF PAGE.)
2. GAIN OF OPERATIONAL AMPLIFIERS IS THE RATIO OF FEEDBACK RESISTANCE (DA2-R41) TO INPUT RESISTANCE (DA2-R_{in}).
3. ZA1 BOARDS ARE ADJUSTABLE GAIN, DC, TRANSISTOR, INVERTING AMPLIFIERS USED TO COMPENSATE FOR DC DRIFT OF OPA, GAM, AND LDP BOARDS. ADJ FOR 0 VDC (NO INPUT) AT CONTROLLED BOARDS' OUTPUTS.
4. SCALE FACTORS ARE VOLTS PER MILE FOR EACH VOLT (ACTUAL) OF REF AT A1A5TA (PIN 14 OR LL). IF REF VOLTAGE IS EXACTLY 50V RMS, MULTIPLY BY 50, ETC. EI AND ANALOG VOLTAGES ARE RMS FOR 50V REF RMS.
5. RATE FEEDBACK IS ZERO WHEN SERVO IS STATIONARY. APPROX 1V RMS AT [illegible]
7. SAME AS [illegible]
8. AMPLITUDES AND LEVELS OF NULL VOLTAGES ARE TYPICAL ONLY. AMPLITUDES WILL VARY APPROX 50% WITH RANGE.

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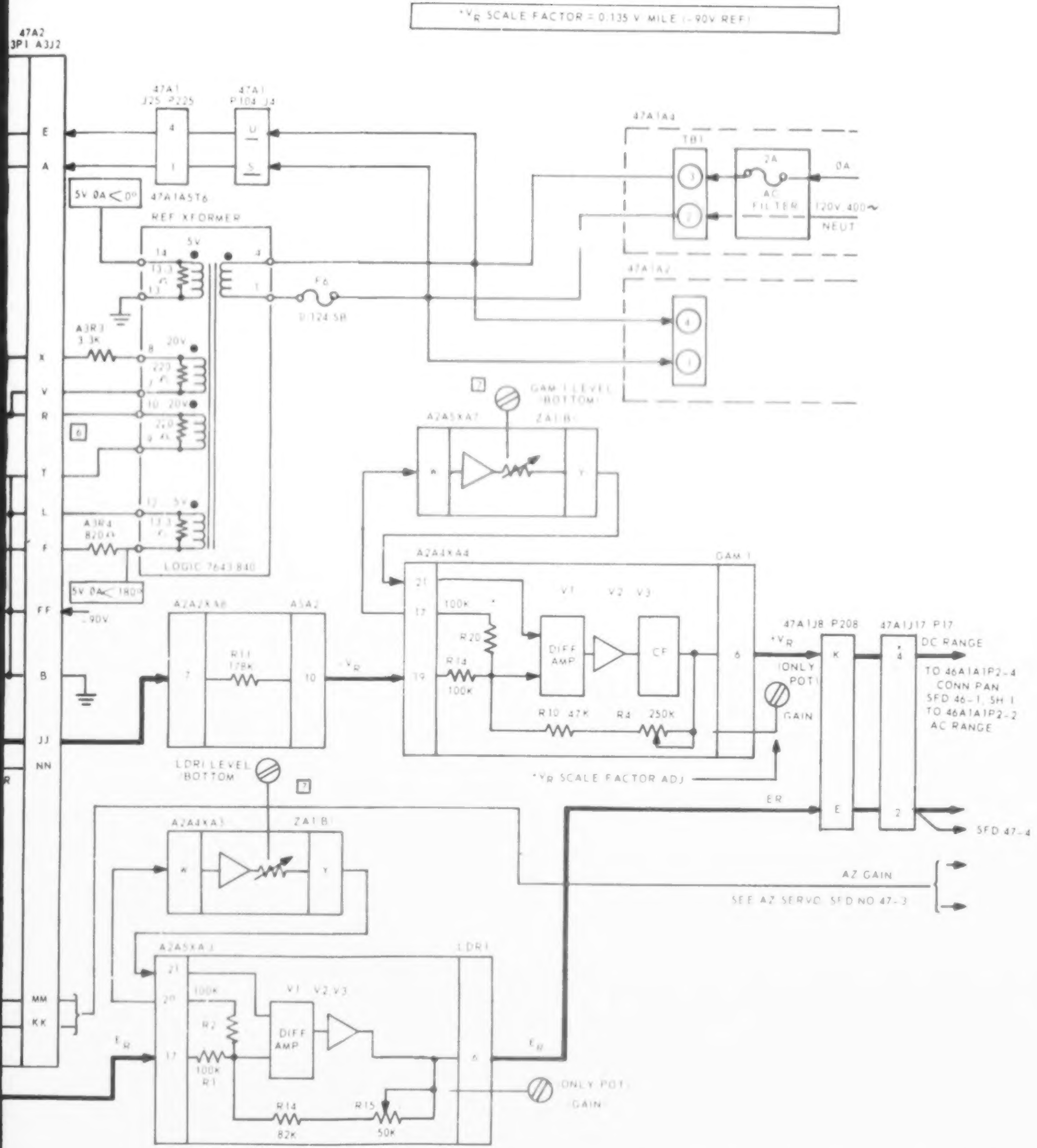
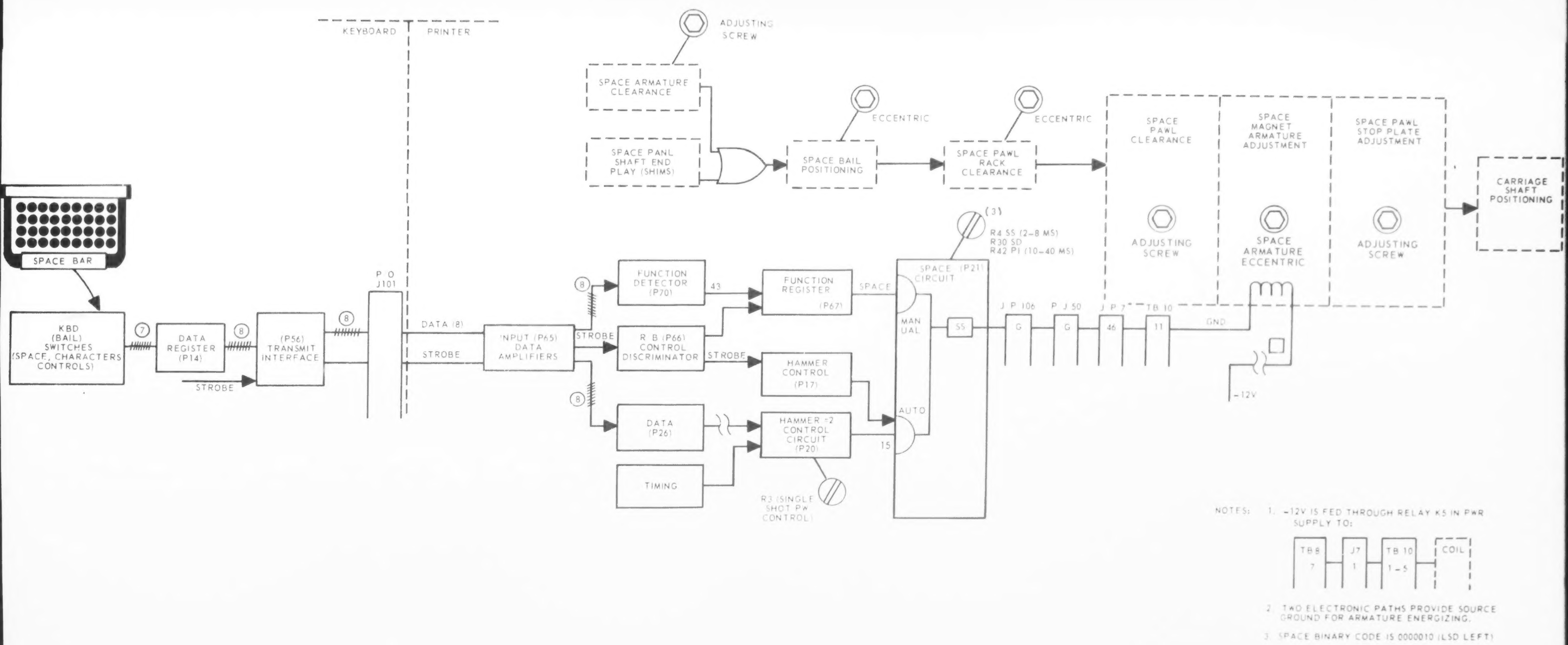

+VR SCALE FACTOR = 0.135 V MILE (-90V REF)
47A2
3P1 A3J2
E
A
X
V
R
T
L
F
FF
B
JJ
NN
MM
KK
47A1
J25 P225
47A1
P104 J4
4
1
U
S
5V ØA < 0°
47A1A5T6
REF XFORMER
5V
14
13.3 Ω
13
4
1
F6
0.124 5B
A3R3
3.3K
8
20V
220 Ω
7
10 20V
220 Ω
9
6
12 5V
13.3 Ω
A3R4
820 Ω
LOGIC 7643 840
5V ØA < 180°
-90V
47A1A4
TB1
3
2
2A
AC
FILTER
ØA
120V 400~
NEUT
47A1A2
4
1
7
GAM 1 LEVEL
(BOTTOM)
A2A5XA7
ZA1(B)
W
Y
A2A4XA4
GAM 1
21
17
19
100K
R20
R14
100K
V1
V2 V3
DIFF
AMP
CF
R10 47K
R4 250K
6
A2A2XA8
A5A2
R11
178K
7
10
-VR
47A1J8 P208
47A1J17 P17
+VR
K
4
DC RANGE
(ONLY
POT)
GAIN
TO 46A1A1P2-4
CONN PAN
SFD 46-1, SH 1
TO 46A1A1P2-2
AC RANGE
+VR SCALE FACTOR ADJ
LDR1 LEVEL
(BOTTOM)
7
ER
E
2
SFD 47-4
A2A4XA3
ZA1(B)
W
Y
AZ GAIN
SEE AZ SERVO SFD NO 47-3
A2A5XA3
LDR1
21
20
17
100K
R2
100K
R1
V1 V2 V3
DIFF
AMP
ER
R14
82K
R15
50K
6
(ONLY POT)
(GAIN)

Foldout 2. Complete servo with interrelated functions, outputs, and test data.


KEYBOARD
PRINTER
SPACE BAR
KBD (BAIL) SWITCHES (SPACE, CHARACTERS CONTROLS)
7
DATA REGISTER (P14)
8
STROBE
(P56) TRANSMIT INTERFACE
8
P O J101
DATA (8)
STROBE
INPUT (P65) DATA AMPLIFIERS
8
STROBE
8
FUNCTION DETECTOR (P70)
43
R B (P66) CONTROL DISCRIMINATOR
STROBE
DATA (P26)
TIMING
FUNCTION REGISTER (P67)
SPACE
HAMMER CONTROL (P17)
HAMMER =2 CONTROL CIRCUIT (P20)
R3 (SINGLE SHOT PW CONTROL)
15
SPACE (P21) CIRCUIT
MANUAL
AUTO
SS
(3)
R4 SS (2–8 MS)
R30 SD
R42 PI (10–40 MS)
ADJUSTING SCREW
SPACE ARMATURE CLEARANCE
SPACE PANL SHAFT END PLAY (SHIMS)
SPACE BAIL POSITIONING
ECCENTRIC
SPACE PAWL RACK CLEARANCE
ECCENTRIC
SPACE PAWL CLEARANCE
ADJUSTING SCREW
SPACE MAGNET ARMATURE ADJUSTMENT
SPACE ARMATURE ECCENTRIC
SPACE PAWL STOP PLATE ADJUSTMENT
ADJUSTING SCREW
CARRIAGE SHAFT POSITIONING
J P 106
G
P J 50
G
J P 7
46
TB 10
11
GND
–12V
TB 8
7
J7
1
TB 10
1 – 5
COIL

NOTES: 1. –12V IS FED THROUGH RELAY K5 IN PWR SUPPLY TO:

2. TWO ELECTRONIC PATHS PROVIDE SOURCE GROUND FOR ARMATURE ENERGIZING.

3. SPACE BINARY CODE IS 0000010 (LSD LEFT)

Foldout 3. Space interrelated functio

30554 03 S21 7807

10001 532 001 7807 CORB

MODULE

CORROSION CONTROL

Proficimus More Irretenti

Extension Course Institute

Air University

754

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THIS PUBLICATION HAS BEEN REVIEWED AND APPROVED BY COMPETENT PERSONNEL OF THE PREPARING COMMAND IN ACCORDANCE WITH CURRENT DIRECTIVES ON DOCTRINE, POLICY, ESSENTIALITY, PROPRIETY, AND QUALITY.

Preface

THIS MODULE applies to any career field that may have problems with corrosion. This includes AF specialties performing maintenance on metal equipment, including aircraft, missiles, support and electronic equipment, and civil engineering facilities and installed equipment.

The information in the module includes theory and causes of corrosion, types and appearances of corrosion, and preventive and treatment methods.

Please note that in this module, we are using the singular pronoun *he, his,* or *him* in its generic sense, not its masculine sense. The word referred to is person.

If you have questions on the accuracy or currency of the subject matter of this text, or recommendations for its improvement, send them to the 3770th Technical Training Group, Sheppard AFB TX 76311.

If you have questions on course enrollment or administration, or on any of ECI's instructional aids (Your Key to Career Development, Study Reference Guides, Behavioral Objective Exercises, Volume Review Exercise, and Course Examination), consult your education officer, training officer, or NCO, as appropriate. If he can't answer your questions, send them to ECI, Gunter AFS AL 36118, preferably on ECI Form 17, Student Request for Assistance.

This module is valued at 6 hours (2 points).

Material in this module is technically accurate, adequate, and current as of April 1978.

NOTE: In this module, the subject matter is developed by a series of Learning Objectives. Each of these carries a 3-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information give you a check on your achievement. When you complete them, see if your answers match those in the back of this module. If your response to an exercise is incorrect, review the objective and its text.

Corrosion Control

CORROSION CONTROL is of major importance in all aircraft and missile maintenance. Our national security depends on the reliability of our weapon systems. Corrosion can weaken structural members enough to destroy system reliability. This weakening can result in a major repair or replacement of the entire system. Such repairs and replacements are costly and time consuming. It is impossible to compute the exact cost of corrosion to United States industry, but experts have estimated the cost at 6 to 10 billion dollars annually. Much of this waste is a result of a lack of knowledge on the subject of corrosion control. To control corrosion effectively, you, the specialist, must understand thoroughly the nature of corrosion reaction and the type of corrosion that these reactions produce.

1-1. Nature of Corrosion

Corrosion is the deterioration of a metal as it reacts to its environment in an attempt to return to its natural state. Why does this reaction take place? Engineers have established that the corrosion of metals is accompanied by both a chemical change and the production of electrical energy. The electrochemical theory of corrosion is generally accepted.

001. List the parts of a corrosion cell, and cite established facts about corrosion reactions.

Electrochemical Corrosion. When you study the electrochemical process of corrosion, you find that corrosion is a flow of electricity between certain areas on a single metal surface or between two different kinds of metals. In either case, there must be a potential difference between these two areas or metals so that electricity (electrons) will flow between them.

Four conditions are required for electrochemical activity; the elimination of any one will stop the corrosion process. The four requirements are: (1) something that corrodes, the metal anode; (2) an area more noble (less potential), the metal cathode; (3) a continuous liquid path (electrolyte), usually condensate, salt or soil; and (4) a conductor to carry the flow of electrons from anode to cathode, usually in the form of metal-to-metal contact such as rivets, bolts, or welds.

These reactions take place until the anodic metal is destroyed or until a surface film has formed, isolating the anode from its corrosive environment, as shown in figure 1-1.

Recent experiments have shown that these electrochemical reactions are the same for all metals, differing only in the severity of the attack. Therefore, we will use iron as a basis for our discussion of the mechanics of corrosion. First, let us review some of the established facts about corrosion reactions.

a. Iron corrodes very slowly at normal temperature in the absence of water.

b. Oxygen is generally needed for any corrosion process to continue.

c. Corrosion products are mainly ferrous hydroxide on the surface of the iron. Ferric hydroxide forms the outer layer of the corrosion products with various mixtures of the two compounds.

d. Iron suspended in an acid solution corrodes more rapidly than in neutral solutions. Corrosion in neutral solutions is more rapid than in alkaline solutions.

e. In natural water, the corrosion products usually combine with the other substances to form a rust coat on the metal. These other substances influence the structure and density of the coating. Coarse coatings may accelerate the rate of corrosion, while dense coatings may form an effective barrier to reduce the corrosion rate.

f. Surface films play an important part in the rate and distribution of corrosion by raising the potential of the metal.

g. In most cases, the initial rate of corrosion is greater than the rate after a short period of time.

h. Dissimilar metals making contact in a solution capable of conducting electricity accelerate local corrosion. This takes place because metals are touching, thus completing a path for electrons to flow from the anode to the cathode.

i. The composition or concentration of the solution can cause current to flow from the anode to the cathode.

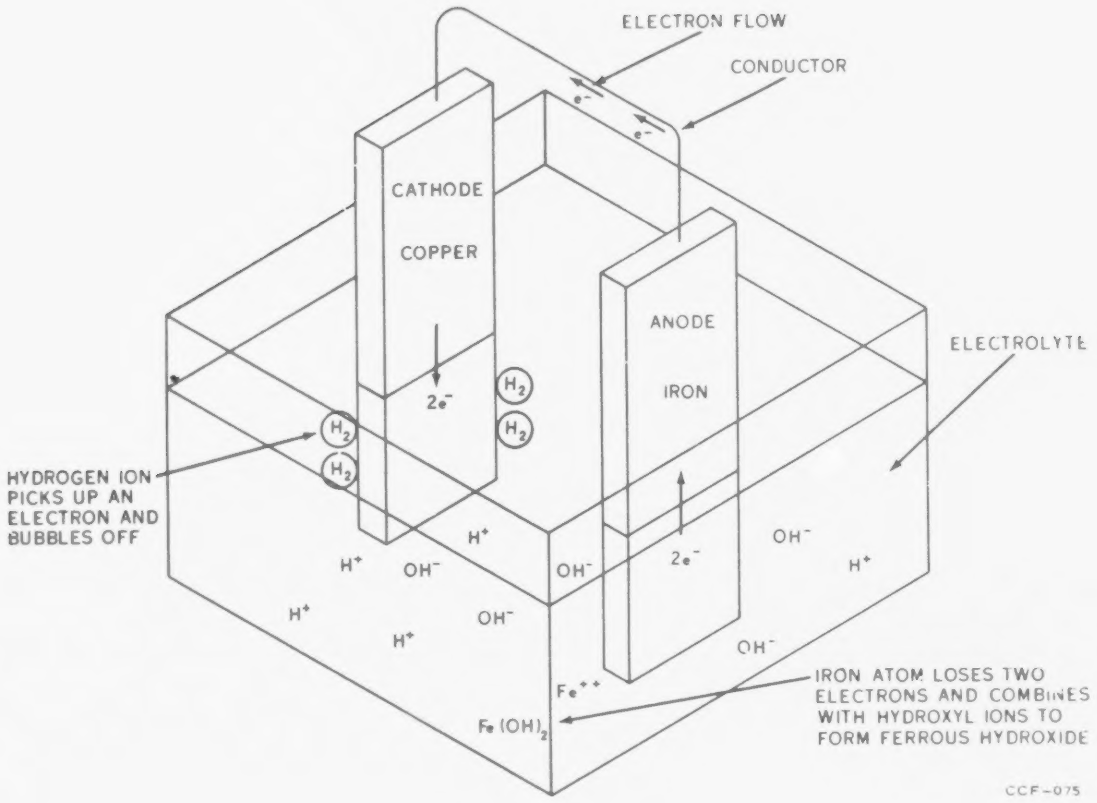
ELECTRON FLOW
CONDUCTOR
e⁻
e⁻
CATHODE
COPPER
2e⁻
H_2
H_2
H_2
H_2
ANODE
IRON
ELECTROLYTE
HYDROGEN ION PICKS UP AN ELECTRON AND BUBBLES OFF
H⁺
OH⁻
OH⁻
2e⁻
OH⁻
H⁺
H⁺
OH⁻
H⁺
H⁺
OH⁻
OH⁻
Fe⁺⁺
Fe(OH)₂
IRON ATOM LOSES TWO ELECTRONS AND COMBINES WITH HYDROXYL IONS TO FORM FERROUS HYDROXIDE
CCF-075

Figure 1-1. Corrosion cell.

j. The condition of the metal surface may not affect the total corrosion, though it may have a tendency to localize the attack.

k. The smaller the anodic area in relation to the cathodic area, the greater the rate of the corrosion at the anode.

Exercises (001):

1. List the parts of a corrosion cell.

2. Which electrode corrodes in a corrosion cell?

3. In which direction does the electron flow in a corrosion cell?

4. _____ is generally needed for any corrosion process to continue.

5. Coarse rust coatings on iron may _____ the rate of corrosion.

6. The smaller the _____ area in relation to the _____ area, the greater the rate of the corrosion at the anode.

002. Identify the effects of reactions that occur at the electrodes in an electrochemical cell.

Steps in the Corrosion Process. A simple corrosion reaction may be explained as follows: Iron in contact with water has an inherent tendency to go into solution as electrically charged iron ions. Since the water must remain electrically neutral, these ions can enter the electrolyte only if an equal number of negatively charged ions are present to unite with the positively charged iron ions. This action displaces hydrogen from the electrolyte. The displaced hydrogen gathers on the surface of the cathode to form a thin, invisible film.

The presence of this film affects the corrosion reaction in two ways: first, by insulating the electrode from the solution; and secondly, by increasing the tendency of the hydrogen to reenter the solution and oppose the corrosion process. This is the first step in the corrosion process, and it may be so effective as to completely stop any further corrosion reaction.

For corrosion to continue, the hydrogen film must be removed. The hydrogen can recombine with oxygen to form water or it can escape from the solution as hydrogen gas. In either event, the hydrogen removal permits the original corrosion reaction to continue at the rate at which the hydrogen film is removed.

This second step in the corrosion process is usually governed by the amount of dissolved oxygen in the water next to the metal. The supply of oxygen is usually governed by many factors, such as the aeration of the water, the temperature, and the concentration of other gases in the solution.

In general, the iron ions that enter into the electrolyte are soon turned to rust. This affects the corrosion reaction by permitting the release of more iron ions. The rust and other substances from the water may form a protective coating on the surface of the metal, or in solutions where the oxygen supply is limited, the oxygen is gradually removed by combining with the iron ions and hydrogen to decrease the rate of corrosion.

Since corrosion involves a two-step process, the rate at which any reaction takes place generally is determined by the rate of the slowest reaction. If the two effective steps are nearly equal, either the slowest or the fastest reaction affects the net corrosion rate.

Exercises (002):

1. Iron in contact with _____ has an inherent tendency to go into _____ as electrically charged iron _____ .
2. Displaced hydrogen will gather on the _____ of the _____ to form a thin, invisible _____ .
3. The presence of the hydrogen film will _____ the electrode from the _____ .
4. If corrosion is to continue, the hydrogen film must be _____ .
5. Hydrogen either _____ as a gas or _____ with oxygen.
6. The hydrogen removal permits the original corrosion reaction to continue at the rate at which the film is _____ .
7. The corrosion process is generally governed by the amount of dissolved _____ in the water.
8. Iron ions that enter into the electrolyte are soon changed to _____ .
9. Rust may form a protective _____ on the metal's _____ .
10. Oxygen combines with _____ ions and _____ to decrease the rate of corrosion.

003. Match basic chemical terms with the correct description or definition.

Basic Chemical Terms. This brief discussion of corrosion reactions has given you an insight into the nature of corrosion. To understand the mechanics of the corrosion process thoroughly, we must define some of the basic chemical terms that will be used throughout our study of corrosion and its control.

Physical properties. The physical properties are those that describe what a specimen is like. Color, odor, taste, density, and freezing point are physical properties that identify various types of matter.

Chemical properties. The chemical properties are those that describe the way matter behaves when it is placed in contact with other kinds of matter. For example, hydrogen combines with oxygen to produce water.

Elements. An element is a substance that cannot be broken down by chemical means to form any other substance or element. Pure water can be broken down into its two elements—hydrogen and oxygen.

Substance. A substance is the physical matter of which a thing consists. It may contain one element or more than one element. For example, the element oxygen is a substance and the element hydrogen is a substance. When you combine hydrogen and oxygen in proper quantities, they form water, which is also a substance.

Atoms. An atom is the smallest unit of an element that can exist alone or in combination with other atoms. The atom is composed of three principal parts: protons, which have a positive charge; electrons, which have a negative charge; and neutrons, which have no charge but contribute to the weight of the atoms. An atom has an equal number of protons and electrons and is electrically neutral (stable).

Ion. An ion is an atom that has gained or lost electrons and has acquired an electrical charge. If one electron is lost (oxidation), the ion exhibits a positive charge. If one electron is gained (reduction), the ion exhibits a negative charge. A positively charged ion attracts a negatively charged ion, and they bond together to form an electrically stable substance.

Oxidation and reduction. Oxidation and reduction are reactions that must take place simultaneously. While one substance is being oxidized, another substance must be reduced, each reaction forming another substance. An example of an oxidation-reduction reaction is when iron changes to iron oxide. The two reactants are iron and oxygen. The iron is oxidized (gave up electrons) and the oxygen was reduced (gained electrons). Oxygen is a very powerful oxidizing agent. Most metals have a tendency to be oxidized; therefore, they are susceptible to corrosion.

Solubility of a substance. Solubility is defined as the amount of a substance that will dissolve into another substance. When a solid is dissolved in a liquid, the solid is termed the solute, the liquid is the solvent.

Exercise (003):

1. Match column A with column B.

Column A

___ 1. Physical properties.
___ 2. Chemical properties.
___ 3. Elements.
___ 4. Substance.
___ 5. Atoms.
___ 6. Ion.
___ 7. Oxidation-reduction.
___ 8. Solubility.

Column B

a. An atom that has gained or lost electrons.
b. Amount of substance that dissolves into another substance.
c. Color, odor, taste, and density.
d. Reactions that take place simultaneously.
e. Smallest unit of an element.
f. Cannot be broken down by chemical means to form any other substance.
g. Describe how matter reacts with other matter.
h. The physical matter of which a thing consists.

1-2. Factors Influencing Corrosion

In any electrochemical corrosion process one or more of many factors may exert influence on the rate of the corrosion. During our study of the corrosion processes, we will not try to list the factors in any order of importance. This is impossible because in a specific environment a different factor may control or dominate the rate of corrosion. We will discuss these factors under the following headings: influence of metals, influence of electrolytes, influence of other elements, and influence of microorganisms.

004. List the factors that influence the rate of corrosion because of the property or condition of the metal and the causes of nonuniformity in metals, and explain selected factors and causes.

Influence of Metals. The factors associated with a metal determine its tendency to corrode. These factors include the electrode potential of a metal, texture of its surface, and its ability to passivate itself or become polarized.

Electrode potential of a metal. The electrode potential of a metal gives an indication of a metal's tendency to return to its natural state. Metals corrode at different rates because of the refinement of their natural compounds. Electrode potential is simply a function of electromotive force. The metals are aligned in chart form (fig. 1-2) according to their single electrode potential. This chart is usually called the activity series of metals, but it is also known as the electrochemical and electromotive series. With data in figure 1-2, you can compare the potentials of the various metals. The element hydrogen is the reference point. As you move up the chart from hydrogen, the metals become increasingly reactive. Accordingly, as you move down from hydrogen, metals become increasingly inert.

In the study of galvanic action, we use a somewhat similar series based upon practical experience. This series, the Galvanic Series of Metals and Alloys, is shown in table 1-1 and consists of combinations of metals in a great variety of environments.

Texture of the metal's surface. If the texture of the surface of a metal is not uniform, there will be localized difference of electrical potential. The nonuniformity of a metal may be caused by differences in the surface composition, different metals in contact, or discontinuous coatings. It may also be caused by unequal stresses or differences in finish. A highly polished finish resists corrosion much better than a rough surface. These nonuniformities always increase the localized rate of corrosion. Observations have shown that these surfaces corrode at the more anodic area rather than uniformly over the entire surface.

Passivation. Some metals and alloys have the inherent ability to become electrochemically inactive or passive under certain conditions because of the formation of oxide films that render a metal more noble. For instance, stainless steel is not far below ordinary steel in its active state (refer to table 1-1); but in its passive state, it is one of the more noble metals. Commonly used metals that do not form natural highly resistant oxide films can be protected by chromate coatings; or if the metal is to be submerged, by the addition of an inhibitor to its liquid environment. Passivity reduces the corrosion rate by (1) reducing the potential difference between the anode and the cathode, (2) polarizing the anode, or (3) polarizing the cathode. Passivity can result from any of the above actions, either acting separately or together.

Polarization. Polarization can be called nature's method of combating corrosion by reducing the electrode potential of a corrosion cell. Polarization is caused by the products that are formed or changed because electrical current has passed through the corrosion cell. It may result from an accumulation of

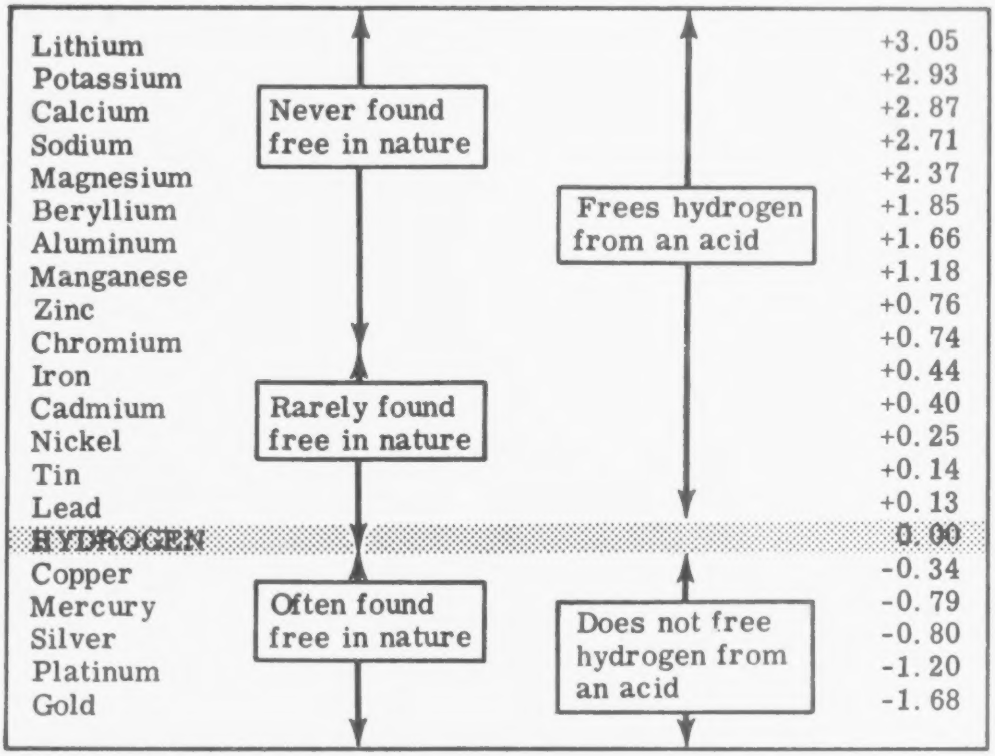
Lithium
Potassium
Calcium
Sodium
Magnesium
Beryllium
Aluminum
Manganese
Zinc
Chromium
Iron
Cadmium
Nickel
Tin
Lead
HYDROGEN
Copper
Mercury
Silver
Platinum
Gold
Never found free in nature
Rarely found free in nature
Often found free in nature
Frees hydrogen from an acid
Does not free hydrogen from an acid
+3. 05
+2. 93
+2. 87
+2. 71
+2. 37
+1. 85
+1. 66
+1. 18
+0. 76
+0. 74
+0. 44
+0. 40
+0. 25
+0. 14
+0. 13
0. 00
-0. 34
-0. 79
-0. 80
-1. 20
-1. 68

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Figure 1-2. Activity series of metal.

metallic ions on the anode, reducing the metal's tendency to go into solution. This process is known as anodic polarization. Cathodic polarization occurs because of the collection of hydrogen bubbles on the cathode surface. When this surface is completely covered with hydrogen, the flow of current is substantially reduced.

Exercises (004):

1. List the factors that influence the rate of corrosion because of the property or condition of the metal.

2. Compare the electrode potential of metals above hydrogen in figure 1-2 to the metals below hydrogen.

3. List the causes of nonuniformity of a metal.

4. How does passivation reduce the corrosion rate?

5. What causes cathodic polarization?

005. Decide whether given statements about the influence of the electrolyte on the rate of corrosion are true or false, and correct any false statements.

Influence of the Electrolyte. The electrolytic factors are those that determine the rate of any subsequent reactions.

Ions and ionization. The conductivity of an electrolyte depends on the presence of small electrically charged particles called ions. Because of these ions, a metal changes to a metallic compound (corroded form of metal). Under the present concept, it is believed that, as metals are being dissolved, some of the atoms break away from the parent metal and enter into the electrolyte as positively charged metallic ions. They leave one or more negatively charged electrons on the parent metal. This process produces ions of one type only.

In addition to this method, ions are also present in the electrolyte because the solution is breaking up (disassociating) into its component parts. To be more specific, in a water electrolyte there are always positively charged hydrogen ions (H^+) and negatively charged hydroxyl ions (OH^-) as a result of the disassociation of the water.

TABLE 1-1

GALVANIC SERIES OF METALS AND ALLOYS

Magnesium (Anodic, or least noble)
Magnesium Alloys
Zinc
Cadmium
Aluminum Alloys
Steel
Cast Iron
Stainless Steel (active)
Lead
Tin
Nickel (active)
Inconel (active)
Brass
Copper
Bronze
Copper-Nickel Alloys
Titanium
Monel
Nickel (passive)
Inconel (passive)
Stainless Steel (passive)
Silver
Platinum
(cathodic, or most noble) Gold

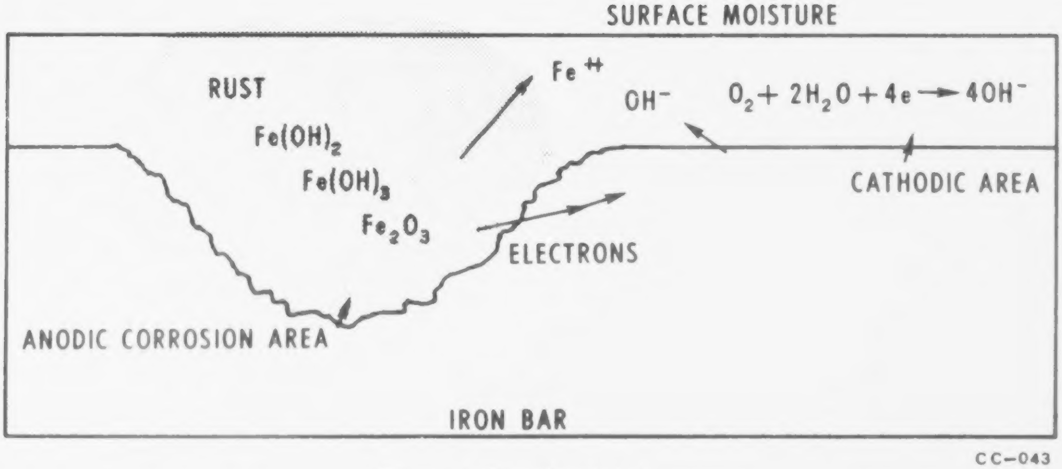

Figure 1-3. Electrochemical cell.

If metal ions from a corroding metal (the anode), such as iron (FE^{++}), to into solution, they are attracted to the hydroxyl ions and join together to form ferrous hydroxide, as shown in figure 1-3. The negatively charged electrons travel through the electrical conductor to the cathode. If there is a sufficient supply of hydrogen ions present, the ions and electrons unite and leave the solution as hydrogen gas.

Generally, the electrolyte is not acidic enough to cause this reaction. More common is the combining of the electrons with oxygen and water to form hydroxyl ions. Oxygen is essential, escept in acidic electrolytes, for the cathodic reaction to take place. Water is essential for both the cathodic reaction and the migration of the ions produced at both electrodes.

The pH of a solution. We pointed out that, in a water electrolyte, hydrogen and hydroxyl ions are present because of the disassociation of water. The amounts of these two ions determine whether a solution has a sour taste and other characteristics of an acid; whether it has a bitter taste, feels soapy, and has other characteristics of an alakli; or whether it is chemically neutral, neither alkaline nor acid.

If the hydrogen ions are in excess, the solution reacts as an acid. If the hydroxyl ions are in excess, the solution reacts as an alkali. If both are present in equal amounts, the solution is neutral. Acids dissolved in water increase the hydrogen ion concentration, while alkalies increase the hydroxyl ions.

The term "pH" plus a numerical figure, e.g., pH 7, designates the hydrogen ion concentration of a solution. The numbers range from pH zero to pH 14, with pH 7 a neutral solution. The pH numbers from 0 to 7 indicate an acidic solution, and the numbers from 7 to 14 indicate an alkaline solution. The farther away from 7 in either direction, the stronger the solution.

The effect of the pH of an electrolyte is illustrated in figure 1-4. Mild steel is the specimen, water is the electrolyte, and sodium hydroxide or hydrochloric acid is added to arrive at the various pH levels. Note that, at about pH 4 to pH 9, the corrosion process takes place at a steady rate because a soluble film of iron oxide has formed, offering some protection.

Corrosion continues as rapidly as the oxygen in the solution can spread through the protective layer. Since the film is unchanged within the above range of pH, the corrosion rate is not altered except by a change in the supply of oxygen. At pH 9.5, an increase of alkalinity extends its effect to the steel surface. As the alkalinity of the solution is further increased, the corrosion rate is

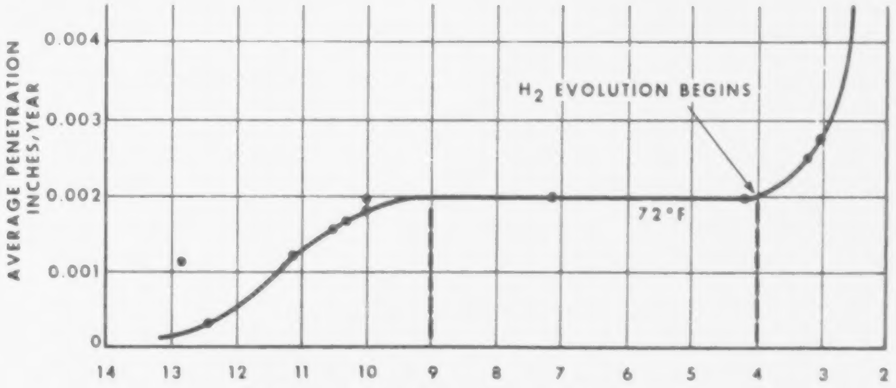

Figure 1-4. Effects of pH of a solution.

expected to decrease as shown. Within the acid region, pH less than 4, the alkaline film is destroyed. The acid reacts directly with the steel surface and rapidly increases the rate of corrosion.

Oxygen in the solution. The influence of dissolved oxygen is by far the most important of the external factors affecting the rate of corrosion. The corrosion rate is usually proportional to the amount of dissolved oxygen in the electrolyte. Gaseous oxygen, as it exists in the atmosphere, must reach the surface of the metal before it can enter into the main corrosion reaction. When the oxygen reaches the surface of the cathode, it combines with the hydrogen ions to destroy the protective film that has formed.

The rate at which oxygen dissolves into the solution is influenced by the solubility of the oxygen, the percent of oxygen saturation of the solution, and the amount of agitation at the solution's surface. The concentration of oxygen in a solution is proportional to the pressure of the oxygen above the solution. Oxygen is more soluble than other gases in the air, and the total volume of oxygen in any solution equals about 35 percent of the total of all the dissolved gases.

The rate of solubility is governed by the concentration of oxygen already in the solution. Thus, it is highest when there is no oxygen in the solution and zero when the solution is completely saturated. In atmospheric corrosion, a film of moisture is always saturated with oxygen so that this important factor always exerts a constant corrosion effect.

While oxygen in the solution is usually a dominating factor in the corrosion process, there have been cases where metals deteriorate rapidly in the absence of oxygen. This may be due to direct chemical attacks under conditions that permit hydrogen gas to escape from the surface. Iron in ordinary tap water allows enough of this reaction to take place to account for about 3 percent of the total corrosion.

Temperature. The temperature at which corrosion takes place has a marked effect on the rate of corrosion. Its main influence is on the supply of dissolved oxygen that is available at the surface of the metal. As the temperature increases, the supply of oxygen decreases. As the supply of oxygen is decreasing in water at pH 7 to 8, the rate of corrosion increases until the maximum rate is reached at about 175° F. As the temperature is further increased, the rate of corrosion decreases until, at about 212° F., it is practically zero.

Also, as the temperature rises, the rate of chemical reaction increases. The chemical reaction rate is usually more rapid than the oxygen depolarization of the cathode. For this reason, the concentration of dissolved oxygen in the solution controls the overall effect of any increase in temperature.

Exercise (005):

1. Identify each statement as true or false by placing a T or F before it, and correct the false statements by changing one or two words.

___ a. Metals, when dissolving, form negatively charged metallic ions.

___ b. The conductivity of an electrolyte depends on charged particles called ions.

___ c. Water dissociates into negatively charged hydrogen ions and positively charged hydroxyl ions.

___ d. If the hydrogen ions are in excess, the solution reacts as an acid.

___ e. A pH number of 0 indicates a neutral solution.

___ f. The corrosion of iron decreases with an increase in pH.

___ g. The corrosion of iron increases with a decrease in pH.

___ h. The corrosion rate is usually proportional to the amount of dissolved oxygen in the electrolyte.

___ i. The rate of solubility is governed by the concentration of oxygen already in the solution.

___ j. A direct chemical attack on metals does not depend upon the oxygen concentration.

___ k. As the temperature increases, the supply of oxygen increases.

___ l. As the temperature rises, the rate of chemical reaction increases.

006. Complete given statements about how other elements influence the rate of corrosion.

Influence of Other Elements. So far, we have been discussing the corrosion of metals in pure water containing oxygen, but pure natural water is rare. Substances other than oxygen are nearly always present and exert their influence on the rate of corrosion. The effects of these impurities are important in any study of corrosion problems. These impurities may be suspended or dissolved in water as solids or gases and may be organic or inorganic. Some of them are in the rain drops when they are formed, while the water picks up others as it flows over the soil and into the earth's structure.

Atmospheric substances are the first to be absorbed in the natural formation of water. Rain is usually saturated with oxygen and nitrogen and absorbs other substances as it falls through the atmosphere. Atmospheric corrosion depends on the nature of the water film that is in contact with the surface of the metal.

In industrial atmospheres, this film is usually acidic because of the presence of the sulfur dioxide and carbon dioxide fumes emitted from factories and automobiles. These fumes combine with elements in the atmosphere to form sulfuric and carbonic acids. Some industrial atmospheres contain as much as 10 parts per million of surfur oxides and 800 to 1,000 parts per million of carbon dioxide, while in rural areas, their concentration is relatively low. The high rate of corrosion in industrial areas is usually due to the sulfur dioxide content of the atmosphere.

Solid matter in the air tends to increase the rate of corrosion (by sulfur dioxide fumes that have changed to acids) by holding the acid in contact with the metal surface for a longer period of time. Other substances that also exert influence on the rate of corrosion are hydrogen sulfide, chlorine, inert gases, acids, alkalies, and salts.

Carbon dioxide. Carbon dioxide is always present in the atmosphere and is usually present in water. Carbon dioxide in the amount usually found in fresh water has little influence on the rate of corrosion. But carbon dioxide acts like an acid, and by decreasing the pH of a solution, it accelerates the rate of corrosion. The main effect of carbon dioxide is its influence on the solubility of the carbonates that commonly form the protective coatings on metals. Normally, these carbonates are only slightly soluble in pure water. However, in the presence of carbon dioxide, more soluble bicarbonates form and the remaining carbonates enter into the solution, leaving a poorly protected metal surface.

Hydrogen sulfide. When hydrogen sulfide is present in water, the water becomes acidic, and rapid corrosion occurs even in the absence of oxygen. As hydrogen sulfide comes into contact with oxygen, it enters into the corrosion reaction as sulfuric acid. When limited oxygen is available, the corrosion products of iron consist mainly of sulfur or iron sulfide. These products are generally cathodic to the surrounding metal and cause localized corrosion while increasing the size of the cathode.

Chlorine. Chlorine does not often occur in solutions except where it is used for water treatment, but the addition of chlorine increases the acidity of the water. The type of corrosion that takes place because of this increased acidity is very similar to the reactions produced by hydrogen sulfide. Small amounts of chlorine have a slightly accelerating effect on the corrosion of steel, because the chlorine ions interfere with the formation of protective films. These ions also tend to destroy any films that have already formed by penetrating the film and breaking its contact with the metal.

Inert gases. As gases enter into a solution, they tend to decrease the rate of corrosion. Previously, we pointed out that oxygen equals approximately 35 percent of the total volume of dissolved gases in a solution. If a large quantity of inert gases is in contact with the same solution, then the percentage of oxygen in contact with the same solution must be less. Consequently, the amount of oxygen dissolving into the solution must also be proportionately lower.

In addition to the gases that it absorbs in the atmosphere, rain, after it reaches the ground, also picks up other substances as it flows along its way. Organic matter is derived from the surface soils and inorganic salts come from deeper sources. As these substances are picked up by the once neutral rainwater, they exert influence on the net corrosion rate.

Again using iron as the basis of our discussion, we will describe the effects of these substances in three general groups: (1) acids, (2) alkalies, and (3) salts.

Acids. Neutral solutions that have become acidic tend to increase the rate of corrosion as the strength of the solution increases. In nonoxidizing acids, corrosion takes place both by the escaping of hydrogen gas and the depolarization of the cathode. In the presence of oxygen, the rate of corrosion by these solutions may be greater than 10 times the rate in the absence of the oxygen.

It has been found that a nonoxidizing acid, such as sulfuric acid, will corrode pure iron more slowly than gray cast iron, which consists of dissimilar ingredients. In oxidizing acids, such as nitric acid, the opposite is true. The reactions of the two acids may differ because the cast iron, because of its dissimilar constituents, becomes passive more quickly than pure iron.

Where both acids and ferrous salts exist in a solution, corrosion is less active than in solutions containing the acid only. However, the addition of ferric salts greatly increases the rate because of their depolarizing power.

Alkalies. Neutral solutions that have become alkaline tend to decrease the rate of corrosion of iron as the pH of the solution is increased. This seems to be more true in hydroxide alkaline solutions than in carbonate alkaline solutions, because the hydroxide increases the hydroxyl ions in the solution.

Diluted hydroxide alkaline solutions may become more corrosive when exposed to air because they absorb carbon dioxide and change to carbonate solutions. As we previously noted (refer to fig. 1-4), a hydroxide solution forms a good corrosion-resistant film on the surface of iron, whereas carbonate solution forms a poorly resistant film.

Salts. Salts that enter into a solution can either retard or increase the rate of corrosion, depending on their nature, their concentration, and other factors. Because different salt solutions or different concentrations of the salt in a solution can cause a difference in potential, we will not attempt to describe all of the effects that result from the existence of salts in a solution. A general observation of the actions of salts on iron or steel is summarized as follows:

a. Potassium chloride, sulphate, or nitrate yields a soluble product and increases the rate of corrosion.

b. Zinc sulfate yields a soluble anodic product and an insoluble cathodic product, slightly increasing the rate of corrosion.

c. Sodium carbonate or phosphate and potassium ferricyanide yields a soluble cathodic product and an insoluble anodic product which form a highly protective film. In such cases the corrosion rate is almost zero.

d. Potassium chromate completely passivates the iron.

One other salt that warrants particular notice is the addition of common salt (sodium chloride) to a solution. It has an important role in any corrosion process because it changes the electrical conductivity of an electrolyte. In solution, salt dissociates into its separate elements, sodium and chloride, and causes the solution to be less resistant to the flow of current between the anode and the cathode.

Exercises (006):

1. Atmospheric corrosion depends on the nature of the water ______ that is in contact with the surface of the metal.
2. Carbon dioxide, in water, acts as an ______ and will ______ the rate of corrosion.
3. When hydrogen sulfide is present in water, the water becomes ______ , and corrosion is ______ .
4. The addition of chlorine to water increases the ______ .
5. Inert gases in water tend to ______ the rate of corrosion.
6. Neutral solutions that have become ______ tend to increase the rate of the corrosion of iron.
7. Neutral solutions that have become ______ tend to decrease the rate of corrosion of iron.
8. A hydroxide solution forms a good ______ film on the surface of iron.
9. Potassium chromate completely ______ iron.
10. Sodium chloride in water changes the conductivity of the ______.

007. List the microorganisms that influence corrosion and describe how each causes corrosion to occur.

Influence of Microorganisms. Certain living organisms in contact with metal surfaces tend to destroy the metal. In some cases microbacteria reduce the rate of corrosion, but in most cases they assist in the formation of electrochemical corrosion cells. In our discussion of these organisms, we will not attempt to describe every type, but we will consider them in three general groups: (1) anaerobic bacteria, (2) aerobic bacteria, and (3) fungi.

Bacterial corrosion occurs either as a direct or an indirect result of the activity of certain bacteria. Their activity influences the rate of reaction at the electrodes, permits a corrosive environment to develop, or produces thick deposits that allow concentration cells to form.

Microorganisms are classified according to their ability or inability to develop in an oxygen environment. Aerobic bacteria develop where there is a high concentration of dissolved oxygen. Anaerobic bacteria develop where there is little or no dissolved oxygen.

Anaerobic bacteria. Anaerobic bacteria are often referred to as the sulfate-reducing bacteria. This group contains several different species. Each species is capable of using cathodic hydrogen or hydrogen from various organic compounds to produce hydrogen sulfide.

Aerobic bacteria. This group also contains several different species, all of which thrive in water that is slightly acidic. One species, thiobacillus thiooxidians, is capable of oxidizing or reducing sulfur to produce sulfuric acid. The species crenothrix does not seem to attack iron directly, but ingests ferrous ions from the solution to produce ferrous hydroxide. The ferrous hydroxide is then oxidized to ferric hydroxide (red dust) by the dissolved oxygen in the solution. Corrosion cells can develop under these red dust deposits because of the absence of oxygen. The corrosive action of the cell may then be accelerated by the formation of anaerobic bacteria under the deposit.

Fungi and slime. The slime-forming organisms are generally members of the lower plant group of the plant kingdom. This group is distinguished from the other plant groups by the absence of leaves, roots, and stems. It is found in nearly all fresh water but is more predominant in tropical atmospheres. The plants can be transported by air currents or by mites carrying various bacteria.

As these carriers die, fungus growths are formed. These growths accumulate moisture that becomes acidic, approximately pH 4, and severely attack metals and other materials. The slimes, algae that thrive in sunlight and attack metals, give off oxygen that combines with cathodic hydrogen to depolarize corrosion cells.

Any one of several factors can exert influence on the rate of a corrosion reaction. A metal exerts influence by its electrode potential, texture, and ability to passivate or polarize during the reaction. The influence exerted by the electrolyte is governed by the solution's constituents, its pH, and ability to absorb oxygen. Microorganisms influence the reaction rate by altering the pH of the electrolyte. Each of these groups of factors, separately or in combination, can speed up or slow down a corrosion reaction to produce one of several forms of corrosion.

Exercises (007):

1. List the microorganisms that influence corrosion.

2. Which type of bacteria develops in the absence of oxygen?

3. Which type of bacteria uses cathodic hydrogen to produce hydrogen sulfide?

4. Which type of bacteria produces sulfuric acid and ferrous hydroxide?

5. What is the effect of fungus growth on metals?

6. How does slime-forming algae attack metals?

1-3. Types of Corrosion

Corrosion is visible in many forms and is typed in different ways. For descriptive purposes, we will discuss the types under their commonly accepted titles: uniform etch, pitting, intergranular, exfoliation, galvanic, concentration cell, stress, fatigue, and filiform.

008. Given a list of descriptive statements about corrosion, match each statement with the applicable type of corrosion.

Uniform Etch. Uniform etch corrosion results from a direct chemical attack on a metal surface. These chemicals may be salts deposited from coastal operations, urine spray, battery acid spillage, or gases absorbed from the environment. There are three factors that can produce a cyclical action of this type of corrosion. These are (1) chemicals, (2) water, and (3) oxygen.

We will use carbon dioxide and iron in an example of a possible uniform etch reaction. The carbon dioxide reacts with water to form carbonic acid. The carbonic acid reacts with the iron to form ferrous ions The ferrous ions are then oxidized by the oxygen in the solution to ferric ions, and thus set free carbon dioxide The hydrogen has also been oxidized to form water. Now the carbon dioxide and water can recombine and repeat the corrosive cycle.

On a polished surface, uniform etch is first seen as a general dulling of the surface. If this corrosion is allowed to continue, the surface becomes rough and sometimes frosted.

Pitting. Though some factors influence the uniform destruction of metal surfaces, other factors influence a localized attach commonly called pitting corrosion. This localized attack can be attributed to any of the factors previously discussed that alter the size of the anodic or cathodic areas on a metal surface. Small, evenly distributed anodic and cathodic areas result in uniform corrosion. Large areas of either type produce pitting corrosion, as shown in figure 1-5.

A pitting corrosion of aluminum or magnesium is first noticed as white or gray powdery deposits that blotch the metal surface. The pitting of iron produces red and brown deposits. When you clean away these deposits, you find pits or holes.

Intergranular. Intergranular corrosion is a selective attack along the grain boundaries of a metal. A highly magnified cross section of an alloyed metal shows the granular structure of that metal. This structure consists of quantities of individual grains, each grain with a definite grain boundary.

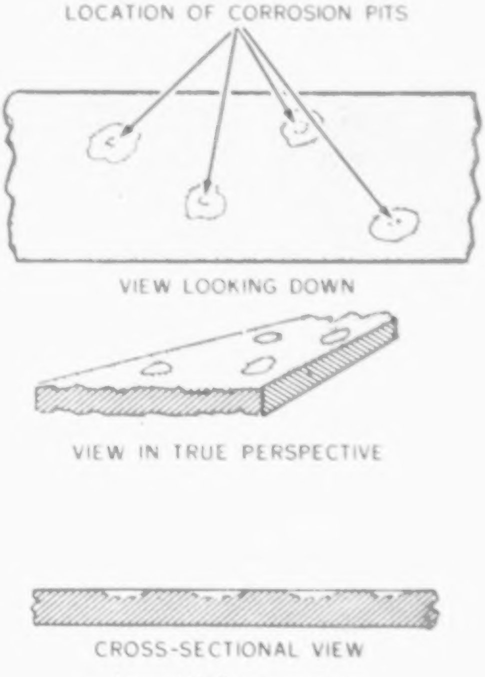

Figure 1-5. Pitting corrosion.

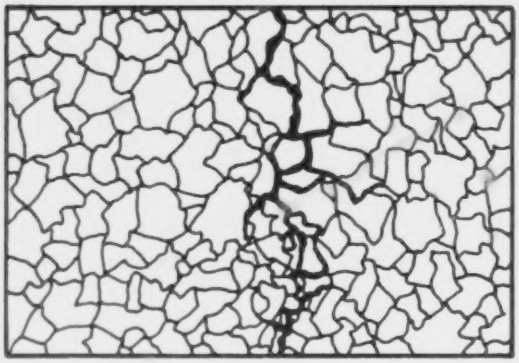

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Figure 1-6. Intergranular corrosion.

Intergranular corrosion, shown in figure 1-6, is caused by the precipitation of the alloying elements out of the grain and into or near the grain boundary. The grain, losing its alloying elements, becomes anodic to the surrounding grains. In the presence of an electrolyte, current flows and rapid intergranular corrosion occurs.

Exfoliation. Exfoliation corrosion, shown in figure 1-7, is a visible form of intergranular corrosion. The expanding corrosion products just below the metal surface cause a blister to form. Exfoliation corrosion is usually found on extruded metals. The blisters usually appear where the extruding dies have forced the crystal structure of the metal to change direction.

Galvanic. The theory of galvanic corrosion is fully explained by the electrochemical theory of corrosion. When two dissimilar metals are coupled together in the presence of an electrolyte, galvanic corrosion occurs. It is usually recognized by the presence of the corrosion deposits at the place where the metals are joined together. A prime example is a brass bolt attached to an aluminum panel, shown in figure 1-8.

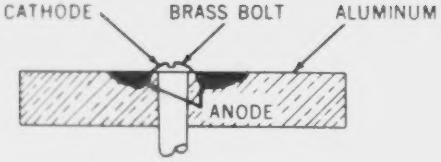

Figure 1-8. Galvanic corrosion.

All commonly used metals cause magnesium to corrode. Therefore, the metals or fasteners that must be in contact with magnesium should be close to magnesium in electrical potential.

Each group of metals and alloys shown in table 1-2 are considered to be similar in potential. Combining metals within a group usually reduces the rate of galvanic corrosion, and combining metals from different groups increases the rate of corrosion.

When practical, use rivets, bolts, and nuts that are of the same material as the main structure. If it is not possible to use the same material, use sacrificial washers, insulating tape, or sealant to isolate the galvanic couple.

Galvanic corrosion is not limited to easily recognizable dissimilarities. It can also occur in the following examples:

- New metal is anodic to old metal.
- Cut surfaces are anodic to normal surfaces.
- Stressed surfaces are anodic to nonstressed surfaces.
- Surface imperfections and impurities are anodic to normal surfaces.

Concentration Cell. Just as two dissimilar metals joined together cause corrosion, so do dissimilar conditions within the electrolyte. This may be due to different substances in the solution or to varying concentrations of these substances. Generally, metals in more concentrated solutions are anodic to metals in contact with the diluted part of the solution. Concentration cells are formed whenever the dissolved oxygen is not uniform throughout the entire solution. We will examine concentration cells under their three main types: metal-ion cell, oxygen concentration cell, and active-passive cell.

Metal-ion cell. As you noted in the discussion of ions and ionization, ions of a metal are given up to enter into the solution. Whenever there is a higher metal-ion concentration in one area than another, an electrical potential is created between these areas. The area with the higher metal-ion concentration will be cathodic to the other area. Current will flow, through the metal, from the lowest to the highest concentration area.

A typical metal-ion cell may be found around a riveted lap joint, as shown in figure 1-9. This reaction is caused by the relatively high ion concentration in the stagnant area just under the edge of a lap joint. These stagnant areas usually result from an electrolyte flow that is not sufficient to carry away all of the metal ions that enter into the solution.

The lower ion concentrations are found at the outer surface of the lap joint. Corrosion is found here because the electrochemical action tries to make the ion concentrations uniform in potential. Therefore, the

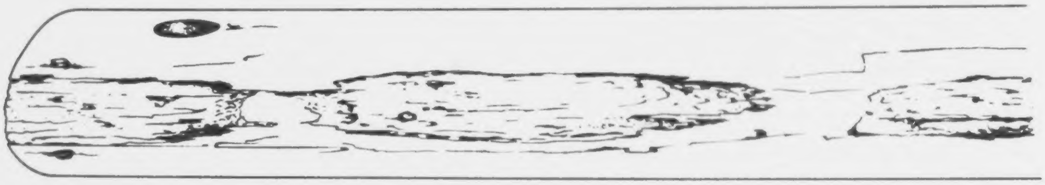

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Figure 1-7. Exfoliation corrosion.

TABLE 1-2

GROUPING OF METAL ALLOYS

GROUP I	Magnesium and its alloys. Aluminum alloys 5052, 5056, 5356, 6061, 6063 and tin.
GROUP II	Aluminum (All), Zinc, Cadmium, Tin, Tin-Lead (Solder)
GROUP III	Zinc, Cadmium, Steel, Lead, Tin, Nickel and Nickel alloys, Tin-Lead (Solder) and Titanium.
GROUP IV	Copper and Copper alloys, Nickel and Nickel alloys, Chromium, Stainless Steel, Gold, Silver, and Titanium.

* Metals listed in the same group are considered similar to one another.

* Metals listed in different groups are considered dissimilar to one another.

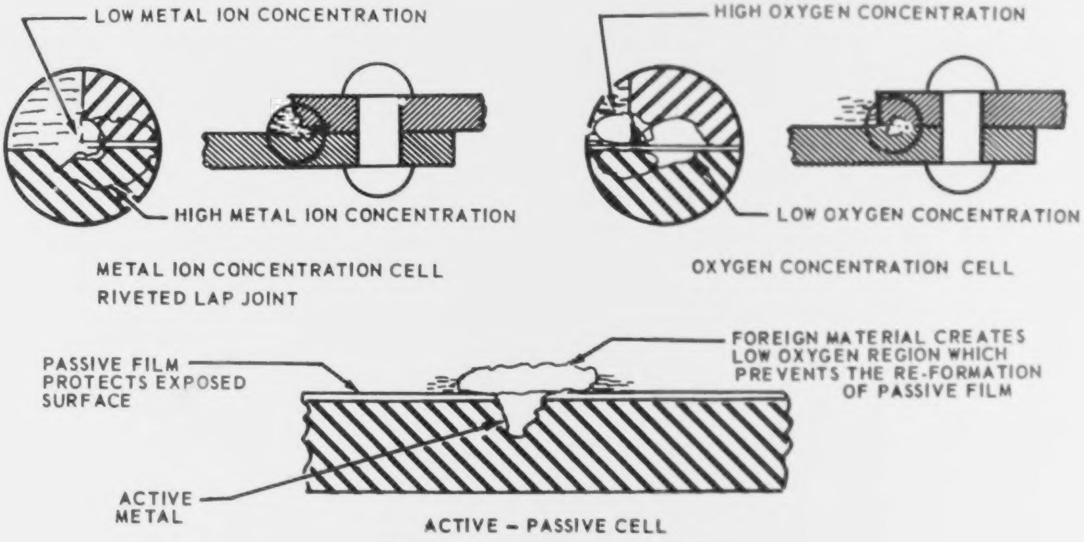
metal at the lower ion concentration is forced to give up more metal ions. The desired ion balance may never be reached because the ions that are forced into solution tend to be carried away by the electrolyte.

Oxygen concentration cell. As we noted in our discussion of oxygen in the solution, the influence of dissolved oxygen is one of the most important external factors affecting the rate of corrosion. Oxygen concentration cells occur when a solution contains varying amounts of dissolved oxygen. A crevice, sharp corner, or lap joint may prevent the oxygen from dissolving uniformly throughout the electrolyte. This nonuniform electrolyte will create an electrochemical corrosion cell, forcing the metal to give up its ions at the area of lowest oxygen concentration, as shown in figure 1-9.

Active-passive cell. Metals that rely on a tightly adherent oxide film for corrosion prevention are prone to active-passive concentration cell corrosion.

These metals—e.g., pure aluminum, titanium, and corrosion-resistant steels—form their own corrosion-resistant films when they are in contact with oxygen from the atmosphere. If the film is broken, it immediately repairs itself as long as the metal remains in contact with the oxygen.

If the surface becomes contaminated—e.g., with carbon, salt, or dirt deposits—and the oxygen cannot reach the surface, the oxide film beneath the deposit


LOW METAL ION CONCENTRATION
HIGH METAL ION CONCENTRATION
HIGH OXYGEN CONCENTRATION
LOW OXYGEN CONCENTRATION
PASSIVE FILM PROTECTS EXPOSED SURFACE
FOREIGN MATERIAL CREATES LOW OXYGEN REGION WHICH PREVENTS THE RE-FORMATION OF PASSIVE FILM
ACTIVE METAL

METAL ION CONCENTRATION CELL
RIVETED LAP JOINT

OXYGEN CONCENTRATION CELL

ACTIVE – PASSIVE CELL

Figure 1-9. Concentration cell corrosion.

will be broken. The passive film around the break will be cathodic to the active metal, producing an active-passive concentration cell, as shown in figure 1-9.

The rate of the corrosive attach depends on the supply of oxygen to the entire surface. Since it cannot diffuse into the pit that has formed, the rate at which it bores into the metal will be very great. As the corrosion products gather over the mouth of the pit, the metal at the bottom of the pit becomes more anodic, and the rate of penetration increases as the pit grows deeper.

Stress Corrosion. Stress corrosion is produced by the simultaneous effects of tensile stress and a corrosive environment. If a part in a stressed condition is in contact with an electrolyte, severe corrosion can occur because the stressed area of a part has been found to be anodic to an unstressed area.

Internal stresses are often produced by nonuniform deformation during cold working, such as bending a piece of metal, driving rivets, bolting, and press fitting. Any metal that has been cold-worked should be stress-relieved (annealed) before it is subjected to a corrosive environment.

Generally, stresses in the neighborhood of the yield strength of the metal are needed to cause stress corrosion cracking. When a crack appears, it usually runs parallel to the granular structure of the metal.

Fatigue Corrosion. Fatigue corrosion is a special form of stress corrosion, produced by the effects of an alternating cyclic stress and a corrosive environment. Fatigue corrosion failure generally occurs in two stages. During the first stage, the combined action of corrosion and the cyclic action concentrates the stresses in the vicinity of any pits.

In the second stage, the concentration of stresses causes cracks to develop in the base of the pits. The cracks develop rapidly and gradually penetrate the section until a fracture occurs, as shown in figure 1-10. Fatigue corrosion cracks are different from stress corrosion cracks because they usually run across the granular structure of the metal.

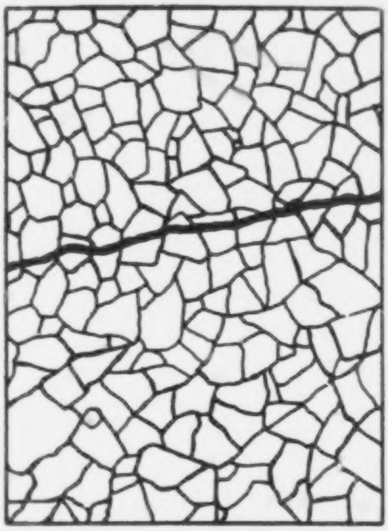


Figure 1-10. Fatigue corrosion.

Generally, fatigue corrosion cracking occurs at a point far below the normal design fatigue limits of the metal. This happens even though there is little evidence of actual corrosion. For this reason, metals subjected to alternating cyclic stresses must be protected, even in mildly corrosive environments.

Filiform Corrosion. Occasionally metals with organic coatings undergo a type of corrosion that results in numerous threadlike filaments of corrosion products under the coating. This type of corrosion is caused by the diffusion of oxygen and water through the coating, and is considered a typical type of oxygen concentration cell. You can control or curtail filiform corrosion by storing aircraft or equipment in a low humidity environment and by using coatings with a high resistance to diffusion by water.

Exercises (008):

1. Match column A with column B. Items in column B may be used more than once.

Column A

___ 1. Expanding corrosion products causing a blister to form.
___ 2. Selective attack along grain boundaries.
___ 3. Threadlike filaments of corrosion products.
___ 4. Metal cracks parallel to grain structure of the metal.
___ 5. Recognized by the presence of corrosion products where dissimilar metals are joined together.
___ 6. Occurring at riveted lap joints.
___ 7. Direct chemical attack.
___ 8. Precipitation of alloy elements out of grain into grain boundary.
___ 9. Metal-ion cell, oxygen concentration cell, and active-passive cell.
___ 10. Metal cracks across the granular structure of the metal.
___ 11. Visible form of intergranular corrosion.
___ 12. Dulling of polished surfaces.
___ 13. Occurring under organic coatings.
___ 14. Localized attack.
___ 15. Caused by the contact of two dissimilar metals in an electrolyte.
___ 16. White or gray powdery deposits on aluminum or magnesium.
___ 17. Alternating cyclic stress and corrosion environment.

Column B

a. Uniform etch.
b. Pitting.
c. Intergranular.
d. Exfoliation.
e. Galvanic.
f. Concentration cell.
g. Stress corrosion.
h. Fatigue corrosion.
i. Filiform.

___ 18. Attributed to factors that alter the size of the anode or cathode on metal.
___ 19. Caused by dissimilar conditions within the electrolyte.
___ 20. Produced by the simultaneous effects of tensile stress and a corrosive environment.

1-4. Appearances of Corrosion

Each metal has its own peculiar indications of corrosion. The effects are the same but corrosion takes different forms.

009. Given a list of descriptive statements about the appearance of corrosion on metal surfaces, match each statement with the applicable type of metal surface.

Magnesium. Since magnesium will always be primed and topcoated, corrosion will appear only where breakdown or removal of the finish occurs. Damaged areas of paint may show a gray powdery corrosion product. If the area has been moist, the corrosion product may be green or black.

Aluminum. This metal appears high in the electrochemical series of elements, and its position indicates that it should corrode very easily. However, the formation of a tightly adhering oxide film offers increased resistance under mild corrosive conditions. Aluminum may be used bare, primed, or painted. Each condition has its own evidence of corrosion.

Bare. Normally bright aluminum will become dull and coated with a whitish powdery residue. Blackened areas and pitting may appear where the residue is removed. Large volumes of white-gray corrosion products may appear on cut edges or corners.

Primed. Corrosion will show up where there is a scratch or gouge, or a blister in the primer. In the early stages a white-gray corrosion product will grow in the damaged area. As the corrosion attack advances, the aluminum will appear etched or mottled around the damaged area.

Primed and painted. Corrosion will appear as a white-gray corrosion product where there is break in the finished coat. Paint will flake off the damaged area. If the area is damp, the paint will lose adhesion and come off in large flakes, leaving the aluminum with a spotted, mottled or etched appearance.

Carbon and Alloyed Steel. If unprotected, ferrous metal surfaces are easily corroded in the presence of moisture. Each type of metal surface treatment has a different appearance of corrosion.

Bare steel surfaces. Bare steel will rust over its entire surface. A severe form of rusting is indicated by a red-to-black scale which may flake off.

Primed steel surfaces. Rust will appear in areas where the primer becomes damaged either mechanically or by exposure to moisture. Since primers used for steel are nearly the same color as rusted steel, light rust will be difficult to identify. Any areas of suspected rust should be wiped lightly with a clean cloth. Rust will wipe off. If it is not removed, further corrosive attack will result in the formation of scale.

Primed and painted steel surfaces. Rust will appear where the paint system has been damaged mechanically or by exposure to moisture, chemicals, or solvents. The underlying steel may be blackened as well as rusted. Again if the corrosion attack is allowed to continue, scale will form.

Cadmium-plated steel. Corroded cadmium will form a dull gray product which can be wiped off. Corrosion will attack steel only if the cadmium is destroyed.

Zinc-plated steel surfaces. Corroding zinc or galvanized coating will form a white corrosion product more voluminous that that of cadmium. Corrosion will attack the steel only in areas where the coating has been destroyed.

Nickel- or chrome-plated steel surfaces. Rust will appear as small spots on the plated surface if there are small pores in the plating. If corrosion is allowed to continue, pitting will result.

Phosphate-coated and grease steel surfaces. Phosphate coatings are applied to steel to hold oil or grease on the surface. Corrosion will start uniformly over the part. It will appear as a red-black darker than common rust.

Corrosion-Resistant Steel. Stainless steels are basic alloys of chromium in iron and are resistant to common rusting, chemical action, and high temperature oxidation. This metal will become black in appearance as it corrodes. The black corrosion product is very tightly bound to the surface and will not come off when rubbed. Corrosion on the surface may appear as pits. If this steel has been plated or painted, the surface will exhibit the same type of corrosion product as described for painted or plated carbon and alloy steels.

Copper and Copper Alloys. These metals are quite resistant to atmospheric corrosion. Protective paint coatings are seldom required because of the inherent resistance of the metal.

Bare copper surfaces. Unfinished copper and its alloys normally take on a darkened copper color. Corroded copper will be greenish-white in color. If the corrosion is caused by an acid environment such as unremoved solder flux, the corrosion products will tend to be more grayish-white and quite voluminous. Corrosion products of copper alloys form a bluish-green coating on the surface.

Primed and top-coated copper. When the coating system is damaged, the exposed copper will darken. After a time, the exposed copper may turn black and be partly covered by a green corrosion product.

Tin-plated copper. As the tin corrodes, a white-yellow corrosion product will appear on the exposed copper. This corrosion is accelerated because tin is sacrificial to copper.

Cadmium-plated copper. If the cadmium plating is removed or damaged, the normal white corrosion products will grow at a rapid rate on the exposed copper. The green-colored corrosion of copper will show up only when the cadmium plating is completely destroyed.

Exercise (009):

1. Match the items in column B with the most appropriate description in column A. Use each item only once.

Column A

___ 1. Appearance of corrosion product will form a white voluminous corrosion product.
___ 2. A severe form of corrosion is indicated by a red-to-black scale which may flake off.
___ 3. A white-yellow corrosion will appear on the exposed metal.
___ 4. A gray powdery corrosion may appear; if wet may be green or black.
___ 5. Black corrosion products which will not come off when rubbed.
___ 6. Surface may become dull and coated with whitish powdery residue. Large volumes of white-gray products may appear on cut edges.
___ 7. Rust will appear as small spots; if corrosion is allowed to continue, pitting will result.
___ 8. In advanced stages of corrosion, surface will appear mottled or etched.
___ 9. Corrosion products are greenish-white.
___ 10. Uniform corrosion on the surface will appear as a red-black deposit.
___ 11. Each type of metal surface treatment has a different appearance of corrosion.
___ 12. After a time the exposed metal may turn black and be partly covered by a green corrosion product.
___ 13. A dull gray corrosion product may appear, which can be wiped off.

Column B

a. Metal surface magnesium.
b. Aluminum bare.
c. Aluminum primed and painted.
d. Bare steel surface.
e. Carbon and alloyed steel.
f. Cadmium-plated steel.
g. Zinc-plated steel.
h. Nickel- and chrome-plated steel.
i. Phosphate-coated steel.
j. Corrosion-resistant steel.
k. Copper - bare.
l. Copper primed and top-coated.
m. Copper tin-plated.

1-5. Corrosion Control Methods

By definition, corrosion control is the effort to minimize the development of and damage from corrosion by properly conducting identification, isolation, and other corrective actions on a timely basis. This means you are to inspect, detect, and promptly perform required maintenance procedures to eliminate the cause of corrosion, and treat the metal surface to prevent further corrosion.

010. Cite three methods of controlling corrosion and list the causes of corrosion.

Methods of Controlling Corrosion. Some of the methods used in decreasing the problem of corrosion damage include frequent inspections, determining the causes of corrosion, and protecting the metal from further attack. The following methods are used:

a. Perform frequent inspections to insure cleanliness and to check for entrapped moisture, the condition of protective coating, and evidence of corrosion. Early detection and prompt action are essential to controlling corrosion.

b. Identify the cause of corrosion. To what environmental condition is the metal exposed? Is there evidence of entrapped moisture in the area? Is there environemnt conducive to fungus and bacteria attack? Have any corrosive chemicals—liquid or vapors—been in contact with the metal? Are two dissimilar metals connected together? Is there any accumulation of dust or other foreign material in the area? If any of the above conditions exist they should be eliminated or corrected.

c. Use protective packing and packaging for shipment and storage of equipment and components.

Exercises (010):

1. Name three methods of controlling corrosion.

2. List the causes of corrosion.

011. List the sequence of treating metal surfaces, name the methods of removing corrosion and protective coatings, and state the processes used for one of the methods.

Metal Surface Treatment. After corrosion has been discovered, the next step is to repair the damage by removing the corrosion and treating the surface to prevent further corrosion attack. The sequence and method of doing this are as follows:

a. Prior to performing corrosion removal procedures, the metal surface must be cleaned to remove foreign matter that mght interfere with the subsequent treatment. Consult the technical order for the correct procedure and type of cleaning material and equipment for the particular task. Soil on the metal surface can be removed by either solvent or displacement action. Besides cleaning the area, the paint coating may have to be removed so that the corrosion can be removed. Paint stripping can be done either mechanically or chemically. The method used depends upon the area in which the corrosion is located. Chemical paint remover can be used if there is no danger of this liquid becoming entrapped in crevices, seams, or interior areas. Mechanical methods of removing paint include grinding, chipping, sanding, and wire brushing.

b. After the metal has been cleaned, corrosion can be removed by mechanical or chemical methods. The removal method will be dictated by the accessibility of the area and the degree and type of corrosion. However, the chemical method should not be used if the chemicals may become entrapped. Consult the appropriate technical order or maintenance manuals in selecting the chemical corrosion removers. Mechanical methods include abrasive blasting, filing, wire brushing, grinding, and polishing.

c. Apply a protective coating system after corrosion removal or if corrective maintenance has damaged the protective coating. A protective coating system includes pretreatment, primers, and top coat. The selection of the proper coating system depends on the metal to be coated, the environment to which the item will be subject, and the service life requirement for the coating.

Exercises (011):

1. What are the steps used in treating a metal surface for corrosion?

2. List the two methods of removing paints and corrosion.

3. When can you use the chemical method?

4. How is corrosion removed mechanically?

ANSWERS FOR EXERCISES

Reference:

001 - 1. Anode, cathode, electrolyte, and conductor.
001 - 2. Anode.
001 - 3. Anode to cathode.
001 - 4. Oxygen.
001 - 5. Accelerate.
001 - 6. Anodic; cathodic.

002 - 1. Water; solution; ions.
002 - 2. Surface; cathode; film.
002 - 3. Insulate; solution.
002 - 4. Removed.
002 - 5. Escapes; combines.
002 - 6. Removed.
002 - 7. Oxygen.
002 - 8. Rust.
002 - 9. Coating; surface.
002 - 10. Iron; hydrogen.

003 - 1 1. c.
2. g.
3. f.
4. h.
5. e.
6. a.
7. d.
8. b.

004 - 1. Electrode potential of a metal; texture of the metal's surface; passivation; polarization.
004 - 2. The metals above hydrogen are more reactive; below, more inert.
004 - 3. Difference in surface composition; different metals in contact; discontinuous coatings; unequal stresses; and differences in finish.
004 - 4. By reducing the potential difference between anode and cathode, polarizing the anode, and polarizing the cathode.
004 - 5. The collection of hydrogen bubbles on the cathode surface.

005 - 1. a. F. Change negatively to positively.
b. T.
c. F. Change negatively to positively and positively to negatively.
d. T.
e. F. Change 0 to 7.
f. T.
g. T.
h. T.
i. T.
j. T.
k. F. Change oxygen increases to oxygen decreases.
l. T.

006 - 1. Film.
006 - 2. Acid; accelerate.
006 - 3. Acidic; rapid.
006 - 4. Acidity.
006 - 5. Decrease.
006 - 6. Acidic.
006 - 7. Alkaline.
006 - 8. Corrosion-resistant.
006 - 9. Passivates.
006 - 10. Electrolyte.

007 - 1. Anaerobic bacteria; aerobic bacteria, and fungi.
007 - 2. Anaerobic bacteria.
007 - 3. Anaerobic bacteria.
007 - 4. Aerobic.
007 - 5. It accumulates moisture which becomes acidic and severely attacks metals.
007 - 6. By giving off oxygen that combines with cathodic hydrogen to depolarize corrosion cells.

008 - 1. 1. d.
2. c.
3. i.
4. g.
5. e.
6. f.
7. a.
8. c.
9. f.
10. h.
11. d.
12. a.
13. i.
14. b.
15. e.
16. b.
17. h.
18. b.
19. f.
20. g.

009 - 1. 1. g.
2. d.
3. m.
4. a.
5. j.
6. b.
7. h.
8. c.
9. k.
10. i.
11. e.
12. l.
13. f.

010 - 1. Frequent inspection, determining cause of corrosion, and protecting metal.
010 - 2. Entrapped moisture, fungus and bacteria attack, corrosive chemicals, and dissimilar metals.

011 - 1. Clean surface, remove paint if necessary, remove corrosion, and apply protective coating.
011 - 2. Chemical and mechanical.
011 - 3. Chemicals can be used when there is no danger of the chemicals becoming entrapped.
011 - 4. Abrasive blasting, filing, wire brushing, grinding, and polishing.

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MODULE 10012

BASIC TECHNIQUES OF WAVEFORM MEASUREMENT USING AN OSCILLOSCOPE

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Preface

A BASIC requirement exists that all electronic maintenance personnel know how to operate and use the oscilloscope. Yet, the o'scope remains as one of the most misused and least understood pieces of test equipment.

This module explains the operation of the oscilloscope and the function of its many controls. It is written from a general viewpoint and should apply to the majority of dual trace, triggered sweep oscilloscopes in use within the military. A conscientious study and use of the material contained in this module should enhance your ability to properly operate and use this versatile test instrument.

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Material in this module is technically accurate, adequate, and current as of May 1981.

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Hewlett-Packard Bench Briefs, March-April 1980,
Basic Techniques of Waveform Measurement Using an Oscilloscope — Part 1.
Hewlett-Packard Bench Briefs, May-June 1980,
Basic Techniques of Waveform Measurement Using an Oscilloscope — Part 2

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Chapter

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NOTE: In this module, the subject matter is developed by a series of student-centered objectives. Each of these carries a three-digit number and is in boldface type. Each sets a learning goal for you. The text that follows the objective gives you the information you need to reach that goal. The exercises following the information gives you a check on your achievement. When you complete them, see whether your answers match those in the back of this module. If your response to an exercise is incorrect, review the objective and its text.

Waveform Measurement

GENERALLY SPEAKING, a technician becoming familiar with a piece of test equipment is concerned about three things:

1. Knowing where and how to connect the test instrument,
2. Knowing how to adjust the controls, and
3. Knowing how to interpret the data.

This module addresses these three basic concerns as they apply to the oscilloscope. Why the oscilloscope? Because it is probably one of the most versatile troubleshooting instruments you have on the bench. You can use it to measure voltage levels (from DC to microwave), phase differences, signal presence (or absence), logic highs or lows, frequency response, distortion, and complex waveform analysis (wave shape, overshoot, etc.), to name a few. We obviously can't show you how to use the scope in all these endeavors. We can, however, give you the basics to cover the three original concerns — how to connect it, adjust it, and read it.

Once these concepts are mastered, the only remaining hurdle for you is to locate the controls on the scope's front panel. Most manufacturers try to help you by grouping similar controls together and separating the different groups by color or lines on the front panel.

001. State the basic operation of an oscilloscope and the purpose of the various vertical and horizontal input controls.

Getting Back to the Basics. The oscilloscope presents a voltage versus time display of the waveform on a cathode ray tube (CRT). Inside the CRT, an electron beam draws the waveform on a phosphor-coated screen. This screen presents three types of information: (1) voltage information on vertical or Y axis, (2) time information on the horizontal or X axis, and (3) intensity information on the Z axis. All oscilloscopes have controls to adjust the voltage, time, and intensity information in order to present a meaningful picture on the CRT. Figure 1-1 shows a block diagram of the basic circuits that these controls operate.

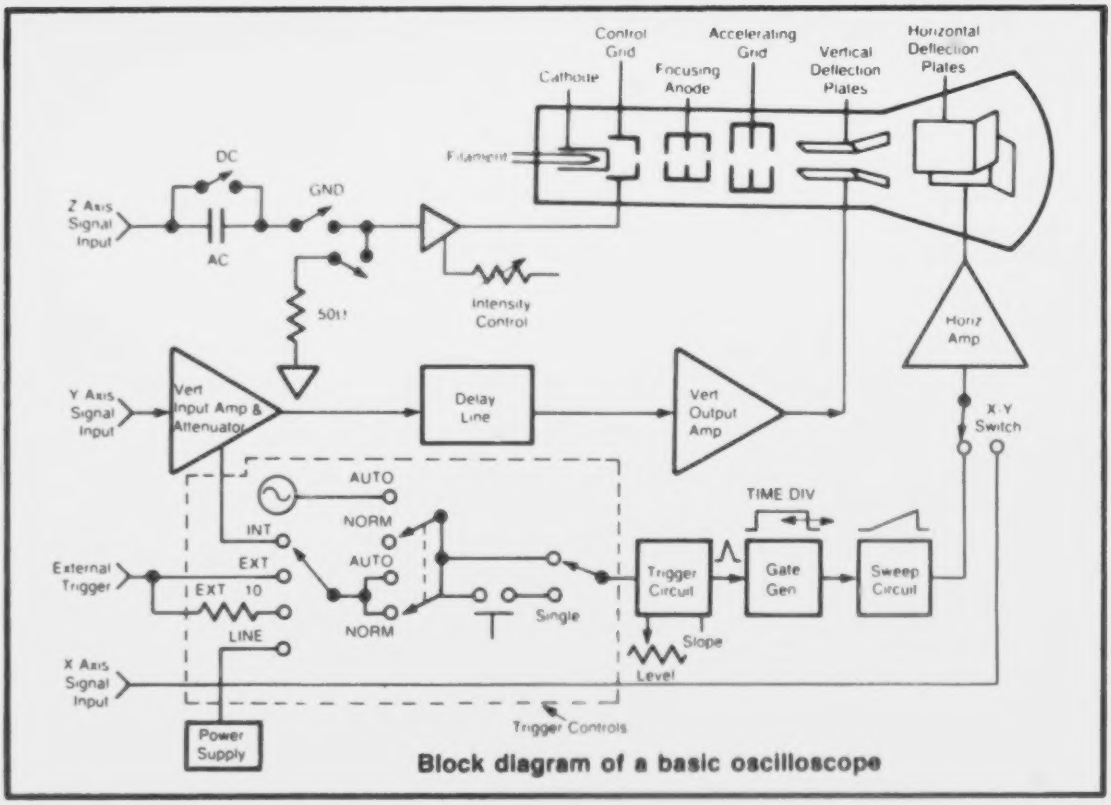
The vertical input. As shown in figure 1-1, the input signal is connected to the vertical input amplifier. The vertical amplifier either attenuates or amplifies the signal for convenient viewing.

The next block the incoming signal encounters is the delay line. The delay line allows the sweep generator circuitry time to start a sweep before the signal reaches the CRT vertical deflection plates. This coordination of vertical and horizontal timing by the delay line enables viewing of the leading edge of the signal. This will be explained in greater detail later on. The vertical output amplifier provides additional amplification that is required by the CRT vertical deflection plates.

The time axis. Although precise horizontal deflection rates are not required in many general-purpose applications, the more sophisticated scope applications require precise control of the sweep timing with respect to the signal under test. This precise control increases time interval measurement accuracy and insures horizontal stability of the trace. Lack of this stability is seen as "jitter."

Intensity. Intensity information is provided in the form of bias control on the CRT grid which controls the density of the electron beam. If the negative bias is sufficient, the CRT is cut off, eliminating the trace.

Vertical Input Controls. The vertical input controls generally consist of an input coupling switch, calibrated attenuator, and position control. A dual-trace scope will


Control Grid
Accelerating Grid
Vertical Deflection Plates
Horizontal Deflection Plates
Cathode
Focusing Anode
Filament
DC
GND
Z Axis Signal Input
AC
Intensity Control
50Ω
Horiz Amp
Y Axis Signal Input
Vert Input Amp & Attenuator
Delay Line
Vert Output Amp
X-Y Switch
AUTO
INT
NORM
TIME DIV
External Trigger
EXT
AUTO
EXT 10
Trigger Circuit
Gate Gen
Sweep Circuit
Single
NORM
LINE
Slope
Level
X Axis Signal Input
Power Supply
Trigger Controls

Block diagram of a basic oscilloscope

Figure 1-1.

also have switches to select single channel, dual channel, or various combinations.

The input coupling switch. The input coupling switch usually has four positions — AC, GND, DC, and 500. The AC and DC positions are designated high impedance, which is typically 1 megohm shunted by about 20 pF. This high input impedance, together with a standard 10-to-1 divider probe, increases the input impedance to 10 megohms, allowing you to measure waveforms with minimum circuit loading. Some scopes also allow you to select 50 input impedance, which is ideal for monitoring pulse and signal generators or other low impedance sources.

AC position. The AC position couples the input signal through a DC blocking capacitor, allowing only the AC component to be viewed. AC coupling can be very useful when you want to measure a small AC signal superimposed on a large DC voltage. For example, to measure the small AC ripple voltage from a power supply, AC couple the signal to block the large DC component. Do not use the AC position to measure low-frequency digital-type signals. The internal DC blocking capacitor will distort the waveform as shown in figure 1-2.

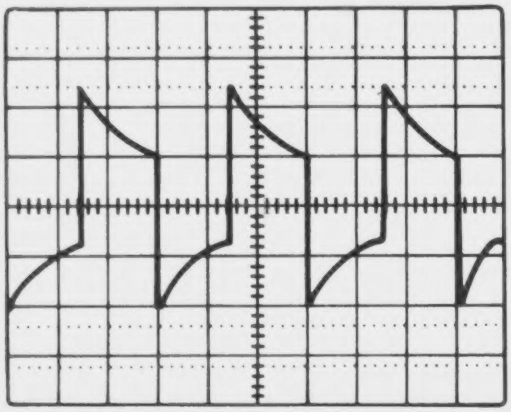
GND position. The ground (gnd) position is useful when you want to set a ground or o-volts reference level on the CRT screen without disturbing the input signal connection. The input signal is internally disconencted and the vertical amplifier's input is grounded. This means that you can leave the input signal connected to your scope. You won't short it out when you switch to the ground position.

DC position. The DC position allows you to view both DC and AC components of the input signal. For example, if you have set the O-volts reference level at the center of the screen (using the gnd position) and then switch to DC, the waveform will appear showing the AC component, if any, and the signal will be offset either up or down depending on whether the DC component is positive or negative. DC coupling is also used when you are measuring digital-type signals or square waves.

The 50-ohm position. The 50-ohm position is a DC input (no blocking capacitor) with the capacitive reactance (Xc) of the input amplifier very large compared to 50 ohms. The 50-ohms input is used to measure high-speed pulses and square waves from 50-ohm sources with minimum distortion and VSWR reflections. Most oscilloscopes with a built-in 50-ohm input have internal compensation that makes it a better match than an external load.

The input attenuator control. Most modern scopes use a combination of variable attenuation and adjustable vertical amplifier gain to control input signal levels. High-level signals will require more attenuation/less gain so that the trace is not deflected off the screen, and low-level signals will need less attenuation/more gain. The vernier portion of the input attenuator provides continuous sensitivity control between the calibrated volts-per-division ranges. Whenever you move the vernier out of its detent position, the UNCAL light will be on, letting you know that the steps marked on the VOLTS/DIV dial are not calibrated.

Some scopes also have a vertical magnification control. MAG × 5 will allow you to increase the vertical sensitivity 5 times, from 5 mV to 1 mV per division, but with a reduction in bandwidth from 100 to 40 MHz. The vertical magnifier is useful when you're trying to measure low-level signals such as power supply ripple.

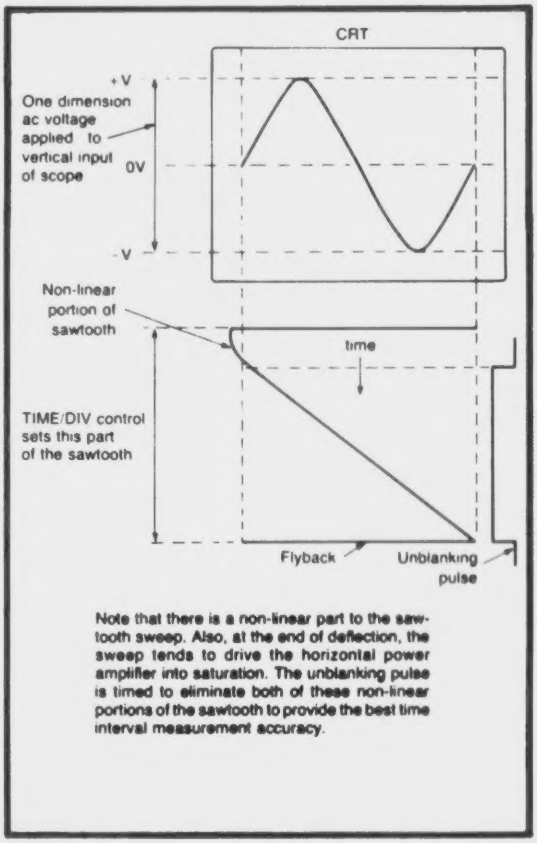


Distorted display as a result of trying to measure a low-frequency digital signal thru the input dc blocking capacitor (input switch in the AC position).

Figure 1-2.

Horizontal Input Controls. The sweep generator, sometimes called the time-base generator, produces the sawtooth waveform which controls the rate the beam is drawn horizontally across the face of the CRT. The generator's most important function is to insure linear beam movement, meaning the beam moves at the same rate from start to finish. Without this precise rate, accurate time measurements are not possible. Another factor of accuracy depends on the delay time. Its function is to delay the vertical input signal just enough so that the trace being displayed is the signal that started the sweep (see fig. 1-3).

Another function of the sweep generator is CRT unblanking. An unblanking pulse is a positive square wave that turns the trace on in relation to the rising portion of the sawtooth. What this means is that the trace is turned on during its left-to-right movement across the screen and then turned off during retrace (sometimes called flyback), which is when the beam resets from right to left. If the beam were not turned off in this manner, you would see the retrace lines with every sweep.


CRT
+V
One dimension ac voltage applied to vertical input of scope
0V
-V
Non-linear portion of sawtooth
time
TIME/DIV control sets this part of the sawtooth
Flyback
Unblanking pulse

Note that there is a non-linear part to the sawtooth sweep. Also, at the end of deflection, the sweep tends to drive the horizontal power amplifier into saturation. The unblanking pulse is timed to eliminate both of these non-linear portions of the sawtooth to provide the best time interval measurement accuracy.

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Figure 1-3. Development of a sine wave pattern on the CRT.

Sweep speed control. The sweep generator's sawtooth waveform is controlled by a front panel control called TIME/DIV or SEC/DIV. This calibrated control lets the operator select many different sweep speeds in order to view waveforms that vary from a few Hertz up to the bandwidth limit of the scope. The control is usually divided into steps in a 1–2–5 sequence covering the ranges of seconds, milliseconds, microseconds, and nanoseconds. These ranges correlate to how fast the beam is drawn across the CRT. The faster the beam is drawn across the CRT, the faster the time reference (i.e., the shorter the scale). For example, if the TIME/DIV control is set for 0.5 seconds per division, the time reference over the full 10 major divisions (vertical graticule on the CRT face) is 5 seconds. If it's set at 5 milliseconds per division, the full-scale time reference is 50 milliseconds. Figure 1-3 shows how the sawtooth waveform produced by the sweep circuit develops a sine wave pattern on the CRT.

Part of the TIME/DIV control is a sweep vernier control that provides continuous adjustment of the sweep speed between the fixed TIME/DIV steps. Whenever you move the vernier out of its detent CAL position, the UNCAL light will be on letting you know that the steps marked on the TIME/DIV dial are not calibrated.

The horizontal magnifier. Another control that interacts with the sweep speed control is the horizontal magnifier. This control expands the sweep time by whatever factor the magnifier is labeled. For example, if your scope has a 10-division time axis (10 squares on the horizontal axis and the magnifier has a factor of × 10), you would have an effective 100-division-wide signal and a 10-division window. This also means the signal has 10 times the horizontal resolution as before.

Exercises (001):

1. On which axis of an oscilloscope is time information presented?

2. What control is used to provide continuous adjustment of the time-base generator?

3. What is the purpose of the delay line at the input of the vertical amplifier?

4. What position of the input coupling switch is used to view digital-type or square wave signals?

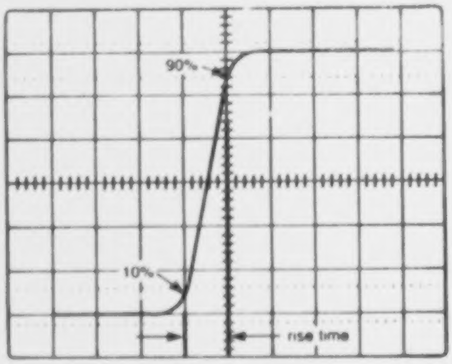
5. What vertical input control is used to increase the vertical sensitivity 5 times?

6. What circuit in an ascilloscope has control of CRT unblanking?

7. Would horizontal resulution increase or decrease if the horizontal magnifier is used?

002. State how rise time, pulse width, and frequency are measured using an oscilloscope.

Measuring Rise Time. High-speed, precisely timed sweeps provide data of fundamental importance in waveform analysis. For example, one of the basic characteristics of a square wave or pulse is its rise time as shown in figure 1-4. Rise and fall times are usually measured between the 10 and 90-percent amplitude points on the leading or trailing edge of the pulse, respectively. These two points are generally accepted as industry standards for waveform measurement.



TIME/DIV DIAL = 0.05μs
1 × 0.05μs = 50ns rise time

Rise time measurement.

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Figure 1-4.

The first step in measuring rise time is to adjust the vertical controls so that pulse height is 6 divisions. Then use the TIME/DIV and horizontal-position controls to expand the sweep speed and position the leading edge of the pulse to intersect the bottom 10-percent amplitude point with a convenient vertical graticule line (see fig. 1-4). Read the rise time by measuring the time between the 10- and 90-percent points. The example shown in figure 1-4 is 1 divsion times 0.05 microseconds, which equals a rise time of 50 nanoseconds.

How accurate is this measurement? Always remember when measuring rise time that the vertical amplifier of your scope has its limits. Many times a new technician will make the mistake of trying to measure the rise time of a 10-kHz pulse train with a 500-kHz scope (sounds reasonable), without realizing that the actual rise time of the pulse is faster than the vertical amplifier can respond to. Refer to your operating manual for rise time specifications. If you don't have a manual, use the following rule of thumb:

Bandwidth × Rise Time = .35

Therefore, if you have a 500-kHz scope, don't try to measure rise time faster than .7 microseconds. In fact, the vertical system of your scope should be 2 to 5 times faster than the rise time of the applied signal. In such a case, the rise time of the signal indicated on the scope will be in error by less than 2 percent. Refer to Appendix A for further information on rise time and bandwidth.

Measuring Pulse Width. Measuring the pulse width of a digital signal is accomplished by using the TIME/DIV control and other sweep circuit controls as necessary to make the pulse as high and wide as possible to take advantage of the full-scale accuracy of the instrument.

The first step in measuring pulse width is to adjust the vertical controls so that pulse height is 6 divisions (i.e., enough height to easily see the 50-percent point). Then use the TIME/DIV control to expand the sweep speed so that one pulse is in the center of the screen. Do not move the vernier control out of its CAL position. Pulse width is measured at the 50-percent amplitude points. Use the vertical and horizontal position controls to center the pulse around the center horizontal graticule line with the pulse's leading edge over a convenient vertical graticule. Count the number of divisions between the 50-percent points and multiply that times the main sweep speed; read from the TIME/DIV dial. The example shown in figure 1-5 is 8 divisions times 0.5 microseconds, which equals a pulse width of 4 microseconds (8 div. × 0.5 microseconds = 4.0 microseconds). To determine the accuracy of this measurement, look up the main time base accuracy specification of your scope and multiply it by the final full-scale setting. For example, an accuracy figure from the manual of 3-percent full scale would be 0.03 times full scale on the scope. Full scale is determined by multiplying the TIME/DIV dial setting times full scale on the CRT (0.5 microseconds per div. *X* 10 div. = 5.0 microseconds). So 5.0 microseconds times 0.03 accuracy equals 150 nanoseconds (0.03 *X* 5 microseconds = 150 microseconds). The pulse shown in figure 1-5 then, is 4.0 microseconds ± 150 nanoseconds.

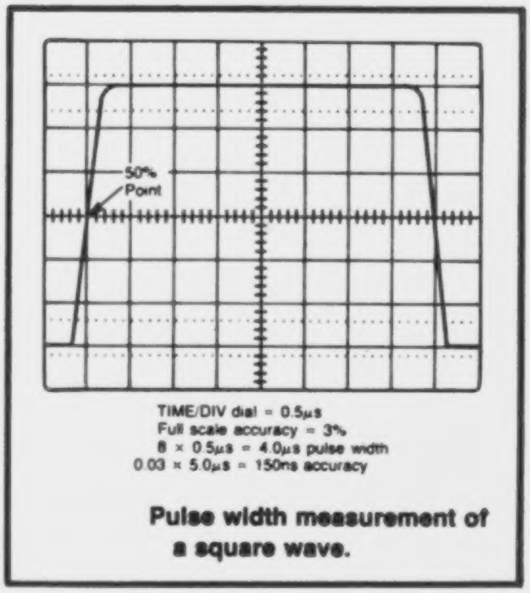
50% Point
TIME/DIV dial = 0.5µs
Full scale accuracy = 3%
8 × 0.5µs = 4.0µs pulse width
0.03 × 5.0µs = 150ns accuracy
Pulse width measurement of a square wave.

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Figure 1-5.

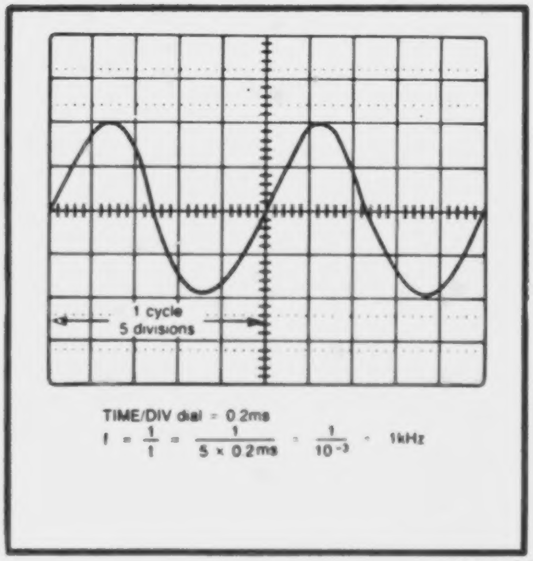

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Figure 1-6. Frequency (time period) measurement of a sine wave.

Frequency Measurements. Frequency (f) is the reciprocal of the time period for one cycle. For example, the time period (t) of the signal shown in figure 1-6 is obtained by counting the number of horizontal divisions covered by one cycle (5) and multiplying that times the setting of the TIME/DIV control (0.2 milliseconds). Then take the reciprocal.

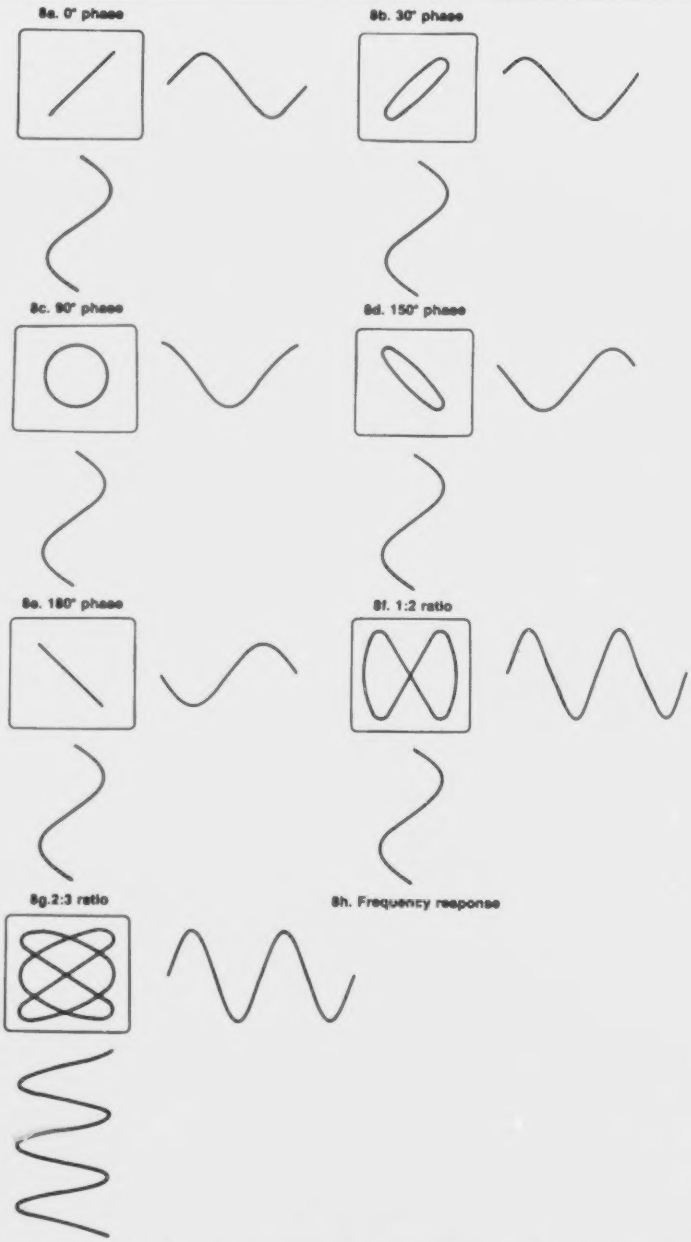
$$f = \frac{1}{t} = \frac{1}{5 \times 0.2\text{ ms}} = \frac{1}{10-3} = 1.0\text{ kHz}$$

Exercises (002):

1. How is rise time measured on a pulse waveform?

2. Where is pulse width measured on a pulse waveform?

3. If the TIME/DIV dial is set a .2 microseconds, and the width of the pulse is measured as 8 divisions on the scope graticule, what is the pulse width?



8a. 0° phase

8b. 30° phase

8c. 90° phase

8d. 150° phase

8e. 180° phase

8f. 1:2 ratio

8g. 2:3 ratio

8h. Frequency response

X-Y mode of operation showing typical examples of Lissajous patterns.

Figure 1-7.

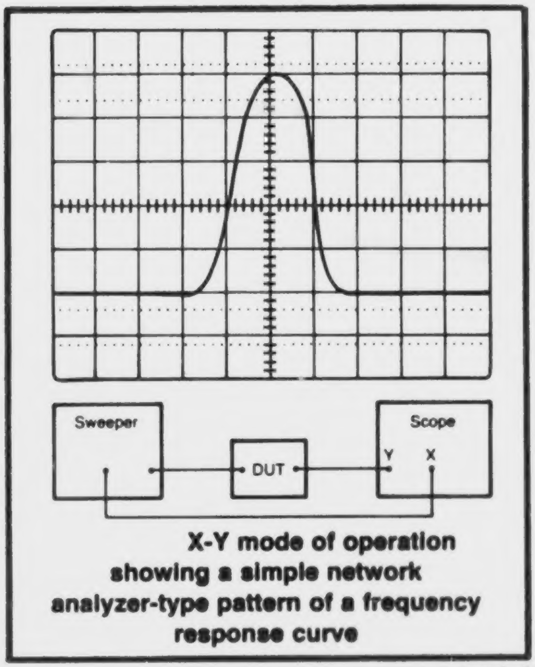
4. Refer to question 3. What is the accuracy of the measurement if the scope manual lists accuracy at 5 percent of full scale?

5. Calculate the frequency of a signal in which one cycle covers 4 horizontal divisions. The TIME/DIV dial is set at 1 microsecond.

003. Specify the purposes and use of the X-Y operation.

X-Y Operation. The X-Y mode of operation is a two-dimensional representation of two AC voltages. The vertical or Y imput signal deflects the beam up and down while the horizontal or X input signal replaces the scope's sweep generator and deflects the beam horizontally. A third dimension can be added by modulating the beam's intensity through the Z axis.

One of the more common uses of the X-Y mode is to generate Lissajous patterns to check phase. Another more sophisticated use is in the area of circuit frequency response where you turn your scope into a simple network analyzer.



X-Y mode of operation showing a simple network analyzer-type pattern of a frequency response curve

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Figure 1-8.

Figure 1-7 shows some of the various Lissajous patterns you can expect using the X-Y mode. Note that figure 1-7 shows what is commonly called a "bow-tie" pattern and is the result of the deflection voltages having a 1:2 frequency ratio. To obtain the ratio of vertical and horizontal deflection frequencies from any Lissajous pattern, count the number of horizontal tangent points and divide this number by the number of vertical tangent points. If you use this method, always make certain that the trace contains visible crossovers and that they are not masked by trace coincidence; that is, the horizontal tangent points don't fall together.

Figure 1-8 represents a frequency response curve that is obtained by connecting a sweep generator to both the input of the circuit under test and the X axis. The output of the circuit is connected to the Y axis. The oscilloscope becomes a simple network analyzer that is a swept receiver that provides a visual display of amplitude versus frequency. It shows how energy is distributed as a function of frequency.

NOTE: X-Y operation is limited by horizontal amplifier frequency response and phase difference between the horizontal and vertical amplifiers. Refer to your operating manual for specifications.

Exercises (003):

1. How can X-Y operation be made to operate in a third dimension?

2. What limits the X-Y operation in a particular oscilloscope?

3. How can an oscilloscope be set up to act as a simple network analyzer?

4. In the X-Y operation, if the vertical input frequency is 1kHz, what is the horizontal frequency with a frequency ratio of 2:1?

004. State the purpose and use of oscilloscope trigger controls.

Trigger Controls. The purpose of the trigger circuit is to produce a stable display. This is done by synchronizing the sweep signal discussed earlier so that each trace is written right on top of the previous one. You see one single trace, but it is actually being refreshed on each sweep.

Several controls allow you to select the source, positive or negative mode, and level of the synchronizing trigger signal as shown in the simplified diagram (fig. 1-1). The following table is an abbreviated description of the basic controls and their functions.

Typical Name	*Positions*	*Functions*
Mode	AUTO	Connects sweep to multivibrator so sweep free-runs in absence of adequate trigger signal.
	NORMAL	Connects trigger circuit to one of three sources: input signal, external signal, or line.
	SINGLE	Sweep will start only upon the occurrence of the trigger signal that meets the conditions of level and slope after the button is pushed.
	INT	Uses sample of input signal to start sweep.
Source	EXT	Uses sample of some external signal to start sweep. External signal is usually related to input signal.
	EXT/10	Same as EXT except attenuates external signal by a factor of 10.
	LINE	Uses sample of power source. Useful for viewing events related to power line frequency.
Trigger Level	VARIABLE —1.5v to +1.5v (EXT) —15v to +15v (EXT/10)	Permits selection of triggering at any point (level) on the postiive- or negative-going edge of the displayed waveform.
Slope	POS (+) NEG (—)	Sets up the triggering circuit so that the displayed signal is triggered on the positive- or negative-going edge.

Auto/normal. This switch is probably the greatest source of "pilot error" in oscilloscope operation. In simple terms, NORMAL mode requires a trigger signal to generate a sweep — AUTO does not.

AUTO mode. The AUTO mode selects an internal oscillator or multivibrator that is used to trigger the sweep generator in order to produce a reference baseline — if there is no other trigger source. As soon as you select one of the three trigger sources (internal, external, or line) that trigger source is used to start the sweep generator. If the trigger source frequency is below approximately 40 Hertz, you must switch to the NORMAL mode to obtain stable triggering. Stated another way, the AUTO mode is used to obtain a reference baseline when you are adjusting the controls for focus, intensity, position, and DC reference. It also keeps the baseline on the CRT if you remove the input signal.

NORMAL mode. The NORMAL mode requires a trigger signal from one of the three sources (internal external, or line) in order to generate a reference baseline or sweep. The "pilot error" mentioned earlier usually occurs when you have set the scope up for internal triggering and the mode switch is in the normal position. If you don't have a signal connected to the vertical input of the scope, you won't have a trigger signal — hence no trace. This loss of trace with loss of input can be a valuable troubleshooting aid. Say, for example, you are probing a circuit looking only for the presence or absence of a signal. If you adjust the trigger level control for an optimum level, and then probe a point in the circuit that has no signal present, there will be nothing to trigger the display and the screen will be blank. Figure 1-1 shows a simplified representation of how the trigger controls are interlocked.

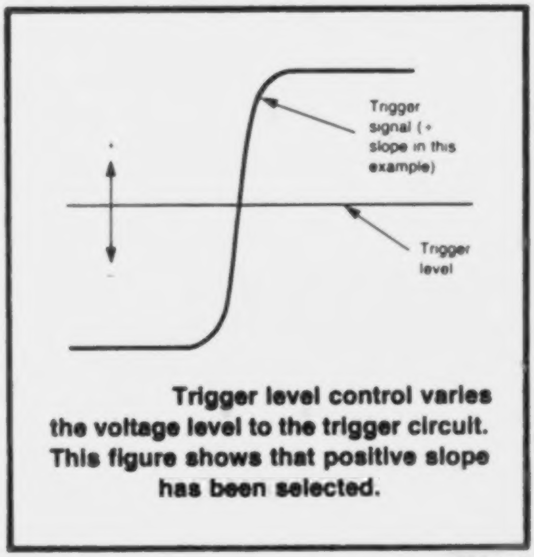
+
Trigger signal (+ slope in this example)
Trigger level
−
Trigger level control varies the voltage level to the trigger circuit. This figure shows that positive slope has been selected.

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Figure 1-9.

Trigger level and slope. Trigger level and slope controls allow you to select any point on the positive or negative edge of the displayed waveform to trigger the sweep circuit (see fig. 1-9). Usually, when the scope is in the *Internal Trigger* mode, the level control will select any point on the vertical waveform displayed. With external trigger signals, the control has a ± voltage limit (refer to the operating manual).

Internal trigger. When the switch is set for internal triggering, it means that a portion of the input signal is tapped off, as shown in figure 1-1, and sent to the trigger circuit. The CRT will display a *portion* of the input signal related to the first occurrence of a positive or negative slope of the input signal (depending on how you have set the Slope and Level controls). *This allows you to view a time event related to the input signal.* If you are using a dual-channel scope, you must know which input channel will trigger the sweep circuit and use that channel for your input.

If you are using the INTERNAL TRIGGER mode for troubleshooting, you may have to readjust the trigger level control to maintain a trace as you probe different points in the circuit under test. The reason this occurs is that the trigger circuit has been initially adjusted (by you) to trigger the sweep at some positive or negative voltage level. Therefore, as you move the probe from point-to-point monitoring different levels, the voltage level to the trigger circuit is also constantly changing. To eliminate this inconvenience, use the EXTERNAL TRIGGER mode and connect the external trigger to a low-repetition-rate timing signal from the circuit under test. In a digital circuit, use a submultiple of the clock pulse rate.

External trigger. When the switch is set for external triggering, you must provide a signal to a connector on the scope marked EXT TRIGGER. If the signal voltage exceeds the input voltage limit (refer to your manual), then use the EXT ÷ 10 trigger input. A good rule of thumb is, use a 10:1 probe on EXT and no probe on EXT ÷ 10. This will help prevent saturation of the trigger comparator. The external trigger signal is usually derived from a low-rep-rate timing signal related to the input signal. The CRT will display the input signal on each occurrence of the trigger signal. *This allows you to view an event time-related to the trigger source.* The trigger level and slope controls work the same for an external triggered signal as an internal triggered signal.

One method of viewing the time relationship between the input signal and external trigger signal is with a dual-channel scope. Use one input to look at the signal and one input to look at the trigger. You must know which input channel will trigger the sweep circuit and use that channel for the trigger input. Then set the source switch for INT.

If you are going to use an external trigger signal, it is advised that you first look at that signal on the input of your scope. You must determine if it has a DC component or noise greater than the trigger level you are trying to set up (or possibly exceeding the limit of the input). For example, the trigger level range of your scope may be ± 1.5 volts (± 15 through EXT ÷ 10). If you try to use an external trigger signal with a DC component greater than 1.5 volts, you won't be able to trigger the sweep unless you block that DC. Some scopes have AC coupling (selectable) built in — others do not. At any rate, you *must* use DC coupling for trigger signals below about 20 Hz.

Your external trigger signal may also have power-line pickup or possibly RF noise. In either case, you need to filter out the unwanted portion in order to obtain a stable display. Some scopes have built-in filters while others do not. The point is, if you use external triggering, make certain the signal is clean.

Line trigger. In the LINE mode, the display is triggered by a sample of the power line which is usually 50 to 60 Hertz. Line triggering is often used when you want to determine if there is any relationship between the displayed signal and the line frequency (often called power-line hum).

Trigger holdoff. Some oscilloscopes may have this specialized variable control that is used in conjunction with the trigger level control. Trigger holdoff increases the time between sweeps and helps stabilize the display when internally triggering off a complex digital or RF signal.

Exercises (004):

1. What is the purpose of the trigger circuit?

2. In the **Normal** mode, a trigger signal *is/is not* required.

3. At a trigger source frequency of 20 Hertz, what mode must be used for stable triggering?

4. What is the purpose of the trigger level and slope control?

5. How can you look at several different voltage level imput signals without constantly changing the trigger circuit to stabilize each display?

6. What control is used to increase the time between sweeps and help stabilize the display when internally triggering off a complex digital signal?

005. Detail the steps necessary to set up an oscilloscope for use.

Putting it all Together. Now that you have an idea of what all the basic controls are for, let's put them all together in step-by-step order to actually set up your scope.

1. Turn On and Preset (before the signal is connected).
   a. Turn on the power and allow approximately 30 seconds for warm up.
   b. Preset the trigger mode switch to AUTO and turn the intensity control up.
   c. If there is still no display, use the beam finder with the horizontal and vertical position controls to bring the trace to center screen

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d. Adjust the intensity control to a comfortable viewing level. Adjust the focus control for sharpest trace.

e. Adjust the input attenuator control to its highest setting. This will prevent the trace from being deflected off screen if the signal has a large DC component or is a very large AC signal.

f. Set the input coupling switch according to the following criteria:
   - 50 ohms if the source is a pulse or signal generator.
   - DC if the source is a low-frequency digital signal (square wave).
   - AC if the source has a large DC component that needs blocking or for general-purpose probing.

g. Connect the input signal and adjust the input attenuator control to obtain a reasonable display.

h. Adjust the sweep speed control until you get a display you can recognize.

2. *Fine tuning.* The following steps are contingent on the type of oscilloscope that you have. Many brands won't have all of the controls that we have been discussing, and some brands may have more. The point is, the theory is the same regardless of what the control is called or even if you have one.

NOTE: The following axioms apply when you are using an external trigger signal.

Axiom #1: The trigger signal must be clean and free of noise. If your scope has built-in filters, use them.

Axiom #2: If the trigger signal has a large DC component, it must be blocked by a capacitor (e.g., 0.1 μF). If your scope has AC/DC selection built into the trigger input controls, use the AC position to block the unwanted DC component.

a. Select the trigger source. You can trigger the sweep from an external, internal, or line frequency signal.

b. If the frequency of the trigger signal is less than approximatly 40 Hertz, change the mode switch to normal.

c. If you have selected external trigger, select either AC or DC trigger coupling. Use AC if the trigger signal contains a large DC component. Use DC if the trigger signal frequency is less than 20 Hertz.

d. Always use the EXT/10 input if you are not using a divider probe to connect the external trigger signal to the scope.

Exercises (005):

1. What are the two major steps in setting up the oscilloscope for operation?

2. What is the next step after centering the trace?

3. The attenuator control should be adjusted for its *lowest/highest* setting.

4. What setting of the input coupling switch should be used to view a low-frequency digital signal?

5. When should your scope's input filters be used?

6. How would you set up your triggering controls if the input trigger signal has a large DC component?

006. Specify the effects that can be caused from signal source loading by an oscilloscope.

Signal Source Loading. Oscilloscopes are versatile instruments that can measure voltage levels, phase differences, signal presence (or absence), logic highs or lows, frequency response, distortion, and complex waveforms. However, the oscilloscope is a useful measurement tool only if the signal to be measured can be accurately coupled to the scope's input amplifiers. This means measuring a circuit point with a minimum of loading.

Oscilloscope input impedance. Typical oscilloscope inputs are 1 megohms shunted by 20 picofarads. Any type of cable you hang on the input increases its capacitance. This capacitance causes measurement errors that are frequently variable. The input capacitance of an oscilloscope requires careful attention to probe selection and point of measurement (source impedance) if these errors are to be minimized. Some problems that become increasingly evident as the input shunt capacitance increases are:

- CW amplitude attenuation.
- CW phase shift.
- Induced pulse perturbations.
- Inaccurate pulse rise time measurements.
- Inaccurate propagation delay measurements.
- Excessive source loading.
- Abnormal circuit operation.

At high frequencies, the oscilloscpoe input behaves like a low-pass filter which shunts the high-frequency information to ground and significantly reduces the oscilloscope input impedance. For example, at 30 MHz the capacitive reactance for 20 pF is 265 ohms, while at 100 MHz it drops to 80 ohms. As will be explained later, many measurements, especially phase shift and pulse rise time, are more adversely affected by input capacitance than by resistive loading. Always remember that the Xc of an oscilloscope input varies as a function of frequency.

Circuit test point impedance. Knowing the source impedance at the point of measurement is critical. If the source impedance is low, rise time and amplitude measurements are generally no problem. For example, batteries and power supplies have source impedances of milliohms. Signal generators are 25, 50 or 600 ohms. The problem occurs when the source impedance is high. TTL has a source impedance of approximately 2.5k ohms, so even at very low fequencies (single-shot), measuring fast transition times is difficult at best.

Exercises (006):

1. What is the typical input impedance of most oscilloscopes?

2. As the frequency of the input signal to an oscilloscope increases, what happens to the input impedance? Why?

3. When making a rise time measurement with an oscilloscope, the measurement will be most accurate when source impedance is *high/low*.

4. What is the approximate source impedance of a transistor-transistor logic (TTL) digital circuit? Is the source impedance high or low?

007. Identify types of probes and specify the proper use of probes with an oscilloscope.

Basic Probe Considerations. If the scope is being used as a monitoring device, the connection between the signal source and scope is usually a direct 50-ohm cable. However, if the scope is being used for signal tracing or circuit analysis, then some type of an isolating device must be used to prevent the scope from loading the circuit and attenuating the signal. Today's modern oscilloscopes use a probe for this isolation.

The frequency of the signal you are measuring and source impedance at the point of measurement influence which probe to use. What you want to measure — rise time or amplitude — is also a weighing factor. In general, there are four types of probes available for common circuit analysis.

(1) High-resistance probes.
(2) Miniature passive divider.
(3) Active (FET).
(4) Current probes.

Any voltage probe will load the circuit you are attempting to measure. If amplitude measurements at low frequencies are all you are interested in, then a passive, 1 to 1, 1-megohm non-attenuating probe may be all you need. A good rule of thumb to remember is to keep resistive loading errors below 1 percent, select a probe/scope combination that has an input resistance (Rin) that is at least 100 times greater than the source impedance.

But as frequencies rise, or pulse rise time becomes very fast, scope input capacitance becomes more and more important, forcing use of a miniature passive divider probe to reduce that input capacitance. At the highest frequencies, if both amplitude and rise time are important in high source impedance circuits, an active FET input probe should be used.

If the ultimate in rise time is needed, a 50-ohm divider may be used. However, you must be careful of DC loading. A 50-ohm divider probe with an input Xc of 500 ohms will attenuate the amplitude of a signal, or upset the bias of the circuit if you probe the wrong point (e.g., collector of a transistor), or burn up the probe if you draw too much current.

A current probe is useful in those certain situations where touching the circuit with any voltage probe at all, even one with the smallest capacitance, changes the circuit's operation. It may be the collector of a transistor where an inductor and capacitance form a tuned circuit.

Probe rules for making amplitude measurements. For making these measurements, the following rules apply:

1. If you have a choice, select a minimum impedance source. For example: emitter-to-base impedance of a transistor is generally lower than the collector-to-base impedance (this implies a balanced input measurement).

2. Select a probe with the highest possible input impedance (Zin) at the frequency of interest. When measuring pulse amplitude, capacitance is not as important as input resistance (Rin) being high relative to the source impedance. While probe capacitance distorts pulse shape, the flat portion of the pulse top (maximum amplitude) can be used to make an accurate amplitude measurement since it contains low-frequency inforamtion. Conversely, if the pulse width is small compared to the measurement system rise time, input capacitance can introduce errors, since the source cannot fully charge the input capacitance during its on time. This problem becomes worse with increasing source impedance.

3. When source impedance is unknown, the probe with the highest Zin usually yields the greatest accuracy. However, for frequencies above 10 MHz, high probe capacitance can reduce accuracy, more than high probe resistance can improve accuracy.

4. If the source voltage is totally unknown, it is wise to start with a 100:1 divider probe to reduce the possibility of damaging ~~the~~ probe. This will also indicate whether or not there is enough signal available to capitalize on the relatively low capacitance of 100:1 divider probe. However, in real-life situations, you probably don't have a 100:1 divider probe. If this is the case, use your standard 10:1 divider probe.

Probe rules for making rise time measurements. Apply the following rulse for making these measurements:

1. Always try to probe the lowest impedance point that contains the waveform of interest. For example: emitter-to-base impedance of a transistor is generally lower than the collector-to-base impedance (this implies a balanced input measurement).

2. The fastest input system will generally have the lowest Rin and input capacitance (Cin). (This rule is limited only by the maximum resistive loading that the source can tolerate.)

3. At high frequencies, the 50-ohms divider probe (500 ohms at 1 pF) is the best bet for accurate rise time measurements. However, you must be careful of DC loading. The 500-ohms input Xc will attenuate the amplitude of a signal, or upset the bias of the circuit if you probe the wrong point (e.g., collector of a transistor), or burn up the probe if you draw too much current.

Probe compensation and calibrating your scope. After you have gone through the rigors of selecting the right probe, you're ready to make some measurements.

Let's begin by making sure your scope is operating properly. You should check its trace alignment; astigmatism and focus adjustments; and finally, if required, probe compensation.

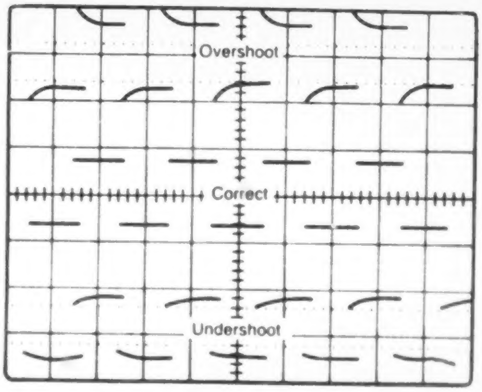
Trace alignment may be needed if your scope is operated near a strong magnetic field. To make this adjustment, ground the input and adjust the TRACE ALIGNMENT control for the best trace alignment with a horizontal graticule line.

The best way to adjust astigmatism and focus is with a dot displayed on the screen. Of course this assumes that your scope has X-Y display capabilities. If it doesn't, select the slowest sweep speed possible. This will prevent a very slow-moving dot which you can use for adjustments. To adjust astigmatism and focus, set the beam intensity to a low level. Position the spot to center screen and then adjust the focus and astigmatism controls for the smallest round dot.

Are you guilty of picking up a divider probe, connecting it to your scope, and taking measurements without first checking the probe's compensation? One of the most common "pilot errors" is using an uncompensated probe to make measurements. An uncompensated probe will cause errors in the display which will be undetected unless some kind of a standard waveform is checked. To be safe, you should always check probe compensation:

- At the beginning of each work day.
- Whenever you reconnect a probe to a different input connector.
- Whenever you change probes.

To compensate the probe, connect it to the calibrator square wave signal, select DC coupling, and adjust the scope's controls for a stable display. Select the lowest VOLTS/DIV setting possible and center the top portion of the square wave on the screen. This provides a more precise adjustment method (if your scope is adjusted properly). Adjust the probe until you get a flat-topped square wave with no rounding or overshoot of the signal's corners. Refer to figure 1-10.



Probe compensation adjustments. Overshoot means the compensating capacitance is too large and the high frequencies are not attenuated enough. Undershoot means the capacitance is too small and the high frequencies are attenuated too much.

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Figure 1-10.

After probe compensation, check the scope's vertical accuracy against the internal calibrator square wave. With the vernier in the CAL position, set the VOLTS/DIV control to obtain a display that is nearly full scale. The displayed square wave should match the p-p value of the calibrator output. If not, the scope should be recalibrated using the main vertical amplifier gain adjustment (check your scope's service manual for the proper procedure).

With the scope checked and the probe compensated, you are now ready to make some adjustments. Refer to Appendix B for further information on probe considerations.

Exercises (007):

1. What is the basic purpose of the oscilloscope probe?

2. List the four types of probes.

3. How can you reduce the input capacitance of an o'scope through the use of a probe?

4. When making an amplitude measurement and the source impedance is unknown, greatest accuracy is achieved when the probe Zin is *maximum/minimum*.

5. What type of probe is best for accurate rise time measurements?

6. What is the first thing to check before using a probe for accurate measurements?

008. Specify techniques used to display more than one signal at a time on an oscilloscope.

Observing Two Signals at the Same Time. There are two techniques oscilloscope manufacturers use to display more than one signal at a time — *dual-beam* and *dual-trace*. The dual-beam scope has two independent deflection systems within its CRT; hence two beams are displayed simultaneously. The dual-trace scope incorporates electronic switching to alternately connect two input signals to a single deflection system; hence two traces are displayed alternately by a single beam. The switching rate is usually in the 250- to 500-kHz range.

Most dual-beam scopes are used in applications where two events that occur simultaneously would not be displayed corectly on a dual-trace scope while it is switching between signals.

Since most oscilloscope users have the dual-trace models, we will confine this text to those types. Most of the following discussion is confined to the input switching controls on the front panel and how they interact to provide the dual trace capability.

Dual-Trace Input Controls. There are many various ways to manipulate two signals through two separate vertical input amplifiers and apply them to a single deflection system CRT. Front panel controls allow you to view the two inputs at what appears to be the same time in either the ALTERNATE or CHOP modes. And you can add or subtract the channels so that you can view the algebraic sum or difference between the two signals. Some oscilloscopes allow you to switch a channel to the horizontal axis so that you can view Channel A on the Y axis plotted against Channel B on the X axis.

Alternate mode. In the ALTERNATE mode, the A and B Channels are alternately displayed, one channel per sweep. At fast sweep speeds, the alternate traces will appear to be displayed at the same time. However, as the sweep speed is slowed, the traces will begin to flicker, showing the alternating pattern.

Chop Mode. In the CHOP mode, both A and B Channels are alternately displayed by switching between channels at a fixed high-speed rate (250 to 500 kHz). Even at slow sweep speeds, both channels seem to be displayed at the same time. Some oscilloscopes have the CHOP mode connected to the sweep control so the scope automatically switches in the CHOP mode at the lower sweep rates. If your oscilloscope does not have this automatic feature, the general rule is to use the ALTERNATE mode for fast sweep speeds and the CHOP mode for slow sweep speeds. On some occasions, fast sweeps might require the CHOP mode if the signal repetition is low or even single-shot.

Algebraic sum. When both Channels A and B are selected (or added), you're in the A-PLUS-B mode. The CRT screen will display the algebraic sum of the two input signals. One use of the A-PLUS-B mode is the dual-channel display of single-shot events. Another use is checking balanced or push-pull type amplifiers. Balanced signals should have equal amplitude and be 180° out of phase. Since the sum of these signals is 0 volt, you would expect to see a straight line. If the signals do not have equal amplitude or are not 180° out of phase, then the signal you see will be a small sine wave.

Algebraic difference. When both Channels A and B are selected and one channel is inverted, you're in the A-MINUS-B mode. The CRT screen will display the algebraic difference between the two input signals. One use of the A-MINUS-B mode is to measure the voltage across an ungrounded component without upsetting (or loading the circuit). This is called a balanced or ungrounded input. For example, to measure the voltage across the base-emitter junction of a transistor, set both channels to the same volts per division; then connect Channel A to the base and Channel B to the emitter of the transistor. Connect the ground clips to circuit ground. This allows you to view the small base-emitter voltage on the CRT without upsetting or grounding the circuit.

Exercises (008):

1. What are the basic oscilloscope techniques used for displaying more than one signal at a time?

2. How does the CHOP mode provide two displays?

3. How does the ALTERNATE mode provide two displays?

4. What is one use of the algebraic sum display method?

990. Specify operating characteristics of trigger controls used with dual-trace oscilloscopes.

Trigger Controls for Dual-Trace Oscilloscopes. The purpose of the trigger circuit is to produce a stable display on the CRT. This is done by synchronizing the scope's sweep signal with the signal to be viewed. Several controls allow you to select the source, positive or negative mode, and level of the synchoronizing trigger signal.

When you're looking at just one signal on a single channel scope, triggering is normally simple and straightforward. However, when dealing with complex digital signals, or RF, or two asynchronous signals, you need all the help you can get in the form of additional trigger controls. You need to be able to tell the scope exactly which signal, and even which portion of the signal, to trigger the sweep on.

As an example, when you're looking at dual trace presentations, you may want to see the correct time relationship between two pulses (i.e., how much a pulse on Channel A leads or trails a pulse on Channel B). Or, maybe you only want to compare the shape of two signals, but their time separation makes comparison difficult. The ability to select various trigger functions from the front panel enhances the scope's useability. Most modern dual-trace oscilloscopes feature controls that allow:

- Trigger selection from either input channel (shows time relationship).
- Trigger selection from both channels (used for pulse shape comparison).
- Delayed triggering (called delayed sweep).
- Trigger holdoff.
- Trigger view (allows you to display the trigger signal).
- Bandwidth limit control.

Selectable triggering. Selectable triggering is a convenience feature. It allows you to look at the display and then select the proper trigger source at the push of a button. Selectable triggering allows you to trigger the display from either one of the input channels.

A typical set-up might be a signal pulse into Channel A and its trigger pulse into Channel B. The correct time relationship between the pulses is obtained when the sweep is triggered by Channel B's signal in the ALTERNATE mode with Internal trigger selected. Figure 1-11 shows how the time relationship between the two signals changes when the triggering is changed from Channel B to Channel A.

Composite triggering. Composite triggering is the only way to show two asynchronous signals. It works like this: In the ALTERNATE mode, Channel A sweeps once, then Channel B, etc. The trigger selection controls cause the sweep to be triggered by the displayed signal; therefore, when Channel A is being displayed, it is the trigger source and when Channel B is being displayed, it is the trigger source.

A typical set-up might be two asynchronous pulses with nanosecond rise times but separated in time by microseconds. You don't care about the time relationship between the two signals but want to compare the pulse shapes. If a fast sweep is used, only one of the pulses can be displayed at a time.

In this situation, the pulses can be compared by selecting composite triggering in the ALTERNATE mode. Figure 1-12 shows how the time relationship between the two pulses is lost when composite triggering is used.

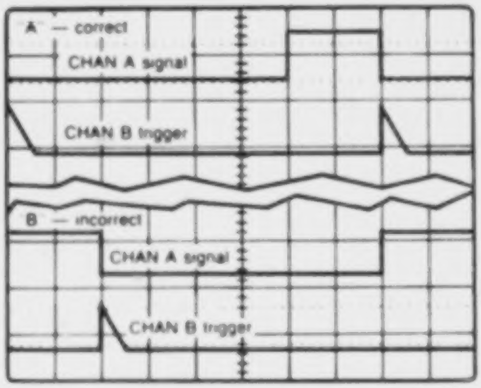
Delayed triggering. Delayed triggering is directly tied to delayed sweep. Delayed sweep allows easy location and expansion of a small portion of the display, permitting detailed analysis of that portion of the waveform. Delayed sweep can be triggered after a programmed delay, eliminating any waveform jitter from the expanded display.

How the sweep is triggered in the delayed sweep mode is described in the next segment. Trying to explain it now may cause some confusion.

Trigger holdoff. Trigger holdoff is a variable control used in conjunction with the trigger level control. Trigger holdoff increases the time between sweeps and helps stabilize the display when triggering off complex digital signals. On scopes without this control, you would use the sweep vernier control as a holdoff, but then your sweep is no longer calibrated.

Trigger view. Some oscilloscopes have a feature called trigger view. Basically it allows you to simultaneously display the external trigger signal on the CRT in addition to the input signals. This can be quite valuable in verifying the time relationship of the trigger signal to the displayed waveforms. In trigger view, the point where the center horizontal graticule line and the trigger waveform intersect is the trigger point. By varying the trigger level and slope controls, you can select any point on the positive or negative edge of the displayed trigger waveform to trigger the sweep circuit, and measure how it affects the input signals.

Bandwidth limit control. The bandwidth of some scopes can be reduced to minimize interference in high noise areas such as airports and broadcast stations. The limiter can effectively reduce the scope's bandwidth from 100 MHz to 20 MHz. For example, suppose you are picking up interference from 27-MHz citizens band equipment. If the test signal is less than 20 MHz, use the bandwidth limit control to reduce the high-frequency interference.



Trigger example showing time relationship between signal connected to CHAN A and its trigger connected to CHAN B.

View 'A' shows the display (sweep) being triggered on the positive-going edge of CHAN B trigger. View 'B' shows the display being triggered on the positive-going edge of CHAN A signal.

'A' = Internal trigger
Alternate display
Trigger on CHAN B (correct)
Positive slope

'B' = Internal trigger
Alternate display
Trigger on CHAN A (incorrect)
Positive slope

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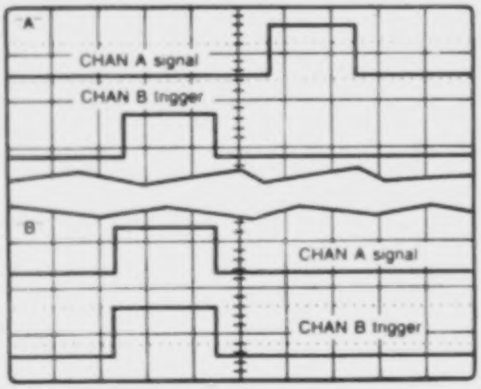
Figure 1-11.

Exercises (009):

1. How does the trigger circuit produce stable displays on the CRT?

2. What is the purpose of "trigger view"?



Composite trigger example showing how to compare two asynchronous signals connected to CHAN A and CHAN B.

"A" = Internal trigger (correct
Alternate display time
Trigger on A or B relationship)

"B" = Internal trigger (incorrect
Alternate display time relationship)
Composite Trigger

In Alternate mode and Composite Trigger, each signal is its own trigger source. Effective for signal shape comparison.

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Figure 1-12.

3. What are two types of triggering besides delayed?

4. What is the purpose of delayed triggering?

5. One method of increasing the time between sweeps and helping to stabilize a display when triggering off complex digital signals is to use the sweep vernier control. What is another, on some o'scopes?

010. Define the purpose and identify uses for the delayed sweep function of an oscilloscope.

Delayed Sweep. The delayed sweep function found on most high-frequency scopes is probably one of the least understood capabilities of modern oscilloscope. In basic terms, the scope with delayed sweep simply has two time bases — main and delayed.

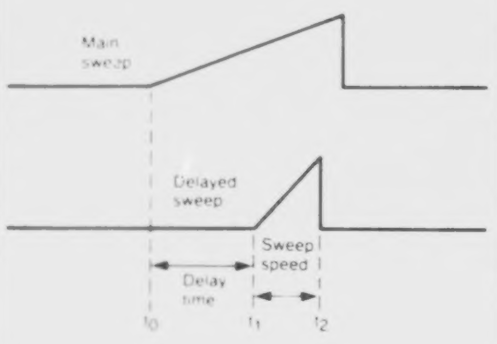
The controls for the two time bases may be labeled and arranged in various ways and have various capabilities, depending on the manufacturer, but their purpose is basically the same — to expand a selection portion of the displayed signal. To accomplish this, each time base has its own complete set of sweep and trigger controls.

In simple terms, delayed sweep functions are as follows: The signal is first triggered by the main sweep at the speed set by the TIME/DIV dial. The delayed sweep speed control is then set to a faster sweep speed than the main sweep (the delayed sweep is triggered after the main). This causes a small part of the main sweep trace to become intensified or brightened, depending on the setting of the delayed sweep speed control. The slower the setting, the larger the intensified portion becomes. This intensified marker can be moved along the signal by rotating the delay control. Then, if we switch the mode to delayed sweep, AUTO mode, only the intensified portion will be displayed over the full screen. In other words, we have magnified a portion of the trace.

We can see what really has happened if we consider the signal being displayed by two time bases; first the main sweep followed by the delayed, faster sweep (the intensified portion). What we have done is to set up a delay time from the start of the trace to the beginning of the intensified portion of the trace. When the delayed sweep is automatically triggered, this time is equal to the distance in centimeters from the start of the trace to the intensified trace, multiplied by the sweep time per centimeter (i.e., it is calibrated). The product is the delay time. When we switch to delayed sweep, we start the main time base with an input trigger, but we do not use it to display the signal. Instead, we use it as a clock that simply marks time until the delay period is over. Then the delayed time base sweeps, displaying the signal. Figure 1-13 shows how the delay system works in the AUTO mode.

There are two ways to cause the delayed sweep to be initiated after the delay time. The first way (discussed above), is called the AUTO mode. The delayed sweep automatically starts at the end of the delay period with no trigger signal or other external command needed. In the other mode, the delayed sweep is *armed* at the end of the delay period and requires a trigger signal (either internal or external) to start the delayed sweep. Since there is no way to know when the trigger signal will occur, the delay time is uncalibrated.

Each of these methods has its own advantages. In the AUTO mode, all of the accumulative rate jitter that has occurred since the start of the delay time is displayed on the delayed sweep. If, on the other hand, rate jitter is not desired in the display and a clear picture is needed, then the armed mode should be used. In this mode, the delayed sweep is retriggered after the delay time. A new time reference is established, eliminating all of the jitter that has occurred previously, providing a clear picture for accurate measurements on the expanded pulse.



Main sweep and delayed sweep sawtooth waveforms. Delay time (t_0-t_1) is set by DELAY control, and sweep speed (t_1-t_2) is set by DLY'D TIME/DIV control. t_1-t_2 is the intensified part of the waveform. When SWEEP AFTER DELAY control is set to AUTO, sweep is triggered automatically at t_1.

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Figure 1-13.

How to use delayed sweep. The delay controls on your oscilloscope usually will be highlighted by color or surrounded by lines on the front panel. But no matter which scope you have, look for the word DELAY in the control nomenclature.

Suppose you want to measure the width and rise time of the 5th pulse in a pulse train. If you try to expand the signal with the main sweep control, the pulse moves off screen. You could use the horizontal magnifier to expand the sweep time and perform the measurements as described earlier. However, you want more accuracy than that method allows. The point about accuracy to remember is that time interval measurements are LEAST accurate using the × 10 magnifier, BETTER using direct delayed sweep, and BEST using differential delayed sweep.

NOTE: If you don't have some type of pulse generator for the following experiments, try using the amplitude calibrator output on your scope.

The first step in measuring pulse width and rise time is to adjust the vertical controls so that pulse height is 6 divisions (i.e., enough height to easily see the 50-percent point). Then move the DLY'D TIME/DIV control out of its OFF position. When this is done, a portion of the waveform should become itensified. This intensified marker is used to locate the portion of the waveform to be expanded. Adjust the delayed sweep speed control so that the marker is a little wider than the pulse to be measured. Set the SWEEP AFTER DELAY control to the AUTO position.

Next, move the intensified marker along the waveform with the DELAY control until it is over the pulse to be measured. Use the horizontal position control to center the intensified pulse. Expand the intensified portion to the full width of the screen by selecting delayed sweep. Slightly readjust the DELAY control to make the leading edge 50-percent point intersect a convenient vertical graticule line. Count the number of divisions between the 50-percent points and multiply that times the delayed sweep speed control setting.

Differential delayed sweep. A more accurate time interval measurement can usually be made using the differential delayed sweep method. To make a differential measurement, select main sweep and adjust the TIME/DIV control to expand the sweep speed to make the pulse you want to measure as wide as possible. If the time interval of the pulse is greater than one-half division on the screen, the differential method will be more accurate than the delayed sweep method.

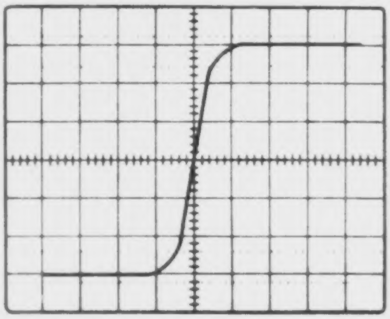
Switch the delayed TIME/DIV control out of its OFF position. When this is done you should see the intensified marker as in the previous measurement. Adjust the delayed TIME/DIV control so that the marker is a little wider than the pulse to be measured.

Next, move the intensified marker along the waveform with the DELAY control until it is over the pulse to be measured. Expand the intensified portion to the full width of the screen by selecting delayed sweep.

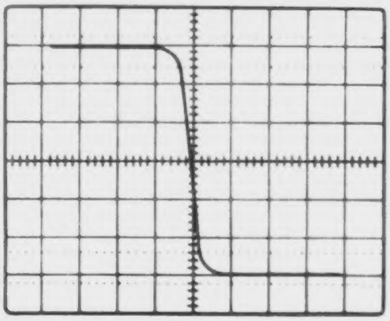
Adjust the DELAY control to position the 50-percent amplitude point of the leading edge over the center vertical graticule line. Read and record the DELAY dial setting. Note that some oscilloscopes use an LED readout for this purpose.

Readjust the DELAY control to position the trailing edge 50-percent amplitude point over the center vertical graticule line. Read and record the DELAY dial setting. The pulse width is the difference between the two readings times the main sweep TIME/DIV setting. Figure 1-14 shows an example pulse width measurement using the differential method.

Time interval measurement accuracy. The absolute accuracy of the differential delayed sweep method relies on the principle that the time interval of the pulse to be measured is greater than 1 cm of the main sweep. In this case, the accuracy is X percent of the reading plus Y percent of full scale. The Y percent of full scale will totally mask out the accuracy of the measurement. For example, with the Hewlett-Packard 1740A, the accuracy is ±0.5 percent of the reading ±0.1 percent of full scale. Therefore, the accuracy of a 10-cm (full scale) measurement is ±0.6 percent. However, as the reading is reduced to smaller and smaller parts of the main display, the accuracy decreases (+ error increases). At one division of main sweep the error is ±1.5 percent at 1/2 division of main sweep the error is now about equal to that of the direct-from-CRT measurement.



Use DELAY control to center leading edge of pulse over center horizontal graticule.



Use DELAY control to center trailing edge of pulse over center horizontal graticule.

Pulse width measurement using the differential delayed sweep method. DELAY control is used to center the leading edge and then trailing edge of pulse over center horizontal graticule. Pulse width is difference between the two readings times the main sweep TIME/DIV dial setting.

TIME/DIV dial = 0.2ms

DELAY dial reading = 7.46
−5.70
1.76

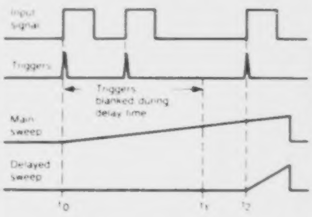
1.76 × 0.2ms = 352μs
Accuracy is ±0.5% for the DELAY dial and ±0.1% of full scale

0.005 × 352 = 176μs (dial)
0.001 × 2ms = 2μs (full scale)
pulse width = 352μs ± 4μs

Figure 1-14.

How to use the delayed trigger method to eliminate waveform jitter. Often, when you expand a signal, waveform jitter becomes more pronounced. This jitter makes it difficult to accurately measure the pulse's rise time or even its width. The scopes we have been discussing usually provide a feature to eliminate this unwanted jitter; it is called delayed trigger.

Delayed trigger controls are much the same as those that control the main sweep. There is a pushbutton that selects either AUTO or TRIG mode (which is similar to the AUTO-NORM mode). When in the TRIG mode, other controls are enabled that allow you to select the delayed sweep to be triggered internally or externally, divide the external trigger amplitude by 10, AC or DC couple the trigger signal, and adjust the slope and trigger level to start the delayed sweep at any point on the waveform. Let's use the input signal as the trigger source to see how the delayed sweep is triggered. Refer to figure 1-15.



Delayed sweep delayed trigger example. The main sweep is started by the first trigger pulse at t_0. The second trigger pulse "arms" the delayed sweep at t_1. The next trigger pulse to arrive after the delay time ends starts the delayed sweep sawtooth at t_2. The time between t_1 and t_2 is unknown which makes the delayed sweep uncalibrated.

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Figure 1-15.

Each input pulse produces a trigger pulse. The main sweep is started by the first trigger pulse. The secod trigger pulse does not do anything because it is blanked by the delay time set by the DELAY control. The delayed sweep is "armed" at t_1 when the delay time ends. The next trigger pulse to arrive after the delay time ends starts the delayed sweep sawtooth which deflects the electron beam across the CRT. Since there is no way to know when the trigger signal will occur. the delay time is uncalibrated. In effect, you have eliminated all interference by triggering the sweep on only that portion of the waveform you have selected to examine.

Mixed sweep mode. There is another mode of delayed sweep operation found on some oscilloscopes, called mixed sweep. In this mode, the main sweep is displayed on the screen for the amount of delayed time desired. Then the sweep increases in speed part way across the screen and finishes up the trace at the faster delayed-sweep rate. The transition point between sweeps is positioned with the DELAY control after the MIXED button is pressed. Mixed sweep is convenient for "peeling off" pulses one by one from a long train and examining them individually.

Exercises (010):

1. How many time bases does the delayed sweep function use? What are they?

2. What is the purpose of the time bases?

3. How is delay time measured?

4. What are the two ways of causing the delayed sweep to be initiated after the delay time?

5. What is the most accurate method of making time interval measurements?

6. What is the purpose of delayed trigger?

011. Detail the steps necessary in using a dual-trace oscilloscope for measurement of propagation delay.

Using the Dual-Trace Scope to Read Propagation Delay. Propagation delay, with reference to digital circuits, is the amount of time it takes for a change at the circuit's input to be noticed at its output. For example, when the input voltage to an AND-gate changes from a low to a high, the output will respond at some later, finite time. You can use your scope to quickly and easily measure this time and check it against the device's specifications.

It would be difficult to specify a test circuit and all the clips and probes required to complete such a test. By now you should already have your scope set-up, probes compensated, and enough background information to complete your own experiment. The necessary scope control settings are as follows:

1. Always use identical probes (a 50-ohm passive probe is useful in high-impedance circuits where maximum rise time accuracy is necessary).

2. Set the input coupling switch to AC.
3. Connect circuit's input signal to CHAN A.
4. Connect circuit's output signal to CHAN B.
5. Alternate display.
6. Set internal trigger on CHAN A in AUTO mode.
7. Adjust vertical controls so that signals are centered and approximately 6 divisions high.
8. Adjust the sweep control so the pulses look like those used for making rise time measurements.

You should see the leading edges of two pulses separated by a measurable distance. Measure the propagation delay at the 50-percent points (center horizontal graticule line) by counting the number of divisions between the two pulses and multiplying that times the setting of the sweep speed control. If you measure 6 divisions and the TIME/DIV dial is set at 5 nanoseconds, the propagation delay is 10 nanoseconds. For greater resolution, use the X10 magnifier or delayed sweep.

Exercises (011):

1. What is propagation delay?

2. What is the first important step in setting up to measure propagation delay?

3. Where on the display should the propagation delay be measured?

4. What is the propagation delay if the number of divisions between pulses is 3 and the TIME/DIV dial is set at 2 nanoseconds?

5. What control or function will provide greater resolution for the delay measurement.

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APPENDIXES

Appendix A. Oscilloscope Amplifier Considerations.

Abbendix B. The 50-Ohm Input Versus the High-Impedance Input.

APPENDIX A

OSCILLOSCOPE AMPLIFIER CONSIDERATIONS

Oscilloscope users generally consider a scope's bandwidth and rise time as its primary parameters. Rise time is usually considered the more important parameter when working with faster waveforms. This is mainly because the axis of the scope's display is the horizontal or time axis, and it offers the greatest resolution — less than 2 percent for timing measurements.

Why is the horizontal or time axis considered the major axis? Consider that the vertical axis has an 8-cm window, whereas the horizontal axis has a 10-cm window. 10 cm provides more resolution than 8 cm. Also, the range of the vertical axis (the HP 1,740 for example) is 2,000 to 1 or from 1 mV/cm to 20V/cm. The time axis has a range of 40,00,000 to 1 from 2 sec/cm to 50 ns/cm. This is 20,000 times greater than the vertical axis offers.

Signal bandwidth is, of course, defined as the frequency range in which signals are handled with less than a 3 dB loss compared to midband performance. However, the vertical system of an oscilloscope is not flat like that of a voltmeter — it is Gaussian.

What does Gaussian response mean? It means that the vertical system of the scope alters the input signal and delays it in such a way that it produces a linear phase response. The linear phase response has a constant group delay, so all the frequency components will reach the deflection plates at the same time. This results in minimum distortion of complex waveforms. Note that this Gaussian response is always falling in gain; therefore, accurate voltage measurements can only be made at DC. The frequency response will be down 1.5 dB at 20 percent of the 3 dB bandwidth, so 3-percent accurate amplitude measurements of sine waves can't be made at frequencies greater than 20 MHz on a 100-MHz oscilloscope. However, the amplitude of a pulse is DC, so accurate pulse amplitude measurements can be made up to the full bandwidth of the scope.

Constraints make bandwidth and rise time numerically related in well-designed general-purpose oscilloscopes. Bandwidth in megahertz multiplied by rise time in nanoseconds is approximately 0.35. Therefore, if your oscilloscope needs are defined in terms of one factor, for example rise time, dividing it into 0.35 will produce bandwidth.

In terms of rise time, scopes ideally should have a vertical system capable of responding at least three to five times as fast as the fastest applied step signal. In such a case, the rise time of the signal indicated on the scope will be in error by less than 2 percent. For example, if you are going to accurately measure X microsecond pulses, the minimal requirements for scope bandwidth using the 5 times faster and 0.35 factors together can be estimated using the following rule of thumb:

$$\text{Bandwidth (minimal)} \quad \frac{1.70}{\text{Fastest Rise Time}}$$

But remember, very accurate, absolute rise time measurements are not always important. When simply comparing the rise times of two signals, scopes with a rise time equal to the rise time of the signals applied are usually considered adequate.

In conclusion, it can be said that the modern oscilloscope with its Gaussian response is designed for pulse parameter analysis but not sine wave analysis. The characteristics of a sine wave can be better measured with instruments other than the oscilloscope. For true RMS, a voltmeter can give better amplitude measurements; a counter, better frequency measurements; and a spectrum analyzer, better distortion measurements. However, for a complex waveform such as a pulse, the oscilloscope is clearly the best choice. The voltmeter can't respond fast enough to make this measurement. The trigger uncertainties of a counter mask its accuracy for pulse measurements, and nothing but a scope can measure parameters such as overshoot, droop, and ringing.

APPENDIX B

THE 50-OHM INPUT VERSUS THE HIGH-IMPEDANCE INPUT

In recent years, there has been a lot of discussion over the merits and demerits of these two types of oscilloscope inputs. The key issue in making a comparison is input impedance versus frequency. The high-impedance input is only high impedance for frequencies below approximately 1 MHz. Above 1 MHz, the shunt capacitance takes over, and there is a fair amount of uncertainty as to what the input impedance actually is. The 50-ohm input starts out with low impedance and has essentially a constant input impedance over the oscilloscope vertical amplifier bandwidth, and virtually eliminates the effects of capacitive loading. These input characteristics dictate the applications for which each input is best suited and the choice of probe to do the job.

Benefits of High-Impedance Scope Inputs.

- Passive probes can be used where high-input resistance is required. No need for an active probe unless signal levels are small relative to vertical sensitivity.
- Can tolerate much greater input voltages than a 50-ohm input.
- Can be used with high-voltage probes.

Problems of High-Impedance Scope Inputs.

- Capacitive loading is much higher than with 50-ohm inputs.
- Input impedance is highly variable with frequency.
- There is a tendency to have confidence that there is no loading because R is high, when in fact, capacitive loading is extremely high.
- Does not offer a good termination for fast 50-ohm signal sources. Even when a 50-ohm termination is used to shunt the high input resistance, the VSWR caused by the remaining capacitance is very high.

Benefits of 50-ohm Oscilloscope Input.

- Minimizes input capacitance and the problems that it causes.
- Presents a better termination for high-speed 50-ohm sources. Minimizes pulse shape distortion, VSWR, reflections.
- When an appropriate probe is added to the 50-ohm input, the input impedance can be considerably higher than that of a high-impedance input scope. The source frequency for which this is true depends on the particular probe selected.

Problems with 50-ohm Input.

- Limited maximum input voltage. Typically, the maximum voltage which can be applied directly is less than ± 10V.
- Requires a probe to increase the input resistance:
  - Passive probes can be used to increase the input resistance to 5k ohms if 100× division ratios can be used.
  - Active probes are generally required to increase the input resistance to the 100k ohms to 100M-ohms area. Active probes are expensive but generally offer a more flexible general probing solution.
  - 50-ohm inputs are not compatible with high-voltage probes.
  - Does not have AC coupling for signal input.

Summary. To summarize, the 50-ohm input offers superior measurement capability in many situations. However, it cannot be considered to be a general purpose solution because a probe is required to increase the input resistance, and AC coupling is not available without an active probe.

The high-impedance oscilloscope input is more general purpose than the 50-ohm input. However, it is generally not as capable for making accurate high-speed pulse measurements, phase-shift measurements, and high-frequency amplitude measurements, even when a probe has been carefully selected.

Most oscilloscope manufacturers offer selectable high impedance and 50-ohm inputs in the same mainframe or plug-in vertical amplifier. The choice of both inputs plus the various probes offered allow the versatility required to make most waveform measurements.

Answers for Exercises

CHAPTER 1

Reference:

001 - 1. The horizontal or × axis.
001 - 2. The sweep vernier control (part of the TIME/DIV control).
001 - 3. It allows the sweep generator circuitry time to start a sweep before the signal reaches the CRT vertical deflection plates. This enables you to view the leading edge of the signal waveform.
001 - 4. DC coupling position.
001 - 5. The vertical magnification control.
001 - 6. The sweep generator circuit.
001 - 7. Increase.

002 - 1. Measured between the 10 and 90-percent amplitude points on the leading edge of a pulse.
002 - 2. At the 50-percent amplitude points.
022 - 3. 1.6 microseconds.
022 - 4. Plus or minus 100 nanoseconds.
022 - 5. 250 Hz.

003 - 1. By modulating the beam's intensity through the Z axis.
003 - 2. It is limited by horizontal amplifier frequency response and the phase difference between the horizontal and vertical amplifiers.
003 - 3. Connect a sweep generator to the input of the circuit under test, and the X axis input of the o'scope. Then the output of the circuit under test is connected to the o'scope's Y axis (vertical input).
003 - 4. 2 kHz.

004 - 1. To produce a stable display.
004 - 2. Is required.
004 - 3. The NORMAL mode.
004 - 4. It permits you to select any point on the positive or negative edge of the displayed waveform to trigger the sweep circuit.
004 - 5. This can be done by selecting the external trigger mode and connecting a low-repetition-rate timing signal from the circuit under test to the external trigger input. In digital circuits, use a submultiple of the clock pulse rate.
004 - 6. The trigger holdoff control.

005 - 1. Turn on and preset, followed by fine tuning.
005 - 2. Adjust the intensity control for comfortable viewing; then adjust the focus for the sharpest trace.
005 - 3. Highest — to prevent the trace from being deflected off the screen if the signal has a large DC component or is a very large AC signal.
005 - 4. DC.
005 - 5. To keep the trigger signal clean and noise free.
005 - 6. Use the AC position of your trigger input controls.

006 - 1. One megohm shunted by 20 picofarad of capacitance.
006 - 2. Decreases. Because as the frequency of the input increases, the capacitive reactance (Xc) of the shunt capacitance decreases and shorts the high-frequency signal to ground.
006 - 3. Low.
006 - 4. 2,500 ohms. High.

007 - 1. To provide isolation for scope inputs.
007 - 2. The high-resistance, miniature passive divider, active (FET), and current probes.
007 - 3. By using a miniature passive divider probe to reduce the input capacitance. Also the active or 50-ohms divider probe can be used.
007 - 4. Maximum.
007 - 5. The 50-ohms divider probe.
007 - 6. Probe compensation.

008 - 1. The dual-beam or dual-trace oscilloscopes.
008 - 2. It displays the A and B Channels alternately by switching between the two input channels at a fixed high-speed rate (250 to 500 kHz).
008 - 3. Displaying A and B Channels alternately, one channel per sweep.
008 - 4. A dual channel display of single-shot events, or checking balanced or push-pull type amplifiers.

009 - 1. By synchronizing the scope's sweep signal with the signal to be viewed.
009 - 2. It allows you to display the trigger signal.
009 - 3. Selectable and composite.
009 - 4. To permit detailed analysis of a portion of a waveform.
009 - 5. The trigger holdoff control.

010 - 1. Two. Main and delayed.
010 - 2. The main time base is used to trigger on the signal first (normal operation). The delay time base triggers on the signal later than the main time base. This causes a small part of the main sweep trace to become intensified or brightened. The portion of the waveform we want to analyze has become magnified.
010 - 3. The delay time is equal to the distance in centimeters from the start of the trace to the intensified trace, multiplied by the sweep time per centimeter.
010 - 4. The AUTO mode and the ARMED mode.
010 - 5. Using differential delayed sweep.
010 - 6. To eliminate unwanted jitter.

011 - 1. The amount of time it takes for a change at the circuit's input to be noticed at its output.
011 - 2. Always use identical probes.
011 - 3. Measure at the 50-percent amplitude points.
011 - 4. 6 nanoseconds.
011 - 5. The × 10 magnifier control or the delayed sweep function.

STOP - 1. MATCH ANSWER SHEET TO THIS EXERCISE NUMBER.
2. USE NUMBER 2 PENCIL ONLY.

EXTENSION COURSE INSTITUTE
VOLUME REVIEW EXERCISE

30554 03 21
SYSTEMS MAINTENANCE

Carefully read the following:

DO's:

1. Check the "course," "volume," and "form" numbers from the answer sheet address tab against the "VRE answer sheet identification number" in the righthand column of the shipping list. If numbers do not match, return the answer sheet and the shipping list to ECI immediately with a note of explanation.
2. Note that item numbers on answer sheet are sequential in each column.
3. Use a medium sharp #2 black lead pencil for marking answer sheet .
4. Write the correct answer in the margin at the left of the item. (When you review for the course examination, you can cover your answers with a strip of paper and then check your review answers against your original choices.) After you are sure of your answers, transfer them to the answer sheet. If you have to change an answer on the answer sheet, be sure that the erasure is complete. Use a clean eraser. But try to avoid any erasure on the answer sheet if at all possible.
5. Take action to return entire answer sheet to ECI.
6. Keep Volume Review Exercise booklet for review and reference.
7. If mandatorily enrolled student, process questions or comments through your unit trainer or OJT supervisor. If voluntarily enrolled student, send questions or comments to ECI on ECI Form 17.

DON'Ts:

1. Don't use answer sheets other than one furnished specifically for each review exercise.
2. Don't mark on the answer sheet except to fill in marking blocks. Double marks or excessive markings which overflow marking blocks will register as errors.
3. Don't fold, spindle, staple, tape, or mutilate the answer sheet.
4. Don't use ink or any marking other than a #2 black lead pencil.

NOTE: **NUMBERED LEARNING OBJECTIVE REFERENCES ARE USED ON THE VOLUME REVIEW EXERCISE.** In parenthesis after each item number on the VRE is the Learning Objective Number where the answer to that item can be located. When answering the items on the VRE, refer to the Learning Objectives indicated by these Numbers. The VRE results will be sent to you on a postcard which will list the actual VRE items you missed. Go to the VRE booklet and locate the Learning Objective Numbers for the items missed. Go to the text and carefully review the areas covered by these references. Review the entire VRE again before you take the closed-book Course Examination.

MULTIPLE CHOICE

Note to Student: Consider all choices carefully and select the best answer to each question.

1. (400) What are the three main classes of maintenance programs?

   a. Diagnostic, performance, and self-checking.
   b. Utility, reliability, and diagnostic.
   c. Utility, self-checking, and performance.
   d. Reliability, report generator, and operating.

2. (400) The maintenance program which is cycled in conjunction with the operational program is the

   a. confidence-diagnostic program.
   b. increasing area program.
   c. decreasing area program.
   d. overlapping area program.

3. (401) The number of digits to be contained in the address portion of an instruction word is determined by the

   a. desired speed of operation.
   b. capacity of the computer memory.
   c. number of different operations to be performed.
   d. number of different types of operations the computer can perform.

4. (402) Which of the following instructions is used by the computer to duplicate a word in another section of the computer?

   a. Shift.
   b. Arithmetic.
   c. Transfer.
   d. Conditional jump.

5. (403) Which type of operation automatically repositions the binary points throughout a computation process?

   a. Fixed point.
   b. Fixed scaling.
   c. Floating point.
   d. Variable scaling.

6. (404) Which component function of a loop changes the address portion of a computer instruction?

   a. Initializing.
   b. Computing.
   c. Modifying.
   d. Testing.

7. (405) Which of the following statements is true of flow chart symbols?

   a. They do not use functional notations.
   b. They may change from system to system.
   c. They do not contain descriptions of computational functions.
   d. They require direction of flow indicators if the direction of flow is from top to bottom.

8. (406) Which type of flow chart normally defines the major functions or the overall aspects of a problem?

   a. Top-level.
   b. Intermediate level.
   c. Low-level.
   d. Detailed flow.

9. (407) Which one of the following is not a form of the more standardized types of operator communcation as pertains to programs?

   a. Interrupts.
   b. Branches.
   c. Printouts.
   d. Manual interventions.

10. (408) What is normally required to initialize a system once it has been placed into operation?

   a. Clearing alarms.
   b. Applying power.
   c. Making cross connects.
   d. Arranging instructions and data in the computer.

11. (409) Indicator panels provide all of the following except

   a. memory contents.
   b. register operation.
   c. system operation.
   d. component operation.

12. (409) How is the output voltage of each phase of the power-generating equipment operation usually monitored?

   a. By metering circuits and alarm lamps.
   b. By indicator switches.
   c. By circuit readers.
   d. By generation switches.

13. (410) Which distribution frame is generally encountered when the subscriber line multiple appears on one side and subscriber line circuit on the other for interconnection?

   a. Red.
   b. Main.
   c. Combined.
   d. Intermediate.

14. (411) The connector alphanumeric A1P3/A2J2 indicates

a. plug A1P3 is a cabinet plug and jack A2J2 is a chassis or drawer jack.
b. plug A1P3 is a cabinet plug and jack J2 is a cabinet plug.
c. jack J2 mates with interconnecting wire A1P2.
d. plug P3 mates with jack J2.

15. (412) Refer to text figure 2-7. What cables route the module 611 output to the SIF and SM-137?

a. 5622 and 5623.
b. 800 and 980.
c. 119 and 12.
d. 101 and 119.

16. (413) Which of the following would be true of assigning numbers or letters to a jack or to plug pins?

a. All numbers and letters may be used.
b. Any number and all letters except i, o, and q may be used.
c. Only lower-case letters and any numbers may be used.
d. Only letters may be used.

17. (414) The primary purpose in performing a maintenance routine is to insure

a. optimum equipment operation.
b. that the technician is kept busy.
c. that the proper TOs are being used.
d. that the equipment is operating.

18. (415) Which abrasive should you use to clean relay prongs?

a. Coarse sandpaper.
b. Emery cloth.
c. Crocus cloth.
d. Steel wool.

19. (416) Which of the following checks made on printers would provide the most reliable results?

a. A visual examination of all moving parts, examining for wear and tear.
b. The printout itself.
c. The measurement of power to determine accuracy of circuit operation.
d. The measurement of tolerances of mechanical assembly parts, i.e., cams, gears, spaces, against a specification.

20. (411) If a high-speed data rate of transmission is required, which of the following requirements would be most essential?

a. Low-gain high-quality amplifiers in repeater station circuitry.
b. Low signal loss, linear amplifiers to provide the best gain and minimize data loss.
c. Noise-free lines for the audio transmission portion of the data transfer.
d. A dipole data transfer to provide frequency-shift keying.

21. (417) At what range does the decibel level of a signal usually enter the phone line from a modulator or transmitter?

a. 0 to +6 dB.
b. 0 to -6 dB.
c. +6 to -25 dB.
d. -6 to +25 dB.

22. (418) The trimmer capacitors used in computer systems most frequently are

a. linear.
b. nonlinear.
c. varied by altering the dielectric material.
d. manufactured with the rotor contained between two sets of stator plates.

23. (418) What is the difference, if any, between a tubular capacitor and a button type?

a. There is no difference.
b. The tubular capacitors have a life cycle expectancy of 250 turns.
c. More critical adjustments can be made with a tubular capacitor.
d. The life turns cycle of a button type exceeds the tubular type by four times.

24. (419) Which meter adjustment requires the disassembly of the meter?

a. Centering.
b. Nulling.
c. Balancing.
d. Zeroing.

25. (420) Variable components are installed in amplifier or pulse generator circuits to serve each of the following primary purposes except

a. to alter the gain ratio of the circuit.
b. to act as a phase-shifting device.
c. to control the pulse duration.
d. to attenuate the input line signals.

26. (420) A pulse generator may be called by each of the following names except

a. a one-shot MV.
b. a single-shot MV.
c. a monostable MV.
d. a bistable MV.

27. (421) What type of meter should be used if the instruction requirement is to "adjust power supply control R10 for 24V ± .001V output"?

a. A frequency meter.
b. A DC voltmeter, model PSM6 or 7.
c. A differential voltmeter.
d. An AC voltmeter.

28. (422) What component is common to most computer system timing generators?

a. Adjustable capacitors.
b. Crystals.
c. Wire-wound resistors.
d. 5-watt resistors.

29. (422) In addition to the master timing unit, all of the following units are frequently used for timing control except

a. free-running oscillators.
b. blocking oscillators.
c. automatic gate length generators.
d. amplitude control circuits.

30. (423) From the following systems, select the type that does not have mechanical adjustment associated with it.

a. Core.
b. Drum.
c. Disk.
d. Tape.

31. (423) Mechanical adjustments in a tape storage system vary according to the design features of the unit. They have all of the following common elements except for

a. stop.
b. start.
c. tension.
d. tape replacement.

32. (423) The potentiometers used in storage tube adjustments control all of the following except for

a. scanning.
b. flood gun intensity.
c. unblanking.
d. frequency compensation.

33. (424) Which of the following is not a main requirement for the alignment of intensity and unblanking circuits?

a. Gate amplitudes.
b. Gate shaping.
c. Amplitude control of video pulses.
d. Frequency.

34. (425) Servoloops operate on a principle of

a. rate feedback.
b. a summing a feedback voltage with an input signal.
c. amplifying a difference signal to drive the motor to a position which produces a null to the input unit.
d. a 180-degree signal feedback summed with a 0-degree input of the same frequency and the motor drive until both signals are of the same magnitude.

35. (425) The direction of rotation in a servo unit is a function of the

a. motor.
b. phase relationship between the signal and reference voltage.
c. phase relationship between the signal and reference windings.
d. relationship of the phase of the input signal and the feedback signal.

36. (425) What portion of the spacing theory is essential to the accomplishment of the alignment performed on the keyboard printer punch carriage unit?

a. The two hammers must trip.
b. The clearances must be preset.
c. The coil must be energized to perform the alignment.
d. The rack is spring-loaded to the left.

37. (426) In coordinate numbering, numbers are assigned from

a. right to left, bottom to top, and back to front.
b. left to right, bottom to top, and front to back.
c. right to left, top to bottom, and back to front.
d. left to right, top to bottom, and front to back.

38. (427) Using figures 3-8 and 3-9 from the text, what is the part number of the PCB that fits into slot A11?

a. 38-204267-01.
b. 39-201803-01.
c. 39-203859-01.
d. 229639-01.

39. (428) What is the usual ohms-per-volt sensitivity of the AC voltmeter circuits in a VOM?

a. 500.
b. 1000.
c. 5000.
d. 10,000.

40. (428) Using the multimeter shown in figure 3-12, if you want to measure a current of 14 mA, what resistors shunt the meter and what resistors are in series with the meter?

a. R1, R2, R3, and R4 are all shunting, no series resistance.
b. R2, R3, and R4 are shunting; R1 is in series.
c. R3 and R4 are shunting; R1 and R2 are in series.
d. R1 is shunting; R2, R3, and R4 are in series.

41. (429) Which of the following is a disadvantage of a multimeter?

a. Short scale.
b. Portability.
c. Versatility.
d. The internal power source.

42. (430) All of the following are advantageous features of the transistor voltmeter (TRVM) except that

a. no warmup is required.
b. it has a high input impedance.
c. it can operate on batteries.
d. it is free from AC pickup.

43. (431) If the range control on a differential voltmeter you wish to use has no apparent effect, you should first

a. supply a separate ground for the meter.
b. return the meter to PME for repair.
c. check the input power source.
d. check the position of the null control.

44. (431) The differential voltmeter can be used as a normal VTVM with the

a. null switch in VTVM.
b. range switch in DC.
c. range switch in CAL.
d. null switch in AV.

45. (431) The range switch of the differential voltmeter determines

a. the null position.
b. the range of voltages to be measured.
c. the current to be measured.
d. the mode of operation.

46. (432) The operation of a digital voltmeter is determined by

a. the probes.
b. the plug-in unit.
c. the timed readings.
d. the digital output jacks.

47. (433) When counting the number of input pulses between a manual START and manual STOP, what type of measurement is being accomplished?

a. Period.
b. Frequency.
c. Rate.
d. Totalizing.

48. (433) When making a measurement from one point on a waveform to another point on the same waveform, the type of measurement being used is the

a. rate.
b. time interval.
c. ratio.
d. period.

49. (434) If only approximate frequency measurements are needed, which of the following devices should you use?

a. A Wheatstone bridge.
b. A signal generator.
c. A slotted-line section.
d. An electrodynamic wattmeter.

50. (435) Which of the following may be used in place of a storage scope?

a. A logic probe.
b. A logic clip.
c. A logic pulser.
d. A logic switch.

51. (436) What tester is used to test suspected assemblies without removing the assemblies from the equipment rack?

a. A trouble analyzer.
b. A drawer tester.
c. A card tester.
d. An IC tester.

52. (437) Meters in motor circuits should be able to handle the motor starting current which may

a. double the normal running current.
b. be 3 to 4 times the normal running current.
c. be 6 to 8 times the normal running current.
d. be 10 times the normal running current.

53. (438) If dust gets inside an item of measuring equipment, what meter characteristics can be affected?

a. Range.
b. Accuracy.
c. Temperature.
d. Adjustment.

54. (439) For maintenance purposes, test equipment is divided into

a. two categories.	c. four categories.
b. three categories.	d. five categories.

55. (440) Which AFTO Form is affixed to equipment requiring no calibration?

a. AFTO Form 108.	c. AFTO Form 257.
b. AFTO Form 256.	d. AFTO Form 273.

56. (441) Which of the following systems provides users with rapid-access, high-quality, worldwide telephone and data communications?

a. AUTOVON.	c. ASC.
b. AUTODIN.	d. DSA.

57. (441) Which of the following is a highly complex computerized communications system designed to transmit and receive narrative messages and data traffic?

a. AUTOVON.	c. PBX.
b. AUTODIN.	d. DSA.

58. (442) Which of the following is a tactical air control system?

a. 407L.	c. 474N.
b. 416M.	d. 490L.

59. (442) Which unit is the headquarters facility for the Air Force component of the JTF?

a. CRC.	c. TACC.
b. CRP.	d. AFCCP.

60. (443) Which system consists of equipment that bounces radar signals off the ionosphere and back to earth?

a. OTH.	c. MEWS.
b. SLBM.	d. BMEWS.

61. (444) In an electrochemical corrosion cell, the flow of electrons is from

a. anode to cathode.	c. cathode to conductor.
b. cathode to anode.	d. anode to the electrolyte.

62. (445) In the second step of the corrosion process, the rate of corrosion is dependent upon the presence of

a. hydrogen.	c. hydrogen and hydroxly ions.
b. dissolved oxygen.	d. unionized ferrous metal.

63. (446) A substance which cannot be broken down by chemical means is

a. a molecule.
b. a compound.
c. an element.
d. an ion.

64. (447) Nature's method of combating corrosion by reducing the electrode potential of a corrosion cell is known as

a. oxidation.
b. ionization.
c. passivation.
d. polarization.

65. (448) When the pH concentration of a solution is less than 4, the alkaline film will be

a. passivated.
b. polarized.
c. destroyed.
d. increased.

66. (449) As they enter into a solution, which of the following tend to decrease the rate of corrosion?

a. Carbon dioxide.
b. Hydrogen sulfide.
c. Chlorine gas.
d. Inert gases.

67. (450) Bacterial corrosion that produces thick deposits forms what type of corrosion?

a. Pitting.
b. Galvanic.
c. Exfoliation.
d. Concentration cell.

68. (451) On a polished surface, uniform etch corrosion is first seen as

a. a discoloration of the paint.
b. white powdery deposits.
c. a general dulling of the surface.
d. small pits or holes.

69. (452) Which of the following descriptions indicate that bare steel is severely corroded?

a. A red-to-black scale.
b. A whitish powdery residue.
c. A tightly bound black residue.
d. A greenish-white color.

70. (453) Which of the following is not a recommended method to be used to decrease corrosion problems?

a. Perform frequent inspections.
b. Determine any cause of corrosion.
c. Remove all evidence of corrosion.
d. Protect the metal from further attack.

71. (454) Which of the following best identifies the correct procedural sequence to be followed when treating metal for corrosion?

a. Clean, strip paint, apply protective coating.
b. Strip paint, clean, apply protective coating.
c. Remove corrosion, clean, apply protective coating.
d. Clean, remove corrosion, apply protective coating.

72. (455) Some of the most important troubleshooting aids which you might use on the job are

a. fault indicators, soldering irons, and system and unit testers.
b. performance test standards, diagnostic programs, and test probes.
c. fault indicators, system and unit testers, performance test standards, and diagnostic programs.
d. flow diagrams, specialized test equipment and unit testers, performance standards, and equipment PMIs.

73. (455) The first step in the general troubleshooting procedure is

a. try to localize the fault through analysis of the symptoms of malfunction.
b. localize the fault to the defective stage by testing techniques.
c. replace or repair the defective part.
d. try to locate the trouble through inspection.

74. (456) The forms of troubleshooting employed in localizing a fault to a defective section are

a. marginal checking, waveform analysis, test routines, and systematic electron flow observations.
b. marginal checking, test routines and programs, and soldering techniques.
c. waveform analysis, voltage sampling, test routines, and schematic electron flow observations.
d. marginal checking, system checking, test routines and programs, and diagnostic checks.

75. (457) The types of test equipment employed in localizing a fault to a defective stage are

a. systems peculiar test equipment and specialized unit test equipment.
b. systems peculiar test equipment and normal test equipment.
c. normal test equipment and contractor designated test equipment.
d. contractor designated test equipment and specialized system test equipment.

76. (458) When making resistance measurements in a circuit installed in equipment, you should be sure that the

a. power is turned off and all filter capacitors are discharged.
b. capacitors are discharged and proper test equipment loading characteristics have been considered.
c. power is turned off and all loading characteristics are considered.
d. all loading characteristics have been considered and that you have selected the proper meter.

77. (459) The group removal and replacement concept dictates that removal and replacement is restricted to

a. one-third of the cards, not to exceed seven.
b. one-half of the cards, not to exceed seven.
c. one-half of the cards, not to exceed six.
d. one-third of the cards, not to exceed six.

78. (460) When using test points as a troubleshooting aid, the most efficient method is called the

a. split-half method.
b. one-third-split method.
c. quarter-split method.
d. split-quarter method.

79. (461) Boolean equations are most useful when troubleshooting with a

a. schematic diagram.
b. logic diagram.
c. block diagram.
d. functional diagram.

80. (462) The pointed end of a soldering aid is used

a. to remove solder from terminal holes and slots.
b. to remove molten solder.
c. to lift the ends of part leads from the terminal.
d. to exert force on wires and leads for security testing.

81. (462) The appropriate wattage rating of a soldering iron used for soldering a heavy-gauge wire is

a. 20 to 40 watts.
b. 50 to 60 watts.
c. 44 to 52 watts.
d. 100 watts or above.

82. (463) What are unplated soldering tips cleaned with?

a. Files.
b. Sponges.
c. Emery cloths.
d. Sandpaper.

83. (464) What is used to prevent wicking during the tinning procedure?

a. A heat sink.
b. Flux.
c. A thermal shunt.
d. Beeswax.

84. (464) Which of the following is an acceptable tool for cleaning terminals?

a. A file.
b. Sandpaper.
c. An emery cloth.
d. A typewriter eraser.

85. (465) Which of the following is characteristic of an acceptable solder connection?

a. A good convex fillet.
b. A flat, dull surface.
c. No pits or holes.
d. The contour of the wire being completely covered with solder.

86. (466) Wire or part leads attached to a turret must be wrapped around the terminal a minimum of

a. 90 degrees.
b. 180 degrees.
c. 270 degrees.
d. 360 degrees.

87. (467) Which statement concerning the preparation of a wick is true?

a. Make the wick diameter larger than the pad being desoldered.
b. Tin the einture wick with a suitable solder.
c. Place the wick on top of the soldering iron.
d. Flatten the wick slightly.

88. (468) The flipping of excess solder can result in

a. an electric short.
b. a serious skin or eye burn.
c. a broken solder tip.
d. the catching of hot solder under a finger ring.

89. (469) The length of bare wire required for a good wire wrap connection is

a. 3/4 to 1 inch.
b. 1-1/4 to 1-3/8 inches.
c. 2 inches.
d. 2 to 3 inches.

90. (470) The two major publications which will aid in the removal and replacement of items are the

a. -1 and -2 TO series.
b. -2 and -3 TO series.
c. -2 and -4 TO series.
d. -2 and -4 TO series.

91. (471) At approximately what temperature will the current-carrying element in a fuse wire melt?

a. 50 degrees C.
b. 100 degrees C.
c. 100 degrees F.
d. 170 degrees F.

92. (472) Which of the following switches would most likely be used to control voltage or current?

a. A toggle.
b. A pushbutton.
c. A circular microswitch.
d. A level contactor microswitch.

93. (473) Multiple connector bodies that eimply solderless pins are designed to hold

a. a single wire.
b. no more than three wires.
c. two wires if 22 gauge or smaller.
d. Four wires if 22 gauge or larger.

94. (474) Which of the following printed circuit wiring patterns is the more commonly used?

a. Metal foil circuit cards.
b. Chemically deposited circuit cards.
c. A printed circuit card with wiring and printed parts.
d. A printed circuit wiring pattern.

95. (475) Carbonized areas that could form leaking paths on a printed circuit board should be cleaned with a prescribed solvent and

a. an emery cloth.
b. a steel wool pad.
c. a stiff brush.
d. a soft brush.

96. (476) Which of the following statements on trouble in a capacitor is false?

a. When the ohmmeter reading goes immediately to zero, the capacitor is shorted.
b. A normal capacitor shows a charging action and the final reading is less than normal, the capacitor is leaking.
c. The electrolytic capacitor must be checked by taking a normal reading, and then reversing the ohmmeter leads and taking another reading.
d. If the capacitor shows no charging action and immediately indicates a high resistance, it is normal.

97. (476) When checking diodes with an ohmmeter, never use a range setting below ohms times

a. 1.
b. 10.
c. 100.
d. 1000.

98. (476) Integrated circuits are divided into each of the following for testing purposes except

a. linear.
b. nonlinear.
c. a committed transistor.
d. an uncommitted transistor (array).

99. (477) A drift punch is helpful in removing a printed circuit board transistor that has been mounted

a. by bolting.
b. in a socket.
c. by clamping.
d. through the board with bonding.

100. (478) What is used in a power supply to maintain the output voltage to the critical level needed?

a. Voltage regulators.
b. Voltage dividers.
c. Transformers.
d. Rectifiers.

101. (479) What offers zero impedance to the folow of current in one direction and an infinite impedance to the flow of current in the opposite direction?

a. An amplifier.
b. A rectifier.
c. A transformer.
d. A power supply.

102. (479) What would be the inverse peak voltage of a full-wave rectifier that has an output peak voltage of 100 volts?

a. 50 volts.
b. 100 volts.
c. 200 volts.
d. 600 volts.

103. (480) Refer to text figure 6-18. With an input frequency of 60 Hz and 60 volts, what is the output ripple frequency and output voltage?

a. 30 Hz, 60 volts.
b. 60 Hz, 60 volts.
c. 60 Hz, 120 volts.
d. 120 Hz, 120 volts.

104. (480) What is the main use of a cascade voltage multiplier?

a. A transformerless high-voltage, low-current supply.
b. A transformerless high-voltage, high-current supply.
c. A transformerless low-voltage, high-current supply.
d. A transformerless low-voltage, low-current supply.

105. (481) What property of a capacitor allows it to be used in a filter network?

a. Stores electrical energy.
b. Discharges rapidly across a load.
c. Increases the flow of alternating current.
d. Permits the flow of electrons more easily in one direction than in the other.

106. (482) What name is given to a family of diodes designed to operate with reverse breakdown voltage?

a. ASR.
b. SCR.
c. Zener diode.
d. Electronic voltage regulators.

107. (482) Which of the following is basically a four-layer, semiconductor device having three electrodes?

a. ASR.
b. EVR.
c. SCR.
d. Zener diode.

108. (483) Refer to text figure 6-45. If load 3 is 60 volts at 2 milliamperes, load 2 is 150 volts at 1 milliampere, and load 1 is 300 volts at 6 milliamperes, what is the value of R3?

a. 30,000 ohms.
b. 37,500 ohms.
c. 45,000 ohms.
d. 60,000 ohms.

109. (484) Refer to text figure 6-46. Transistors Q7 and Q8 form a part of

a. a series regulator.
b. a differential amplifier.
c. a voltage divider network.
d. a filter network for the +3V power supply.

110. (485) An open-circuited rectifier in a single-phase half-wave rectifier circuit will

a. cause no DC output.
b. cause an increased AC ripple voltage.
c. cause an increased DC output voltage.
d. have no effect on the output voltage.

111. (485) A 60-Hz ripple frequency from a singe-phase full-wave rectifier unit indicates

a. no trouble with the unit.
b. that a zener diode is week.
c. that a rectifier diode is probably defective.
d. a voltage increase.

112. (486) What part of the vertical input section of an oscilloscope enables you to review the leading edge of a signal?

a. The delay line.
b. The input attenuator.
c. The vertical input amplifier.
d. The input coupling switch in the 50-ohm position.

113. (487) What measurement is made between the 10-percent and 90-percent amplitude points on the trailing edge of a pulse waveform?

a. Rise time.
b. Fall time.
c. Pulse width.
d. Pulse bandwidth.

114. (488) Concerning the use of the X-Y operation to check phase, what Lissajous pattern is generated when the phase shift is 90 degrees?

a. A straight line from lower left to upper right.
b. A straight line from upper left to lower right.
c. A bow tie.
d. A circle.

115. (489) What mode of trigger control operation requires a trigger signal to generate a reference baseline?

a. Internal.
b. Single.
c. Normal.
d. Auto.

116. (490) During the Turn-On and Preset operation before using a scope, what position of the input coupling switch is used when the signal source is pulse or signal generator?

a. 50 ohms.
b. GND.
c. DC.
d. AC.

117. (491) Which of the following can happen as input shunt capacitances increase?

a. Reduced source loading.
b. Abnormal circuit operation.
c. Increased CW phase stability.
d. Rise time measurements become more accurate.

118. (492) What type of probe should be used for the most accurate rise time measurements?

a. A miniature passive adder.
b. A high resistance probe.
c. A 50-ohm divider.
d. An active probe.

119. (493) Which dual-trace display mode causes both channels to be displayed by switching between channels at a high-speed rate?

a. Chop.
c. Algebraic sum.
b. Alternate.
d. Algebraic difference.

120. (494) What type of triggering is used on a dual-trace scope to show two asynchronous signals?

a. Composite.
c. Delayed.
b. Selectable.
d. Double.

121. (495) Time interval measurements are least accurate using

a. the X 5 magnifier.
c. direct delayed sweep.
b. the X 10 magnifier.
d. differential delayed sweep.

122. (496) At what points on the pulse waveform is the propagation delay measured?

a. Between 10-percent and 90-percent points.
b. Between leading and trailing edges.
c. Between the 50-percent amplitude points on the waveform.
d. Between the maximum and minimum amplitude points.

END OF EXERCISE

ATC/ECI SURVEY

The remaining questions (125-135) are not part of the Volume Review Exercise (VRE). These questions are a voluntary ATC/ECI survey. Using a number 2 pencil, indicate what you consider to be the appropriate response to each survey question on your answer sheet (ECI Form 35), beginning with answer number 125. Do not respond to questions that do not apply to you. Your cooperation in completing this survey is greatly appreciated by ATC and ECI. (AUSCN 100)

PRIVACY ACT STATEMENT

A. Authority: 5 U.S.C. 301, Departmental Regulations

B. Principal Purpose: To gather preliminary data evaluating the ATC/ECI Career Development Course (CDC) Program.

C. Routine Uses: Determine the requirement for comprehensive evaluations in support of CDC program improvement.

D. Whether Disclosure is Mandatory or Voluntary: Participation in this survey is entirely voluntary.

E. Effect on the Individual of not Providing Information: No adverse action will be taken against any individual who elects not to participate in any or all parts of this survey.

QUESTIONS:

125. If you have contacted ECI for any reason during your enrollment, how would you describe the service provided to you?

a. Excellent.
b. Satisfactory.
c. Unsatisfactory.
d. Did not contact ECI.

126. My ECI course materials were received within a reasonable period of time.

a. Strongly agree.
b. Agree.
c. Disagree.
d. Strongly disagree.

127. The condition of the course materials I received from ECI was:

a. A complete set of well-packaged materials.
b. An incomplete set of well-packaged materials.
c. A complete set of poorly packaged materials.
d. An incomplete set of poorly packaged materials.

128. The reading level of the material in the course was too difficult for me.

a. Strongly agree.
b. Agree.
c. Disagree.
d. Strongly disagree.

129. The technical material in the course was too difficult for me at my present level of training.

a. Strongly agree.
b. Agree.
c. Disagree.
d. Strongly disagree.

130. The illustrations in the course helped clarify the information for me.

a. Strongly agree.
b. Agree.
c. Disagree.
d. Strongly disagree.

131. Approximately how much information in the course provides general information about your AFSC?

a. Between 80 and 99%.	c. Between 40 and 59%.
b. Between 60 and 79%.	d. Between 20 and 39%.

132. Approximately how much information in this course was current?

a. Between 80 and 99%.	c. Between 40 and 59%.
b. Between 60 and 79%.	d. Between 20 and 39%.

133. The format of the text (objective followed by narrative and exercises) helped me study.

a. Strongly agree.	c. Disagree.
b. Agree.	d. Strongly disagree.

134. The volume review exercise(s) helped me review information in the course.

a. Strongly agree.	c. Disagree.
b. Agree.	d. Strongly disagree.

135. Check the rating which most nearly describes the usefulness of the information in this CDC in your upgrade training program.

a. Excellent.	c. Marginal.
b. Satisfactory.	d. Unsatisfactory.

NOTE: If you know this CDC contains outdated information or does not provide the knowledge that the current specialty training standard requires you to have for upgrade training, contact your OJT advisor and fill out an AF Form 1284, Training Quality Report.

STUDENT REQUEST FOR ASSISTANCE

PRIVACY ACT STATEMENT

AUTHORITY: 44 USC 3101. PRINCIPAL PURPOSE(S): To provide student assistance as requested by individual students. ROUTINE USES: This form is shipped with every ECI course package. It is utilized by the student, as needed, to place an inquiry with ECI. DISCLOSURE: Voluntary. The information requested on this form is needed for expeditious handling of the student's need. Failure to provide all information would result in slower action or inability to provide assistance.

SECTION I: CORRECTED OR LATEST ENROLLMENT DATA: MAIL TO: ECI, GUNTER AFS, ALA 36118

1. THIS REQUEST CONCERNS COURSE
2. TODAY'S DATE
3. ENROLLMENT DATE
4. PREVIOUS SERIAL NUMBER
5. SOCIAL SECURITY NUMBER ☐☐☐ – ☐☐ – ☐☐☐☐
6. GRADE/RANK
7. INITIALS ☐☐ LAST NAME
8. OTHER ECI COURSES NOW ENROLLED IN
9. ADDRESS: (OJT ENROLLEES - ADDRESS OF UNIT TRAINING OFFICE/ALL OTHERS - CURRENT MAILING ADDRESS)

ZIP CODE ☐☐☐☐☐

10. NAME OF BASE OR INSTALLATION IF NOT SHOWN ABOVE:
11. AUTOVON NUMBER
12. TEST CONTROL OFFICE ZIP CODE/SHRED

SECTION II: Old or INCORRECT ENROLLMENT DATA

1. NAME: 2. GRADE/RANK: 3. SSAN:

4. ADDRESS: 5. TEST OFFICE ZIP/SHRED:

SECTION III: REQUEST FOR MATERIALS, RECORDS, OR SERVICE

(Place an "X" through number in box to left of service requested)

ADDITIONAL FORMS 17 available from trainers, OJT and Education Offices, and ECI. The latest course workbooks have a Form 17 printed on the last page.

1 EXTEND COURSE COMPLETION DATE. (Justify in Remarks)
2 SEND VRE ANSWER SHEETS FOR VOL(s): 1 2 3 4 5 6 7 8 9 - ORIGINALS WERE: NOT RECEIVED, LOST, MISUSED
3 SEND COURSE MATERIALS (Specify in remarks) - ORIGINALS WERE: NOT RECEIVED, LOST, DAMAGED.
4 COURSE EXAM NOT YET RECEIVED. FINAL VRE SUBMITTED FOR GRADING ON (Date):
5 RESULTS FOR VRE VOL(s): 1 2 3 4 5 6 7 8 9 NOT YET RECEIVED. ANSWER SHEET(s) SUBMITTED ON (Date):
6 RESULTS FOR CE NOT YET RECEIVED. ANSWER SHEET SUBMITTED TO ECI ON (Date):
7 PREVIOUS INQUIRY (ECI FORM 17, LTR, MSG) SENT TO ECI ON:
8 GIVE INSTRUCTIONAL ASSISTANCE AS REQUESTED ON REVERSE:
9 OTHER (Explain fully in remarks)

REMARKS: (Continue on Reverse)

OJT STUDENTS must have their OJT Administrator certify this request.

ALL OTHER STUDENTS may certify their own requests.

I certify that the information on this form is accurate and that this request cannot be answered at this station. (Signature)

ECI FORM JUN 77 17 PREVIOUS EDITIONS MAY BE USED

SECTION IV: REQUEST FOR INSTRUCTOR ASSISTANCE

NOTE: Questions or comments relating to the accuracy or currency of textual material should be forwarded directly to preparing agency. Name of agency can be found at the bottom of the inside cover of each text. All other inquiries concerning the course should be forwarded to ECI.

VRE ITEM QUESTIONED:

MY QUESTION IS:

Course No. ___________

Volume No. ___________

VRE Form No. _________

VRE Item No. _________

Answer You Chose (Letter) __________

Has VRE Answer Sheet been submitted for grading?

☐ YES ☐ NO

REFERENCE

(Textual support for the answer I chose can be found as shown below)

In Volume No: ________

On Page No: __________

In_____ (Left)_____(Right) Column

Lines_____Through_____

Remarks:

AU GAFS, AL. (864355)1100